1

Basic Equations of the PLLs

1.1 INTRODUCTION

Phase lock loops (PLLs) belong to a larger set of regulation systems. As an independent research and design field it started in the 1950s [1] and gained major practical application in cochannel TV. On this occasion, we find one of the first fundamental papers [2].

Some 15 years later, we encounter a surveying book by Gardner [3], still mentioned and used. Since a dozen books were published on the topic of PLL problems proper [4] and in connection with frequency synthesis, we would find chapters on PLLs in all of the relevant books. Here we shall only mention some of them [5–8]. But the importance of the topic is testified by the publication of new books on PLLs (e.g., [9–12]) and a wealth of journal articles, the important ones of which will be cited at the relevant places. A major advantage of modern PLLs is the possibility of a widespread use of off-the-shelf *IC chips*. Their application results in low-volume, low-weight, and often power-saving devices. At the same time we also appreciate short switching times and very high-frequency resolution. We shall find PLLs in communications equipment, particularly, in mobile applications in low-gigahertz ranges, in computers, and so on, where we appreciate short switching times and very high-frequency resolution. However, there are shortcomings too: the limited range for high frequencies (today commercial dividers hardly exceed the 5 GHz bound and only laboratory devices work in higher ranges).

In the following paragraphs we summarize the basic properties of PLLs with some design-leading ideas and repeat all the major features and use terminology introduced years ago by mechanical engineers [13] and also used by Gardner [3] and many others.

1.2 BASIC EQUATIONS OF THE PLLs

The task of the PLLs is to maintain coherence between the input (reference) signal frequency, f_i, and the respective output frequency, f_o, via phase comparison. Another

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feature of PLLs is the filtering property, particularly with respect to the noise where its behavior recalls a very narrow low-pass arrangement that is not to be realized by other means. The theory was explained in many textbooks as we have mentioned in the previous section.

Each PLL system is composed of four basic parts:

1. the reference generator (RG)
2. the phase detector (PD)
3. the low-pass filter $F_L(f)$ (in higher-order systems)
4. the voltage-controlled oscillator (VCO)

and works as a feedback system shown in Fig. 1.1.

Without any loss of generality, we may assume that input and output signals are harmonic voltages with additional phase modulation

$$v_i(t) = V_i \sin[\omega_i t + \phi_i(t)] \equiv V_i \sin \Psi_i(t) \tag{1.1}$$

where $\phi_i(t)$ and $\phi_o(t)$ are slowly varying quantities.

$$v_o(t) = V_o \cos[\omega_o t + \phi_o(t)] \equiv V_o \cos \Psi_o(t) \tag{1.2}$$

Later we shall prove that realization of the phase lock requires that input and output voltages must be in quadrature, that is, mutually shifted by $\pi/2$.

Phase detector (PD) is a nonlinear element of a different design and construction (we shall deal with PDs later in Chapter 8, Section 8.4). For the present discussion, we assume that the PD is a simple multiplier. In this case the corresponding output voltage will be

$$v_d(t) = K_m v_i(t)\ v_o(t) \tag{1.3}$$

where K_m is the transfer constant with the dimension [1/V]. After introduction of eqs. (1.1) and (1.2) in the above relation, we get

$$\begin{aligned} v_d(t) &= K_m V_i V_o \sin \Psi_i(t) \cos \Psi_o(t) \\ &= \tfrac{1}{2} K_m V_i V_o [\sin[(\omega_i - \omega_o)t + \phi_i(t) - \phi_o(t)] \\ &\quad + \sin[(\omega_i + \omega_o)t + \phi_i(t) + \phi_o(t)]] \end{aligned} \tag{1.4}$$

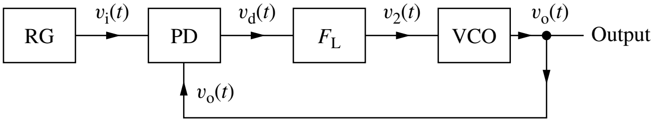

Figure 1.1 Basic feedback network of PLL.

In the simplest case we shall assume that the low-pass filter removes the upper sideband with the frequency $\omega_i + \omega_o$ but leaves the lower sideband $\omega_i - \omega_o$ without change. Evidently the VCO tuning voltage will be

$$\begin{aligned} v_2(t) &= K_d \sin[(\omega_i - \omega_o)t + \phi_i(t) - \phi_o(t)] \\ &\equiv K_d \sin \Psi_e(t) \end{aligned} \tag{1.5}$$

where we have introduced the so-called PD gain $K_d = K_m V_i V_o$ of dimension [V/rad]. Note that the phase difference between the input and the output voltages is

$$\Psi_e(t) = \Psi_i(t) - \Psi_o(t) \tag{1.6}$$

Voltage $v_2(t)$ will change the free running frequency ω_c of the VCO to

$$\dot{\Psi}_o(t) = \omega_c + K_o v_2(t) \tag{1.7}$$

where the proportionality constant K_o is designated as the *oscillator gain* with the dimension [2π Hz/V]. After integration of the above equation and introduction into relation (1.6), we get for the phase difference $\Psi_e(t)$

$$\Psi_e(t) = \Psi_i(t) - \omega_c t - \int K_o v_2(t)\, dt \tag{1.8}$$

which can be rearranged as follows:

$$\Psi_e(t) = \omega_i t - \omega_c t - \int K_o K_d \sin \Psi_e(t)\, dt \tag{1.9}$$

and differentiation reveals

$$\frac{d\Psi_e(t)}{dt} = \Delta\omega - K \sin \Psi_e(t) \tag{1.10}$$

where we have introduced $\omega_i - \omega_o = \Delta\omega$ and $K_d K_o = K$. Note that K is indicated as the gain of the PLL with the dimension [2πHz].

The conclusion that follows from the foregoing discussion is that the phase lock arrangement is described with a nonlinear eq. (1.10), the solution of which for arbitrary values $\Delta\omega$ and K is not known. With certainty we can state that for $\Delta\omega/K \gg 1$ an aperiodic solution does not exist. This conclusion testifies the phase plane arrangement (Fig. 1.2). Without an aperiodic solution, the feedback system in Fig. 1.1 cannot reach the phase stability, that is, the output frequency of the VCO, ω_o, will never be equal to the reference frequency ω_i. However, the DC component in the steering voltage $v_2(t)$ reduces the original difference between frequencies

$$|\omega_i - \omega_c| > |\omega_i - \omega_o| \tag{1.11}$$

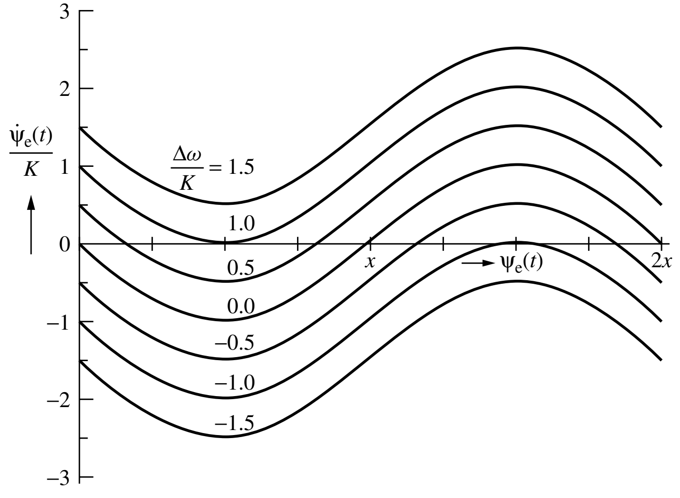

Figure 1.2 Plot of relation (1.10) in the phase plane for different ratios $\Delta\omega/K$.

1.3 SOLUTION OF THE BASIC PLL EQUATION IN THE TIME DOMAIN

To arrive at the solution we have to introduce some simplifications. Nevertheless, we gain more insight into the problem.

1.3.1 Solution in the Closed Form

In the case where $\Delta\omega/K \ll 1$, the differential eq. (1.10) has a solution after application and separation of variables.

$$\frac{\mathrm{d}\Psi_e(t)}{\Delta\omega - K \sin \Psi_e(t)} = \mathrm{d}t \tag{1.12}$$

With the assistance of tables [14, p. 804], we get a rather complicated closed-form solution

$$t - t_0 = -\frac{2}{\sqrt{(\Delta\omega)^2 - K^2}} \arctan\left[\sqrt{\frac{\Delta\omega + K}{\Delta\omega - K}} \tan\left(\frac{\pi}{4} - \frac{\Psi_e}{2}\right)\right] \tag{1.13}$$

where t_0 is a not-yet-defined integration constant. As long as $K > \Delta\omega$, the rhs will be imaginary and with the assistance

$$\tan(-\mathrm{j}x) = -\mathrm{j} \cdot \tanh(x) \tag{1.14}$$

we arrive at

$$t - t_0 = -\frac{2}{\sqrt{K^2 - (\Delta\omega)^2}} \operatorname{arctanh}\left[\sqrt{\frac{K + \Delta\omega}{K - \Delta\omega}} \tan\left(\frac{\pi}{4} - \frac{\Psi_e}{2}\right)\right]$$

$$= \frac{1}{\sqrt{K^2 - (\Delta\omega)^2}} \ln \frac{1 + \sqrt{(K + \Delta\omega)/(K - \Delta\omega)} \tan(\pi/4 - \Psi_e/2)}{1 - \sqrt{(K + \Delta\omega)/(K - \Delta\omega)} \tan(\pi/4 - \Psi_e/2)} \tag{1.15}$$

and after computing $\tan(\pi/4 - \Psi_e/2)$ the sought solution is

$$\Psi_e = 2 \arctan\left[\sqrt{\frac{K - \Delta\omega}{K + \Delta\omega}} \cdot \frac{1 - \exp[-\sqrt{K^2 - (\Delta\omega)^2}(t - t_0)]}{1 + \exp[-\sqrt{K^2 - (\Delta\omega)^2}(t - t_0)]} + \frac{\pi}{2}\right] \tag{1.16}$$

For the steady state, that is, for $t \to \infty$, the lhs of eq. (1.10) equals zero, with the result

$$\Psi_{e\infty} = \arcsin \frac{\Delta\omega}{K} \tag{1.17}$$

1.3.2 Linearized Solution

From the preceding analysis we conclude that the solution of the respective differential equation, in the closed form, is very complicated even for a very simple PLL arrangement. Consequently, we may suppose that for more sophisticated PLL systems it would be practically impossible. However, the situation need not be so gloomy after the introduction of simplifications that are not far from reality. In the first step we find that the time-dependent phase difference $\Psi_e(t)$ at the output of the PD in the closed PLL is small and prone to the simplification

$$\sin \Psi_e(t) \approx \Psi_e(t) \tag{1.18}$$

This assumption is supported with the reality that a lot of PDs are linear or nearly linear in the working range (see discussions in Chapter 8). In such a case, the introduction of (1.18) into (1.10) results in the following simplification:

$$\frac{d\Psi_e(t)}{dt} = \Delta\omega - K\Psi_e(t) \tag{1.19}$$

Solution of this differential equation is easy,

$$\Psi_e(t) = e^{-Kt}\left(\Psi_{e0} - \frac{\Delta\omega}{K}\right) + \frac{\Delta\omega}{K} \tag{1.20}$$

where Ψ_{e0} is the integration constant, that is, the phase at the start for $t = 0$. Further investigation reveals that the phase difference in the steady state compensates the frequency difference (cf. (1.17)).

$$\Psi_{e\infty} = \frac{\Delta\omega}{K} \tag{1.21}$$

1.4 SOLUTION OF BASIC PLL EQUATIONS IN THE FREQUENCY DOMAIN

By assuming the phase difference $\Psi_e(t)$, in the locked state, to be always smaller than $\pi/2$, the result is the equality between input and output frequencies

$$\omega_i = \omega_o \tag{1.22}$$

In other words the PLL system is permanently in the phase equilibrium. The situation being such, we can rearrange relation (1.7) to

$$\omega_o + \dot{\phi}_o(t) = \omega_c + K_o v_{2o} + K_d K_o \sin[\phi_i(t) - \phi_o(t)] \tag{1.23}$$

where the term $K_o v_{2o}$ shifts the VCO frequency ω_o to be equal to the input frequency ω_i (of (1.22)). Evidently, in the steady state we get the following relation between the VCO free running frequency and the locked frequency

$$\omega_o = \omega_c + K_o v_{2o} \tag{1.24}$$

Combination with (1.23) reveals

$$\dot{\phi}_o(t) = K \sin[\phi_i(t) - \phi_o(t)] \tag{1.25}$$

where $K = K_d K_o$.

In the steady state the difference ϕ_e

$$\phi_e(t) = \phi_i(t) - \phi_o(t) \tag{1.26}$$

is generally small. Consequently, we may apply the following linearization

$$\dot{\phi}_o(t) = K[\phi_i(t) - \phi_o(t)] \tag{1.27}$$

and employ advantages of the Laplace transform (with a tacit assumption of the zero initial conditions)

$$s\Phi_o(s) = K[\Phi_i(s) - \Phi_o(s)] \tag{1.28}$$

After rearrangement we arrive at the basic PLL transfer function

$$\frac{\Phi_o(s)}{\Phi_i(s)} = H(s) = \frac{K}{s + K} \tag{1.29}$$

or at

$$\frac{\Phi_i(s) - \Phi_o(s)}{\Phi_i(s)} = \frac{\Phi_e(s)}{\Phi_i(s)} = 1 - H(s) = \frac{s}{s + K} \tag{1.30}$$

between input and PD output error.

1.5 ORDER AND TYPE OF PLLs

The PLL system described with relations (1.29) and (1.30) is indicated as PLL of the *first order* since the polynomial in the denominator is of the first order in s (K being a constant).

However, generally PLLs are much more complicated. To get better insight into the PLL properties, we shall simplify, without any loss of generality, the block diagram to that shown in Fig. 1.3 and introduce the Laplace transfer functions of the individual building circuits, suitable for investigation of the small signal properties.

Investigation of the above figure reveals that the input phase $\varphi_{\mathrm{i}}(t)$ is compared with the output phase $\varphi_{\mathrm{o}}(t)$ in the phase detector (ring modulator, sampling circuit, etc.). At its output we get a voltage, $v_{\mathrm{d}}(t)$, proportional to the phase difference of the respective input signals where

$$v_{\mathrm{d}}(t) = [\varphi_{\mathrm{i}}(t) - \varphi_{\mathrm{o}}(t)]K_{\mathrm{d}} \tag{1.31}$$

the proportionality factor, K_{d}[V/rad], is called the *phase detector gain.*

Next, $v_{\mathrm{d}}(t)$ passes the loop filter, $F(s)$ (a low-pass filter attenuating “carriers” with frequencies $\omega_{\mathrm{i}} = \omega_{\mathrm{o}}$, and ideally all undesired sidebands). Note that the useful signal $v_2(t)$ is a slowly varying “DC” component, the output voltage of which is given by the following convolution:

$$v_2(t) = v_{\mathrm{d}}(t) \otimes h_{\mathrm{f}}(t) \tag{1.32}$$

where $h_{\mathrm{f}}(t)$ is the time response of the loop filter. After applying $v_2(t)$ on the frequency control element of the VCO, we get the output phase

$$\varphi_{\mathrm{o}}(t) = \int \omega_{\mathrm{o}}(t)\,\mathrm{d}t = \omega_{\mathrm{c}}t + \int K_{\mathrm{o}}v_2(t)\,\mathrm{d}t \tag{1.33}$$

with ω_{c} being the VCO free-running frequency. The proportionality factor, K_{o} [2π Hz/V], is designated as the *oscillator gain*. Since, in most cases, K_{d} and K_{o} are voltage-dependent, the general mathematical model of a PLL is a nonlinear differential equation. Its linearization, justified in small signal cases (“steady state” working modes), provides a good insight into the problem. After reverting to the

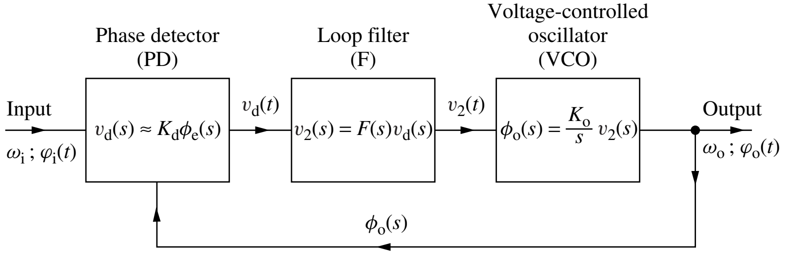

Figure 1.3 Simplified block diagram of the PLL with individual transfer functions.

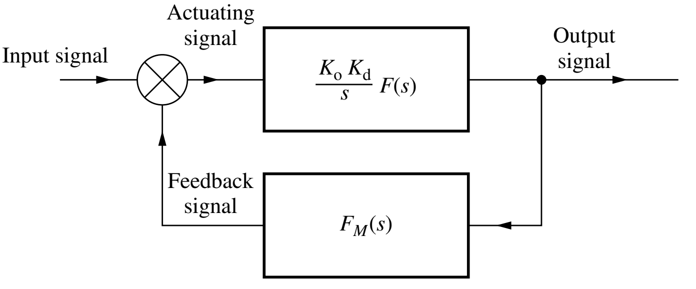

Figure 1.4 Simplified block diagram of the PLL with a transfer function in the feedback path.

whole feedback system (Fig. 1.4), we can write for the relation between the input and the output phases in the Laplace transform notation

$$[\Phi_i(s) - \Phi_o(s)F_M(s)]\frac{K_d K_o F(s)}{s} = \Phi_o(s) \tag{1.34}$$

The ratio, $\Phi_o(s)/\Phi_i(s)$, the PLL transfer function, is given by

$$H(s) = \frac{\dfrac{KF(s)F_M(s)}{s}}{1 + \dfrac{KF(s)F_M(s)}{s}} = \frac{G(s)}{1 + G(s)} \tag{1.35}$$

where we have introduced the forward loop gain $K = K_d K_o$ and the open loop gain $G(s)$

$$G(s) = \frac{KF(s)F_M(s)}{s} \tag{1.36}$$

1.5.1 Order of PLLs

In the simplest case there are no filters in the forward or the feedback paths. The PLL transfer function simplifies to

$$H(s) = \frac{K}{s + K} \tag{1.37}$$

This PLL is designated as the *first-order loop* since the largest power of s in the polynomial of the denominator is of the order *one*. Generally, the transfer functions of the loop filters $F(s)$ are given by a ratio of two polynomials in s. The consequence is that the denominator in $H(s)$ is of a higher order in s and we speak about PLLs of the *second order, third order*, and so on, in accordance with the order of the respective polynomial in the denominator of (1.35).

1.5.2 Type of PLLs

In instances in which the steady state errors are of major interest, the number of poles in the transfer function $G(s)$, that is, the number of integrators in the loop, is of importance. In principle, every PLL has one integrator connected with the VCO (cf. eq. (1.33)). For the phase error at the output of the PD we find

$$\Phi_e(s) = \Phi_i(s) - F_M(s)\Phi_o(s) \tag{1.38}$$

where

$$\Phi_o(s) = \Phi_e(s)\frac{KF(s)}{s} \tag{1.39}$$

After elimination of $\Phi_o(s)$ from the above relations, we get for the phase error $\Phi_e(s)$

$$\Phi_e(s) = \Phi_i(s)\frac{1}{1 + G(s)} \tag{1.40}$$

Introducing the gain, $G(s)$, which is a ratio of two polynomials

$$G(s) = \frac{A(s)}{s^n B(s)} \tag{1.41}$$

we get for the phase error

$$\Phi_e(s) = \Phi_i(s)\frac{s^n B(s)}{A(s) + s^n B(s)} \tag{1.42}$$

and eventually with the assistance of the Laplace limit theorem, we get for the final value of the phase error $\varphi_e(t)$

$$\lim_{t\to\infty}[\phi_e(t)] = \lim_{s\to 0}\left[\Phi_i(s)\frac{s^{n+1} B(s)}{A(s) + s^n B(s)}\right] \tag{1.43}$$

Note that every PLL contains at least one integrator, that is, VCO; consequently, $n \geq 1$ (cf. relation (1.34)).

1.5.3 Steady State Errors

Investigations of the steady state errors in PLLs of different orders and types will proceed after introduction of the Laplace transforms of the respective input phase steps, input frequency steps, and input steady frequency changes into (1.43).

$$\Delta\omega_i = \frac{\Delta\phi_i}{s}; \quad \frac{\Delta\omega_i}{s} = \frac{\Delta\phi_i}{s^2}; \quad \frac{\Delta\dot{\omega}}{s} = \frac{\Delta\omega_i}{s^2} = \frac{\Delta\phi_i}{s^3} \tag{1.44}$$

1.5.3.1 Phase steps

After introducing the Laplace transform of phase steps, $\Delta\phi/s$, into (1.43), we find out that the final value is *zero* in all PLLs.

1.5.3.2 Frequency steps

For the frequency steps, $\Delta\omega/s$, we get

$$\lim_{t\to\infty}\phi_{\mathrm{e}2}(t) = \Delta\omega_{\mathrm{i}}\left[\frac{B(0)}{A(0)}\right]_{n=1} = \frac{\Delta\omega_{\mathrm{i}}}{KF(0)F_{\mathrm{M}}(0)} = \frac{\Delta\omega_{\mathrm{i}}}{K_v} \tag{1.45}$$

Evidently in all PLLs of the second order, a frequency step results in a steady state phase error inversely proportional to the so-called *velocity error constant* K_v, in agreement with the terminology used in the feedback control systems (cf. [13]).

In PLLs of type 2, with two integrators in the loop, the DC gain $F(0)$ is very large, so K_v and consequently the steady state error is negligible.

1.5.3.3 Frequency ramps

However, the steady frequency change, $\Delta\omega/s^2$, results in the so-called *acceleration* or *dynamic tracking error* K_a

$$\lim_{t\to\infty}\phi_{\mathrm{e}3}(t) = \Delta\dot{\omega}_{\mathrm{i}}\left[\frac{B(0)}{A(0)}\right]_{n=2} = \frac{\Delta\dot{\omega}_{\mathrm{i}}}{K_a} \tag{1.46}$$

PLLs of type 3 can eliminate even the steady state error $\varphi_{\mathrm{e}3}(t)$ for $t\to\infty$ to zero. However, PLLs of this type are encountered exceptionally, for example, in time services [15], in space and satellite devices [3], and so on.

Note that the frequency locked loop may be considered as 0 *type PLL.*

1.6 BLOCK DIAGRAM ALGEBRA

Actual PLLs are often much more complicated than block diagrams in Figs. 1.3 or 1.4. For arriving at transfer functions, $H(s)$ and *1−H(s)*, we can apply the rules of *block diagram algebra* [13].

Two or more blocks in series can be combined into one after multiplication of their Laplace transform symbols (see Fig. 1.5a). A typical example is the addition of independent sections to the fundamental low-pass filter.

In the case where two blocks are in parallel, the final combination is provided with a mere addition (see Fig. 1.5b).

Investigation of the relation (1.35) reveals that the feedback block can be put outside of the basic loop [5]

$$H'(s) = \frac{1}{N}H(s) \tag{1.47}$$

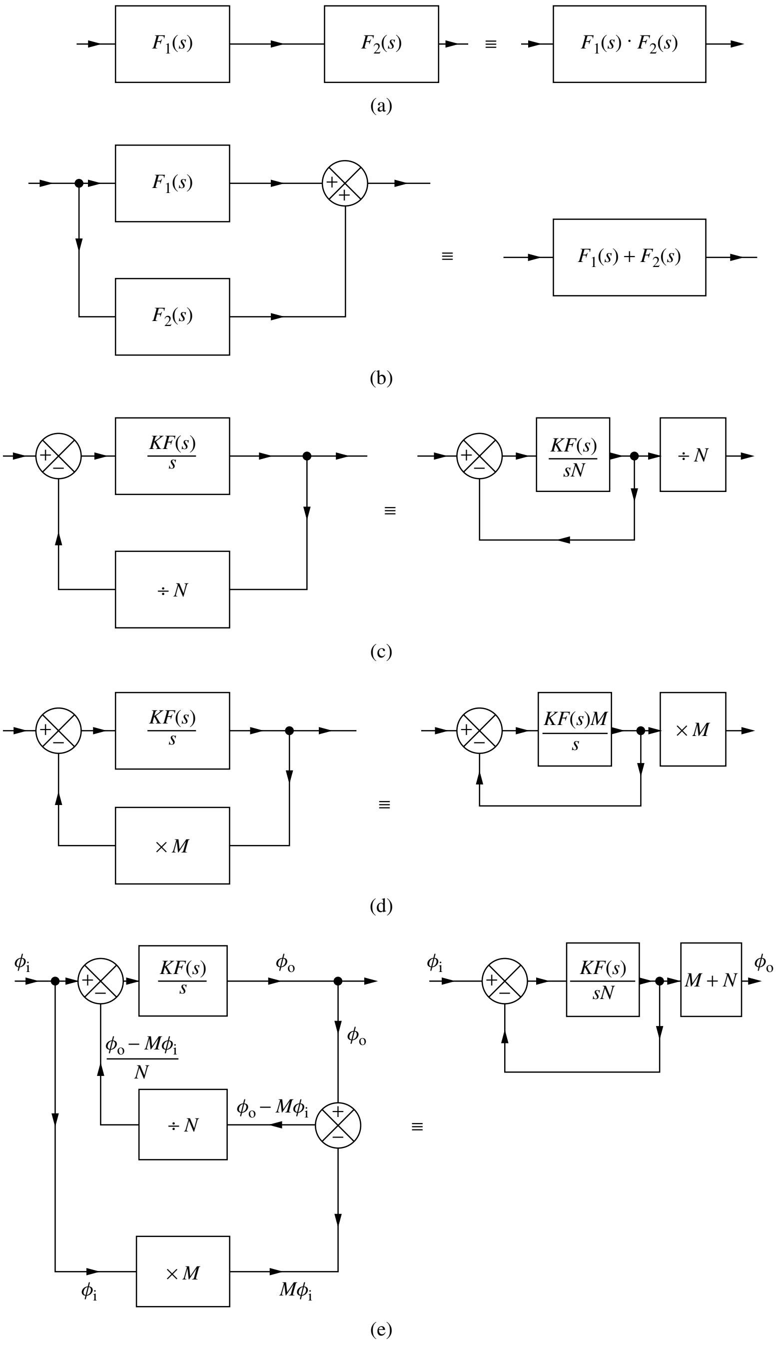

Figure 1.5 Simplification of the block diagrams of PLLs: (a) series connection; (b) parallel connection; (c) and (d) feedback arrangement; (e) more complicated system. (Reproduced from Fig. 1.20 in C.J. Savant Jr., *Basic Feedback Control System Design*. New York, Toronto, London: McGraw-Hill, 1958 by permission of McGraw Hill, 2002).

or

$$H'(s) = MH(s) \tag{1.48}$$

In this way we arrive at the effective transfer functions, $H'(s)$ and $1 - H'(s)$, which contain information about the PLL filtering properties, which will be discussed later. We appreciate this approach in instances in which a simple frequency divider or frequency multiplier is in the feedback path of the PLL. The rearrangement is reproduced in Figs. 1.5(c) and 1.5(d).

Finally, we shall consider the system containing a mixer in the feedback path. Relation between output and input phases is

$$\Phi_o(s) = \left[\Phi_i(s) - \frac{\Phi_o(s) - M\Phi_i(s)}{N}\right]\frac{KF(s)}{s} \tag{1.49}$$

and rearrangement leads to the simplification in accordance with Fig. 1.5(e).

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