1

Introduction to Power Electronic Converters

Power electronic converters are a family of electrical circuits which convert electrical energy from one level of voltage/current/frequency to another using semiconductor-based electronic switches. The essential characteristic of these types of circuits is that the switches are operated only in one of two states – either fully ON or fully OFF – unlike other types of electrical circuits where the control elements are operated in a (near) linear active region. As the power electronics industry has developed, various families of power electronic converters have evolved, often linked by power level, switching devices, and topological origins. The process of switching the electronic devices in a power electronic converter from one state to another is called *modulation,* and the development of optimum strategies to implement this process has been the subject of intensive international research efforts for at least 30 years. Each family of power converters has preferred modulation strategies associated with it that aim to optimize the circuit operation for the target criteria most appropriate for that family. Parameters such as switching frequency, distortion, losses, harmonic generation, and speed of response are typical of the issues which must be considered when developing modulation strategies for a particular family of converters.

Figure 1.1 presents a categorization of power electronic converters into families according to their type of electrical conversion. Of these families, converters that change energy to or from alternating current (AC) form involve much more complex processes than those that solely involve direct current (DC). The purpose of this book is to explore the converter modulation issue in detail as it relates to high power DC/AC (inverting) and AC/DC (rectifying) converters, with particular emphasis on the process of open-loop pulse width modulation (PWM) applied to these types of converters. This chapter presents the fundamentals of inverter structures, block-switching voltage control, and space vector concepts, as a foundation for the material to follow.

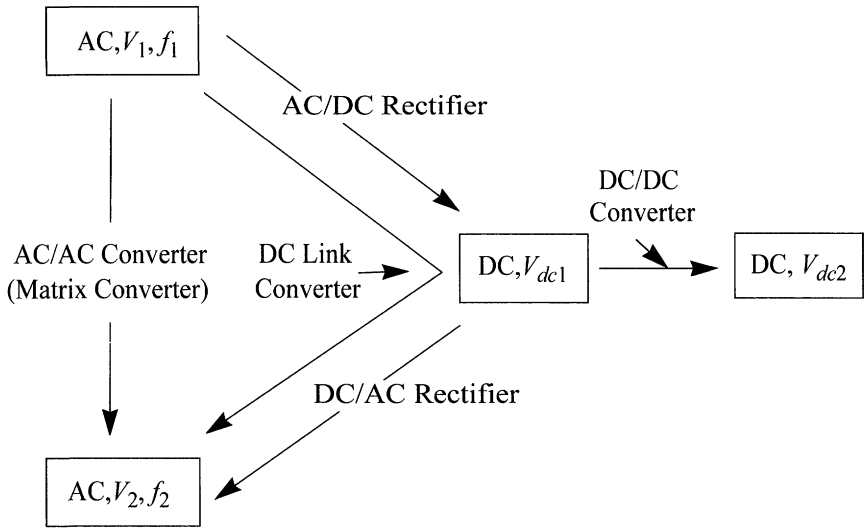

Figure 1.1 Families of solid state power converters categorized according to their conversion function.

1.1 Basic Converter Topologies

1.1.1 Switch Constraints

The transistor switch used for solid state power conversion is very nearly approximated by a resistance which either approaches zero or infinity depending upon whether the switch is closed or opened. However, regardless of where the switch is placed in the circuit, Kirchoff's voltage and current laws must, of course, always be obeyed. Translated to practical terms, these laws give rise to the two basic tenets of switch behavior:

- The switch cannot be placed in the same branch with a current source (i.e., an inductance) or else the voltage across the inductor (and consequently across the switch) will become infinite when the switch turns off. As a corollary to this statement it can be argued that *at least one* of the elements in branches connected via a node to the branch containing the switch must be non-inductive for the same reason.

- The switch cannot be placed in parallel with a voltage source (i.e., a true source or a capacitance) or else the current in the switch will become infinite when the switch turns on. As a corollary it can be stated that if more than one branch forms a loop containing the switch branch then *at least one* of these branch elements must not be a voltage source.

If the purpose of the switch is to aid in the process of transferring energy from the source to the load, then the switch must be connected in some manner so as to select between two input energy sources or sinks (including the possibility of a zero energy source). This requirement results in the presence of two branches delivering energy to one output (through a third branch). The presence of three branches in the interposing circuit implies a connecting node between these branches.

One of the three branches can contain an inductance (an equivalent current source frequently resulting from an inductive load or source), but the other branches connected to the same node must not be inductive or else the first basic tenet will be violated. The only other alternatives for the two remaining branches are a capacitance or a resistance. However, when the capacitor is connected between the output or input voltage source and the load, it violates the second tenet. The only choice left is a resistance.

The possibility of a finite resistance can be discarded as a practical matter since the circuit to be developed must be as highly efficient as possible, so that the only possibility is a resistor having either zero or infinite resistance, i.e., a second switch. This switch can only be turned on when the first switch is turned off, or vice versa, in order to not violate Kirchoff's current law. For the most common case of unidirectional current flow, a unidirectional switch which inhibits current flow in one direction can be used, and this necessary complementary action is conveniently achieved by a simple diode, since the demand of the inductance placed in the other branch will assure the required behavior. Alternatively, of course, the necessary complementary switching action can be achieved by a second unidirectional switch. The resulting circuits, shown in Figure 1.2, can be considered to be the *basic switching cells* of power electronics. The switches having arrows in (b) and (c) denote unidirectional current flow devices.

When the circuit is connected such that the current source (inductance) is connected to the load and the diode to the source, one realizes what is termed a *step-down chopper*. If the terminals associated with input and output are

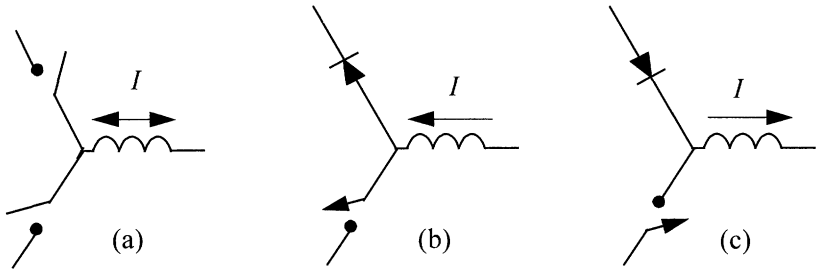

Figure 1.2 Basic commutation cells of power electronic converters using (a) bidirectional switches and (b) and (c) unidirectional switches.

reversed, a *step-up chopper* is produced. Energy is passed from the voltage source to the current "source" (i.e., the load) in the case of the step-down converter, and from the current source to the voltage "source" (load) in the case of the step-up converter.

Since the source voltage sums to the voltage across the switch plus the diode and since the load is connected across the diode only, the voltage is the quantity that is stepped down in the case of the step-down chopper. Because of the circulating current path provided by the diode, the current is consequently stepped up. On the other hand the sum of the switch plus diode voltage is equal to the output voltage in the case of the step-up chopper so that the voltage is increased in this instance. The input current is diverted from the output by the switch in this arrangement so that the current is stepped down.

Connecting the current source to both the input and output produces the *up-down chopper* configuration. In this case the switch must be connected to the input to control the flow of energy into/out of the current source. Since the average value of voltage across the inductor must equal zero, the average voltage across the switch must equal the input voltage while the average voltage across the diode equals the output voltage. Ratios of input to output voltages greater than or less than unity (and consequently current ratios less or greater than unity) can be arranged by spending more or less than half the available time over a switching cycle with the switch closed. These three basic DC/DC converter configurations are shown in Figure 1.3.

1.1.2 Bidirectional Chopper

In cases where power flow must occur in either direction a combination of a step-down and a step-up chopper with reversed polarity can be used as shown

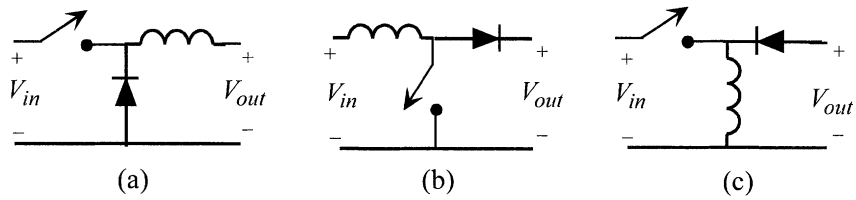

Figure 1.3 The three basic DC/DC converters implemented with a basic switching cell (a) step-down chopper, (b) step-up chopper, and (c) up-down chopper.

in Figure 1.4. The combination of the two functions effectively places the diodes in inverse parallel with switches, a combination which is pervasive in power electronic circuits. When passing power from left to right, the step-down chopper transistor is operated to control power flow while the step-up chopper transistor operates for power flow from right to left in Figure 1.4. The two switches need never be (and obviously should never be) closed at the same instant.

1.1.3 Single-Phase Full-Bridge (H–Bridge) Inverter

Consider now the basic switching cell used for DC/AC power conversion. In Figure 1.4 it is clear that current can flow bidirectionally in the current source/sink of the up-down chopper. If this component of the circuit is now considered as an AC current source load and the circuit is simply tipped on its side, the half-bridge DC/AC inverter is realized as shown in Figure 1.5. Note that in this case the input voltage is normally center-tapped into two equal DC voltages, $V_{dc1} = V_{dc2} = V_{dc}$, in order to produce a symmetrical AC voltage waveform. The total voltage across the DC input bus is then $2V_{dc}$. The parallel combination of the unidirectional switch and inverse conducting diode forms

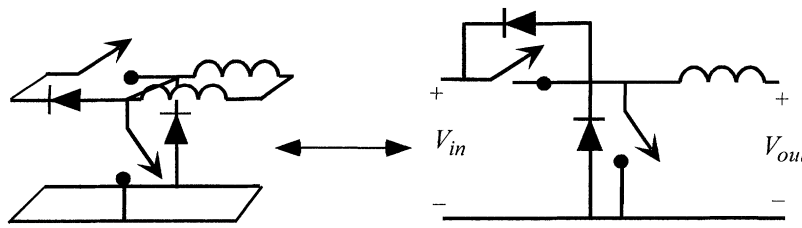

Figure 1.4 Bidirectional chopper using one up-chopper and one down-chopper.

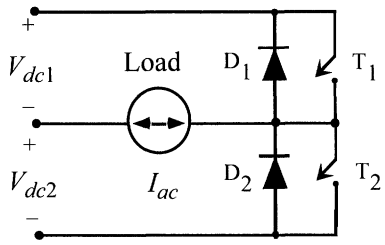

Figure 1.5 Half-bridge single-phase inverter.

the first type of practical inverter switch. The switch combination permits unidirectional current flow but requires only one polarity of voltage blocking ability and hence is suitable, in this case, for operating from a DC voltage source.

It is important to note that in many inverter circuits the center-tap point of the DC voltage shown in Figure 1.5 will not be provided. However, this point is still commonly used either as an actual ground point or else, in more elaborate inverters, as the reference point for the definition of multiple DC link voltages. Hence in this book, the total DC link voltage is considered as always consisting of a number of DC levels, and with conventional inverters that can only switch between two levels it will always be defined as $2V_{dc}$.

The structure of a single-phase full-bridge inverter (also known as a H–bridge inverter) is shown in Figure 1.6. This inverter consists of two single-phase leg inverters of the same type as Figure 1.5 and is generally preferred over other arrangements in higher power ratings. Note that as discussed above, the DC link voltage is again defined as $2V_{dc}$. With this arrangement, the maximum output voltage for this inverter is now twice that of the half-bridge inverter since the entire DC voltage can be impressed across the load, rather than only one-half as is the case for the half-bridge. This implies that for the same power rating the output current and the switch currents are one-half of those for a half-bridge inverter. At higher power levels this is a distinct advantage since it requires less paralleling of devices. Also, higher voltage is preferred since the cost of wiring is typically reduced as well as the losses in many types of loads because of the reduced current flow.

In general, the converter configurations of Figures 1.5 and 1.6 are capable of bidirectional power flow. In the case where power is exclusively or primarily intended to flow from DC to AC the circuits are designated as *inverters*, while the same circuits are designated *rectifiers* if the reverse is true. In cases

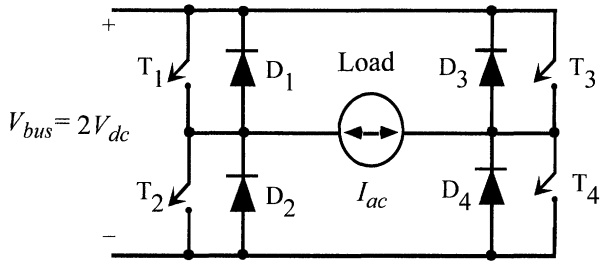

Figure 1.6 Single-phase full-bridge (H–bridge) inverter

where the DC supplies are derived from a source such as a battery, the inverter is designated as a *voltage source inverter* (VSI). If the DC is formed by a temporary DC supply such as a capacitor (being recharged ultimately, perhaps, from a separate source of energy), the inverter is designated as a *voltage stiff inverter* to indicate that the link voltage tends to resist sudden changes but can alter its value substantially under heavy load changes. The same distinction can also be made for the rectifier designations.

1.2 Voltage Source/Stiff Inverters

1.2.1 Two-Phase Inverter Structure

Inverters having additional phases can be readily realized by simply adding multiple numbers of half-bridge (Figure 1.5) and full-bridge inverter legs (Figure 1.6). A simplified diagram of a two-phase half-bridge inverter is shown in Figure 1.7(a). While the currents in the two phases can be controlled at will, the most desirable approach would be to control the two currents so that they are phase shifted by 90° with respect to each other (two-phase set) thereby producing a constant amplitude rotating field for an AC machine. However, note that the sum of the two currents must flow in the line connected to the center point of the DC supplies. If the currents in the two phases can be approximated by equal amplitude sine waves, then

$$\begin{aligned} i_{\text{neutral}} &= I\sin\omega_o t + I\sin\left(\omega_o t + \frac{\pi}{2}\right) \\ &= \sqrt{2}I\sin\left(\omega_o t + \frac{\pi}{4}\right) \end{aligned} \tag{1.1}$$

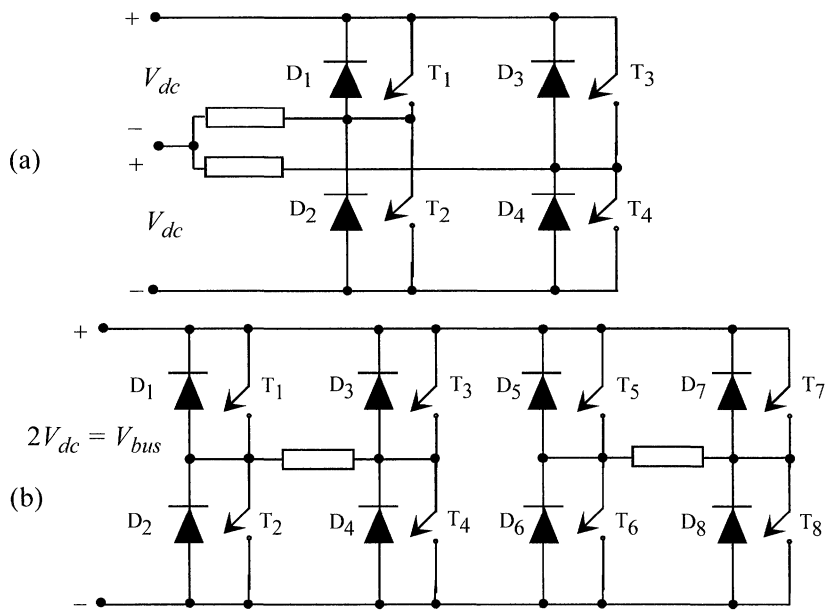

Figure 1.7 Two-phase (a) half-bridge and (b) full-bridge inverters.

Since a relatively large AC current must flow in the midpoint connection, this inverter configuration is not commonly used. As an alternative, the midpoint current could be set to zero if the currents in the two phases were made equal and opposite. However, this type of operation differs little from the single-phase bridge of Figure 1.6 except that the neutral point of the load can be considered as being grounded (i.e., referred to the DC supply midpoint). As a result this inverter topology is also not frequently used.

The full-bridge inverter of Figure 1.7(b) does not require the DC midpoint connection. However, eight switches must be used which, in most cases, makes this possibility economically unattractive.

1.2.2 Three-Phase Inverter Structure

The half-bridge arrangement can clearly be extended to any number of phases. Figure 1.8 shows the three-phase arrangement. In this case, operation of an AC motor requires that the three currents are a balanced three-phase set, i.e., equal amplitude currents with equal 120° phase displacement between them. However it is easily shown that the sum of the three currents is zero, so that the connection back to the midpoint of the DC supply is not required. The

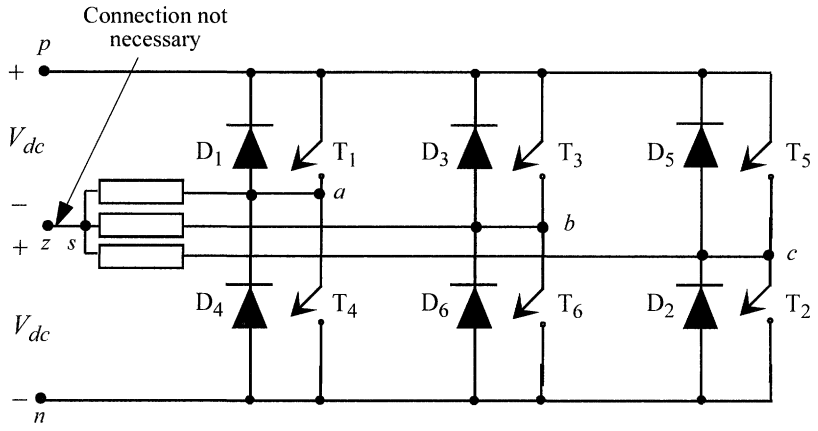

Figure 1.8 Three-phase bridge-type voltage source inverter.

simplification afforded by this property of three-phase currents makes the three-phase bridge-type inverter the de facto standard for power conversion. However while the connection from point *s* (neutral of the *star-connected stationary* load to the midpoint *z* (*zero* or *reference* point of the DC supply) need not be physically present, it remains useful to retain the midpoint *z* as the reference (ground) for all voltages. Also note that *p* and *n* are used in this text to denote the positive and negative bus voltages respectively, with respect to the midpoint *z*.

1.2.3 Voltage and Current Waveforms in Square-Wave Mode

The basic operation of the three-phase voltage inverter in its simplest form can be understood by considering the inverter as being made up of six mechanical switches. While it is possible to energize the load by having only two switches closed in sequence at one time (resulting in the possibility of one phase current being zero at instances in a switching cycle), it is now accepted that it is preferable to have one switch in each phase leg closed at any instant. This ensures that all phases will conduct current under any power factor condition. If two switches of each phase leg are turned on for a half cycle each in nonoverlapping fashion, this produces the voltage waveforms of Figure 1.9 at the output terminals *a, b,* and *c*, referred to the negative DC bus *n*. The numbers on the top part of the figure indicate which switches of Figure 1.8 are closed. The sequence is in the order 123, 234, 345, 456, 561, 612, and back to 123.

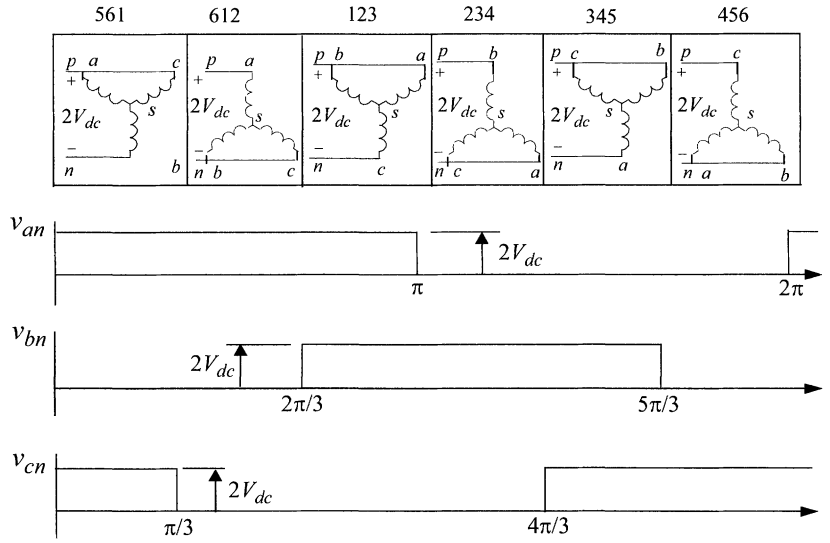

Figure 1.9 The six possible connections of a simple three-phase voltage stiff inverter. The three waveforms show voltages from the three-phase leg outputs to the negative DC bus voltage.

The line-to-line (*l–l*) voltage v_{ab} then has the *quasi-square* waveform shown in Figure 1.10. As will be shown shortly, the line-to-line voltage contains a root-mean-square (RMS) fundamental component of

$$V_{1,\,ll,\,rms} = \frac{2\sqrt{6}V_{dc}}{\pi} \cong 1.56V_{dc} \tag{1.2}$$

Thus, a standard 460 V, 60 Hz induction motor would require 590 V at the DC terminals of the motor to operate the motor at its rated voltage and speed. For this reason a 600 V DC bus (i.e., $V_{dc} = 300$ V) is quite standard in the United States for inverter drives.

Although motors function as an active rather than a passive load, the effective impedances of each phase are still *balanced.* That is, insofar as voltage drops are concerned, active as well as passive three-phase loads may be represented by the three equivalent impedances [and electromotive forces (EMFs)] shown in Figure 1.10 for the six possible connections. Note that each individual phase leg is alternately switched from the positive DC rail to the negative DC rail and that it is alternately in series with the remaining two phases con-

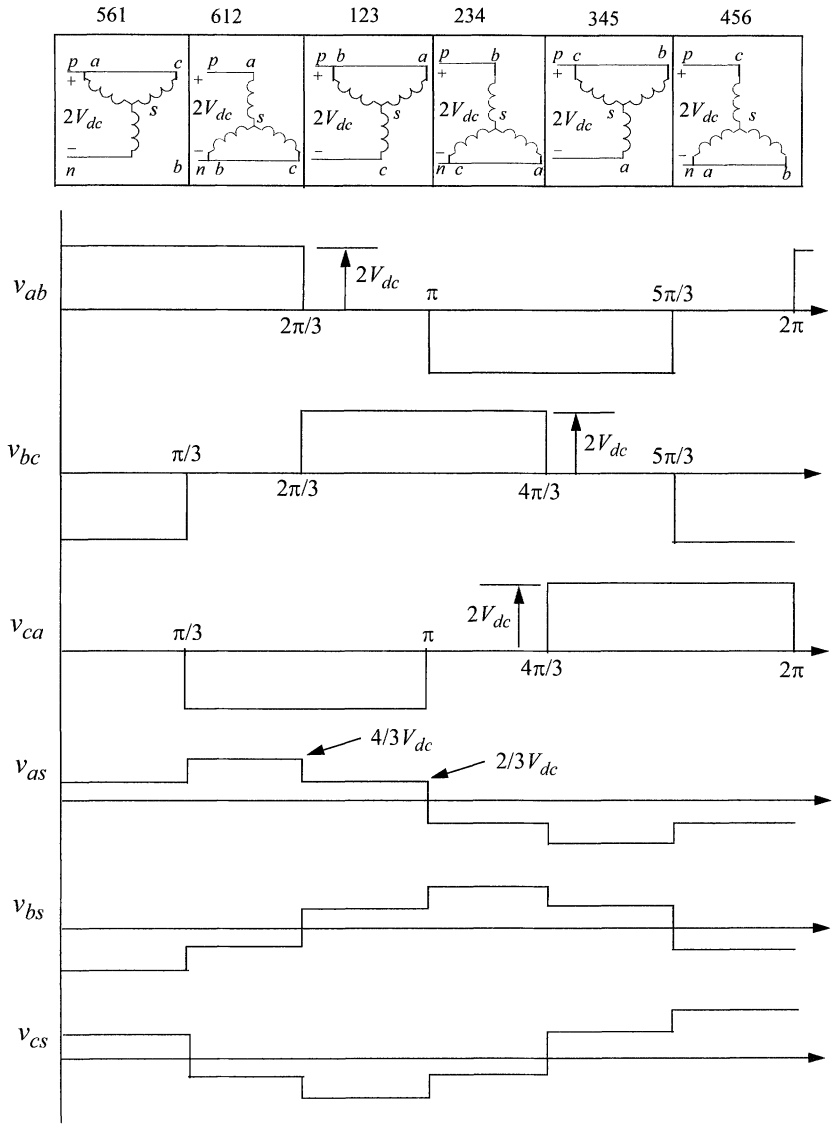

Figure 1.10 The three line-to-line and line-to-neutral load voltages created by the six possible switch connection arrangements of a six-step voltage stiff inverter.

nected in parallel, or it is in parallel with one of the other two phases and in series with the third. Hence the voltage drop across each phase load is always one-third or two-thirds of the DC bus voltage, with the polarity of the voltage

drop across the phase being determined by whether it is connected to the positive or negative DC rail.

A plot of the line and phase voltages for a typical motor load is included in Figure 1.10. The presence of six "steps" in the load line-to-neutral voltage waveforms v_{as}, v_{bs}, and v_{cs}, is one reason this type of inverter is called a *six-step* inverter, although the term *six-step* in reality pertains to the method of voltage/frequency control rather than the inverter configuration itself.

A Fourier analysis of these waveforms indicates a simple square-wave type of geometric progression of the harmonics. When written as an explicit time function, the Fourier expansion for the time-varying *a* phase to negative DC bus voltage *n* can be readily determined to be

$$v_{an}(t) = V_{dc}\frac{4}{\pi}\left[\frac{\pi}{4} + \sin\omega_o t + \frac{1}{3}\sin 3\omega_o t + \frac{1}{5}\sin 5\omega_o t + \frac{1}{7}\sin 7\omega_o t + \cdots\right] \quad (1.3)$$

The *b* and *c* phase to negative DC bus voltages can be found by replacing $\omega_o t$ with $(\omega_o t - 2\pi/3)$ and $(\omega_o t + 2\pi/3)$, respectively, in Eq. (1.3).

The v_{ab} line-to-line voltage is found by subtracting v_{bn} from v_{an} to give

$$v_{ab}(t) = V_{dc}\frac{4\sqrt{3}}{\pi}\left[\sin\left(\omega_o t + \frac{\pi}{6}\right) + \frac{1}{5}\sin\left(5\omega_o t - \frac{\pi}{6}\right) + \frac{1}{7}\sin\left(7\omega_o t + \frac{\pi}{6}\right) + \cdots\right] \quad (1.4)$$

Similar relationships can be readily found for the v_{bc} and v_{ca} voltages, phase shifted by $-2\pi/3$ and $+2\pi/3$, respectively. Note that harmonics of the order of multiples of three are absent from the line-to-line voltage, since these *triplen* harmonics cancel between the phase legs.

In terms of RMS values, each harmonic of the line-to-neutral voltages has the value of

$$V_{n,ln,rms} = V_{dc}\frac{2\sqrt{2}}{\pi}\frac{1}{n} \quad (1.5)$$

and, for the line-to-line voltages,

$$V_{n,ll,rms} = V_{dc}\frac{2\sqrt{6}}{\pi}\frac{1}{n} \quad \text{where } n = 6k \pm 1,\ k = 1,2,3,\ldots \quad (1.6)$$

Because of its utility as a reference value for pulse width modulation in later chapters, it is useful to write the fundamental component of the line-to-neutral voltage in terms of its peak value referred to half the DC link voltage, in which case

$$V_{1,ln,pk} = \frac{4}{\pi} V_{dc} = V_1 \tag{1.7}$$

This value is, of course, the fundamental component of a square wave of amplitude V_{dc}. It should be noted also that since the use of peak rather than RMS quantities will predominate in this book, quantities in capital letters will denote only DC or peak AC quantities. Hence, for simplicity V_1 in Eq. (1.7) has the same meaning as $V_{1,ln,pk}$. When the quantity is intended to be root-mean-square, the subscript *rms* will always be appended. For example, the term $V_{1,ln,rms}$ designates the RMS fundamental value of the line-to-neutral voltage.

Assuming an *R–L*–EMF load, the current as well as voltage waveforms are sketched for both wye and delta connections in Figure 1.11(a). Note that when the inverter current flows in opposite polarity to the voltage, the current is carried by the feedback diode (in a step-up chopper mechanism) in much the same manner as for the single-phase inverter. The transfer of current from main to auxiliary switches is illustrated by the conduction pattern of Figure 1.11 and can be used to determine the DC side inverter current waveform I_{dc}. For example, from the moment that T_3 is turned off to the instant that D_2 turns on, the input current is equal to the current in T_1, that is, i_a. This interval lasts one-sixth of a period or 60°. During the next 60°, switch T_6 returns current to the

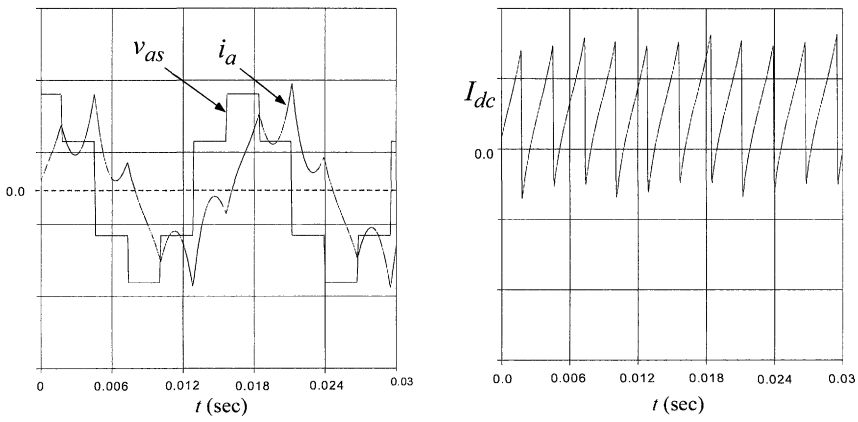

Figure 1.11 Current flow in three-phase voltage stiff inverter: (a) phase voltage and current waveform, wye-connected load, and (b) DC link current.

DC link. In effect, the link current is equal to $-i_c$. Continuing through all six 60° intervals generates the DC link current shown in Figure 1.11(b). For the case shown, I_{dc} is both positive and negative so that a certain amount of energy transfers out of and into the DC supplies. If the load current is considered to be sinusoidal, it can be shown that I_{dc} is always positive only when the fundamental power factor is greater than 0.55. However, in any case, the source supplies the average component of the link current while a current with frequency six times the fundamental frequency component circulates in and out of the DC capacitor. The sizing of the capacitor to accommodate these harmonics, regardless of the modulation algorithm, is a major consideration in inverter design.

1.3 Switching Function Representation of Three-Phase Converters

The basic three-phase inverter circuit operation shown in Figures 1.9 and 1.10 can be condensed to equation form by defining logic-type *switching functions* which express the closure of the switches [1, 2][1]. For example, let $m_1, m_2, \ldots, m_6$ take on the value "+1" when switches $T_1, T_2, \ldots, T_6$ are closed and the value "zero" when opened. The voltages from the three-phase legs to the DC center point can then be expressed as

$$\begin{aligned} v_{az} &= V_{dc}(m_1 - m_4) \\ v_{bz} &= V_{dc}(m_3 - m_6) \\ v_{cz} &= V_{dc}(m_5 - m_2) \end{aligned} \tag{1.8}$$

Considering now the constraints imposed by the circuit it is apparent that both the top and bottom switches of a given phase cannot be closed at the same time. Furthermore, from current continuity considerations in each phase leg

$$\begin{aligned} m_1 + m_4 &= 1 \\ m_3 + m_6 &= 1 \\ m_5 + m_2 &= 1 \end{aligned} \tag{1.9}$$

1 References referred to throughout this text are given at the end of each chapter. A more exhaustive set of references are located in the Bibliography.

Substituting Eq. (1.9) into Eq. (1.8) gives

$$\begin{aligned} v_{az} &= V_{dc}(2m_1 - 1) \\ v_{bz} &= V_{dc}(2m_3 - 1) \\ v_{cz} &= V_{dc}(2m_5 - 1) \end{aligned} \tag{1.10}$$

Since the quantities in the parentheses of Eq. (1.10) take on the values ± 1, it is useful to define new variables m_a, m_b, m_c, such that $m_a = 2m_1 - 1$, etc. Hence, more compactly,

$$\begin{aligned} v_{az} &= V_{dc}m_a \\ v_{bz} &= V_{dc}m_b \\ v_{cz} &= V_{dc}m_c \end{aligned} \tag{1.11}$$

The current in the DC link can be expressed as

$$I_{dc} = i_a\frac{m_a + 1}{2} + i_b\frac{m_b + 1}{2} + i_c\frac{m_c + 1}{2} \tag{1.12}$$

However, since

$$i_a + i_b + i_c = 0$$

Equation (1.12) reduces to

$$I_{dc} = \frac{1}{2}(i_a m_a + i_b m_b + i_c m_c) \tag{1.13}$$

The line-to-line AC voltages are

$$\begin{aligned} v_{ab} &= v_{az} - v_{bz} = V_{dc}(m_a - m_b) \\ v_{bc} &= v_{bz} - v_{cz} = V_{dc}(m_b - m_c) \\ v_{ca} &= v_{cz} - v_{az} = V_{dc}(m_c - m_a) \end{aligned} \tag{1.14}$$

If the load is star connected, the load line-to-neutral (phase) voltages can be expressed as

$$\begin{aligned} v_{as} &= v_{az} - v_{sz} \\ v_{bs} &= v_{bz} - v_{sz} \\ v_{cs} &= v_{cz} - v_{sz} \end{aligned} \tag{1.15}$$

For most practical cases, the phase impedances in all three legs of the star load are the same. Hence, in general,

$$\begin{aligned} v_{as} &= Z(p)i_a \\ v_{bs} &= Z(p)i_b \\ v_{cs} &= Z(p)i_c \end{aligned} \tag{1.16}$$

where the operator $p = d/dt$ and the impedance $Z(p)$ is an arbitrary function of p (which is the same in each phase). The phase voltages can now be solved by adding together the three parts of Eq. (1.16), to produce

$$\begin{aligned} v_{as} + v_{bs} + v_{cs} &= v_{az} + v_{bz} + v_{cz} - 3v_{sz} \\ &= Z(p)(i_a + i_b + i_c) = 0 \end{aligned} \tag{1.17}$$

Thus

$$\begin{aligned} v_{sz} &= \frac{1}{3}(v_{az} + v_{bz} + v_{cz}) \\ &= \frac{1}{3}V_{dc}(m_a + m_b + m_c) \end{aligned} \tag{1.18}$$

The phase voltages can now be expressed as

$$v_{as} = \frac{2}{3}v_{az} - \frac{1}{3}v_{bz} - \frac{1}{3}v_{cz} \tag{1.19}$$

so that, from Eq. (1.8),

$$v_{as} = V_{dc}\left(\frac{2}{3}m_a - \frac{1}{3}m_b - \frac{1}{3}m_c\right) \tag{1.20}$$

Similarly

$$v_{bs} = V_{dc}\left(\frac{2}{3}m_b - \frac{1}{3}m_a - \frac{1}{3}m_c\right) \tag{1.21}$$

$$v_{cs} = V_{dc}\left(\frac{2}{3}m_c - \frac{1}{3}m_a - \frac{1}{3}m_b\right) \tag{1.22}$$

Finally, the power flow through the inverter is given by

$$P_{dc} = 2V_{dc}I_{dc} = V_{dc}(i_a m_a + i_b m_b + i_c m_c) \tag{1.23}$$

Equations (1.20) to (1.22) are convenient for use in defining switching functions representing the converter's behavior in different frames of reference [2].

1.4 Output Voltage Control

A power electronic inverter is essentially a device for creating a variable AC frequency output from a DC input. The frequency of the output voltage or current is readily established by simply switching for equal time periods to the positive and the negative DC bus and appropriately adjusting the half-cycle period. However, the variable frequency ability is nearly always accompanied by a corresponding need to adjust the amplitude of the fundamental component of the output waveform as the frequency changes, i.e., *voltage control.* This section introduces the concept of voltage control, a central theme of this book.

1.4.1 Volts/Hertz Criterion

In applications involving AC motors, the load can be characterized as being essentially inductive. Since the time rate of change of flux linkages λ in an inductive load is equal to the applied voltage, then

$$\lambda = \int v \, dt \tag{1.24}$$

If one is only concerned with the fundamental component, then, if a phase voltage is of the form $v = V_1 \cos \omega_o t$, the corresponding flux linkage is

$$\lambda_1 = \frac{V_1}{\omega_o} \sin \omega_o t \tag{1.25}$$

suggesting that the fundamental component of voltage must be varied in proportion to the frequency if the amplitude of the flux in the inductive load is to remain sensibly constant.

1.4.2 Phase Shift Modulation for Single-Phase Inverter

The method by which voltage adjustment is accomplished in a solid state power converter is the heart of the issue of *modulation.* Much more detail will be developed concerning modulation techniques in later chapters. However, a very simple introductory example of modulation can be obtained by taking a single-phase inverter as shown in Figure 1.12(a) and operating each phase leg with a 50% duty cycle but with a phase delay of $\pi - \alpha$ between the two phase legs. Typical waveforms for this inverting operation (DC-to-AC power conversion) in what can be termed *phase shift voltage control* or *phase shift modula-*

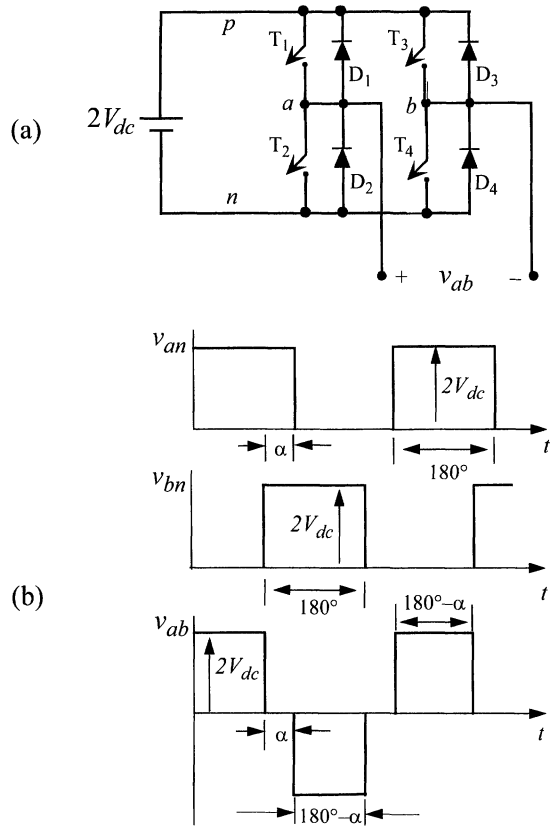

Figure 1.12 Full-bridge, single-phase inverter control by phase shift cancellation: (a) power circuit and (b) voltage waveforms.

tion are shown in Figure 1.12(b). Clearly, as the phase delay angle α changes, the RMS magnitude of the line-to-line output voltage changes.

The switched output voltage of this inverter can be represented as the sum of a series of harmonic components (a Fourier series in fact). The magnitude of each harmonic can be conveniently evaluated using the quantity $\beta = 90° - \alpha/2$ where α is as shown in Figure 1.12. Conventional Fourier analysis gives, for each harmonic n, a peak harmonic magnitude of

$$V_{ab(n)} = \frac{2}{\pi} \int_{-\pi/2}^{\pi/2} 2V_{dc} \cos n\theta \, d\theta \tag{1.26}$$

$$= V_{dc}\frac{4}{\pi}\int_{-\beta}^{\beta}\cos n\theta d\theta$$

$$= V_{dc}\frac{8}{\pi n}\sin n\beta$$

$$= V_{dc}\frac{8}{\pi n}\cos\frac{n\alpha}{2} \qquad \text{where } n \text{ is odd} \tag{1.27}$$

Figure 1.13 shows the variation of the fundamental frequency and harmonic components as a function of the overlap angle α. The components are normalized with respect to $2V_{dc}$.

1.4.3 Voltage Control with a Double Bridge

While voltage control is not possible with a conventional six-step inverter without adjusting the DC link voltage, some measure of voltage control is pos-

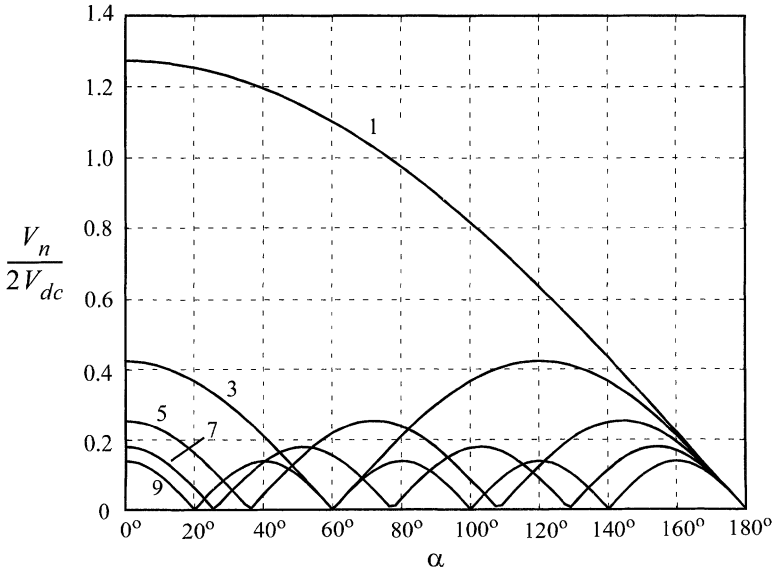

Figure 1.13 First five odd (nonzero) harmonic components of single-phase inverter with phase shift control as a function of phase shift angle α normalized with respect to $2V_{dc}$.

sible with a double bridge as shown in Figure 1.14. Note that this type of bridge is essentially three single-phase bridges so that voltage control can again be accomplished by phase shifting in much the same manner as the overlap method described by Figure 1.12. To avoid short circuits the three-phase load must either be separated into three electrically isolated single-phase loads or a transformer must be used to provide electrical isolation. Figure 1.14 shows the output phase voltages of this inverter.

Recall also that when the phase output voltages are coupled through a transformer into a three-phase voltage set with a common neutral, harmonics of multiples of three are eliminated in the line-to-line output voltages by virtue of the 120° phase shift between the quasi square waves of each phase.

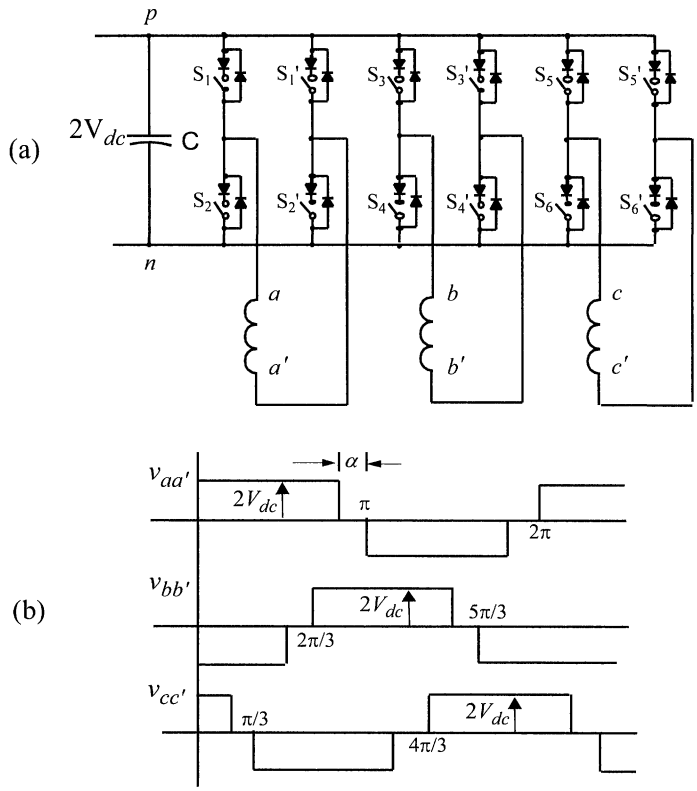

Figure 1.14 Double three-phase bridge arrangement: (a) basic circuit and (b) voltage waveforms.

1.5 Current Source/Stiff Inverters

Up to this point the focus has been on the most popular class of power converters, i.e., those operating with a voltage source or with a stiff capacitor on the DC side of the converter. However, another class of inverters evolve from the dual concept of a current source or stiff inductor on the DC side. These converters can be developed from essentially the same starting point using the basic commutation cells of Figure 1.2, except that the diode is replaced with a second switch in order to have complete control over the direction of the inductor current. Figure 1.15 briefly depicts the evolution of the three-phase current source/stiff inverter. In Figure 1.15(a) the current source commutation cell is shown, and in Figure 1.15(b) the inductor is chosen as the source so that the switch branches become loads. Since the switch branches are connected in series with the load, these loads must clearly be noninductive so as to not produced infinite voltage spikes across the switches. In order to create AC currents in the load two such commutation cells are used – one to produce positive current and the other to produce negative current in the load as shown in Figure 1.15(c). A single-phase bridge is produced by recognizing that no current need flow in the center point connection between the two current sources if they produce the same amplitude of current, as shown in Figure 1.15(d). Finally, a third phase is added in the same manner to produce a three-phase current source inverter, Figure 1.15(e). This evolution realizes the second practical switch combination suitable for DC current sources, a bidirectional voltage blocking, unidirectional current conducting switch. At the present time, such a switch is typically realized by a series-connected transistor and diode arrangement, as shown in Figure 1.15(f).

The basic switching strategy for this converter can again be summarized using switching functions. If $m_1, m_2, \ldots, m_6$ are defined as +1 when switches $T_1, T_2, \ldots, T_6$ are closed and zero when they are open, then to ensure current continuity in the DC side inductor, it is evident from current continuity considerations and Figure 1.15 that

$$m_1 + m_3 + m_5 = 1 \tag{1.28}$$

and

$$m_2 + m_4 + m_6 = 1 \tag{1.29}$$

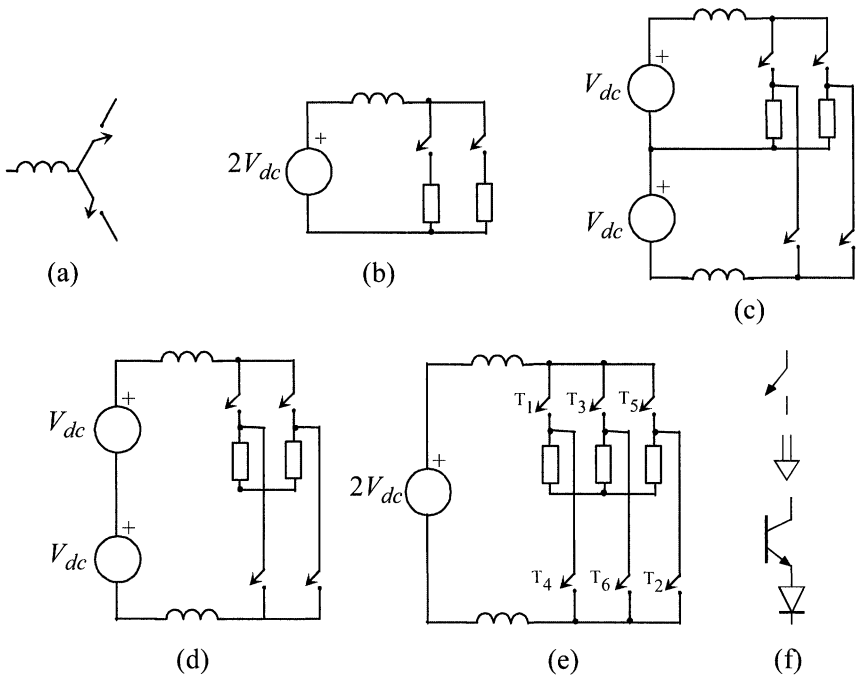

Figure 1.15 Evolution of three-phase current source/stiff inverter from basic commutation cell.

The load currents can also be defined as

$$\begin{aligned} i_a &= I_{dc}(m_1 - m_4) \\ i_b &= I_{dc}(m_3 - m_6) \\ i_c &= I_{dc}(m_5 - m_2) \end{aligned} \tag{1.30}$$

The line voltages can then be expressed in terms of the switching functions as

$$\begin{aligned} v_{ab} &= 2V_{dc}(m_1 m_6 - m_4 m_3) \\ v_{bc} &= 2V_{dc}(m_3 m_2 - m_6 m_5) \\ v_{ca} &= 2V_{dc}(m_5 m_4 - m_2 m_1) \end{aligned} \tag{1.31}$$

where it is assumed that the voltage drop across the link inductor is negligible for any reasonable size of inductor, since the current will then be very nearly constant.

The phase voltages can be determined in much the same manner as for the voltage link converter, i.e.,

$$\begin{aligned} v_{an} &= v_{as} + v_{sn} \\ v_{bn} &= v_{bs} + v_{sn} \\ v_{cn} &= v_{cs} + v_{sn} \end{aligned} \tag{1.32}$$

where n again represents the voltage at the negative bus of the DC link voltage and s denotes the center point of the load. Adding together the voltages of Eq. (1.32) gives

$$\begin{aligned} v_{an} + v_{bn} + v_{cn} &= v_{as} + v_{bs} + v_{cs} + 3v_{sn} \\ &= 0 + 3v_{sn} \end{aligned} \tag{1.33}$$

from which

$$\begin{aligned} v_{sn} &= \frac{1}{3}(v_{an} + v_{bn} + v_{cn}) \\ &= \frac{2}{3}(m_1 + m_3 + m_5)V_{dc} \\ &= \frac{2}{3}V_{dc} \end{aligned} \tag{1.34}$$

Thus

$$\begin{aligned} v_{as} &= \left(m_1 - \frac{1}{3}\right)2V_{dc} \\ v_{bs} &= \left(m_3 - \frac{1}{3}\right)2V_{dc} \\ v_{cs} &= \left(m_5 - \frac{1}{3}\right)2V_{dc} \end{aligned} \tag{1.35}$$

A plot of the load current assuming a star- and wye-connected load is given in Figure 1.16. If the load is inductive, it is apparent that the idealized current waveforms of Figure 1.16 would produce infinite spikes of voltage. Hence, strictly speaking, the harmonic content for this converter is infinite. In reality, the slopes corresponding to the rapidly changing *di/dt* would not be infinite but would change at a rate dominated by the capacitance of a commutating circuit. For example, the autosequentially commutated inverter (ASCI) of Figure 1.17 is widely used for implementing a current source/stiff converter. Alternatively, capacitive filters can be placed on AC output terminals to absorb the rapid changes in current.

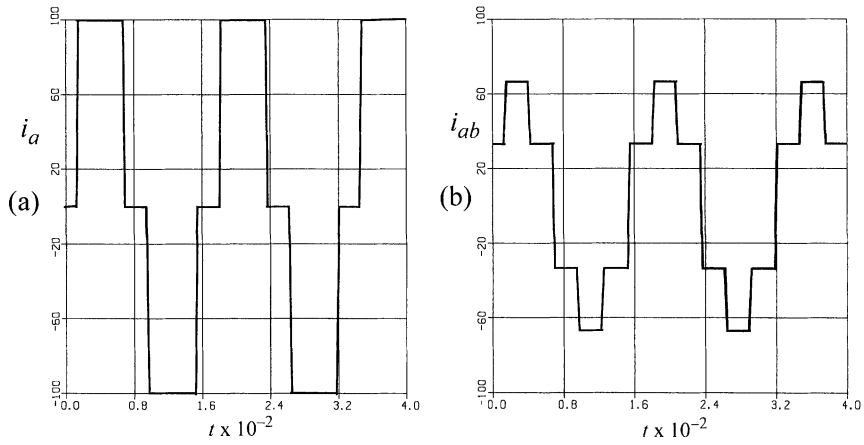

Figure 1.16 Current source inverter waveforms: (a) line current for a star-connected load and (b) phase current for a delta-connected load assuming a DC link current of 100 A.

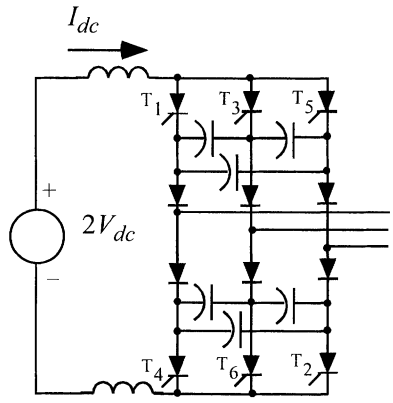

Figure 1.17 Autosequentially commutated current source/stiff converter.

1.6 Concept of a Space Vector

The highly coupled nature of inverter loads such as induction and synchronous machines has led to the use of artificial variables rather than actual (phase) variables for the purpose of simulation as well as for visualization. The essence of the nature of the transformation of variables that is utilized can be under-

stood by reference to Figure 1.18, which shows three-dimensional orthogonal axes labeled *a*, *b,* and *c* [3]. Consider, for instance, the stator currents of a three-phase induction machine load which is, in general, made up of three independent variables. These currents (phase variables) can be visualized as being components of a single three-dimensional vector (*space vector*) existing in a three-dimensional orthogonal space, i.e., the space defined by Figure 1.18. The projection of this vector on the three axes of Figure 1.18 produces the instantaneous values of the three stator currents.

In most practical cases as has been noted already, the sum of these three currents adds up to zero since most three-phase loads do not have a neutral return path. In this case, the stator current vector is constrained to exist only on a plane defined by

$$i_a + i_b + i_c = 0 \tag{1.36}$$

The fact that Eq. (1.36) defines a particular plane is evident if it is recalled from analytic geometry that the general definition of a plane is $ax + by + cz = d$. This plane, the so-called *d–q plane*, is also illustrated in Figure 1.18. Components of the current and voltage vector in the plane are called the *d–q components* while the component in the axis normal to the plane (in the event that the currents do not sum to zero) is called the *zero component.*

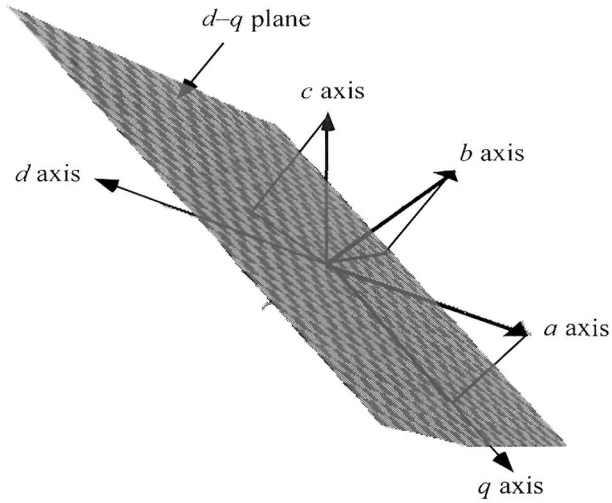

Figure 1.18 Cartesian coordinate system for phase variables showing location of the *d–q* plane and projection of phase variables onto the plane.

When the phase voltages and phase flux linkages also sum to zero, as is the case with most balanced three-phase loads (including even a salient pole synchronous machine), this same perspective can be applied to these variables as well. By convention it is assumed that the projection of the phase a axis on the d–q plane forms the reference q axis for the case where the d–q axes are not rotating. A second axis on the plane is defined as being orthogonal to the q axis such that the cross product $d \times q$ yields a third axis, by necessity normal to the d–q plane, that produces a third component of the vector having the conventional definition of the zero sequence quantity. The components of the phase current, phase voltage, or phase flux linkage vectors in the d–q–0 stationary coordinate system in terms of the corresponding physical variables are

$$\begin{bmatrix} f_q^s \\ f_d^s \\ f_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{1.37}$$

where f is a general variable used to denote the current variable i, voltage v, flux linkage λ or charge q. The superscript s on the d–q variable is used to denote the case where the d–q axes are *stationary* and fixed in the d–q plane.

In the dominant case where the three-phase variables sum to zero (i.e., the corresponding current, voltage, and flux linkage vectors are located on the d–q plane and have no zero sequence component) this transformation reduces to

$$\begin{bmatrix} f_q^s \\ f_d^s \\ f_0 \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{3}{2}} & 0 & 0 \\ 0 & -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{1.38}$$

where the last row is now clearly not necessary and often can be discarded.

Figure 1.19 shows the location of the various axes when projected onto the d–q plane. Note that the projection of the a phase axis on the d–q plane is considered to be lined up with the q axis (the a phase axis corresponds to the magnetic axis of phase a in the case of an electrical machine). The other axis on the

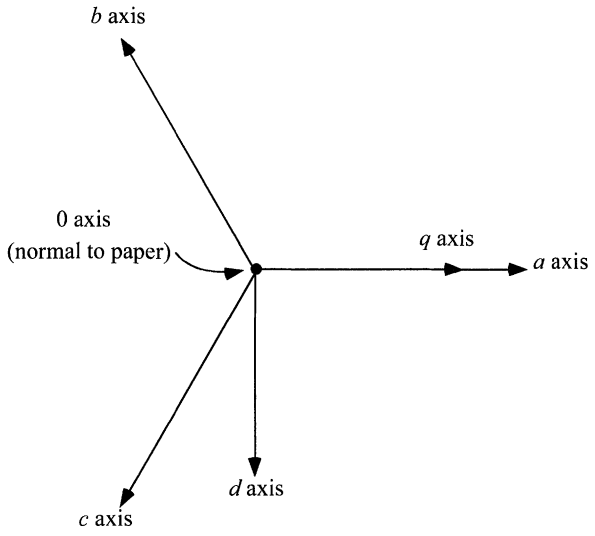

Figure 1.19 Physical *a–b–c* and conceptual stationary frame *d–q–*0 axes when viewed from an axis normal to the *d–q* plane.

plane is, by convention, located 90° clockwise with respect to the *q* axis. The third axis (necessarily normal to the *d–q* plane) is chosen such that the sequence *d–q–*0 forms a right-hand set.

Sometimes another notation, using symbols α,β (Clarke's components), is used to denote these same variables. However, the third component, Fortesque's zero sequence component, is normally not scaled by the same factor as the two Clarke components, and this can cause some confusion. With the transformation shown, when viewed from the zero sequence axis, the *d* axis is located 90° clockwise with respect to the *q* axis. Unfortunately, these two axes are sometimes interchanged so that the reader should exercise caution when referring to the literature. When the *d–q* axes are fixed in predefined positions in the *d–q* plane, they are said to define the *stationary reference frame* [2].

1.6.1 *d–q–*0 Components for Three-Phase Sine Wave Source/Load

When balanced sinusoidal three-phase AC voltages are applied to a three-phase load, typically, with respect to the supply midpoint *z*

$$
\begin{aligned}
v_{az} &= V_1 \sin \omega_o t \\
v_{bz} &= V_1 \sin\left(\omega_o t - \frac{2\pi}{3}\right) \\
v_{cz} &= V_1 \sin\left(\omega_o t + \frac{2\pi}{3}\right)
\end{aligned}
\tag{1.39}
$$

It can be recalled from Eqs. (1.15) and (1.16) that for a three-wire wye-connected load with balanced impedances the load voltages can be expressed in terms of the supply voltages as [2]

$$
\begin{aligned}
v_{az} &= v_{as} + v_{sz} = Z(p) i_a + v_{sz} \\
v_{bz} &= v_{bs} + v_{sz} = Z(p) i_b + v_{sz} \\
v_{cz} &= v_{cs} + v_{sz} = Z(p) i_c + v_{sz}
\end{aligned}
\tag{1.40}
$$

where, again, s is the load neutral point, p represents the time derivative operator $p = d/(dt)$, and $Z(p)$ denotes the impedance operator made up of an arbitrary circuit configuration of resistors, inductors, and capacitors. If the circuit is at rest at $t = 0$, then summing the rows of Eq. (1.40) gives

$$
v_{az} + v_{bz} + v_{cz} = Z(p)(i_a + i_b + i_c) + 3v_{sz} \tag{1.41}
$$

Since the three currents sum to zero and $Z(p)$ is common to all three-phases, the voltage between load neutral and inverter zero voltage points, for balanced loads but arbitrary source voltages, is

$$
v_{sz} = \frac{1}{3}(v_{az} + v_{bz} + v_{cz}) \tag{1.42}
$$

In the special case of balanced source voltages [Eq. (1.39)] the right-hand side of Eq. (1.42) is zero and the corresponding phase and source voltages are identical. From this result it can readily be determined that, in the d–q–0 coordinate system,

$$
\begin{aligned}
v_{qs}^{s} &= \sqrt{\frac{3}{2}} V_1 \sin \omega_o t \\
v_{ds}^{s} &= -\sqrt{\frac{3}{2}} V_1 \cos \omega_o t \\
v_{0s}^{s} &= 0
\end{aligned}
\tag{1.43}
$$

The use of the subscript s used here to denote the load neutral point can be remembered as the *star point*, *c(s)enter point*, or *neutral point* of the stationary circuit. It should be apparent from the orthogonality of the d–q axes and the

sine/cosine relationships that the phase voltage vector traces out a circle on the d–q plane with radius $\sqrt{\frac{3}{2}}V_1$ where V_1 is the amplitude of the phase voltage. The vector rotates with an angular velocity equal to the angular frequency of the source voltage (377 rad/s in the case of 60 Hz). The current and flux linkage vectors, being a consequence of applying the voltage to a linear, balanced load will also trace out circles on the d–q plane in the steady state.

The fact that the length of the rotating vector differs from the amplitude of the sinusoidal variable has prompted researchers to introduce methods to "correct" this supposed deficiency. The difference in length essentially comes about because the a–b–c axes are not in the plane of the d–q axes but have a component in the third direction (0 axis) as evidenced by the third row of Eq. (1.37). However, if the transformation of Eq. (1.37) is multiplied by $\sqrt{2/3}$ a scale change is made in moving from a–b–c to d–q–0 variables which eliminates this difference. The transformation becomes

$$\begin{bmatrix} f_{qs}^{s} \\ f_{ds}^{s} \\ f_{0s} \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & -\frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \\ \frac{\sqrt{2}}{3} & \frac{\sqrt{2}}{3} & \frac{\sqrt{2}}{3} \end{bmatrix} \begin{bmatrix} f_{as} \\ f_{bs} \\ f_{cs} \end{bmatrix} \tag{1.44}$$

with the inverse relationship of

$$\begin{bmatrix} f_{as} \\ f_{bs} \\ f_{cs} \end{bmatrix} = \begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} f_{qs}^{s} \\ f_{ds}^{s} \\ f_{0s} \end{bmatrix} \tag{1.45}$$

Since the same scale change has been made for all three components, the zero component uses somewhat unconventional scaling. More conventionally, Fortesque's scaling for this component is

$$f_{0s} = \frac{1}{3}(f_{as} + f_{bs} + f_{cs}) \tag{1.46}$$

and is also widely used. When the projection of the vector on the zero sequence axis is zero, Eq. (1.44) reduces to

$$\begin{bmatrix} f_{qs}^{s} \\ f_{ds}^{s} \\ f_{0s} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & -\frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} f_{as} \\ f_{bs} \\ f_{cs} \end{bmatrix} \tag{1.47}$$

or inversely as

$$\begin{bmatrix} f_{as} \\ f_{bs} \\ f_{cs} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 0 \end{bmatrix} \begin{bmatrix} f_{qs}^{s} \\ f_{ds}^{s} \\ f_{0s} \end{bmatrix} \tag{1.48}$$

Note that Eq. (1.47) does not formally have an inverse, but a suitable equivalent can be obtained by first inverting Eq. (1.44) and then setting the zero sequence component to zero. This modified definition of the stationary frame *d*–*q*–0 components will be used in the remainder of this book.

1.6.2 *d*–*q*–0 Components for Voltage Source Inverter Operated in Square-Wave Mode

In general it is readily determined that there are only eight possible switch combinations for a three-phase inverter, as shown in Figure 1.20. Two of these states ($\overline{SV_0}$ and $\overline{SV_7}$) are a short circuit of the output while the remaining six produce active voltages, as previously indicated in Figure 1.10. Figure 1.21 shows how the eight switch combinations can be represented as stationary vectors in the *d*–*q* plane simply by repetitive application of Eq. (1.47). It is relatively easy to determine the values of the six vectors in the *d*–*q* plane by investigating each nonzero switch connection. For example, for vector $\overline{SV_3}$, switch S_3 is closed connecting phase *b* to the positive terminal, while switches S_4 and S_2 are closed connecting phases *a* and *c* to the negative terminal. Assuming a wye-connected load, the phase *b* voltage receives two-thirds of the DC pole-to-pole voltage while the parallel connected phases *a* and *c* receive one-third of this voltage. With due regard for polarity, the *d*–*q* voltages are, from Eq. (1.44),

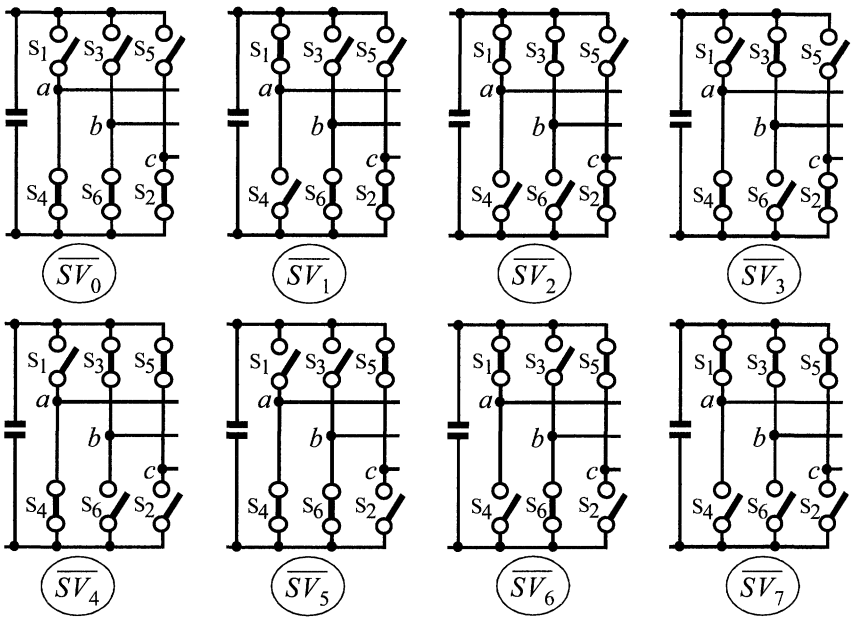

Figure 1.20 The eight possible phase leg switch combinations for a VSI.

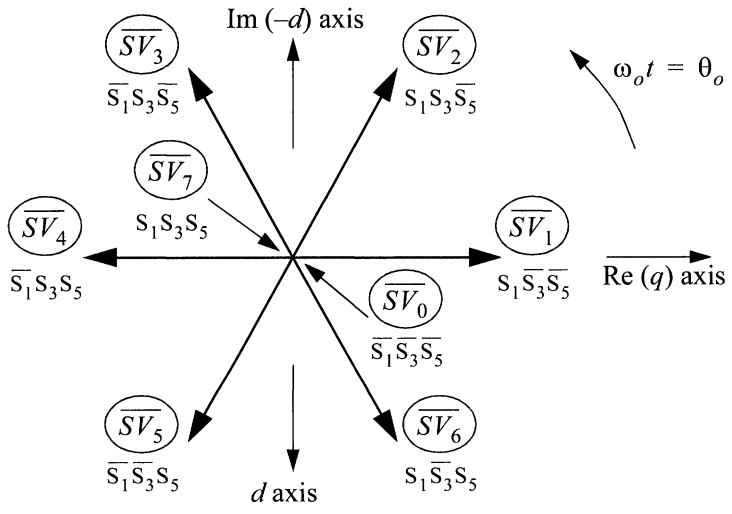

Figure 1.21 Eight possible stationary vectors on the *d*–*q* plane for a VSI.

$$v_{qs} = -\frac{2}{3}V_{dc}$$
$$v_{ds} = \frac{1}{\sqrt{3}}\left(-\frac{2}{3}V_{dc} - \frac{4}{3}V_{dc}\right) = -\frac{2}{\sqrt{3}}V_{dc} \tag{1.49}$$

The magnitude of this vector is

$$\left|\overline{SV_3}\right| = \sqrt{v_{qs}^2 + v_{ds}^2} = \sqrt{\left(\frac{2}{3}V_{dc}\right)^2 + \left(\frac{2}{\sqrt{3}}V_{dc}\right)^2} = \frac{4}{3}V_{dc} \tag{1.50}$$

as is the case for all six of the nonzero vector locations. For convenience, the projection of axes of the three-phase voltages can also be located on the *d–q* plane since vectors $\overline{SV_1}$, $\overline{SV_3}$, and $\overline{SV_5}$ also result in a positive maximum voltage on phases *as*, *bs*, and *cs*, respectively.

Note that the lower phase leg switches (S_4, S_6, S_2) are represented as "NOT" the upper phase leg switches ($\overline{S}_1$, $\overline{S}_3$, $\overline{S}_5$) in Figure 1.21, reflecting the fact that the upper or lower switch in each phase leg must always be turned on to maintain current continuity through each phase leg for a voltage source inverter.

In general, the inverter attempts to follow the circle defined by the balanced set of voltages, Eqs. (1.39) and (1.43). However, since only nonzero inverter states are possible, as illustrated by $\overline{SV_1}$, $\overline{SV_2}$, $\overline{SV_3}$, ..., $\overline{SV_6}$ in Figure 1.20, the vector representing the voltage applied to the load jumps abruptly by 60 electrical degrees in a continuous counterclockwise fashion, approximating the circle by the points on a hexagon. While only crudely approximated in this case, more accurate tracking of the target circle on the *d–q* plane can be accomplished by more sophisticated pulse width modulation techniques, as will be considered later in this book. If a simple inductive load is assumed, Figure 1.22 shows a typical plot of the transient progression of the voltage vector and current vector for a typical *r–L* load initially at rest (zero initial conditions) without PWM. The voltage vector remains confined to the six points of a hexagon while the current vector traces out a hexagon rotated by roughly 90 electrical degrees.

Since any vector has spatial content (length and direction), it is frequently convenient to abandon the matrix notation and to assign directional unit vectors to identify the components of the vector in the three-dimensional space defined by the *d–q–*0 coordinates. In this case, however, one is concerned

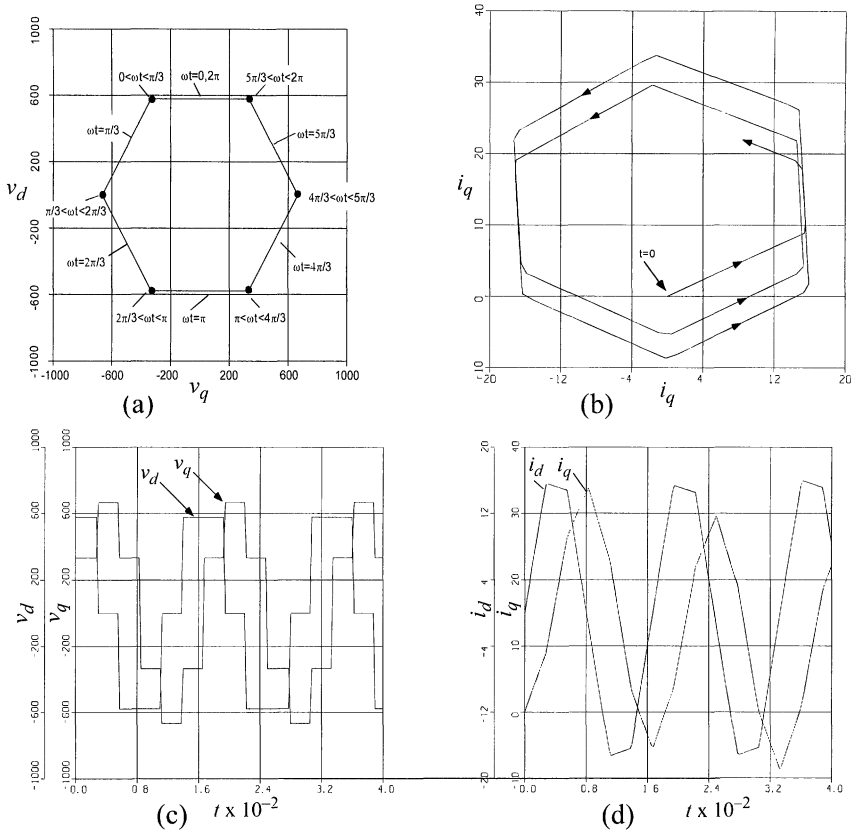

Figure 1.22 Locus of the (a) voltage and (b) current space vectors for square-wave voltage source inverter assuming a balanced *r–L* load and (c), (d) corresponding time domain waveforms. Parameters: $V_{dc} = 500$ V, $r = 2.0\ \Omega$, $L = 0.1$ mH.

almost entirely with rotation in the *d–q* plane as opposed to linear translation in the three dimensional *d–q–*0 space. In such cases, rotation is most readily represented in complex polar form so the most convenient method of representing the rotating vector is simply to convert the *d–q* plane to one which is complex, whereupon, by definition,

$$\begin{aligned} \mathrm{Re}(\bar{f}_s) &= f_{qs}^s \\ \mathrm{Im}(\bar{f}_s) &= -f_{ds}^s \end{aligned} \tag{1.51}$$

The "jumps" in the vector representing the inverter voltage can now be conveniently represented by defining the operator

$$\bar{a} = e^{j(2\pi/3)} = -\frac{1}{2} + j\frac{\sqrt{3}}{2} \tag{1.52}$$

where $j = \sqrt{-1}$. In terms of the vector $\bar{a}$ the axes of the three-phase voltages can be located by the vectors 1, $\bar{a}$, and $\bar{a}^2$, respectively.

Since the phase voltages have been assigned spatial attributes, it is now possible to visualize the phase variables as *space vectors* in the complex plane. In general, this vector is given by

$$\bar{f}_s = f_{qs}^s - jf_{ds}^s \tag{1.53}$$

and, from Eq. (1.47),

$$\bar{f}_s = f_{as} - j\left(\frac{f_{cs} - f_{bs}}{\sqrt{3}}\right) \tag{1.54}$$

The quantity $-j$ can be written in terms of the operator $\bar{a}$ as

$$-j = \frac{1}{\sqrt{3}}(\bar{a}^2 - \bar{a}) \tag{1.55}$$

so that Eq. (1.54) becomes

$$\begin{aligned} \bar{f}_s &= f_{as} + \frac{1}{3}(\bar{a}^2 - \bar{a})(f_{cs} - f_{bs}) \\ &= f_{as} + \frac{1}{3}(\bar{a}^2 f_{cs} + \bar{a} f_{bs}) - \frac{1}{3}(\bar{a}^2 f_{bs} + \bar{a} f_{cs}) \end{aligned} \tag{1.56}$$

Since the sum of the three components f_{as}, f_{bs}, f_{cs} equals zero, this equation can be written as

$$\bar{f}_s = f_{as} + \frac{1}{3}(\bar{a}^2 f_{cs} + \bar{a} f_{bs}) - \frac{1}{3}[\bar{a}^2(-f_{as} - f_{cs}) + \bar{a}(-f_{as} - f_{bs})]$$

which simplifies to

$$\bar{f}_s = \frac{2}{3}(f_{as} + \bar{a} f_{bs} + \bar{a}^2 f_{cs}) \tag{1.57}$$

Note the presence of the 2/3 factor, which is necessary to preserve the correct amplitude when represented in phase variable coordinates.

The six nonzero switch combinations can also be considered to be stationary snapshots of a three-phase set of time-varying sinusoids with a phase voltage magnitude V_m as shown in Figure 1.23. The magnitude of each of the six active vectors is determined by recognizing that the line voltage at each snap-

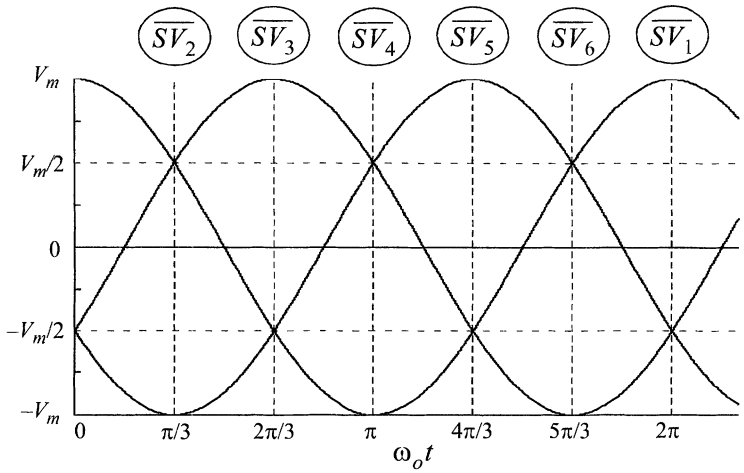

Figure 1.23 VSI phasor angular positions in fundamental cycle for space vector.

shot of voltage in Figure 1.23 is $1.5V_m$ where V_m is the peak phase voltage, and that this voltage is equal to the DC bus voltage $2V_{dc}$. That is,

$$V_m = \frac{4}{3}V_{dc} \tag{1.58}$$

1.6.3 Synchronously Rotating Reference Frame

The visualization of vector rotation on the *d–q* plane has also led to transformations which rotate with these vectors. For example, if axes are defined which rotate with the stator voltage, one realizes the *synchronous voltage reference frame*. In general, it is not necessary to define rotating axes to rotate synchronously with one particular vector but to simply define a general rotating transformation which transforms the phase variables to rotating axes on the *d–q* plane, viz:

$$\begin{bmatrix} f_{qs}(\theta) \\ f_{ds}(\theta) \\ f_{0s} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}\begin{bmatrix} f_{as} \\ f_{bs} \\ f_{cs} \end{bmatrix} \tag{1.59}$$

For completeness, the zero component is also again included, together with the scale change of $\sqrt{2/3}$. The angle θ is the angular displacement of the vector on the *d–q* plane measured with respect to the projection of the *as* axis onto this plane. Since the same scale change has been made for all three components, the zero component again uses somewhat unconventional scaling. Alternatively, Fortesque's scaling for this component can also be selected, namely

$$f_{0s} = \frac{1}{3}(f_{as} + f_{bs} + f_{cs}) \tag{1.60}$$

and this is also widely used.

Note that the zero axis does not enter into the rotational transformation. Hence, the zero axis can be considered as the axis about which the rotation takes place, i.e., the axis of rotation. Because of the scaling, the power (and subsequently the torque if the load is a motor) is different in *d–q–*0 components than in *a–b–c* variables and a 3/2 multiplier must be added to the power as calculated in the transformed system of equations since both current and voltage variables have been scaled by $\sqrt{2/3}$.

In vector notation, Eq. (1.59) can be written as

$$\boldsymbol{f}_{qd0} = \boldsymbol{T}_{qd0}(\theta)\boldsymbol{f}_{abc} \tag{1.61}$$

where

$$\boldsymbol{T}_{qd0}(\theta) = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{1.62}$$

The transformation $\boldsymbol{T}_{qd0}(\theta)$ can, for convenience and for computational advantage, be broken into two portions, one of which takes variables from physical phase quantities to nonrotating *d–q–*0 variables (stationary reference frame) while the other goes from nonrotating to rotating *d–q–*0 variables (rotating reference frame). For this case one can write,

$$\boldsymbol{f}_{qd0} = \boldsymbol{T}_{qd0}(\theta)\boldsymbol{f}_{abc} = \boldsymbol{R}(\theta)\boldsymbol{T}_{qd0}(0)\boldsymbol{f}_{abc} \tag{1.63}$$

where

$$\boldsymbol{T}_{qd0}(0) = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & -\frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \\ \frac{\sqrt{2}}{3} & \frac{\sqrt{2}}{3} & \frac{\sqrt{2}}{3} \end{bmatrix} \tag{1.64}$$

and

$$\boldsymbol{R}(\theta) = \begin{bmatrix} \cos\theta & -\sin\theta & 0 \\ \sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{1.65}$$

Note that $\boldsymbol{T}_{qd0}(0)$ is obtained by simply setting $\theta = 0$ in Eq. (1.62). The inverse transformation is

$$\boldsymbol{f}_{abc} = \boldsymbol{T}_{qd0}(\theta)^{-1}\boldsymbol{f}_{qd0} = \boldsymbol{T}_{qd0}(0)^{-1}\boldsymbol{R}(\theta)^{-1}\boldsymbol{f}_{qd0} \tag{1.66}$$

where

$$\boldsymbol{T}_{qd0}(\theta)^{-1} = \frac{3}{2}\boldsymbol{T}_{qd0}(\theta)^{T} = \begin{bmatrix} \cos\theta & \sin\theta & \frac{1}{\sqrt{2}} \\ \cos\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta - \frac{2\pi}{3}\right) & \frac{1}{\sqrt{2}} \\ \cos\left(\theta + \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{1.67}$$

$$\boldsymbol{T}_{qd0}(0)^{-1} = \frac{3}{2}\boldsymbol{T}_{qd0}(0)^{T} = \begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{1.68}$$

$$\boldsymbol{R}(\theta)^{-1} = \boldsymbol{R}(\theta)^{T} = \begin{bmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{1.69}$$

Figure 1.24 shows the locus of the same voltage and current vector as Figure 1.22, but viewed in a synchronously rotating reference frame. Here, the superscript e is used on the d–q variables to denote that they are rotating with the *electrical* frequency. In this case the locus of the vector continually jumps ahead by 60 electrical degrees at each switching instant. However, since the vector subsequently remains stationary while the synchronous frame continues to rotate, the locus of the vector slowly retreats backward and then jumps forward, repeating the locus shown six times each cycle.

1.7 Three-Level Inverters

Another voltage source/stiff inverter configuration which is becoming increasingly important for high power applications is the so-called *neutral-point clamped* (NPC) inverter [4]. This inverter, shown in Figure 1.25, has a zero DC voltage center point, which is switchable to the phase outputs, thereby creating the possibility of switching each inverter phase leg to one of three voltage levels. The major benefit of this configuration is that, while there are twice as many switches as in the two-level inverter, each of the switches must block only one-half of the DC link voltage (as is also the case for the six center-tapped diodes). However, one problem, that does not occur with a two-level inverter, is the need to ensure voltage balance across the two series-connected capacitors making up the DC link. One solution is to simply connect each of

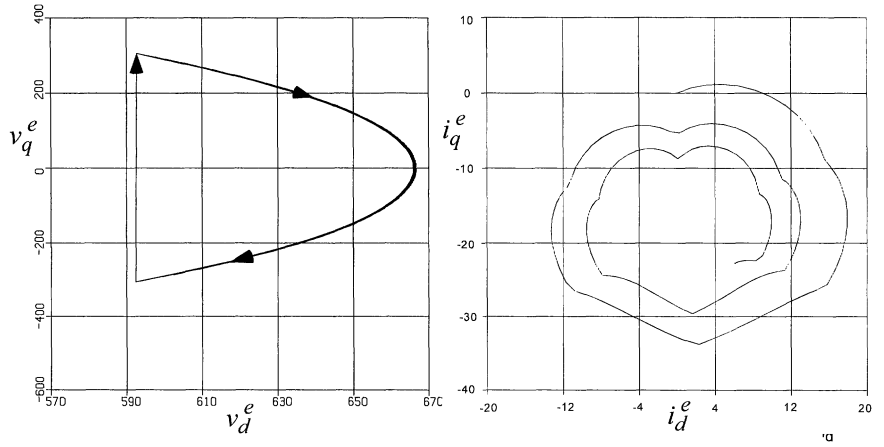

Figure 1.24 Locus of phase voltage and line current in the synchronously rotating reference frame for the same parameters as Figure 1.22.

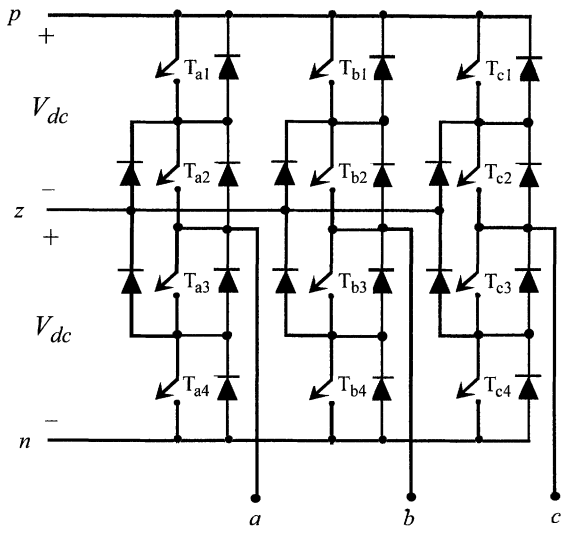

Figure 1.25 Three-level voltage source/stiff inverter.

the capacitors to its own isolated DC source (for example the output of a diode bridge fed from a transformer secondary). The other method is to balance the two capacitor voltages by feedback control. In this case the time that each inverter leg dwells on the center point can be adjusted so as to regulate the average current into the center point to be zero [5, 6].

In order to produce three levels, the switches are controlled such that only two of the four switches in each phase leg are turned on at any time. For example, when switches T_{a1} and T_{a2} are turned on, the positive DC link voltage is applied to the phase *a* terminal, when T_{a2} and T_{a3} are turned on, the center point voltage (zero volts) is applied, while when T_{a3} and T_{a4} are turned on, the negative DC link voltage appears at the terminal of phase *a*. Defining variables m_{x1}, m_{x2}, and m_{x3} ($x = a, b,$ or c) as a logical one when switch combinations (T_{x1}–T_{x2}), (T_{x2}–T_{x3}), (T_{x3}–T_{x4}) are true, respectively, and zero otherwise, the three terminal voltages can be written as

$$\begin{aligned} v_{az} &= V_{dc}(m_{a1} - m_{a3}) \\ v_{bz} &= V_{dc}(m_{b1} - m_{b3}) \\ v_{cz} &= V_{dc}(m_{c1} - m_{c3}) \end{aligned} \tag{1.70}$$

In a similar manner to previous work, the line-to-line and line-to-neutral voltages (in the case of a star-connected load) are given by

$$\begin{aligned} v_{ab} &= V_{dc}(m_{a1} - m_{a3} - m_{b1} + m_{b3}) \\ v_{bc} &= V_{dc}(m_{b1} - m_{b3} - m_{c1} + m_{c3}) \\ v_{ca} &= V_{dc}(m_{c1} - m_{c3} - m_{a1} + m_{a3}) \end{aligned} \tag{1.71}$$

and

$$\begin{aligned} v_{as} &= \frac{2}{3}V_{dc}\left[m_{a1} - m_{a3} - \frac{1}{2}(m_{b1} - m_{b3} + m_{c1} - m_{c3})\right] \\ v_{bs} &= \frac{2}{3}V_{dc}\left[m_{b1} - m_{b3} - \frac{1}{2}(m_{a1} - m_{a3} + m_{c1} - m_{c3})\right] \\ v_{cs} &= \frac{2}{3}V_{dc}\left[m_{c1} - m_{c3} - \frac{1}{2}(m_{a1} - m_{a3} + m_{b1} - m_{b3})\right] \end{aligned} \tag{1.72}$$

The load neutral-to-inverter-midpoint voltage is, for this case,

$$v_{sz} = \frac{1}{3}V_{dc}(m_{a1} - m_{a3} + m_{b1} - m_{b3} + m_{c1} - m_{c3}) \tag{1.73}$$

The three DC link currents are

$$\begin{aligned} I_{dc}^{+} &= m_{a1}i_a + m_{b1}i_b + m_{c1}i_c \\ I_{dc}^{-} &= m_{a3}i_a + m_{b3}i_b + m_{c3}i_c \\ I_{dc}^{z} &= m_{a2}i_a + m_{b2}i_b + m_{c2}i_c \end{aligned} \tag{1.74}$$

It is clear from the constraints of the circuit that

$$m_{a1} + m_{a2} + m_{a3} = 1 \tag{1.75}$$

and so forth, so that I_{dc}^{z} from Eq. (1.74) can also be written as

$$I_{dc}^{z} = -(m_{a1} + m_{a3})i_a - (m_{b1} + m_{b3})i_b - (m_{c1} + m_{c3})i_c \tag{1.76}$$

Examination of Eq. (1.72) identifies that the line-to-neutral voltage can take on seven distinct values, namely $\pm 4V_{dc}/3$, $\pm V_{dc}$, $\pm 2V_{dc}/3$, and zero.

Figure 1.26 shows the switched phase leg, line-to-line and line-to-neutral phase voltages for a three level NPC inverter, where the phase legs are switched with a 30° zero voltage plateau between the $+V_{dc}$ and the $-V_{dc}$ steps to achieve minimum total harmonic distortion (THD). It is obvious that the switched waveforms of Figure 1.26 are significantly improved compared to those of a square-wave, two-level converter shown in Figure 1.10.

The fundamental component of the load voltage can now be determined by calculating the fundamental component of the voltage from one phase leg to

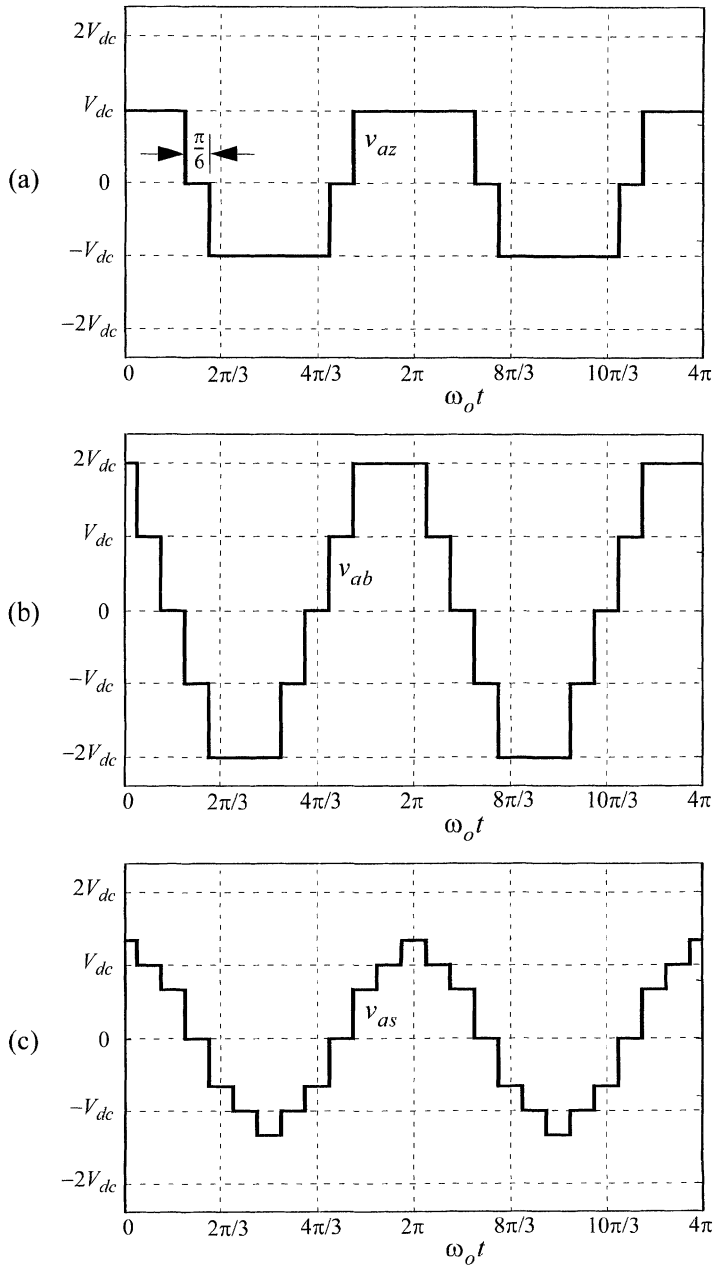

Figure 1.26 Switched (a) line-to-midpoint, (b) line-to-line and (b) line-to-neutral voltages produced by three-level NPC inverter. Phase leg zero voltage step width arranged for minimum THD.

the DC center point, which will be the same as the fundamental component measured with respect to the load neutral. Hence

$$V_{1,rms} = \frac{1}{\sqrt{2}}\frac{4}{\pi}\int_0^{5\pi/12} V_{dc}\cos\theta\, d\theta$$

$$= \frac{2\sqrt{2}}{\pi}\sin\frac{5\pi}{12}V_{dc} = 0.87V_{dc} \tag{1.77}$$

This is not quite as large as the $0.90V_{dc}$ RMS voltage that is obtained from a two-level inverter with the same overall DC link voltage of $2V_{dc}$ by dividing the result of Eq. (1.7) by $\sqrt{2}$ to convert it to RMS. Of course, the same RMS voltage could still be obtained if the midpoint voltage was never selected, but this results in a higher harmonic content and more or less defeats the purpose of having a three-level inverter.

The space vector approach, discussed in Section 1.6, can be utilized to analyze these types of converters as well. For example, when the possible phase voltage switching states of the three-level inverter of Figure 1.25 are expressed as space vectors, a double hexagon is obtained as shown in Figure 1.27.

1.8 Multilevel Inverter Topologies

1.8.1 Diode-Clamped Multilevel Inverter

It has been shown that the principle of diode-clamping to DC link voltages can be extended to any number of voltage levels [7]. Figure 1.28 shows the circuit implementation for four- and five-level inverters. Since the voltages across the semiconductor switches are limited by conduction of the diodes connected to the various DC levels, this class of multilevel inverters is termed *diode-clamped multilevel inverters*. For the case of the four-level inverter, switches T_{a1}, T_{a2}, and T_{a3} are turned on simultaneously, then T_{a2}, T_{a3}, and T_{a4} and so forth to produce the desired level. A possible total of 12 voltage vectors are produced, being $\pm kV_{dc}/3$, $k = 1,...,6$ where the $k = 2$ state does not appear in the line-to-neutral voltage output. In the same manner, four switches are always triggered to select a desired level in the five-level inverter, producing 19 voltage levels, $\pm kV_{dc}/3$, $k = 1,...,9$ plus zero where the $k = 1$ and $k = 3$ levels do not appear in the output line-to-neutral voltage. Since several intermediate levels are now created, the problem of ensuring voltage balance across each

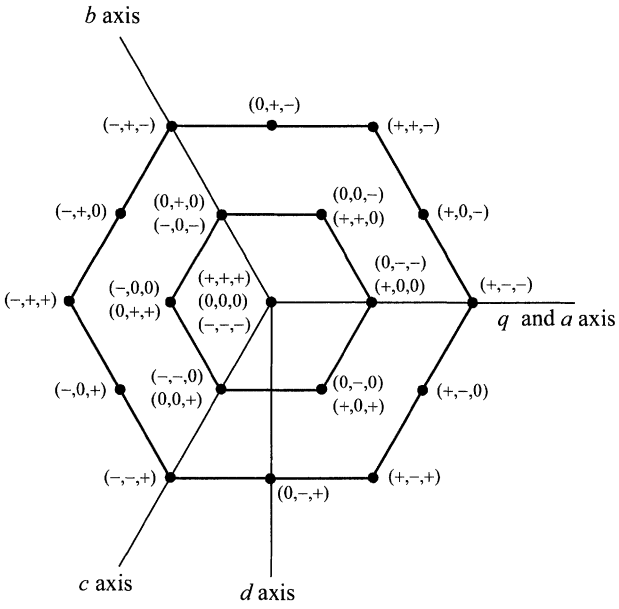

Figure 1.27 Hexagons of possible switching states for three-level DC voltage source/stiff inverter.

of the series-connected capacitors becomes a challenging problem. The problem is most easily solved by feeding each DC link capacitor with an independent DC supply but this sometimes adds undesirable cost to the system. When supplied by a single DC supply, the issue has been shown to be solvable by the use of appropriate control algorithms [8]. However, complete control of the DC link voltages is lost when the output phase voltage reaches roughly 65% of its maximum value, somewhat restricting the use of this circuit [9].

The switching operation of these converters and the current path for positive and negative current can further identified by considering the seven-level diode-clamped inverter of Figure 1.29. The three DC voltages are labeled as V_{dc1}, V_{dc2}, V_{dc3} to distinguish them in the inverter output, although in most cases $V_{dc1} = V_{dc2} = V_{dc3}$. The phase leg switch states required to achieve the seven output levels can be determined by connecting say phase leg *b* to the negative DC bus by triggering all switches in the lower portion of its phase leg. Then the phase leg *a* output voltage with respect to the negative DC rail, v_{an}, can be identified for various switch combinations, as summarized in Table 1.1.

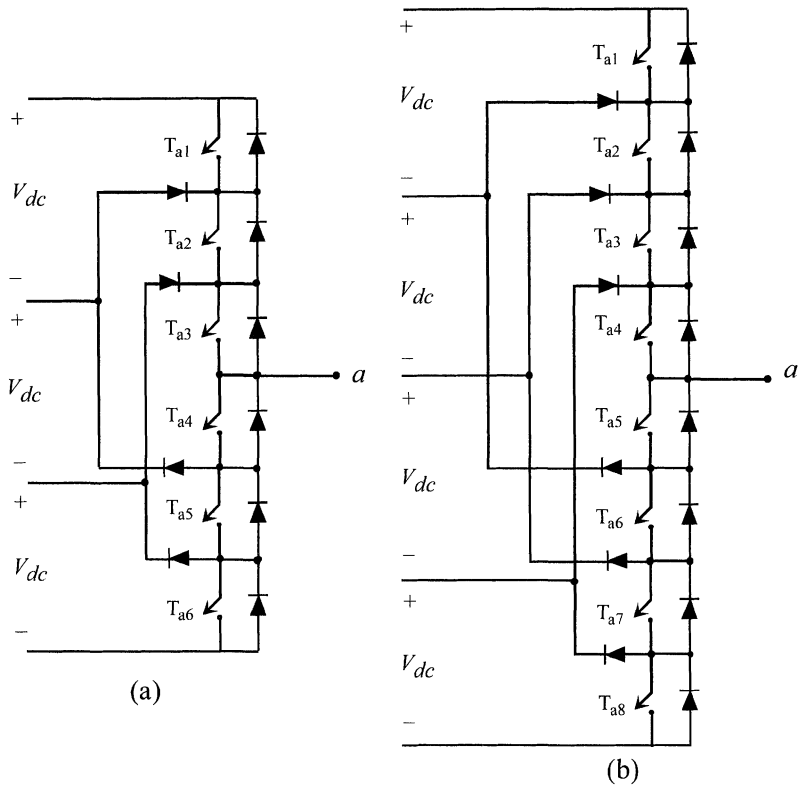

Figure 1.28 (a) Four-level and (b) five-level diode-clamped inverter implementations (one phase only shown).

Figures 1.30, 1.31, and 1.32, show the switched phase leg, line-to-line and line-to-neutral phase voltages for a four-level, five-level, and a seven-level, diode-clamped inverter, respectively. In this case the phase legs have been switched between the voltage levels at the appropriate times to eliminate low-order harmonics, as discussed in Section 10.3.1 and summarized in Table 10.1. The progressive improvement in the quality of the switched waveform is obvious as the number of inverter voltage levels increases.

Regardless of the number of levels, the blocking voltage of the switches in this type of topology is limited to V_{dc}, so that inverters operating at the medium AC voltage range (2 to 13.2 kV) can be implemented with low cost, high-performance Insulated Gate Bipolar Transistor (IGBT) switches. Unfortunately the same is not true of the diodes connecting the various DC levels to

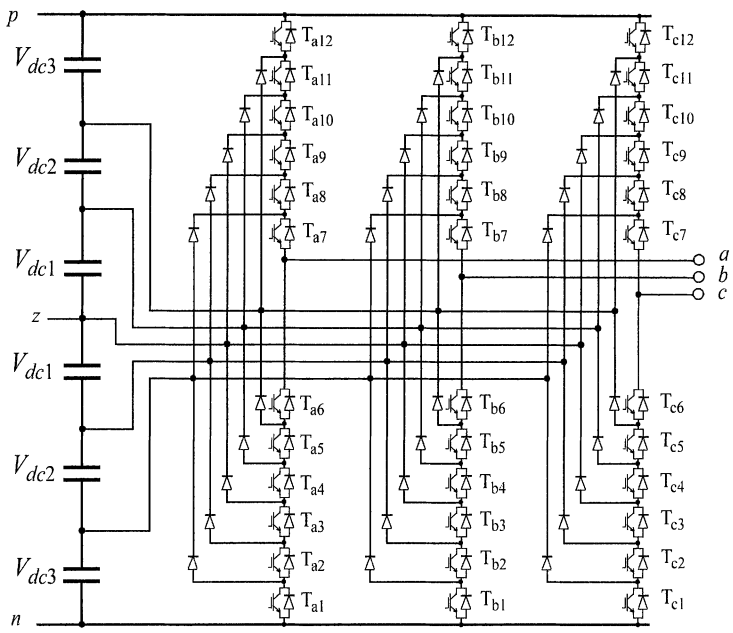

Figure 1.29 A seven-level diode-clamped inverter.

Table 1.1 Switch States and Corresponding Current Path for Diode-Clamped Converter Illustrating Seven Positive Levels for Phase Leg *a* Voltage v_{an}, Phase *b* Assumed Connected to the Negative DC Bus

Switch State	Phase Leg *a* Voltage v_{an}	Devices Turned on	Current Path with I_a Positive	Current Path with I_a Negative
1	$v_{an} = 0$	T_{a1} to T_{a6}	T_{a6}>T_{a5}>T_{a4}> T_{a3}>T_{a2}>T_{a1}	T_{a6}>T_{a5}>T_{a4}> T_{a3}>T_{a2}>T_{a1}
2	$v_{an} = V_{dc3}$	T_{a2} to T_{a7}	D_{a7}>T_{a7}	T_{a6}>T_{a5}>T_{a4}> T_{a3}>T_{a2}>D_{a2}
3	$v_{an} = V_{dc3}+V_{dc2}$	T_{a3} to T_{a8}	D_{a8}>T_{a8}>T_{a7}	T_{a6}>T_{a5}>T_{a4}> T_{a3}>D_{a3}
4	$v_{an} = V_{dc3}+V_{dc2}$ $+V_{dc1}$	T_{a4} to T_{a9}	D_{a9}>T_{a9}>T_{a8}> T_{a7}	T_{a6}>T_{a5}>T_{a4}> D_{a4}
5	$v_{an} = V_{dc3}+V_{dc2}$ $+2V_{dc1}$	T_{a5} to T_{a10}	D_{a10}>T_{a10}>T_{a9}> T_{a8}>T_{a7}	T_{a6}>T_{a5}>D_{a5}
6	$v_{an} = V_{dc3}$ $+2(V_{dc2}+V_{dc1})$	T_{a6} to T_{a11}	D_{a11}>T_{a11}>T_{a10}> T_{a9}>T_{a8}>T_{a7}	T_{a6}>D_{a6}
7	$v_{an} = 2(V_{dc3}$ $+V_{dc2}+V_{dc1})$	T_{a7} to T_{a12}	T_{a12}>T_{a11}>T_{a10}> T_{a9}>T_{a8}>T_{a7}	T_{a7}>T_{a8}>T_{a9}> T_{a10}>T_{a11}>T_{a12}

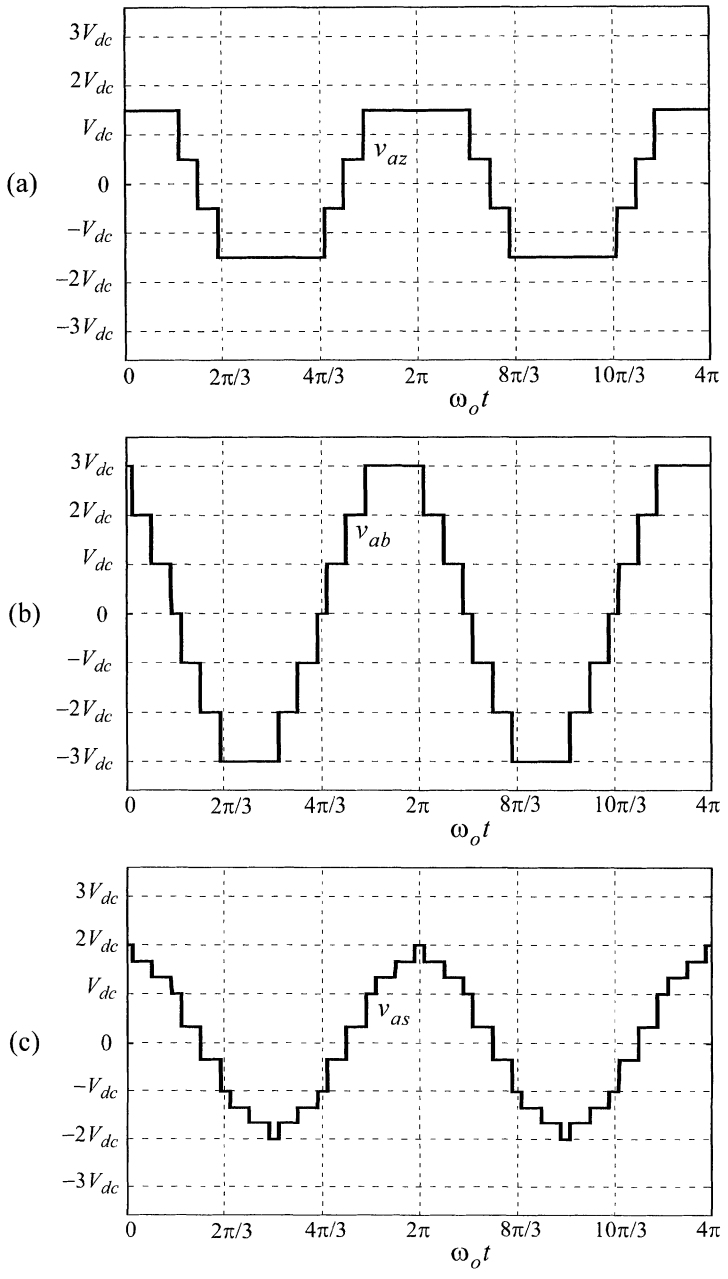

Figure 1.30 Switched (a) line-to-midpoint, (b) line-to-line and (b) line-to-neutral voltages produced by four-level diode-clamped inverter. Switching times defined in Table 10.1.

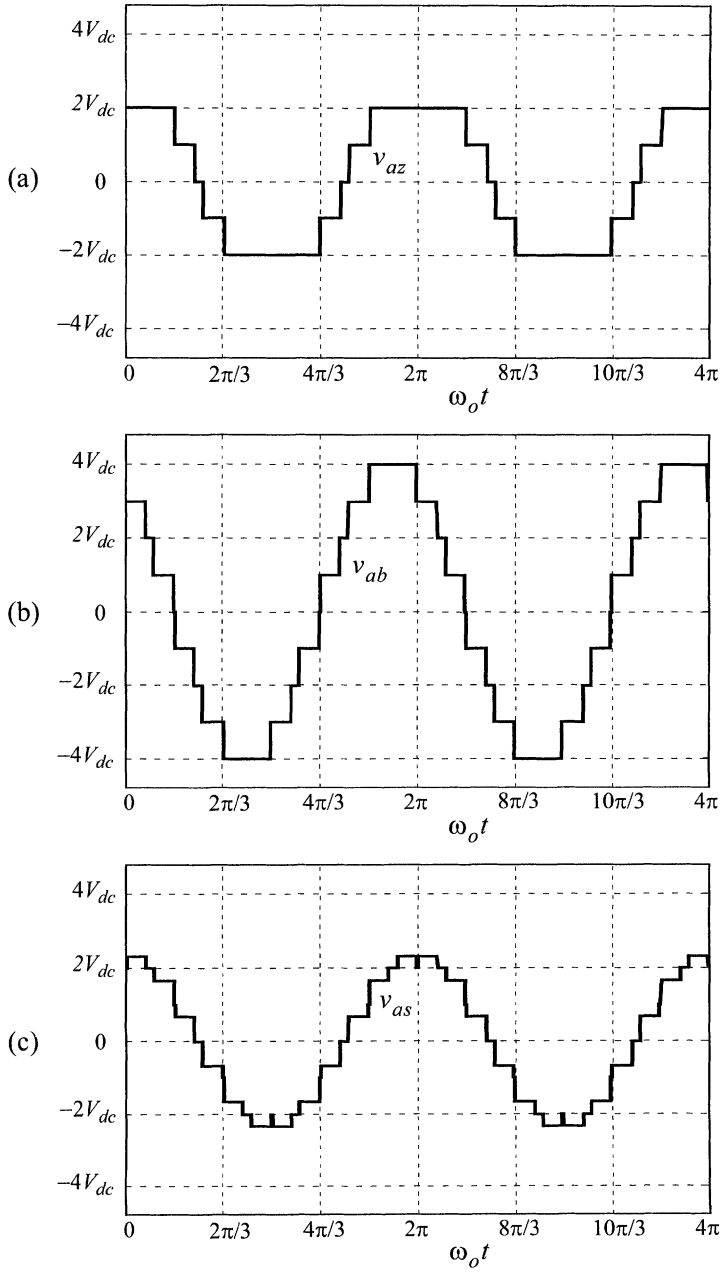

Figure 1.31 Switched (a) line-to-midpoint, (b) line-to-line and (b) line-to-neutral voltages produced by five-level diode-clamped inverter. Switching times defined in Table 10.1.

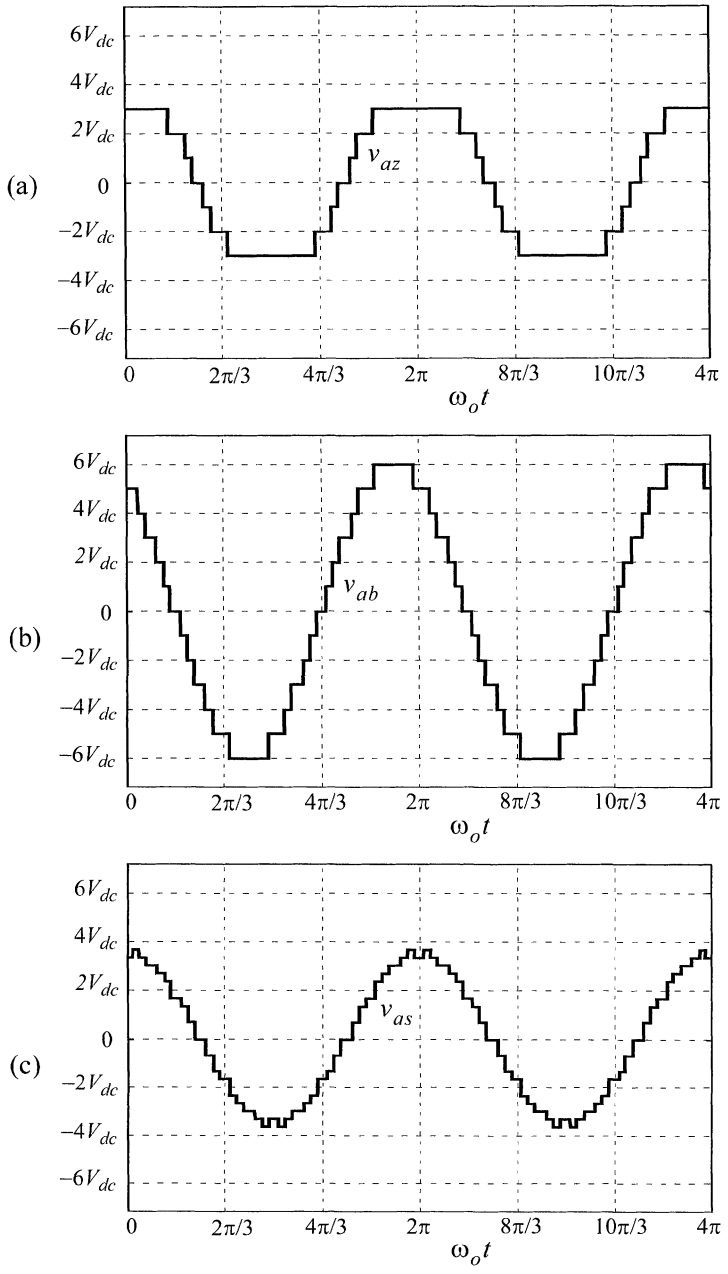

Figure 1.32 Switched (a) line-to-midpoint, (b) line-to-line and (b) line-to-neutral voltages produced by seven-level diode-clamped inverter. Switching times defined in Table 10.1.

the switches, some of which must be rated at $(k-2)V_{dc}$ where k is the number of levels ($k \geq 3$). The voltage rating of the diodes therefore quickly becomes a problem and levels greater than five are not considered as practical at the present time. This problem can be overcome by simply connecting several diodes in series, but the stress across the series-connected devices must then be carefully managed. Also since the number of series-connected switches increases with the number of levels, the switch conduction losses clearly increase in the same proportion. Fortunately, the power rating also increases at the same rate so the efficiency of the inverter remains roughly unaffected by the number of series-connected switches.

1.8.2 Capacitor-Clamped Multilevel Inverter

The capacitor-clamped VSI proposed by Meynard and Foch is an alternative to the diode-clamped VSI and shares many of the advantages of this topology [10]. Figure 1.33 illustrates the capacitor-clamped VSI topology for a seven-level system.

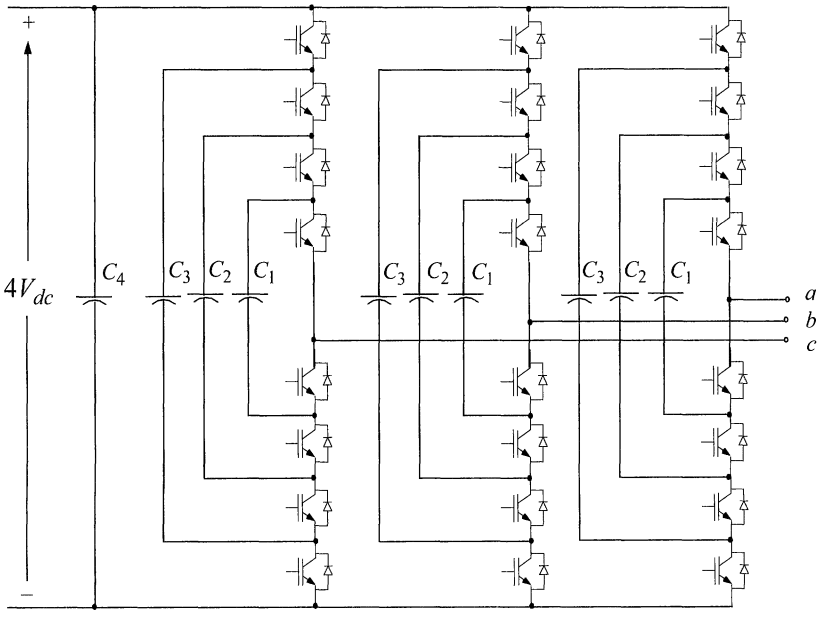

Figure 1.33 Topology of a five-level capacitor-clamped inverter.

The circuit operation of the capacitor-clamped topology is best explained by considering the simple three-level single-phase version shown in Figure 1.34. To obtain an output voltage level of $2V_{dc}$, switches S_1, S_2, S_7, and S_8 are turned on. To obtain $-2V_{dc}$, switches S_3, S_4, S_5, and S_6 are turned on. To obtain V_{dc}, S_1–S_3–S_7–S_8 are turned on, and to obtain $-V_{dc}$, S_3–S_4–S_5–S_7 are turned on. If clamping capacitors C_1 are maintained at voltage V_{dc}, the voltage on these capacitors in series with the load will partially cancel the source voltage. To obtain the zero voltage level, the combinations of either S_1–S_3–S_5–S_7 or S_2–S_4–S_6–S_8 can be turned on. The charge of C_1 can be balanced by proper management of the switch combinations.

This topology shares the advantages of all multilevel voltage source converters (VSCs) listed above, as well as those of a diode-clamped system, in that the required number of voltage levels can be obtained without the use of a transformer. This assists in reducing the cost of the converter and again reduces power loss. Unlike the diode-clamped structure where the series string of capacitors share the same voltage, in the capacitor-clamped VSC the capacitors within a phase leg are charged to different voltage levels. To synthesize the phase voltage waveform the various switches within the phase leg are switched ON to combine the various capacitor voltage levels with the constraint that no capacitor is short circuited and current continuity with the DC link is maintained for each capacitor. This leads to a significant amount of redundancy in

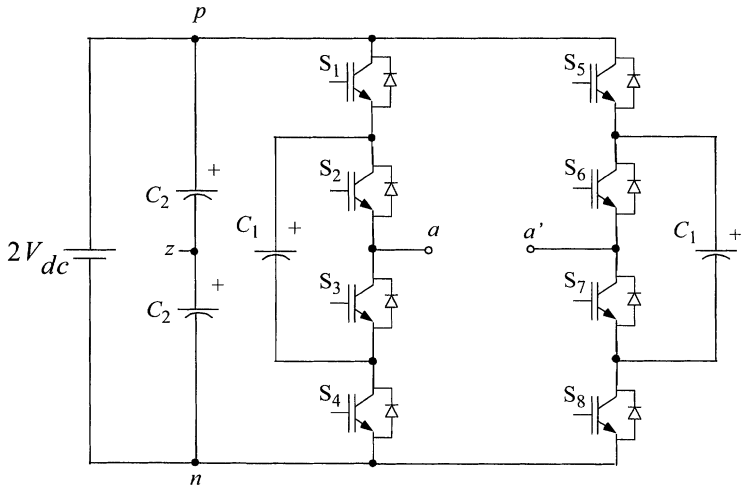

Figure 1.34 Three-level capacitor-clamped inverter, voltage on capacitors C_1 regulated to V_{dc}.

the switching states that lead to the same phase voltage levels. A similar table to Table 1.1 can be readily prepared for the capacitor-clamped circuit of Figure 1.33.

The capacitor-clamped (alternatively known as flying-capacitor) topology has several disadvantages that have limited its use. The first of these is the converter initialization. Before the capacitor-clamped VSC can be modulated, the clamping capacitors must be set up with the required voltage levels. This complicates the modulation process and hinders the performance of the converter under ride-through conditions. The capacitor voltages must also be regulated under normal operation in a similar fashion to the capacitor neutral points for a diode-clamped VSC. However, due to the large degree of redundancy in the phase voltage states, this regulation problem is generally combined with the modulation strategy. Another problem concerns the rating of the capacitors that form the clamping network. Since these have large fractions of the DC bus voltage across them, the voltage rating of the capacitors must be large when compared to the diode-clamped topology. It is this requirement and the initialization problems of the capacitor-clamped VSC that have limited its continued development.

1.8.3 Cascaded Voltage Source Multilevel Inverter

The third topological alternative for a multilevel inverter is to series-cascade single-phase full-bridges to make up each phase leg of the main inverter, as shown in Figure 1.35 for a seven-level system. Each full-bridge can switch between $+V_{dc}$, 0, and $-V_{dc}$, so that, for the seven-level example shown in Figure 1.35, each phase leg as a whole can switch in steps of V_{dc} over the range $+3V_{dc}$ to $-3V_{dc}$. Note also that the DC link voltage of each full-bridge has been redefined to V_{dc} rather than $2V_{dc}$ as was used in Section 1.1.3. This is the usual convention for cascaded voltage source multilevel inverter systems. In general, N series connected full-bridges can generate $(2N+1)$ switching levels per phase leg.

For this topology, the DC link supply for each full-bridge converter element must be provided separately, and this is typically achieved using diode rectifiers fed from isolated secondary windings of a three-phase transformer. A very simple approach is shown in Figure 1.36 using single-phase diode bridges. Other types of input side converters can also be used such as three-phase diode bridge rectifiers fed from a secondary star or delta connection. It

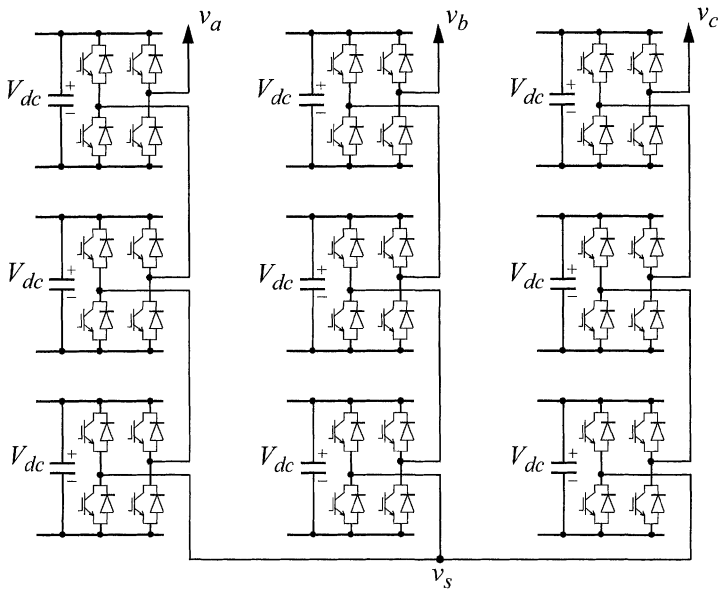

Figure 1.35 Seven-level series-bridge cascaded inverter.

can be shown that with progressive phase shifting of the three-phase secondaries by 60/(k–1) degrees where k is the number of levels, significant harmonic cancellation can be achieved in the transformer input current.

The cascaded inverter topology has several advantages that have made it attractive in power conditioning systems and medium to high power drive applications [11, 12, 13]. The first advantage concerns the ease of regulation of the DC buses described above, while the second advantage concerns the modularity of control that can be achieved. Unlike the diode-clamped inverter and the capacitor-clamped inverter where individual phase legs must be modulated by a central controller, the full-bridge inverters of a cascaded structure can be modulated independently of each other. Communication between the full-bridge inverters is required in order to achieve the synchronization of reference and carrier waveforms, but the controller can be distributed. This makes for a simpler controller structure than for either of the two previously discussed topologies. However, the cascaded inverter topology has not been applied particularly successfully at low power levels to date because of the need to provide separate isolated DC supplies for each full-bridge converter element.

Clearly, while the control logic to realize the switched state varies, the same switched phase leg voltages can be accomplished by any of the three

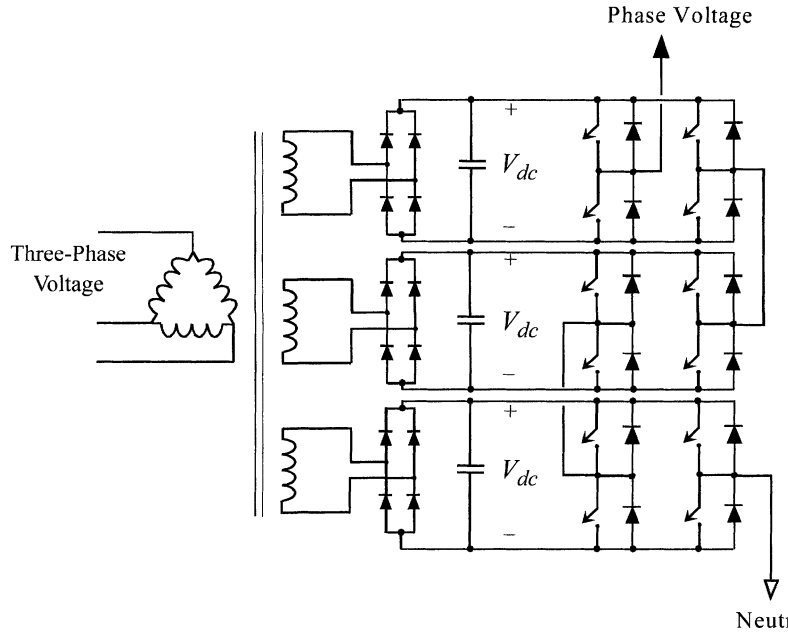

Figure 1.36 Isolated DC voltage supplies obtained from separate transformer secondary windings for 7-level cascaded multilevel inverter (one output phase only shown).

multilevel inverter topologies described here, provided, of course, they have the same number of available voltage levels. Hence, one would anticipate that the harmonic signature produced by the three circuits would be essentially the same. This property will be shown to be the case later in Chapter 11. However, in general the various switches of the phase leg of a multilevel converter are not equally loaded. This presents some difficulties with a practical multilevel inverter implementation, but it is possible at least for a cascaded inverter to rotate its switching between the series-connected full-bridges and hence balance the average power flow through each bridge. This approach is presented in Chapters 10 and 11.

One important difference between the three multilevel circuits, which will not be addressed in this book, concerns the issue of capacitor voltage balancing. Since the capacitors of each individual single-phase inverter derive from a different DC source, balancing is inherent. However, this is not the case for the diode-clamped or capacitor-clamped inverters. In this case the inner capacitors, such as those producing voltages V_{dc2} and V_{dc1} in Figure 1.29 will become

over or undercharged if the average current fed to the inner taps on the DC link is not zero. Regulation of the link capacitor voltages has been resolved for these inverters [14, 15], but the details will not be pursued in this text.

1.8.4 Hybrid Voltage Source Inverter

The hybrid VSC proposed by Manjrekar et al. is a cascaded structure that has been modified such that the full-bridge inverters that comprise the phase leg of a hybrid inverter have different magnitude DC buses [16]. Figure 1.37 shows the structure of a seven-level hybrid inverter, in which it can be seen that each phase leg is constructed from a high-voltage (HV) stage and a low-voltage (LV) stage. In terms of operation, the hybrid converter uses the HV stage to achieve the bulk power transfer and uses the LV stage as a means to improve the spectral performance of the overall converter. Also note that the HV stage is shown to be constructed using devices that have high-voltage blocking characteristics but not necessarily fast switching characteristics [e.g., integrated gate controlled thyristors (IGCTs)], while the LV stage is constructed using devices that have fast switching characteristics but not necessarily high-voltage blocking characteristics (e.g., IGBTs). The major advantages of the hybrid structure include the fact that it marries the best performance characteristics of two different power electronic devices, and that it can achieve similar perfor-

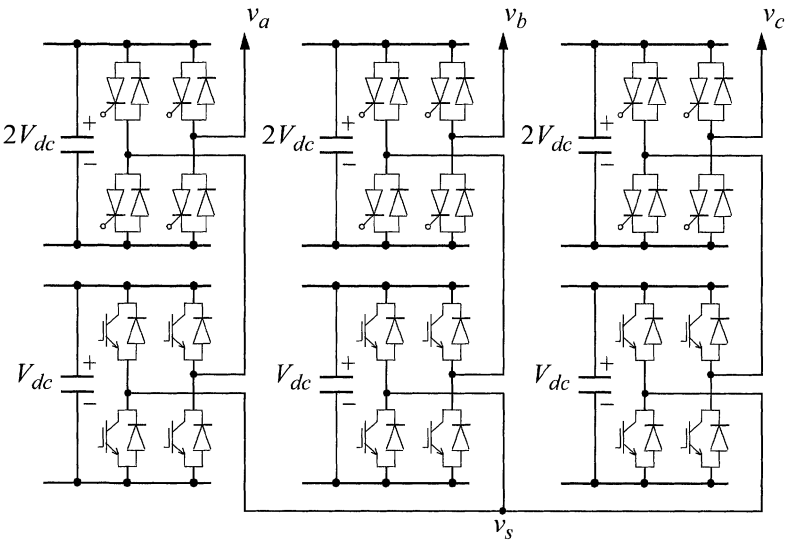

Figure 1.37 Topology of a seven-level hybrid voltage source inverter.

mance to other multilevel VSCs with a reduced switch count (e.g., 24 switches for a seven-level hybrid VSC as opposed to 36 for diode-clamped, cascaded, and capacitor-clamped VSCs).

The hybrid system again requires the use of a transformer to produce the isolated DC supplies for each full-bridge inverter, and the control of the converter is more complex than the standard cascaded structure. However, the control is still modular in that the LV stage and HV stage have their own reference waveforms, but the LV stage reference must be created from the HV reference. Another problem that must be addressed for the hybrid converter is that the HV stage will supply more power than the load requires in the middle ranges of the modulation index. Under these operating conditions the LV stage will be required to operate in a rectification mode, which means that the DC link must be capable of bidirectional power flow [16]. This necessitates the use of a PWM rectifier on the front end of the LV stage and further complicates the control of the hybrid converter system. However, the reduced switch count and more effective use of the power electronic devices that comprise the hybrid system make it a particularly attractive system at medium to high power levels.

1.9 Summary

This introductory chapter has presented the *switching circuits* and *block modulation* concepts involved in the application of power electronic converters. While block modulation is still used to produce a variable frequency AC supply in some applications, it has largely been supplanted by more sophisticated modulation strategies such as pulse width modulation, which have the major advantage of allowing simultaneous phase and amplitude control of the output voltage. Some time has also been spent here introducing the concept of *space vectors*, which have great utility in the analysis of the more complex inverter switching processes that are presented later in this book.

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