PREFACE

In 1965, Gordon Moore formulated his now famous Moore's law, which became the catalyst for advancements in the semiconductor industry. The semiconductor industry has brought us the sub-100-nm era with all the advancements we see today. With these advancements come difficulties in process control and subsequent challenges to circuit and physical design. As a result, the degrees of freedom in design methodology are fast shrinking and will require a revolutionary change in the way we put together chips that are not only functional but also meet the design objectives and are high yielding.

However, the explosive growth of semiconductor models developed in the absence of fabrication facilities has resulted in the isolation of process/device engineers from circuit design engineers, leading to some lack of understanding of the impact of their designs upon manufacturability, yield, and performance, due to the fundamental limitations of technology and device physics. As we enter the nano-CMOS era, knowing how to traverse these issues is critical to the success of products and companies. These communities of engineers must work together to fill each other's knowledge gaps, which are ever widening as we travel down the road of dimensional scaling. Only by doing this can goals be realized.

While faced with these issues during the course of our duties, we could find no book that addresses them in a single bound volume. The information exists in bits and pieces and mostly locked up in the minds of experts, some of whom we have consulted in the course of our jobs. This book is an attempt to provide a seamless entity that talks about these interactions and their impact on manufacturability, yield, and performance. It provides practical guidelines to help designers avoid some of the pitfalls inherent in advanced semiconductor processes as well as the strongly needed bridge from physical and circuit design to fabrication processing, manufacturability, and yield. The concepts we present in this text are extremely significant, especially as technology moves into the nano-CMOS feature sizes.

The book is organized into three parts. In the first part we provide detailed descriptions of the deep-submicron processes to help designers understand the issues associated with them and to provide more insight into the limitations brought about by dimensional scaling. In the second part we provide an overview of the impact of process scaling on circuit design and physical implementation. In the final part we cover issues concerning manufacturability and yield and provide guidance to ensure that a part is manufacturable and meets the yield and performance targets.

Chapter 1 provides an overview of the issues designers face in the deep-submicron processes. This chapter provides a framework for the rest of the book. Part I contains Chapters 2 and 3. In Chapter 2 we review the current status and possible future solutions of FEOL and BEOL processing systems for 90 nm and below. The FEOL section deals with gate dielectric and strain engineering developments, including related equipment issues. It also provides an in-depth discussion of CMOS scaling issues such as gate tunneling and NBTI. In the BEOL section we discuss local and global interconnect scaling, copper wire development, and low-κ interlayer dielectric challenges along with integration schemes such as dual damascene. Chapter 3 is a tutorial on optical lithography which encompasses the physics and theory of operation, including issues associated with advanced processes and corresponding solutions.

Part II consists of Chapters 4 through 9. In Chapter 4 we provide a brief overview of design issues facing mixed-signal circuits and guidance for avoiding some of the pitfalls associated with designing circuits for advanced processes. In Chapter 5 we provide an overview of the ESD issues designers face in the creation of complex systems on a chip. Issues such as multiple supply protection are covered in detail to equip designers in the evaluation of specific ESD requirements. The latest SCR structures are also included as yet another option for developing an ESD protection strategy. Chapter 6 outlines the current trends in I/O buffer design. An overview of the various I/O specifications is provided along with current trends for implementing designs. Power busing issues and simultaneous switching noise issues are discussed at length to illustrate the importance of developing the I/O power bus scheme up front. On-die decoupling is also discussed at length, as this is becoming a key feature required to meet high-speed interface specifications. Chapter 7 takes the reader through the basics of DRAM design and then goes into the techniques to successfully scale the storage capacitor, access transistor, and sense amplifier into nano-CMOS processes. Chapter 8 focuses on signal integrity analysis and design solutions for on-chip interconnects. First, efficient parasitics extraction techniques are presented, with particular emphasis on inductance issues. Then analytical approaches for signal timing, crosstalk noise, and waveform integrity analysis are discussed. In the last part of the chapter we investigate physical and circuit design solutions to improve signal integrity in high-speed signaling. Chapter 9 provides a comprehensive overview of existing design- and run-time low-power design techniques on different levels of a system design, with a focus on circuit-level logic and memory design approaches. The perspective of ultralow power design techniques for future technology nodes beyond 90 nm is discussed at the end of the chapter.

Part III comprises Chapters 10 and 11. Chapter 10 provides guidelines for achieving a manufacturable design. Numerous examples, including post-OPC simulations, are shown of potential issues with the physical layout of circuits along with methods for improvements. In Chapter 11 we cover the design principles for robust and high-performance circuits despite process variation. The chapter begins with a discussion of the sources of process and other variations, and their impact on circuit functionality and performance. Three principal design areas (clocks, SRAM, and selected digital circuits) were chosen as case studies to illustrate these principles. The chapter also includes some guidelines for a DFM-friendly design. The chapter concludes with a brief overview of the need for statistical device modeling for nano-CMOS designs, followed by a brief description of the new features incorporated in the BSIM4 model.

ACKNOWLEDGMENTS

We would like to acknowledge the many people who contributed to the completion of this book. First we thank the subject experts who wrote some of the chapters or sections. We thank the technologists at Applied Materials, Inc.—Reza Arghavani, Faran Nouri, and Gary Miner—for their contributions to the section on equipment requirements for front-end processing. We are indebted to Khaled Ahmad of Applied Materials, Inc. for providing the oxide characteristic data used in the front-end processing section of Chapter 2. We thank Qiang Lu, a technologist at the University of California at Berkeley, currently with Advanced Micro Devices, Inc., for his contributions to the FEOL section. We also thank lithography expert Franz Zach of IBM Microelectronics for the excellent tutorial on optical lithography for the nano-CMOS regime, included as Chapter 3. For Chapter 5 we thank Professor Ming-Dou Ker of the National University of Taiwan, who is a recognized authority on the subject. We thank Martin Brox, the memory guru of Infineon, for Chapter 7. We acknowledge Xuejue Huang of Rambus for her excellent contributions to Chapter 8, and Huifang Qin of UC–Berkeley for writing most of Chapter 9 and combining the work of the authors into this excellent chapter.

We also thank Altera Corporation for supporting this effort, especially Wanli Chang, William Hwang, Kang Wei Lai, Richard Chang, Leon Zheng, Mian Smith, and Howard Kahn for the simulations they ran. We thank Cynthia P. Tran for the physical layouts used as illustrations in this book as well as providing input to the lithographic simulation. We thank John Madok and Michael Smayling for help finding experts within Applied Materials to help write sections of the book as well as acting as consultants.

We gratefully acknowledge Shuji Ikeda of Trecenti/Hitachi; Ryuichi Hashishita, Yashushi Yamagata, and Toshiaki Hoshi of NEC; Richard Klein and Qiang Lu of Advanced Micro Devices for supplying technical data and numerous SE and TE micrographs used in the book. We thank Fung Chen, Armin Liebchen, and Sabita Roy of ASML Masktools for their help with the lithographic simulations as well as supplying the simulation tool used in generating the simulated aerial view of the resist profile used as illustrations.

We thank Professor Mark Greenstreet of the University of British Columbia for reviewing the initial table of contents and for the many valuable suggestions. Last but not least, we express our gratitude toward Professor Chenming Hu for his insightful suggestions and the affirming foreword he has written for the book.