I

INTRODUCTION AND OVERVIEW

THE three papers in this first section present surveys of the present state of the art in analog IC design for radio transceivers and evaluations of new trends in the field, as well as projections of future developments emerging from current research activity.

Low-Power Radio-Frequency IC's for Portable Communications

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Invited Paper

The contributions of integrated circuits to the RF front-end of wireless receivers and transmitters operating in broadcast and personal communications bands are surveyed. It is seen from this that when IC's enable a rethinking of the RF architecture, the wireless device can sometimes become significantly smaller, and consume much less power. Examples are taken from FM broadcast receivers, pagers, and cellular telephone handsets.

Many semiconductor technologies are competing today to supply RF-IC's to cellular telephones. The various design styles and levels of integration are compared, with the conclusion that single-chip silicon transceivers, combined with architectures which substantially reduce off-chip passive components, will likely dominate digital cellular telephones in the near future.

The survey also projects future trends for IC's for miniature spread-spectrum transceivers offering robust operation in the crowded spectrum. With sophistication in baseband digital signal processing, its increasing interaction with the RF sections, and with increasing experience in simplified radio architectures, all-CMOS radios appear promising in the 900 MHz to 2 GHz bands. A specific CMOS spread-spectrum transceiver project underway at the author's institution is discussed by way of example.

I. INTRODUCTION

The portable revolution is upon us today. It promises to empower individuals throughout the world by giving them low-cost access to information wher ever they may be, thus allowing them to make informed decisions and to be more productive in business and at home, without necessarily being tied down to a physical location. It is expected that in the near future, individuals will be equipped with capabilities of local computing and of communications enabling them to perform almost all the tasks that today require the equipment on the office desktop: the telephone, the computer, its connection to a ubiquitous wired network, the fax machine, and so on [1].

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The portable revolution has been many years in the making. The personal broadcast radio receiver and cassette player, as pioneered by Sony, was a runaway global success. The user could construct a private audio environment anytime and anywhere, using a device so small and light that its presence was easily forgotten. Portable computers brought about the next wave of change. The personal computer has had such a large impact on the broad working habits of individuals that without it they are lost. The luggable computer has evolved in a matter of one decade into the portable, the notebook, and the subnotebook. With the establishment of a wide-area network of radio paging transmitters, the personal radio pager has also became very popular since the mid-1980's. Today, the pager network spans the entire continental US and many other parts of the world, enabling the user to receive alphanumeric electronic mail messages. Two-way paging is actively under development. The cellular telephone became widely available shortly thereafter. The user could hook into the international switched-telephone network through the nearest cellular base station with a portable transceiver, which too has scaled down remarkably in size until its weight and volume is the smallest practical [2].

There are many competing visions of how these various portable devices and services will evolve and integrate in the next few years. These are covered extensively in the popular press, and in numerous keynote speeches in technical meetings. A common theme is that users will want a multimedia terminal, capable of wireless access to a global network which can transport communications, images, and databases to the user in an on-demand, interactive fashion [3], [4]. Such a terminal will have capabilities of computing, image acquisition and display, and obviously, of communications. It will likely derive as a hybrid of the various portable technologies available today.

What obstacles must be overcome to realize this vision? There include the very highly integrated electronics, effective displays, and a philosophy of design based on low power dissipation to prolong the battery life of the portable

device. Sometimes single-battery operation will impose the additional constraint of operation at low voltage, as low as 1 V, which will require entirely new ways of doing electronic circuit design.

In the past few years, most designers of mass-market digital IC's have been preoccupied with low-power operation [5]. Principles such as operating CMOS logic at the lowest possible supply voltage have become widely known, and power-down modes, gear-shifting of operating clock frequencies, pipelining and parallelism, subthreshold operation, and other such methods which were once the province of specialized areas such as electronic wristwatches and implantable biomedical devices are becoming commonplace [6]. Studies into the fundamental thermodynamic limits to the energy required for computation are being initiated or revived. There is good reason to believe that all this activity will lead to significant improvements in the conventional circuit and system design styles for digital signal processing and computation.

How will this activity affect the communications aspects of the portable device? What similar principles to low-power digital design are there for energy-efficient wireless communications transceivers? These questions do not have simple answers. Low-power communication systems will result from use of the correct architectures, a sensible partition between analog and digital signal processing, low-power circuit techniques everywhere, and a judicious division between active and passive components. There is still not a widely known, integrated vision on this subject. Furthermore, there remains a gap between the IC design used in the portable applications described above, and the new designs that will be required over the next few years for advanced portable communicators. Consumers are demanding a great deal more functionality and performance, which is stressing present-day technology to its limits, and wireless communicator design itself is in transition from the classic analog modulation techniques used over the past 50–70 years to more sophisticated methods using digital signalling formats and signal-processing methods in transceivers.

This paper summarizes the key developments in the discipline so far, and from them forecasts wireless IC design trends in the near future.

II. Key Signal-Processing Issues in Wireless Transceivers

Were it not for the advent of the portable communications revolution, radio technique would almost certainly have become a lost art. The first edition of the last definitive textbooks on the subject dates to 1943 [7]. Whereas once radio engineering was synonymous with electronics [8], few university electronics curricula today offer a course on radio communications circuits. Only a few modern textbooks on radio design have been written in the past 25 years [9]–[13]. Radio communication methods, at least for nonmilitary applications, have remained relatively unchanged since World War II, and the evolutionary improvements in consumer equipment mainly owes to the use of high-frequency discrete transistors [14], smaller passive components, and building-block IC's which improve the long-term reliability and manufacturability of radio and TV receivers. The major impact of IC technology in these consumer items has probably been at baseband, in adding more user features. In contrast, the front-end radio architectures have evolved almost not at all in the past 40 or so years. For instance, IC's have contributed digital volume-control, digital frequency-tuning, features to alleviate manual effort on the part of the user, but the RF and IF sections still contain discrete and passive components in rather conventional architectures.

Why is this? It is partly because radio frequencies were too high for the low-cost IC technologies traditionally used in the consumer electronics industry. It is also because advances in component packaging alone have led to rapid downscaling in the size of consumer devices, often obviating the need to rethink the electronics. As a result, only a few individuals in a handful of institutions worldwide have concerned themselves with thinking about these problems. Today, as conventional solutions no longer suffice for the future wireless communications devices, there is a rekindling of interest in this subject, which has led to much rediscovery and some invention. Baseband IC designers are now attempting to apply familiar techniques to wireless, while microwave IC designers are exploring what to them are low-frequency commercial opportunities for their technologies.

To set the stage for further discussion, some of the unique problems of radio receivers and transmitters are first described. Unlike familiar wireline communications, the wireless environment accommodates essentially an unlimited number of users sharing different parts of the spectrum, and very strong signals coexist next to the very weak. The radio receiver must be able to select the signal of interest, while rejecting all others. It must do so using less than perfect active and passive components. There are two important problems in the receiver: *image-rejection* and *dynamic range*. Image-rejection relates to the receiver's ability to select the desired signal from the array of signals occupying the spectrum. Ideally, it might do so with a tunable bandpass filter, whose center frequency could be positioned at will in the RF, and whose passband was one channel wide. A filter with this small a fractional passband does not exist. Instead, a practical RF bandpass filter, which may or may not be tunable, will preselect an array of radio channels including the one of interest (Fig. 1). The other preselected channels are then removed at a lower intermediate-frequency (IF), by translating them in frequency with a downconversion mixer, and centering the desired channel within a bandpass filter at IF. The other mixer input is a frequency-tunable local oscillator (LO), offset by IF from the desired channel. As the preselected band after downconversion will very likely occupy an interval greater than (0, IF) on the frequency-axis, the IF bandpass filter will select both the desired channel, and another *image* channel the mixer has translated to –IF. The subsequent detector circuit will be unable to distinguish

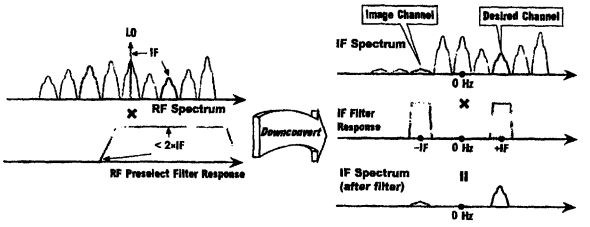


Fig. 1. The image-reject problem in radio receivers. The RF preselect filter passband must be determined with prior knowledge of the IF. The preselect filter is responsible for image-channel suppression before downconversion.

between the desired and the image channels, and therefore its output will be the result of the superposition of both. However, if the stopband of the preselect filter lies less than $2 \times$ IF away from the desired channel it will attenuate the image, so only the desired channel will contribute energy at IF. The receiver designer first studies the available filter technologies, and then chooses an appropriate IF which yields an acceptable image suppression. A high IF relaxes the prefilter passband specification, but it also means that the downconverted signal requires high-frequency amplifiers, which are usually power-inefficient. Further, the IF filter requires a smaller fractional passband. In such cases, following image rejection at this high IF, the channel may be selected after downconversion to a second, lower IF. In such a double superheterodyne, or dual-conversion receiver, the first IF may actually lie at a higher frequency than the incoming RF to make image rejection easier.

The noise-level and nonlinearity in the RF amplifier and first mixer usually set the receiver dynamic range. Consider reception of a weak channel surrounded by large undesired channels in the preselection band (Fig. 2(a)). First, the input-referred noise of the receiver directly adds to the sought signal, corrupting its signal-to-noise ratio (SNR). Second, the large adjacent channels will experience the nonlinearities in the RF amplifier and mixer, and some of the products of the ensuing intermodulation distortion may overlap the desired channel. The IF filter cannot reject these unwanted products, which, like noise, will degrade the received SNR. As the receiver frequency response is normally bandpass, its nonlinearity is measured by applying two tones of equal amplitude closely spaced in frequency (f_1 and f_2) at it input, and measuring the rise in the third-order intermodulation products (at $2f_1-f_2$ and $2f_2-f_1$) with input level (Fig. 2(b)). All other intermodulation tones usually lie outside the receiver passband. On a logarithmic plot, the third-order intermodulation level rises at a slope of 3 relative to the fundamental tone at the output. The two lines intersect at a point called the input-referred 3rd-*order intercept* (IP3). The intercept point is usually extrapolated from measurements at low levels, because the receiver front-end will saturate at large inputs. The 1-dB *compression point*, the input level which causes the receiver gain to drop by 1-dB relative to the small-signal gain, specifies the onset of saturation. The input-referred noise-level may be included in this plot to define a spurious-free dynamic range (SFDR), although this is rarely used in radio

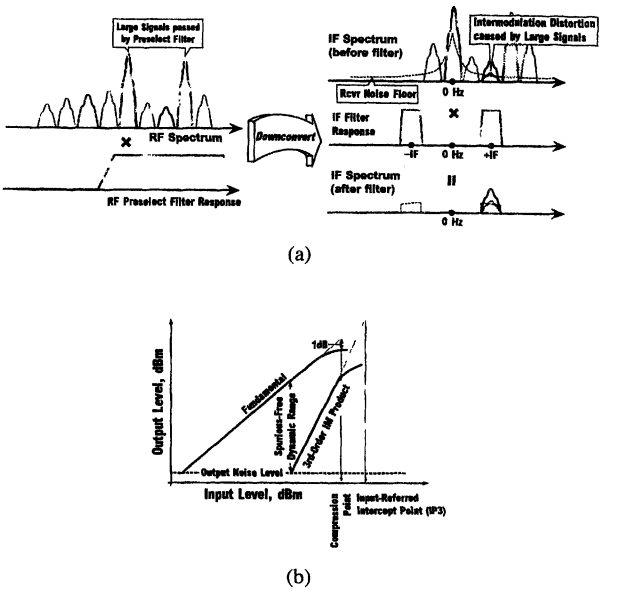


Fig. 2. The dynamic range problem in the radio receiver. (a) Adjacent large signals may create intermodulation products superimposed on the desired channel. Receiver noise floor is fundamental limit to sensitivity. Receiver dynamic range is specified (b) in terms of extrapolated 3rd-order intercept point, and noise level.

specification. Usually the input noise-figure (NF) and the input-referred intercept point (IP3) are separately specified.

Similar specifications apply to the transmitter, which operates at much larger signals. Suppose, as is almost always the case, that the transmitter is required to emit a single-sideband, suppressed-carrier output. Owing to circuit imperfections, it may also emit small amounts of the carrier and the unwanted sideband, which typically lie in the passband of the subsequent RF filter (Fig. 3). These unwanted emissions may become interferers for adjacent channels. Nonlinearities in the power amplifier may also produce emissions of intermodulation products at other frequencies. Phase-noise in the local oscillator responsible for upconverting to RF will convert to noise added to the signal, and the amplitude of this noise increases with the transmitted signal. This noise could possibly overwhelm nearby weak channels. Transmitter performance is usually specified in terms of the relative levels of unwanted signals to the desired signal, and in terms of absolute spectral density of output noise at maximum output power.

To understand the rationale underlying receiver architecture, let us use as an example the familiar broadcast FM receiver. The architecture to be described is the same that Armstrong, the inventor of FM and the superheterodyne, had originally proposed for FM reception. The desired channel consists of a carrier in the 88–108 MHz band, modulated by up to ± 75 kHz. Neighbouring channels are spaced apart by 200 kHz. The receiver must select the desired channel while rejecting nearby channels, and it must be sensitive to a signal of a few tens of microvolts induced on the antenna. A simple FM antenna is wideband, and will pick up signals well outside the broadcast FM band. The low-noise bandpass amplifier in the front-end may at best mildly attenuate the out-of-band signals—the

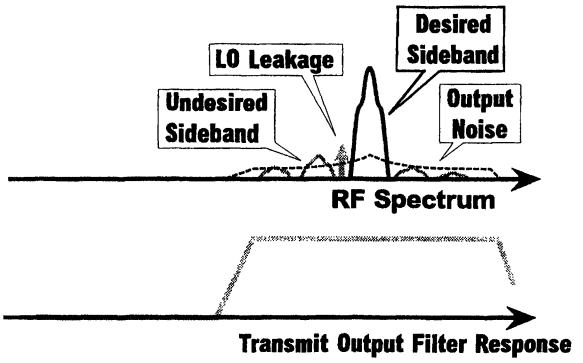


Fig. 3. Transmitter imperfections (such as mismatches in a quadrature upconverter) result in the appearance of spurii in the emitted spectrum (referred to as "spectral regrowth"). The spurii may not be removed by the output filter, and may superimpose on adjacent channels. Emitted noise might overwhelm weak adjacent channels.

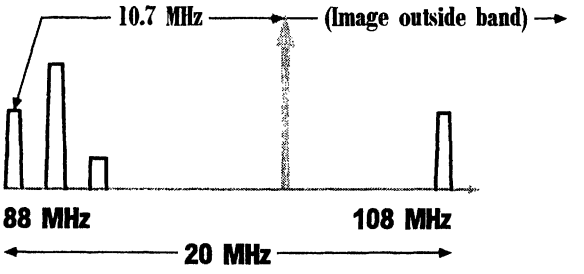


Fig. 4. The 10.7 MHz intermediate frequency conventionally used in FM receivers is the lowest frequency which will guarantee that the image lies outside the FM broadcast band. The FM demodulator will reject a (non-FM) image channel entering the receiver. 10.7 MHz passive bandpass filters in the IF strip select the desired channel.

actual channel selection must be done elsewhere. The RF amplifier uses an inductive load to resonate with the transistor and tuning capacitances, thereby transforming an inherently low pass characteristic to bandpass centered on the frequencies of interest. The transistor $f_{\max}$ limits the highest frequency at which such a tuned amplifier can still provide a gain greater than unity. This figure-of-merit is familiar to microwave circuit designers and to device designers, whereas baseband IC designers deal more often with transistor f_T, the capacitance-limited unity current-gain frequency. In bipolar IC processes not optimized for small-signal high-frequency use, $f_{\max}$ is comparable to f_T, whereas in the best RF processes it may be twice f_T [15], [16].

It is impossible to select the desired channel at RF, because no tunable filters exist with the required fractional bandwidth of 0.15% at 100 MHz. Therefore, following sufficient amplification at RF to overcome the noise-level of the following circuits, the signal is mixed down by a variable-frequency local oscillator to a lower IF. Furthermore, a filter to select the desired channel at IF will have a fixed center frequency, and the fractional bandwidth in the passband will be more reasonable. From this perspective, it is desirable to use as low an IF as possible. However, image-rejection poses yet another constraint on choice of IF. Conventional broadcast FM receivers use an IF of 10.7 MHz as a compromise. This IF guarantees that the image always lies outside the FM band (Fig. 4). It is unlikely, however, that the preselect filter can suppress this image, which will therefore either add noise or AM to the desired signal. However, the subsequent FM detector is inherently insensitive to both these forms of impairment. In this way, a medium-valued IF is made possible by exploiting properties of the detector, and thereby the fractional passband specification for the preselect filter is relaxed. The first mixer downconverts the entire FM band, with the desired channel centered at 10.7 MHz. A varactor-tuned Colpitts oscillator may be used as the first local oscillator. Prior to detection, a cascade of identical, fixed-frequency ceramic bandpass filters, each with a 200 kHz passband centred at 10.7 MHz, passes the desired channel while rejecting neighbouring channels [17]. In a high-quality receiver, the RF amplifier may be a discrete GaAs MESFET with a tuned load ganged to the LO tuning element, and another ganged tuned circuit may couple the antenna signal into the receiver [17].

To transplant this style of discrete radio-circuit design to IC's, one would have to implement LC tuned circuits and filters on silicon. One can indirectly surmise these concerns in the Motorola series of IC design textbooks from the 1960's, which discuss loss in spiral metal inductors fabricated on silicon substrates [18], as well as issues relating to simulated inductors for active filters at IF for radios, made with gyrators and capacitors [19]. However, on-chip spiral inductors of useful values were found to suffer excessive capacitance to the substrate, which lowered their self-resonant frequency to the point that they were not usable beyond the VHF band. It gradually became part of the collective consciousness of IC designers that on-chip tuned circuits are generally impractical.

When useful tuned amplifiers did appear on monolithic integrated circuits, it was not for the VHF to UHF range of relevance to consumer applications. Instead, it was military applications at much higher frequencies which drove the development of monolithic microwave integrated circuits (MMIC's) during the 1980's. MMIC's typically use MESFET's as the active device on semi-insulating GaAs substrates. This technology has enabled miniature radar, remote sensing, and communications at frequencies up to tens of GHz. The on-chip wavelengths are so small that monolithic distributed circuits may be built. MMIC's take advantage of the semi-insulating substrate in two important ways. Transistors on these substrates have lower parasitic capacitance, which means that they amplify to higher frequencies. It is also possible to build low-capacitance interconnect with airbridge structures, and high-frequency passive components such as spiral inductors required for narrowband tuned circuits. Thus on MMIC's, the board-level design styles used hitherto by radio- and microwave-engineers could be miniaturized. However, over its many years of existence, GaAs MMIC technology has not had the major impact on consumer electronics that its adherents had hoped for. Makers of consumer electronics favor silicon IC technology wherever feasible because of its low-cost, high

yields, and the relative ease of mixing analog and digital circuits on a large scale.

It is anticipated that by the year 2000 about 300 million portable consumer wireless devices will be in use [20]. What IC technologies will enable the RF front-end of these devices? Do miniaturization and long battery-life call for architectural innovations in transceivers? What new circuit design styles will evolve in response? There is much curiosity and speculation on these matters, yet little is generally known about RF-IC design, or on the possible impact of large-scale integration and power-reduction strategies in the front-end of wireless transceivers. This paper presents a brief survey of the use of IC technology in wireless receivers and transmitters since the 1970's to date, and from this projects some future trends. RF-IC's are roughly defined as integrated circuits operating in the band of frequencies from 400 MHz to 2500 MHz, which covers most consumer wireless communication devices. As opposed to MMIC's, which were almost exclusively fabricated on III-V compound semiconductor substrates at small-scales of integration, mature silicon technologies will play a large, if not the dominant, role in RF-IC fabrication. It is the author's belief that in response to pressing demands for ubiquitous wireless access, both the underlying semiconductor technology and the design styles will rapidly evolve to realize the single-chip "VLSI radio" in the not too distant future.

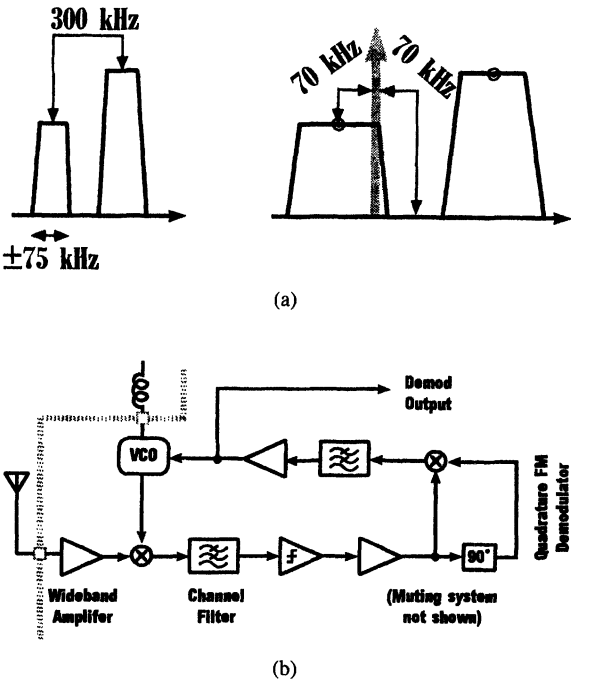


Fig. 5. (a) An alternative choice of IF in the FM band, which places the image in the gap between adjacent channels. The IF strip, including the channel filters, now operate at a 70 kHz frequency. (b) An FM receiver using a 75 kHz IF. The channel filter is an active-*RC* implementation on-chip. A frequency feedback loop compresses the incoming frequency swing. Except for a tuning inductor, no high-frequency off-chip components are required.

III. IC's in Broadcast Radio Receivers

The two-way wrist radio has fascinated the popular imagination since its introduction in the popular American cartoon strip, *Dick Tracy*, in 1946 [21]. This is the ultimately unobtrusive piece of consumer electronics. Let us now see how feasible it is to build an FM receiver of this size with microelectronics technology. For the average user to accept such a radio, its selectivity and sensitivity must be comparable to that of tabletop models. If in the FM receiver described in the previous section all the transistors in the receiver electronics were to be integrated on to one silicon chip, the radio would still need a considerable number of off-chip tunable inductors and ceramic filters, and in spite of state-of-the-art miniature packaging, the components could not plausibly all fit into a wristwatch. Neither would the power dissipation be commensurate with the life of a wristwatch battery.

The first generation of silicon bipolar IC's developed in the late 1970's for the IF and baseband portions of broadcast receivers more or less contained the transistors of conventional receivers assembled on to one or more IC's [22]–[24]. However, integration did afford freedom to use transistor-rich circuits for higher performance. Circuit techniques such as double-balanced mixers using the Gilbert analog multiplier, phase-locked loops as FM demodulators, and balanced on-chip signal paths to attain greater immunity to pickup and common-mode noise became widely used as a result. By eliminating many of the coupling coils and other noncritical discrete components found in older radio circuits, IC's contributed to lowering the cost of assembling and aligning the final product. In the RF section, though, the receivers still used the conventional 10.7 MHz IF superheterodyne architecture implemented with shielded discrete-component circuits.

In the early 1980's, Kasperkovitz at Philips [25] made the first significant explorations into alternative architectures for highly integrated radio receivers. He realized that to reduce receiver size and power dissipation, it was very important to eliminate the many off-chip passive components. If certain passive inductors, capacitors, and resistors could not be eliminated, they could at least be packaged in surface-mount outlines for very small size. However, neither the volume of the IF ceramic filters could be readily scaled down, nor could their characteristic impedance be scaled much above 50Ω. Each filter requires an on-chip analog driver of comparable impedance. Alternatively, the filter may be realized on-chip as an active bandpass circuit of sufficient selectivity and dynamic range. Although a gyrator-capacitor based active filter is possible in principle, small phase-shifts in the gyrator transistors at the 10.7 MHz IF can seriously upset the filter passband shape. Active resonators are also known to suffer from a larger internal noise level than their passive counterparts, and this discrepancy worsens with increasing pole-Q and pole frequency [26]. Kasperkovitz solved the problem with an *architectural innovation*, by dramatically lowering the IF from 10.7 MHz to 70 kHz. This makes it a great deal easier to implement an IF active channel-select filter, which

now need only be lowpass. Further, at a given dynamic range, the power dissipation in an active filter also scales down with the IF [26]. The low IF eliminates the off-chip channel-select filter and reduces power dissipation, both very desirable properties. But what of the image frequency, the principal reason for the choice of 10.7 MHz?

At a 70 kHz IF, the image frequency lies half-way to the adjacent FM channel (Fig. 5(a)). The image therefore is the inter-channel noise in the FM band. As an RF preselect filter cannot possibly reject an image this close to the desired signal, it will pass unattenuated to worsen the received signal-to-noise ratio (SNR) by 3-dB. Another consequence of this choice of IF is that after the first downconversion, an instantaneous frequency deviation in the received FM signal of more than 70 kHz will alias around dc to produce distortion. This is avoided by compressing the frequency deviation to $\pm$ 15 kHz with a negative feedback frequency-locked loop prior to downconversion (Fig. 5(b)). The FM mono/stereo radio [27]–[29] requires, in addition to the single-chip receiver, only 15 small capacitors and two inductors, and this collection of parts readily fits inside a wristwatch. A miniature earphone is plugged into the watch, and the earphone lead serves as the antenna. The radio when active drains 8 mA from a 4.5 V supply.

Sony, one of the world's leading makers of miniature radios, has also recently modified its integrated FM radio-receiver architecture from the conventional 10.7 MHz IF [30] to low-IF [31]. In the new architecture, a high first-IF of 30 MHz is used, so any out-of-FM band image falls in the stopband of a fixed 80 to 110 MHz bandpass preselect SAW filter after the antenna. A wideband IF amplifier boosts the received signal level of *all* FM channels *without* any filtering—amplification at 30 MHz is not a problem on this modern silicon bipolar IC process. Further, at a 30 MHz IF the entire broadcast FM band falls to one side of the LO frequency, which means that any channel in the FM band may be selected after the first downconversion. Following this, another mixer converts to a low second-IF of 150 kHz, and thereafter an on-chip 9th-order active-RC lowpass filter rejects adjacent channels. The low second-IF, however, will pass an image FM channel as well as the desired channel, and as there is no filtering at all at the first IF, an *image-reject mixer* is used for the second downconversion (Fig. 6). The variable-frequency first LO tunes the desired channel, while the second LO, which must produce quadrature outputs for the image-reject mixer, is at a fixed frequency.

The image-reject mixer provides a trigonometric solution to a difficult filtering problem [32]. The desired channel and its image are frequency-converted into two paths by mixers driven by quadrature phases of an LO. The mixer outputs are then phase-shifted 90° with respect to one another. The sum of these two signals will select the desired channel and suppress the image, while, *vice-versa*, the difference will select the image. The extent of image suppression depends on the gain matching of the two paths, and on the phase-accuracy of the LO quadrature outputs. For these reasons, this concept has only become practical with IC technology,

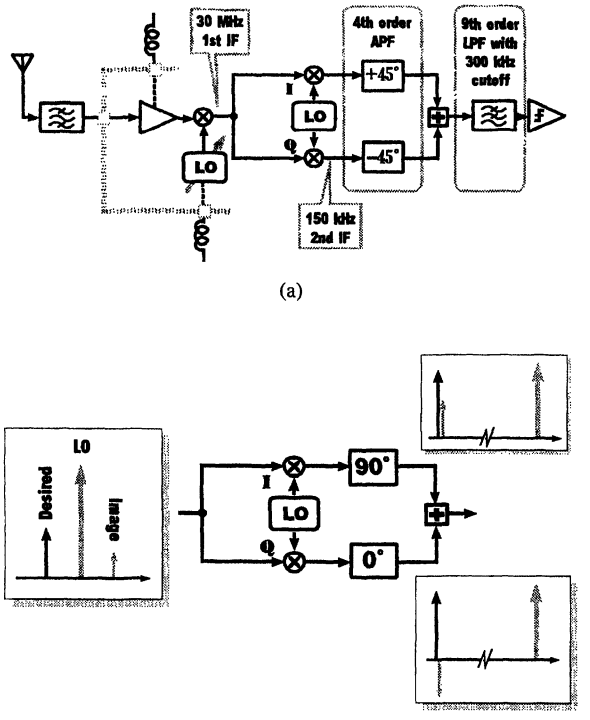


Fig. 6. (a) An alternative architecture for a single-chip FM receiver, with a 30 MHz IF chosen for strong image-rejection, and to translate the all channels in the FM band to IF on to one side of dc on the frequency-axis. The image-rejection mixer at 150 kHz selects the desired channel, while rejecting the undesired one 300 kHz away. Aside from a noncritical RF preselect filter, the remaining filters are active on-chip, including the phase-shifts in the two arms of the mixer. (b) The image-rejection downconversion mixer. The image and desired tones are at positive- and negative-frequency offsets from the local oscillator, and are discriminated in the mixer by a relative inversion of polarities in the two arms.

where the two paths are well matched on-chip and track each other over temperature. Image suppression on the Sony chip is limited to about 40–45 dB by residual gain mismatch in the two paths. An allpass active RC-CR filter produces 90° phase-shifted versions of the downconverted input. This receiver drains about 15 mA from voltages as low as 0.9 V in either FM or AM mode. All the necessary transistors are integrated on-chip—the RF amplifier portion, however, uses an off-chip load inductor and the local oscillator needs an off-chip LC tuned circuit.

The circuit techniques which enable sub-1 V operation are also interesting (Fig. 7). The antenna signal drives the emitter of a common-base NPN, which forms the tail of a differential pair. The input resistance of the common-base stage matches the antenna impedance. The signal develops at one inductively loaded collector of the differential pair, while the other collector dumps a fraction of the signal current into the supply in response to an AGC differential control voltage. Following amplification by a resistively loaded differential pair in cascade, the balanced RF signal is level-shifted into the first mixer, a simplified double-balanced Gilbert-cell with resistors instead of current sources in the tails.

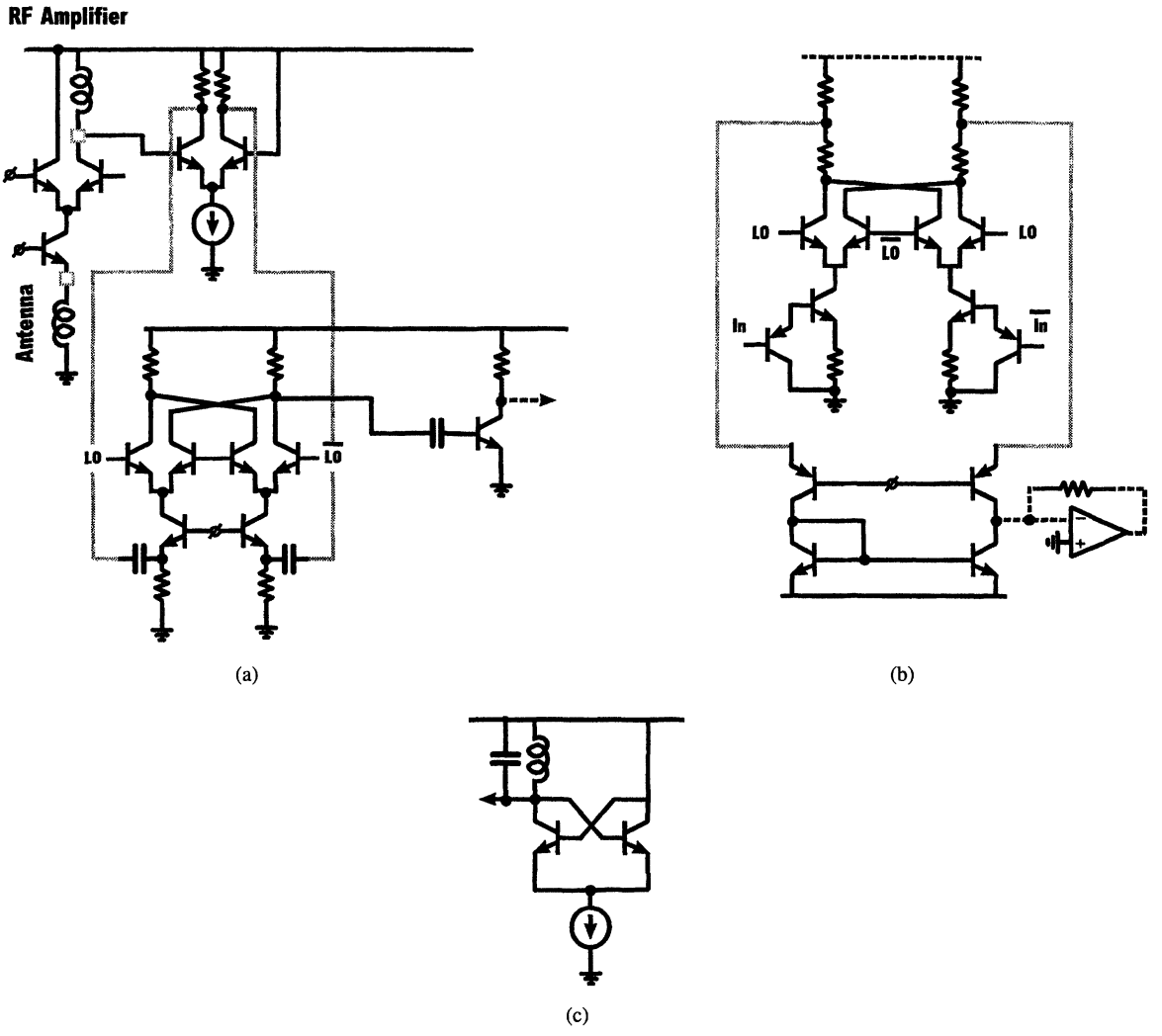


Fig. 7. Low-voltage circuits capable of operation with a 0.9-V supply. (a) RF amplifier. Note how the antenna carries the RF amplifier bias current, and how the on-chip capacitors level-shift the RF signal path. (b) IF amplifier. As the signal is downconverted in frequency, active level-shift and op amp circuits appear. (c) The cross coupled differential pair negative resistance is popular for LC oscillators.

As inductors do not drop a dc voltage, they make convenient loads for stacked transistor circuits operating at a low supply voltage. The signal on the free end of the inductor will swing above the supply. This is the case in the local oscillator, which implements a negative resistance of $-1/g_m$ with a cross coupled differential pair, causing an LC tuned circuit across it to oscillate. The oscillation amplitude is limited by the differential pair nonlinearity to a small multiple of kT/q.

As the signal propagating through the receiver downconverts in frequency, low-frequency circuit techniques and devices with a lower f_T are used. For instance, the 30 MHz IF signal couples into the second mixer through PNP emitter followers. At the 150 kHz IF, common-base PNP's and current mirrors level-shift down the signal, which is further amplified in an op amp.

This receiver is a significant example of how architectural rethinking combined with appropriate IC design styles has resulted in a very different solution to the well established broadcast FM receiver.

IV. IC's in Wireless Paging Receivers

Miniature wireless communicators to page people on the move were first developed in the late 1950's. The Bell System's Bellboy™ paging receiver [33] anticipated many of the concepts underlying today's pagers. The system operated at a 150 MHz RF, addressing a receiver by frequency-modulating the carrier with a unique set of three tones, which the intended receiver recognized at baseband by the simultaneous response of three passive reed resonators. The superheterodyne receiver operated at 4 V using a total of only ten transistors [34], a notable early example of low-power and low-voltage circuit design. The low IF of 6 kHz meant that simple, capacitively coupled 10 kHz lowpass (rather than bandpass) filters could select the desired channel. Also, all low frequency amplifiers after the RF section used transistors biased at small currents. The two stages in the cascode RF amplifier were inductively coupled to share, or reuse, the same bias current, a power-saving method found even in todays MMIC's.

Paging receivers have been in continuous evolution since then. They are supported by a sophisticated nationwide wireless infrastructure. The modern pager uses digital signalling at rates anywhere from 500 to 1200 b/s, encoding binary data with a simple positive- or negative-offset of the carrier frequency—the binary frequency-shift keyed (FSK) modulation. In spite of market pressure to reduce the battery drain and miniaturize the unit, paging receivers until the early 1980's used conventional radio architectures without exploiting the powerful simplifications implied by this signaling scheme. Such a double-superheterodyne receiver [35] might consist of a *first upconversion* of the received signal to suppress the image channel with an RF crystal bandpass filter, and then a *downconversion*, followed by channel-selection with a ceramic bandpass filter. An analog frequency-discriminator demodulated the FSK. Much as in broadcast FM receivers, this architecture required tuned amplifiers and passive filters, which constrained further miniaturization of the paging receiver.

Vance at ITT Standard Telecommunication Laboratories first realized that by taking the idea of low-IF to its limit of *zero-IF*, an FM receiver could be scaled down to one chip with only one or two passive RF components. A quadrature downconversion mixer could discriminate positive- and negative-frequency modulation centered around dc [36]. There is now *no* image to be rejected, and a lowpass filter suppresses adjacent channels. If applied to analog FM as in broadcast signals, however, this scheme suffers from the dc offsets in the amplifiers and their flicker noise, which will seriously corrupt the SNR at mid-channel. Furthermore, the limiting amplifier which analog FM receivers use in place of AGC does not respond to dc inputs, because there are no zero-crossings. In paging receivers, however, the spectral energy clusters in two lobes on either side of dc owing to the relatively large modulation index, and zero-IF (or direct-conversion) is exactly the right solution [37], [38]. This remarkably simple receiver (Fig. 8) consists only of a quadrature demodulator, lowpass filters in each arm, limiters, and a D-type flip-flop detector. When integrated on an early bipolar chip, it drains 2.5 mA from 1.8 V when active, although in standby the current drain falls to a mere 50 μA. Large-value off-chip capacitors are used for ac coupling and for the lowpass filters. A second low-frequency digital CMOS IC performs all the user interface functions. Data is encoded by offseting the carrier frequency by $\pm$ 4.5 kHz, so capacitive coupling with a corner frequency below 1 kHz blocks out receiver dc offsets and lower frequency flicker noise from corrupting the signal-to-noise ratio. A 10 kHz lowpass filter suppresses high frequency out-of-band noise and adjacent channels. Vance also pointed out that data in a binary-FSK signal downconverted in quadrature to dc may be recovered by a simple flip-flop, when the limited output from one arm of the downconversion mixer is applied to the D-input, and from the other arm to the Clock-input. Although exceptionally simple, this flip-flop detector makes instantaneous decisions and therefore has poor immunity to a single noise spike. More sophisticated detectors must be used to get an acceptably low bit-error

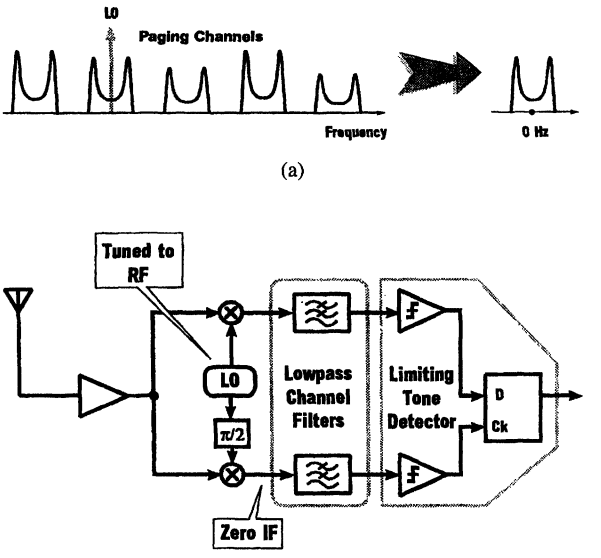


Fig. 8. A direct-conversion single-chip receiver for FSK demodulation. (a) There is no image channel here, and all channel-selection filtering is on-chip at baseband. (b) Note that the receiver requires no AGC, only limiters, as all information is contained in the zero crossings. The signal path must be capacitively coupled to suppress the undesirable dc offsets in the receiver electronics. Quadrature paths discriminate positive and negative frequency offsets.

rates at typical received SNR's. For instance, the inputs of two flip-flops may be cross coupled to the quadrature channel outputs, and the decision may be derived from the analog average of the two outputs [37]. The optimum binary-FSK detector in the presence of Gaussian noise correlates the downconverted signal with the two possible offset frequencies, integrates the output, and declares a valid bit when one of the integrator outputs crosses a threshold [39]. Even the most complex detector will dissipate a small power, because it operates at the low baseband data rate.

Pager IC's from Philips originally used a frequency-offset receiver principle [40], [41], whereby the local oscillator frequency is adaptively offset from the received carrier by 2 kHz, thus converting the FSK tones to 2.5 kHz and (aliased to) 6.5 kHz. This avoids a quadrature downconversion to differentiate between positive and negative frequency, but it requires a fairly sophisticated automatic frequency control. A frequency discriminator detects data. In addition to the local oscillator crystal (operated here at its fifth-overtone), this chip requires three off-chip tuned circuits. Philips later recognized the simplicity of a zero-IF receiver for this application [42]. In this single-chip receiver, the RF amplifier requires one off-chip inductor, the quadrature phase-shift circuits in the mixer another; both inductors are combined into one off-chip signal path. The channel-select filters are entirely on-chip. They consist of a third-order active *RC* lowpass filter, followed by a 7th-order gyrator-based lowpass filter with a 15 kHz cutoff. Most of the signal amplification occurs at these low frequencies.

NEC's paging receivers evolved from the superheterodyne [35], [43] to direct-conversion [44] in an effort to reduce receiver volume and parts count. Others have de-

veloped similar zero-IF bipolar integrated front-ends [45], [46]. A notable feature of the chips is that much of the die area is taken up by the capacitors for ac coupling the signal path and for the on-chip lowpass filters. Most pager IC's operate at supplies of 2 V to as low as 1V, and are implemented in silicon bipolar technology. In addition, full-featured pagers require 20 000 gate-equivalent digital IC's for the user interface [47], low-voltage EEPROMs for customization and software, and capability to drive a liquid-crystal display. The basic paging receivers can fit within a wristwatch [48]. The direct-conversion FSK digital paging receiver concept has also been successfully used at very low carrier frequencies (100's of kHz) with much lower data rates in implanted devices for biomedical applications [49].

V. IC's in Cellular Telephone Transceivers

Mobile and handheld cellular telephones are the first widespread two-way radios for consumer use. They were preceded by cordless telephones for local-area use. These wireless telephones must meet stringent demands for low weight and volume, long battery life, low cost, and reliable network access to be successful with consumers. In contrast, walkie-talkie transceivers were always aimed at specialized markets, and did not face these pressures for miniaturization. The average consumer, for instance, will not voluntarily accept a transceiver of the size and weight that policemen or soldiers carry as part of their outfit. Further, to support large numbers of users in a crowded radio spectrum, wireless telephones use more internal signal processing than other common transceivers, and must be capable of connecting to the public switched-telephone network [50]. Features such as digitally selected channels, direct-sequence spread spectrum, and diversity-selection are now becoming common. The transceivers perforce must use highly integrated, low-power electronics. Thus it may be said that with the advent of the modern cellular telephone the conventions of wireless design are being reexamined, and sometimes rewritten.

The first generation of cellular telephones carried voice signals by analog frequency modulation of a carrier. In the US AMPS system, for example, the handset receives at a carrier selected from the 869–894 MHz band, while it transmits on a carrier in the 824–849 MHz band. These 25 MHz wide bands are separated by 45 MHz between the uplink and downlink, enabling the user to talk and listen at the same time much as on the wired telephone (users are not too fond of the "over, over-and-out" protocol). An antenna duplexer suppresses coupling from the transmitter into the sensitive receiver, acting as the equivalent of a two-to-four wire hybrid transformer in a telephone. This duplexer is a passive three-port designed to pass energy in the receive frequency band from the antenna port to the receive port, while attenuating energy in the transmit band from the transmitter into the receiver. It is either made with high-dielectric ceramic resonators [51], or with a SAW filter and coaxial resonator in parallel [52]. The receive portion of a conventional handset resembles a broadcast

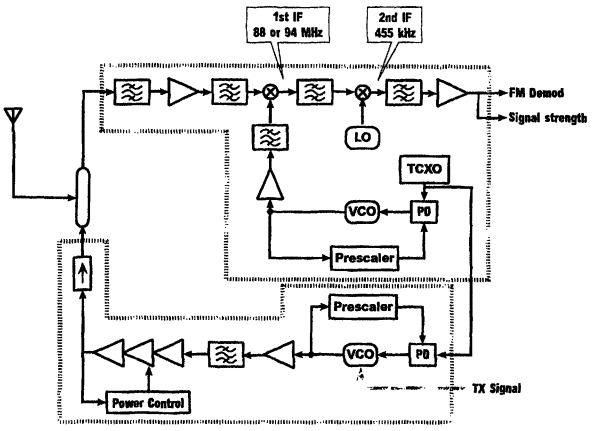


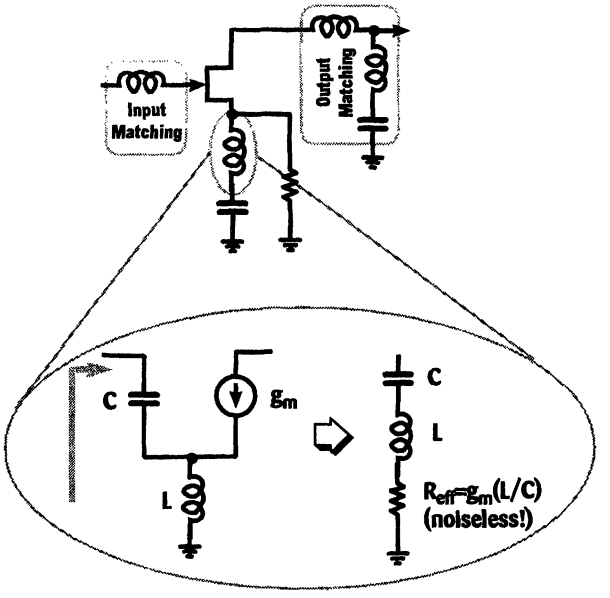
Fig. 9. The transmit and receive front-end of an analog cellular telephone. Receiver uses conventional double-superheterodyne architecture, while transmitter is one-step upconversion.

FM receiver (Fig. 9). If the local oscillator at the first mixer lies at a higher frequency than 894 MHz, the image is guaranteed to lie outside the AMPS band. Furthermore, an LO offset of more than 45 MHz ensures that the image is attenuated by the receive-band SAW filter, suffering at least 20 dB loss in each of the two filters in the handset [53]. A first IF of 90 MHz is therefore often used; this also avoids problems caused outside the handset by parasitic LO leakage through the antenna [54]. The desired channel is selected by locally synthesizing the first IF. This is followed by downconversion to a fixed second IF of 455 kHz, then demodulation by a frequency discriminator.

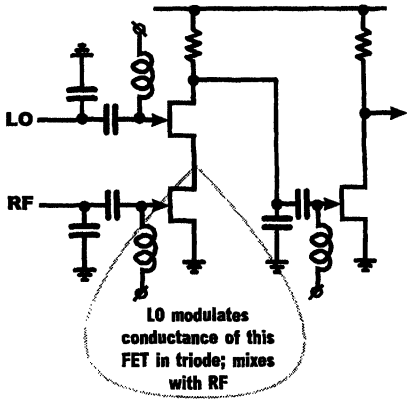
The first-generation of small-scale IC's for portable communication devices offered building-blocks for the intermediate-frequency chain, such as the mixer and local oscillator for conventional single or double-superheterodyne receivers [55], the IF amplifier chain and signal-strength indicator [55], or a standalone image-reject mixer [56]. Today, almost every major semiconductor company with an interest in the communications market offers building-block IC's at this scale of integration.

Although IC's entered the IF portions, the RF front-end circuits continued to be made from discrete components. An RF amplifier and a first mixer may be mounted with the associated filters on a dense miniature board [57], [58]. Discrete bipolar transistors responded to needs for portable RF applications, by offering, for instance, a low noise figure and f_T exceeding 5 GHz at less than 1 mA bias currents [59], [60]. Manufacturers of passive components, too, have steadily scaled-down their package sizes for high-density board mounting.

There is little argument, though, that the RF front-end components must also be integrated to reduce power dissipation. In competing with passive solutions, the RF-IC's must cross some important thresholds of low-price and high-performance [61]. However, they offer the prospect of an order-of-magnitude reduction in physical volume of the front-end electronics, and power savings will accrue by routing RF signals at a high impedance on-chip, while eliminating the low characteristic impedance interconnects



(a)



(b)

Fig. 10. Typical standalone GaAs MMIC's implementing (a) Low noise amplifier and (b) downconversion mixer. Concept of series-feedback inductor for low-noise matching illustrated.

between discrete packages. Various reasons have been advanced for why GaAs MMIC technology is now the right choice for cellular telephones [62]–[64]. They are summarized as follows: first, that owing to the semi-insulating nature of the GaAs substrate, reasonable-size inductors may be integrated with transistors to make high-frequency monolithic tuned circuits, which allows for lower current operation at a given frequency than would be possible with RC broadbanding techniques; and, second, that MESFET's afford lower noise figures at a given bias current than a bipolar transistor in a comparable silicon bipolar technology. Most GaAs MMIC's integrate front-end components for cellular applications at a small scale. For instance, a chip may integrate a tuned RF low-noise amplifier in the 900 MHz band, or a mixer and a local oscillator [64]–[72].

The typical RF amplifier may consist of only one or two FET's, with LC matching circuits on the input and the

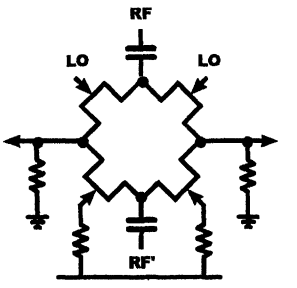


Fig. 11. A four-FET commutating switch mixer. The balanced LO signal switches the FET's, which chop the RF signal to produce the sum and difference frequencies.

output ports for standalone operation in a 50 Ω environment (Fig. 10(a)). A powerful and popular method to match the capacitive FET input is to insert a series feedback inductor, L, in the FET source, which at high frequencies contributes a *resistance* $g_m L/C_{GS}$ at the input port [73]. This method is preferred to resistive feedback found in wideband amplifiers for impedance matching, because unlike feedback resistors, the inductor does not degrade the noise figure. MMIC's from Matsushita favour the use of dual-gate MESFET's with RC matching instead of inductors [74], possibly because spiral inductors consume too large a chip area. GaAs IC designers must closely watch their chip real-estate to remain competitive in price. The various low-noise amplifiers operate in the 0.9–2 GHz bands, with gains of 15–20 dB, and noise figures of around 3 dB. These submicron MESFET IC's drain anywhere from 3–5 mA.

The received RF is typically downconverted by the local oscillator modulating the conductance of the mixer FET through a cascode FET (Fig. 10(b)). The mixers yield conversion gains greater than 10 dB, noise figures of 10–12 dB, and third-order input-referred intercept points of -5 to 0 dBm. Dual-gate MESFET's are naturally suited for mixer use, and offer a similar performance [74]. A recent 0.7 μm GaAs MMIC offers an LNA-mixer pair draining 3 mA from 3 V, with the LNA producing 13 dB gain, 3.6 dB noise figure, and an input-referred IP3 of -11 dBm [75].

Slicing across the system a little differently, another MMIC implements the downconversion and upconversion mixers for the receiver and transmitter, respectively, integrating their shared local oscillator on the same substrate [76]. The four-FET switch mixer (Fig. 11) is very linear, but it suffers from two disadvantages: it requires a large local oscillator drive to turn the switches on and off [77], and unlike the bipolar transistor Gilbert-cell analog multiplier, the switch mixer is lossy, requiring additional signal amplification from the following stages.

The current generation of analog cellular telephones transmits power levels of more than 1W (30 dBm). RF power amplifiers are usually packaged in a separate module with some form of integral heat-sink. A preamplifier, or in radio terminology, exciter, in the transmitter section boosts the modulated carrier level close to 0 dBm to drive the power amplifier input. The power amplifier module itself usually consists of a cascade of two or three FET's, tapering up to a single large-size FET which will deliver the

required signal current into the antenna load. Furthermore, as the power amplifier is the largest single source of battery drain, it must have a *high conversion-efficiency*. Much as in baseband power amplifiers, an efficient RF power amplifier is biased close to cutoff to reduce the dc standing current, and then driven by the input signal in Class A-B or Class-B mode. Narrowband filters at the amplifier output remove harmonic distortion caused by nonlinear operation at RF [78]. These filters may be merged into the passive matching networks required for optimum power transfer from the amplifier to the load. As designers of RF power amplifiers have observed [10], [79], [80], much of their work consists of synthesis and iteration of the interstage, input, and output *matching networks*. It is easier to design efficient power amplifiers for constant-envelope modulations, such as analog FM or digital FSK, where distortion may be tolerated because the useful information is all contained in the zero crossings. Further, it is argued that owing to the lower parasitic capacitance of a GaAs MESFET relative to silicon devices, a GaAs power amplifier at 1W power levels affords a higher efficiency (~60%) compared to silicon bipolars or FET's (~ 45%) [47]. A monolithic power amplifier consisting of a four-stage cascade of MESFET's with on-chip lumped LCR input and inter-stage matching networks, delivers 1W at 900 MHz at 63% efficiency from a 5.5 V supply [80]. The distributed element output matching network at 900 MHz would be exhorbitantly large on an IC, and is therefore printed on an off-chip alumina substrate. The high efficiency is attributed to an improved method of suppressing the 2nd harmonic at the amplifier output. This multi-component module approach to mate IC's with matching networks is widely used in GaAs power amplifiers [81]. Another 900 MHz power module uses two discrete MESFET's, wirebonded to a hybrid IC containing a combination of distributed circuits and chip capacitors and resistors in the matching network, to attain 65% efficiency when delivering over 1.3 W from a 4.7 V supply [82]. The output FET is 12 mm wide, with a 1 μm channel length. A separate negative supply is required in many of these MESFET power amplifiers to bias the gate. The circuit was recently modified [83] to produce the same output power equally efficiently, now with a single 3.5 V supply and FET's of 0.6-μm channel length. The desired low-voltage operation, much more suitable for one battery, is the result of an improved device structure. The matching networks in the RF signal path are fabricated on separate passive-only GaAs IC's, which the authors claim are three times cheaper than GaAs IC's with FET's, while the bias networks reside on a miniature PC board. The various components are wirebonded to one another, and mounted on an AlN substrate with ten times higher thermal conductivity than alumina. Power amplifiers may also be built with silicon NMOSFET's: among the major semiconductor vendors, Hitachi has pursued this option. A MOSFET gracefully accepts large voltage swings on the gate, without possibility of Schottky conduction as in a MESFET gate. With an offset-gate FET structure and 0.8-μm channel length, a MOSFET power amp delivers 2 W

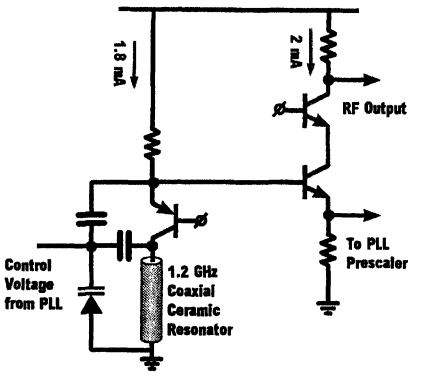


Fig. 12. Colpitts oscillator with coaxial resonator. Varactor controls frequency with control voltage. Series-connected buffer distributes RF oscillation to mixer and to PLL prescaler.

at 1.5 GHz with 55% efficiency from a single 6-V supply [84]. The power amplifier module embeds these FET's into matching networks [85].

The foregoing discussion is not meant to imply that cellular telephones mainly use GaAs MMIC's in the RF front-end. Silicon bipolar and BiCMOS technologies have made tremendous strides in improving f_T, and today silicon MMIC's offer comparable performance to what is available in GaAs. A recent 1 GHz BiCMOS LNA-mixer combination [86] uses familiar circuits to baseband designers, such as a Gilbert-multiplier type mixer, and the chip yields a comparable performance to the MMIC's described above. The RF signal path consists of bipolar circuits only, while the FET's are used as switches to select various power-down modes. There are no on-chip inductors to tune the low-noise amplifier, which is wideband; instead, the LNA output is routed off-chip into a passive bandpass filter, then returned to the chip for downconversion. This is part of a complete chipset from Philips for a digital cellular telephone handset [87].

The first LO in a cellular telephone receiver is programmed to the incoming RF channel with a phase-locked loop synthesizer, while the second LO at IF is fixed in frequency. The transmit LO oscillates in yet another frequency band. Both the receiver and the transmitter therefore require 900 MHz voltage-controlled oscillators. These are most often implemented with bipolar transistors, whose very small flicker noise means low phase-noise sidebands in the VCO. A stripline resonator sets the nominal frequency of a Colpitts oscillator, and this is voltage-controlled by a varactor diode in parallel [54], [57], [88]. Phase noise levels of -110 to -120 dBc/Hz are attained at a 50 kHz offset from the oscillation frequency. The VCO application has created a brisk demand for varactors with large voltage-coefficient and low-loss [60]. The VCO and its buffer may be connected in series to reuse the bias current between the two stages [57, [88] (Fig. 12). The nominal oscillation frequency may be slaved in a frequency multiplying PLL to a 12 or 15 MHz crystal oscillator.

The Motorola MicroTac, first introduced in 1989, set an industry standard for a miniature cellular hand set. Small

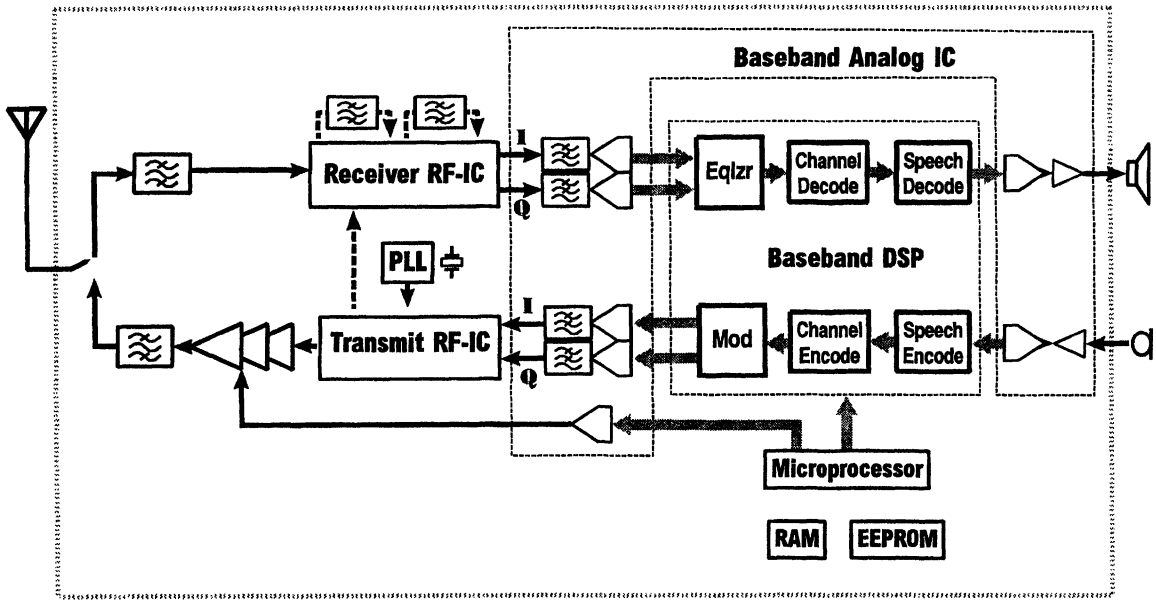


Fig. 13. Block diagram of digital cellular telephone. Chip partitions reflects current state-of-the-art technology.

handsets [89] continue to use conventional architecture, but attain a small size with discrete filters in miniature packages [52], [53], [58], [90], [91], and with lower power electronics which reduces battery weight. The electronics entail carefully designed standby modes, better software for the on-board microprocessors, and, among other items, lower power PLL-prescalers, digital counters which must operate all the time for frequency synthesis and which often posed a significant power drain [92], [93]. In the transmit mode, greater efficiency is sought in the power amplifier to prolong battery life, as well as smart control circuits to maintain maximum efficiency across the range of output power levels [89]. It was generally agreed that by 1992 the handset volume should scale down to less than 150 cc, and that its weight should be less than 230 gm [20], [94]. NTT demonstrated the prototype of such a telephone in 1991 [95], while noting that the volume should be no smaller than this target both for the sake of ergonomics, and to ensure adequate heat removal from the package so that the internal temperature rises no more than 15°C. These small telephones might be powered by a 6-V NiCd battery with 400 mA · h capacity.

With the emergence of the IS-54 standard, there is some convergence in the US on a digital cellular technology. Upward compatibility is sought with the existing analog cellular bands, which is why handsets conforming to IS-54 are referred to as dual-mode cellular. A recent 12 GHz f_T silicon bipolar transceiver IC from AT&T uses a conventional double-superheterodyne architecture with an 80 MHz first-IF, and after IF amplification the signal path bifurcates into a conventional 455 kHz second-IF FM demodulator, or a digital I-Q PSK detector [96]. An interesting alternative is to downconvert the second-IF, without preceding AGC, in a delta-sigma A/D converter for subsequent digital baseband signal processing [97].

VI. Digital Cellular and Cordless Telephones

Analog cellular telephones use the frequency spectrum inefficiently. The modulation schemes consume a large bandwidth, and every cellular telephone transmits at constant power all the time it is in use, thereby appearing as an interferer to other users at nearby frequencies. As a result, the spectrum allotted to cellular phones in large metropolitan areas nears exhaustion.

Digital cellular telephones are one solution to better utilize the scarce spectrum. They use more efficient modulation schemes, such as minimum frequency-shift keying or phase-shift keying, and multiple users may share time-slots on the same part of the spectrum. The complex modulation formats used in these telephones and the greater capabilities required to withstand nearby blocking signals are prompting large-scale integration of the RF and IF electronics. Examples of digital telephony standards are the European GSM, North American Digital Cellular, and the emerging Japanese personal handy phone (PHP) [98]. The salient charecteritics of these various systems, as well as key digital cordless standards, DECT and CT-2, are summarized in Table 1.

The typical handset involves an RF/IF front-end, followed by a baseband digital signal processor (Fig. 13). The first significant set of RF-IC's for GSM handsets appeared in 1990. Notable among them is a receiver and transmitter 7.5 GHz f_T silicon bipolar chip-set from Siemens (Fig. 14) [99], [100]. The double-superheterodyne receiver uses a selectable first-IF of anywhere from 45–90 MHz, which places the image channel in the stopband of the 25 MHz-wide RF preselect bandpass filter. A 71 MHz IF, for instance, guarantees that the image lies outside the GSM band. The desired 200 kHz channel is selected by a SAW filter at the first IF. The receiver IC provides an on-chip

Table 1

	GSM Europe	NADC North America	J-PHP Japan	CT-2 Europe, Asia	DECT Europe
Downlink Frequency Band	935–960 MHz	869–894 MHz	1.9 GHz	864–868 MHz	1.88–1.9 GHz
Uplink Frequency Band	890–915 MHz	824–849 MHz	1.9 GHz	864–868 MHz	1.88–1.9 GHz
Multiple Access Method	TDMA	TDMA	TDMA/TDD	FDMA/TDD	TDMA/TDD
Modulation	GMSK	$\pi/4$-DQPSK	$\pi/4$-QPSK	B-FSK	GMSK
Speech data rate	13 kb/s	8 kb/s	32 kb/s	32 kb/s	32 kb/s
Handset output power	3.7 mW → 1W	2.2 mW → 6 W	10 mW	1 mW → 10 mW	250 mW
Modulation rate	271 kb/s	49 kb/s	384 kb/s	72 kb/s	32 kb/s
Channel spacing	200 kHz	30 kHz	300 kHz	100 kHz	1.762 MHz
Burst length	156 b	324 b			424 b

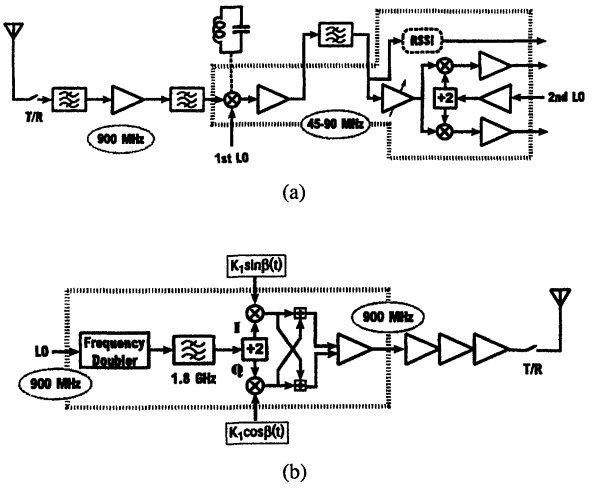


Fig. 14. Siemens receiver and transmitter IC's for GSM handsets. (a) Receiver is double-superheterodyne architecture. Requires one off-chip tuned circuit, SAW resonator at first IF, and low-noise amplifier. (b) Transmitter doubles LO frequency and then divides-by-2 to accurately obtain quadrature phases.

buffer to drive this filter. Following an RF amplifier with an off-chip LC tuned load, the input signal is downconverted by a Gilbert-cell mixer. There is AGC with 70 dB range and a signal-strength indicator at the first IF, and the selected channel is then downconverted to baseband in a quadrature demodulator to acquire both amplitude and phase for GMSK vector demodulation. The on-chip gain may be as large as 80 dB at the highest VGA setting, but as it is distributed in different frequency bands, there is little on-chip crosstalk and the monolithic receiver operates stably. The receiver uses a fully balanced signal path, and an input noise figure of 7 dB. It drains 27 mA from 5 V in active mode, and 10 μA in standby mode.

In the transmitter IC, a precision quadrature upconversion mixer produces a single-sideband, suppressed-carrier QPSK output from a baseband vector input. An RF differential input amplifier selects one sideband from the upconverted outputs in the two arms of the mixer. As the other sideband would occupy a nearby channel's spectrum, it must be adequately suppressed (relative to the level of the wanted sideband). Imperfect cancellation of the unwanted sideband arises from gain mismatch in the I and Q channels of the upconversion mixer, and in deviations from quadrature in the two LO outputs. The goal in this transmitter was quadrature phase-errors of less than 2°, which with adequate gain matching, implies unwanted sideband suppression of at least 40 dB relative to the wanted sideband. The stringent GSM requirements on low LO phase noise are only met with a 900 MHz off-chip coaxial-resonator based, varactor-tuned, Colpitts oscillator [101], which inherently provides a single-phase output. There are several methods to accurately derive quadrature phases. Siemens uses the double-frequency method. An on-chip nonlinear element doubles the oscillator frequency to 1.8 GHz, following which an on-chip bandpass filter removes harmonics. Then, the oscillation is divided by 2 by positive- and negative-edge triggered flip-flops, which will yield quadrature outputs with a phase-accuracy set by how close the duty-cycle of double frequency oscillation is to 50%. Combined with an output stage to drive an off-chip power amplifier module, the IC drains 40 mA. Using a similar superheterodyne architecture with 71 MHz IF, AT&T Microelectronics has recently combined the GSM receiver and transmitter blocks, including the frequency synthesizer, on to one chip [102].

In an effort towards even greater miniaturization at Alcatel, the transmitter and receiver sections are both integrated on to one 9 GHz f_T silicon bipolar chip (Fig. 15) [103], [104]. From the point of view of integration, the main advantage of the zero-IF, direct-conversion architecture is that it eliminates the IF passive high-frequency bandpass filters. The disadvantage, on the other hand, is that the downconverted signal has energy at dc, to which will add the receiver's offsets and low-frequency noise. An off-chip low-noise amplifier drives directly into quadrature (I-Q)mixers. The mixer dynamic range is wide enough so that a large blocking signal only 3 MHz away from the desired signal produces insignificant intermodulation distortion. The bipolar Gilbert-cell mixer is linearized with emitter degeneration resistors, which also degrade its noise figure. The receiver section requires large (650 pF) off-chip capacitors at its output for anti-alias lowpass filters, before the baseband signal is sent to a companion mixed-signal CMOS IC. This baseband CMOS IC contains a high-order switched-capacitor lowpass filter for channel selection, a digital GMSK detector, and various DSP functions [105]. An RC and CR network with off-chip trimming shifts the phase of an external local oscillator by precisely ±45° to produce the quadrature drive to the mixers. Upconversion mixers in the transmitter drive a power amplifier module.

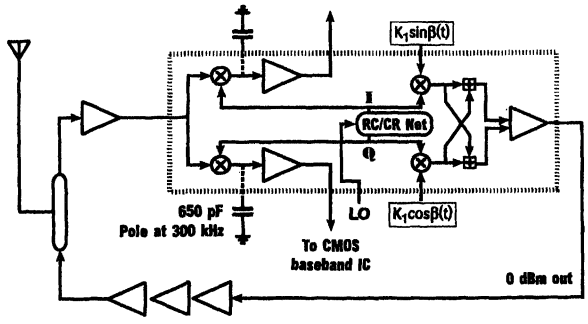


Fig. 15. Alcatel direct-conversion single-chip transceiver. Channel selection done by switched-capactior lowpass filters in companion CMOS mixed-signal baseband IC. On-chip, trimmed RC-CR network generates quadrature phases for mixers.

The chip drains 25 mA from 5 V in the receive mode, and 45 mA in the transmit mode, rather comparable figures to the previously decribed Siemens chip set. The transmitter suppresses the unwanted sideband and carrier by about 40 dB.

There is increasing interest in the 1.9 GHz band for digital cellular telephony. All the current approaches (Table 1) use time-divison duplexed (TDD) receive and transmit frames, wherein users are assigned different time slots. Two-way communications take place over the same frequency band. A host of IC's is appearing to serve the European DECT standard. The majority cater to a superheterodyne receive-architecture with 110 MHz IF [106]–[109]; some of the literature [107], [109] also describes procedures for system design. The RF sections are usually integrated at small scales, embodying, say, the low-noise amplifier and first mixer on one chip, the quadrature modulator on another, and the exciter and power amplifier on a third and fourth chip. RF-IC's operating at 1.9–2.5 GHz exist in both GaAs [68], [110]–[112] and silicon [106], [113]–[115] technologies. Some of these standalone GaAs IC low-noise amplifiers achieve impressive gain and noise figure with 1–2 mA current drain from 3 V [69], [116]. At the system level, though, functionality and overall dynamic range in these short-haul wireless links takes precedence over raw component performance. Thus system-level input noise figures of 10–15 dB are acceptable [109], as are input-referred intercept points of -16 dBm, and a 20 dB power amplifier control range [112]. The less than stringent system specifications lead to simplifications in the transmit path, such as direct VCO-modulation by the baseband signal by opening the transmit PLL over the duration of the transmit-frame [107].

The power amplifier continues to be built almost exclusively as a separate GaAs IC, and at 1.9 GHz the on-chip wavelength is short enough that it is now possible to integrate distributed matching networks [68], [117], [118]. Efficiencies of 50% are attained when delivering almost 1 W to the load from 3 V. Either the transmitter or the receiver is active in TDD digital transceivers, so fast-switching power-down modes are designed into the various components. In particular, the switching trajectory must be shaped to suppress spurious emissions when the power amplifier is switched on and off [85]. Finally, the transmit and receive signals are directed to the antenna via a three-port passive circulator, or preferably through a low-loss, monolithic transmit/receive (T/R) RF switch [112], [119], [120]. A good FET switch must not appreciably distort the RF signal, or incur more than 1-dB insertion loss when ON, yet when OFF it should offer at least 30 dB isolation. Microcell applications, such as the Japanese handy phone, require an average output power of only 10 mW (20 dBm), although the $\pi/4$-QPSK modulation requires the power amplifier to handle larger peak powers. An exciter amplifier, power amplifier, and T/R switch have been integrated together [121]. The exciter and power amplifier attain a 44% efficiency at 23 dBm output from a 4.8-V supply, and the on-chip matching network uses LC lumped elements. Although matching networks will eliminate harmonic distortion, they are ineffective in suppressing near-carrier spurii produced by intermodulation distortion. Feedback linearization techniques have been proposed which predistort the digitally synthesized exciter input waveform to anticipate the power-amplifier nonlinearities [122]. Use of these techniques makes a highly nonlinear but efficient power amplifier appear linear. These remain at the experimental stage today, and with the move to microcells and low emitted power levels, they may soon not be necessary in handsets.

The building-block IC's described so far are important advances in realizing small, relatively low-power transceivers, but the ultimate goal remains to integrate the entire transceiver on to a single-chip. To this end, some early breadboard-level experiments show that direct-conversion receiver architectures seem well suited to the DECT application [123], [124]. A 16 GHz f_T silicon bipolar IC from Alcatel operating at 1.9 GHz contains a complete direct-conversion DECT transceiver [125]. The architecture resembles the previously described Alcatel direct-conversion GSM transceiver [103], requiring a separate low-noise amplifier in the receive path, a power amplifier module, and a baseband CMOS mixed-signal signal processor IC. From a 5-V supply, the transceiver drains 50 mA in receive mode and 80 mA in transmit mode. One of the challenges in realizing this system was a fast-switching PLL frequency synthesizer with low phase-noise and low spurious output levels, which was built here with an improved charge-pump and loop filter.

Siemens has extended its dual-conversion GSM transmitter/receiver chip set [99], [126] to a generalized front-end for digital cellular telephones operating in any part of the RF spectrum from 800 MHz to 2.1 GHz [127]. The 25 GHz f_T silicon bipolar chip set ope rates at a supply as low as 2.7-V, the transmitter chip draining 60 mA and the receiver 33 mA. Both have power-down modes. An external power amplifier module is required. A notable low-voltage circuit on this chip is a modified Gilbert-cell mixer, with resistors instead of current sources to the negative supply [31]. To accommodate a wide input dynamic range, the gain of the RF low-noise amplifier in the receiver may be switched from -5 dBm to $+15$ dBm, a powerful technique

that has also been used in paging receivers [46]. This assumes that the recever does not instantaneously require a very wide dynamic range, but either receives mostly strong signals or mostly weak ones. The downconversion mixer, with a 13 dB noise figure and −3 dBm input IP3, is followed by an IF variable-gain amplifier with an 80 dB digitally programmable range [126]. The on-chip RF oscillator requires an off-chip resonator and varactor, and its phase noise at a 2 kHz offset is −88 dBc/Hz. A balanced signal path is used throughout. One good measure of the quality of on-chip gain matching in the I and Q paths in the direct upconverter, as well as of the quadrature accuracy of the upconversion clocks, is given by the relative levels of spurious emissions from the transmitter IC. The unwanted sideband is suppressed by 48 dB, while the RF carrier tone, emitted due to dc offsets in the two paths, is 37 dB down. A 3rd-order modulation tone at −46 dB appears due to mixer nonlinearity. The absolute output noise level at a 25 MHz offset is −141 dBm/Hz.

VII. Direct-Conversion Transceivers and Their Problems

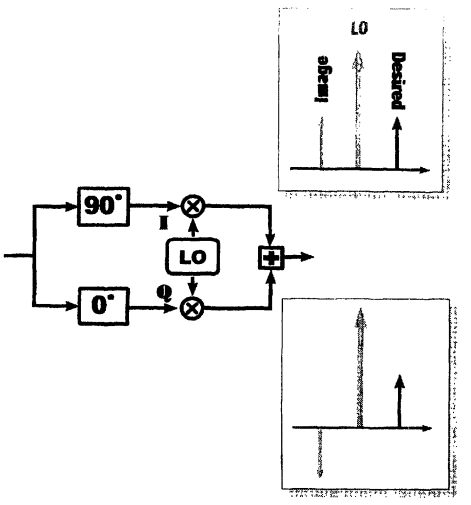
A receiver with zero-IF is called a *direct-conversion* receiver. When the local oscillator is synchronized in phase with the incoming carrier frequency, this is also referred to as the *homodyne*. This architecture is sufficiently promising for single-chip transceivers to warrant a separate section to its study.

The desired channel is translated by the first mixer to a 0 Hz center frequency, and instead of adjacent channel rejection with a bandpass resonator, a more flexible and easier to implement lowpass filter is required—in effect, a bandpass filter centered at dc when the negative frequency axis is included. With zero-IF, there is *no* image frequency. As early as 1924, radio pioneers had considered homodyne architectures for crude receivers requiring only a single vacuum-tube, but it was in 1947 that a homodyne was first used to full effect, with a high-order lowpass filter for channel-selection, in a measuring instrument for carrier-based telephony [32].

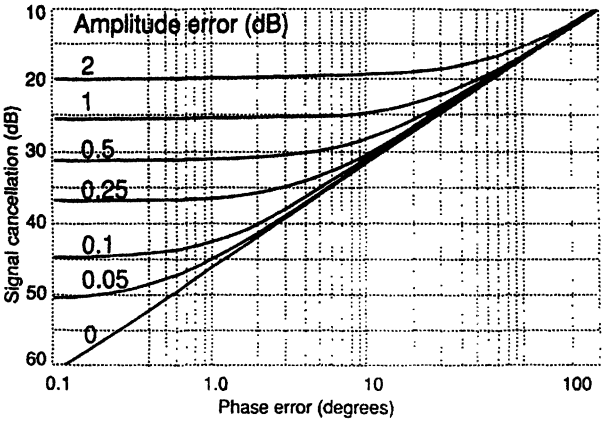
A. Direct-Conversion Single-Sideband Synthesizers

For reasons of spectral efficiency, the transmitted signal in digital communications is always single-sideband with suppressed carrier. This is most often produced with the so-called *phasing method* [128]. The modulated signal is first synthesized in quadrature at baseband, *directly upconverted* into two paths by a quadrature LO centered at the carrier frequency, and added or subtracted to select either the upper or lower sideband (Fig. 16(a)).

The unwanted side band is suppressed to an extent limited by the gain mismatch in the two upconversion paths, and by departures from quadrature in the two LO outputs (Fig. 16(b)). Unequal dc offsets in the paths produce an output signal at the LO frequency. The unwanted sideband and LO leakage are spurious but unavoidable components of the transmitted spectrum. Although on the same IC the



(a)



(b)

Fig. 16. (a) Single-sideband direct upconverter using the phasing method (also called the quadrature modulator). Extent of suppression of unwanted (image) sideband versus gain mismatch and phase-errors from quadrature in two arms of modulator.

two upconversion paths are well matched, a gain mismatch as small as 1% (0.1 dB) will limit suppression of the unwanted sideband to 45 dB. With this gain mismatch, a phase-error of up to 1° may be tolerated between the two LO outputs. These mismatches may be trimmed down at time of transceiver manufacture, or self-calibrated with loopback modes which are activated during idle times to sense and suppress the unwanted spurii.

An off-chip resonator, often connected to an on-chip unbalanced oscillator circuit, may also become a cause of spurious RF leakage if it couples energy into the power amplifier or the antenna. Frequency-offset upconversion schemes have been proposed [129] to combat this coupling problem. Other spurious output tones may arise from parasitic remixing of the modulated output with the baseband signal, and by intermodulation distortion in the output stage [96]. Balanced circuit topologies, on-chip LO's requiring no external resonators [130], and lowered transmit power levels in microcells, are all expected to lessen the magnitude of the spurious leakage problem.

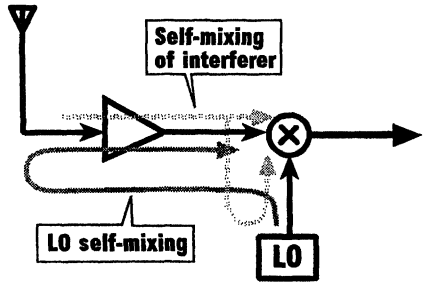


Fig. 17. Sources of leakage in a direct-conversion receiver, and how through self-mixing they create dc offsets.

Cellular wireless systems operate best with tightly regulated power control, the handsets transmitting only the minimum power required for reliable reception by the base station, and *vice-versa*. Whereas in the receiver the front-end is the main source of noise, in a transmitter the upconversion LO phase-noise appears as added noise on the emitted signal. Direct upconversion has the advantage over two-step schemes that only *one* LO contributes noise.

B. Direct-Conversion Receivers for GSM Digital Cellular Telephones

Among the various RF-IC suppliers for the European GSM digital cellular telephone handset, only Alcatel at present uses a direct-conversion receiver architecture [103], [125], [131]. This results in a relatively small silicon bipolar RF front-end chip, and the remainder of the signal processing, including lowpass channel-select filtering, is at baseband in mixed-mode CMOS. Why are the others reluctant to use direct-conversion in their receivers? Given the many decades of superheterodyne experience, the most likely reason is conservatism. But direct-conversion also suffers from some unique problems.

A well known problem is that spurious LO leakage from the receiver into the antenna becomes an in-band interferer to other nearby receivers tuned to the same band. Superheterodynes, with their frequency-offset LOs, do not suffer from this problem. However, experimental studies suggest that with standard shielding in the receiver, this problem is not so severe as to handicap the use of direct-conversion [132].

A more serious problem is dc *offset* in the receiver. Offset arises from three sources [131]: transistor mismatch in the signal path; the LO signal leaking to the antenna because of poor reverse isolation through the mixer and RF amplifier, then reflecting off the antenna and self-downconverting to dc through the mixer (Fig. 17); and a large near-channel interferer leaking into the LO port of the mixer, then self-downconverting to dc. Good circuit design may reduce these effects to a certain extent, but they cannot be eliminated.

The spectrum of the GMSK modulation used in GSM has a peak at dc. Offsets will directly add to the spectral peak of the downconverted signal. These offsets are usually much larger than the rms front-end noise, and may therefore significantly degrade the SNR at the detector. To remove the offsets by ac-coupling the receiver will require impractically large capacitors, if the signal-bearing spectrum around dc is not to be sacrificed. However, they may be compensated with DSP-based self-calibration [105], [133]. The baseband signal processor makes long-term measurements on the dc level in the receiver, and subtracts off this level from the downconverted signal. The spectrum loss around dc is only a few hertz, and digital filtering does not distort the midchannel group delay in the receiver.

C. Local Oscillators with Quadrature Outputs

A *carrier-frequency* local oscillator with quadrature outputs is a key circuit component in direct-conversion transmitters and receivers. Usually this oscillator is tuned by an LC circuit or an off-chip resonator, and inherently produces a single-phase output. Quadrature phases are often derived by passing the oscillator output through a CR and an RC network, whose time constant is equal to the oscillation period. The two resultant outputs are then phase-shifted by $+45°$ and $-45°$, respectively. Inaccuracies in the actual values of R and C will lead to errors in quadrature, and are compensated by some form of on-chip trimming [103], [125].

An alternative method is to divide an oscillation at twice the carrier frequency with positive- and negative-edge triggered flip-flops [99]. The resulting two outputs at the desired frequency are in quadrature. Residual phase errors caused by unequal delays in the two flip-flops, and by departures from 50% duty cycle in the double-frequency oscillation, are found to be less than 1°. However, the double-frequency portions of the circuit may become a speed bottleneck.

Quadrature outputs may also be derived from a polyphase oscillator, such as a variable-frequency ring oscillator. In a four-delay stage ring oscillator, taps at diametrically opposite points will yield quadrature phases at all frequencies [134] (Fig. 18). In oscillators with an odd-number of unit delays, they may be synthesized from two taps by a voltage-controlled phase-shifter in feedback around a quadrature-sensing circuit [135]. Mismatches in transistor characteristics limit the attainable phase accuracy. This type of resonator-less oscillator is practical when the specifications on phase-noise are not too stringent (say up to -80 dBc/Hz at a 100 kHz offset from the carrier). The free-running oscillator must be slaved to a crystal reference in a frequency-locked loop, whose loop gain and bandwidth are specifically designed to suppress phase noise.

When circuit techniques cannot contribute further improvements to gain- and phase-matching in the two arms of a quadrature modulator or demodulator, digital adaptive algorithms may be used at baseband to sense and compensate for these errors [136].

VIII. IC's for Spread-Spectrum Wireless Transceivers

Spread-spectrum communications offer greater user capacity than narrowband techniques in a given piece of

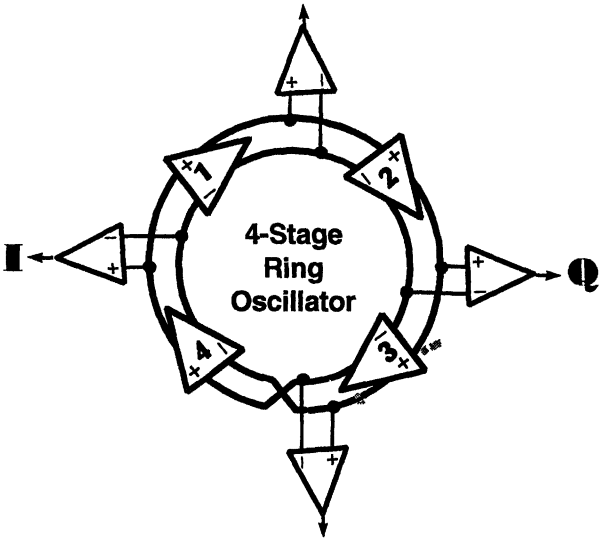


Fig. 18. A four-phase voltage-controlled ring oscillator. Diametrically opposite taps give quadrature phase at any frequency. Unequal loadings and device mismatch set phase errors. VCO must be embedded in PLL whose closed-loop bandwidth is tailored to suppress oscillator noise.

wireless spectrum. Much has been written on this subject [137]. Spread-spectrum techniques were developed during World War II as a form of secure communication with low probability-of-intercept and resilience to jamming [138]. Over the years, this technology has been further developed and refined for military communications. With the wireless revolution at hand and the IC technology now available to implement complex transceivers, spread-spectrum has awakened commercial interest [139]. Spread-spectrum communications make it easy for users to access the wireless channel. Whereas conventional narrowband wireless communications require a careful discipline, which the FCC or other government agencies enforce by issuing licenses so as to prevent use of the same frequency by nearby operators, for spread-spectrum use the FCC has allocated certain *unlicensed* bands in the US, referred to as the Instrumentation, Scientific, and Medical (ISM) bands, wherein the user is only required to spread spectrum by a minimum amount, and not to exceed an upper limit on transmitted power. The extent of spectrum spreading may be measured by the amount of *processing gain* in the receiver required to de-spread and detect the signal [140].

As analog cellular telephones begin to saturate the available radio frequency allocations, spread-spectrum techniques are being deployed in cordless telephones and wireless modems [141]. These devices usually operate in the two lower ISM bands: 902–928 MHz and 2.4–2.48 GHz. A ubiquitous wireless environment is envisioned, in which mobile users, wherever they may be, can access data and communications services through an intricate network of base stations [2]. The greatest hardware challenge in realizing this scenario is the development of a low-power, miniature handset.

There are two different methods to spread the spectrum of a signal: by *direct-sequence* modulation, or by *frequency*

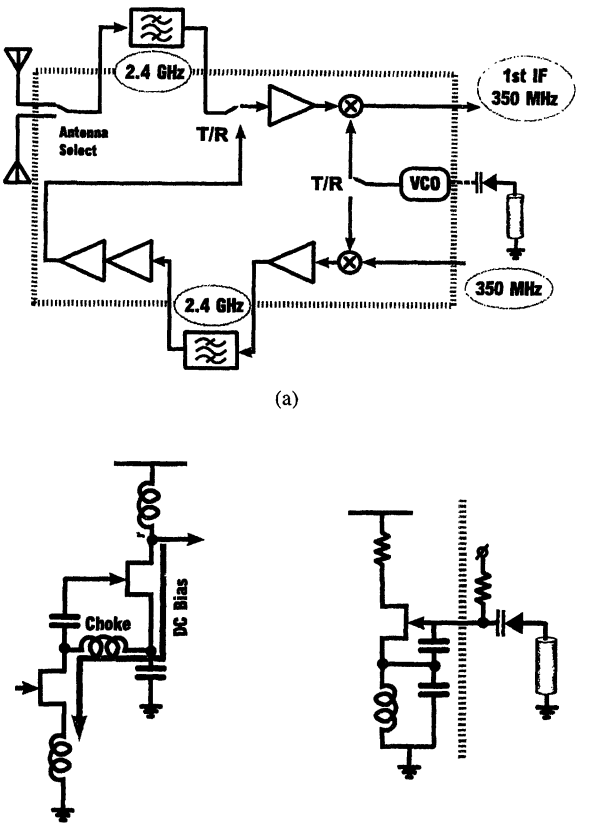


Fig. 19. Front-end GaAs MMIC transceiver for spread spectrum communications in 2.4 GHz band. Receiver is double-superhetorodyne. Note use of off-chip filters. (b) Low noise amplifier in transceiver IC (left) reuses bias current in two stages. Clapp voltage-controlled local oscillator (right) combines on-chip LC network with off-chip resonator and varactor.

hopping [140]. Direct sequence is conceptually the simpler, as well as the more straightforward to implement. Each data bit (either $+1$ or -1) at the transmitter multiplies a prescribed sequence of bits, or *chips* as they are called. The chip sequence is selected for very low autocorrelation, and is often referred to as a pseudo-noise, or PN, sequence. Each user is either assigned a unique PN sequence with very low cross correlation with other user sequences, or a time-shifted version of some long PN sequence. The receiver, after an initial acquisition search to align itself with the start of the PN sequence, correlates the incoming sequence with the pattern it knows to be its own. On detection of a correlation peak, the sign of the peak signals the source data bit. The longer the PN sequence for each bit, the greater the spreading factor, and the more reliable the detection. Here, the processing gain is the sequence length per bit. The spectrum of the transmitted data, composed from a concatenation of PN sequences, is noise-like; thus the term *spread-spectrum*. Several baseband and IF modem IC's have already appeared to support BPSK and QPSK direct-sequence spread-spectrum transceivers [142]–[144].

Whereas direct-sequence modulation spreads the spectrum by randomizing the waveform, frequency-hopping spreads spectrum by *hopping* the carrier according to a

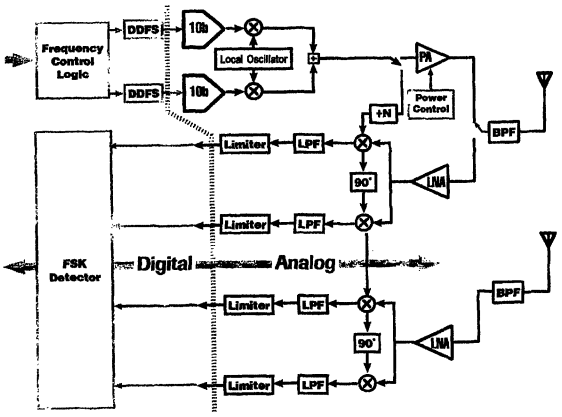


Fig. 20. The UCLA frequency-hopped spread-spectrum transceiver. This uses direct-conversion in both transmit and receive path, and binary-FSK modulation. In the transmitter, the spread-spectrum waveform i synthesized at baseband, and upconverted to RF. During receive mode, the DDFS under control of a synchronization loop hops with the incoming data, and demodulates it to baseband. The entire mixed analog-digital, baseband/RF system is to be integrated on a 1-μm CMOS IC.

prescribed sequence across the entire band. The effect in the frequency-domain is similar to direct-sequence, except for one fundamental difference: with direct-sequence, spreading across a wide bandwidth requires each data bit to be mapped into a long PN sequence. The resultant high "chip-rate" requires high-speed signal processing at the receiver front end. On the other hand, if the carrier frequency is hopped with a wideband synthesizer, the output spectrum may span an arbitrarily wide frequency range, even at low bit rates. Therefore, if a fast and agile frequency synthesizer is readily available, the receiver front-end operates at the actual data rate in frequency-hopped spread-spectrum, rather than at the considerably higher chip-rate in a direct-sequence receiver. The former will very likely lead to a low-power solution.

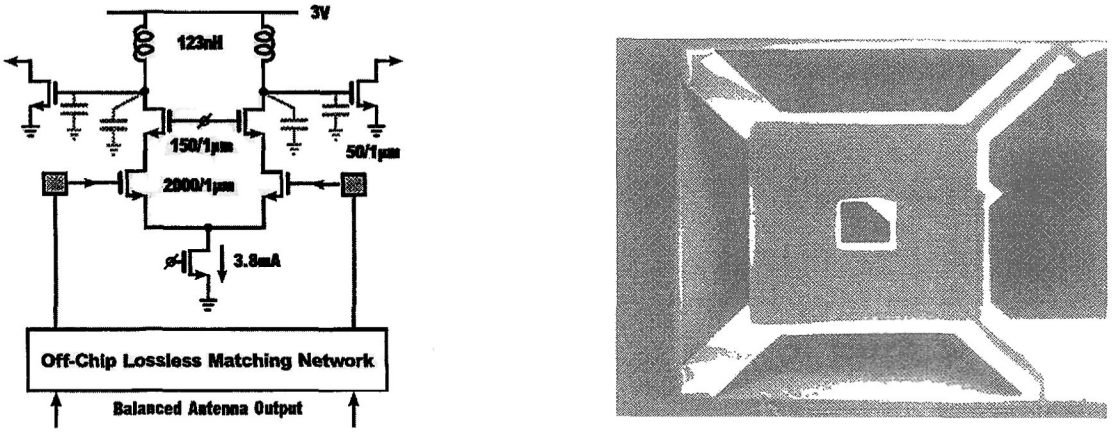
As a notable recent example of a miniature spread-spectrum transceiver, Plessey has introduced a 700 kb/s frequency-hopped device operating in the 2.4 GHz ISM band. The transceiver is entirely contained on a $2'' \times 3''$ PCMCIA card for insertion into notebook computers [109], [145]. FSK data modulates the carrier frequency, and a variable-modulus PLL synthesizer slowly hops the carrier to spread the spectrum across the 80 MHz band. All the active devices in the transceiver are on three IC's, consisting of a GaAs RF front-end, a silicon bipolar IF receiver, and a CMOS IC for the hopping-frequency synthesis. As in any spread-spectrum two-way communication system, transmission and reception is time-division-duplexed on the same frequency band. The receiver architecture is a conventional double-superheterodyne. In addition, the transceiver requires 50 passive components, including six rather bulky filters, and when transmitting 100 mW RF power it dissipates more than 1 W.

By the norms of GaAs MMIC's, the single-chip IC front-end in this transceiver is highly integrated (Fig. 19(a)) [146]. It includes the power amplifier, and drivers for 2-GHz passive filters in the transmit and receive paths. Interesting features are the dc series connection of the single-ended two-stage low-noise amplifier, which shares the same bias current in both stages through a bypass inductor; the Clapp VCO; and the four-FET switched mixers in the transmit and receive paths (Fig. 19(b)). In its first version, the IC includes more than 20 on-chip spiral inductors, perhaps the largest number on any MMIC at the time of this design. A second bipolar IC processes the 350 MHz IF signal. In receive mode, the GaAs front-end IC drains 30 mA from a 5 V supply. The receiver selects one of two external antennas through an on-chip RF switch to attain spatial diversity. This work has spurred a flurry of similar GaAs IC's at the same level of integration [147]–[149], all operating at ± 5 V supplies, with similar functionality and performance. One of them [149] uses a very high IF of 915 MHz, so that spurious products at the transmitter output lie well in the stopbands of the output filter, and where the IF signal is processed by a 915 MHz cellular-telephone type IC.

IX. IC's to Enable Future Transceivers

What will portable wireless communicators of the future look like? We may draw some conclusions from the foregoing summary of RF-IC developments. The crowded spectrum means that future wireless communicators will predominantly use spread-spectrum techniques. Coupled to this is a need for low-power dissipation, which will force *architectural innovations* and *higher levels of integration* in the electronics. As an example of such an advanced transceiver, the author with his colleagues and their graduate students at UCLA is investigating the architecture and circuit design of a frequency-hopped, binary frequency-shift keyed, zero-IF, all-CMOS two-chip transceiver capable of delivering up to 160 kb/s (the base ISDN rate) in the 900 MHz ISM band [39], [150]. The transceiver architecture is inspired by the modern paging receiver, a very low energy wireless device widely used today. The transceiver implementation (Fig. 20) will freely mix analog and digital circuits, which makes CMOS the IC technology of choice. Further, to avoid the routing of high-frequency signals off- and on-chip and thereby save the power the buffers would use to drive stray capacitance and off-chip low-impedance lines, it is preferred to integrate all the blocks, *including* the RF front-end. Finally, it is most desirable to use an unmodified, standard production CMOS process.

Low-power operation requires the entire system to operate on a 3 V supply. This supply voltage cannot be any lower because in many places the analog circuits contain stacked cascode transistors, and the FET threshold voltages are about 0.8 V. RF amplifiers are normally tuned with inductor loads, which on silicon IC's are almost always off-chip passive components [151]. However, this is itself wasteful of power, because in addition to the current supplied into the inductor, the circuit must also drive the various parasitic capacitances in off-chip routing the RF signal.



(a) (b)

Fig. 21. (a) Balanced input CMOS RF amplifier. Cascode stage driving on-chip inductor substantially enhances voltage gain. Outputs common-source stages are for measurement only. LNA will directly drive mixer. (b) A microphotograph of a 110 nH spiral inductor suspended over a pit on substrate.

Spiral inductors on silicon substrates suffer from a large capacitance to the conducting silicon substrate. However, after many years of the belief that no useful inductors could be made on silicon, it was found that spiral inductors as large as 10 nH with self-resonance beyond 2 GHz, could be fabricated with the standard interconnect metallization. These inductors were used to build passive filters, a tuned amplifier, and an LC voltage-controlled oscillator on a silicon bipolar IC [152]–[154]. This work has rekindled interest in the design and modelling of small value spiral inductors on silicon (usually bipolar) IC's, with values in the range of 1–10 nH [155], [156]. In some instances, higher inductor Q's are obtained with thicker metallization, or higher resonant frequencies with thicker oxides. In search of larger value inductors for low-power, high-gain amplifiers, we have developed a fabrication method whereby the silicon substrate is selectively removed under the inductor, substantially reducing the capacitance to the substrate, and thus extending self-resonance to a higher frequency (Fig. 21(b)) [157]. The self-resonant frequency is now almost as high as it is on a semi-insulating GaAs substrate. Using two such inductors as loads in a balanced circuit, a 900 MHz RF amplifier has been built in 1-μm CMOS with a 30 dB gain draining only 3 mA (Fig. 21(a)). The amplifier IP3 is about 0 dBm, owing to the wide linear range of the MOS differential pair.

The front-end mixer in a direct-conversion receiver must be highly linear to suppress unwanted intermodulation produced by interferers. Also, as the local oscillator frequency is centered at RF in this direct-conversion receiver, inadequate reverse isolation or shielding may cause this frequency to leak through the antenna and to interfere with other nearby receivers tuned to the same RF. We use an unusual mixer—one that happens to be particularly well suited to MOS implementation—to circumvent both these problems. The desired signal is downconverted to baseband by sub-sampling the incoming RF [158]. The mixer circuit is a track-and-hold, with such a wide track-mode bandwidth that it can follow the RF waveform, and a short enough aperture to acquire the *instantaneous* value of the RF waveform on receipt of the sampling clock edge (Fig. 22). The received RF in our system is a 26 MHz wide spread-spectrum centered on a 915 MHz carrier, so by sub-sampling this waveform at a clock rate of 52 MHz or higher, the spectrum is translated to baseband without aliasing. However, the mixer also acquires wideband noise accompanying the signal from dc up to the gigahertz track bandwidth, and aliases the rms noise into a bandwidth at half the sample-rate, thereby raising the baseband noise spectral density by the ratio of the track-bandwidth to the sample-rate. Sub-sampling mixers therefore have a higher noise figure than conventional mixers. However, as such a mixer tends to be more linear than an analog multiplier, its dynamic range is also large, provided a high-gain, low-noise RF amplifier precedes it. The overall front-end spurious-free dynamic range is jointly set by the individual specifications of the RF amplifier and mixer. In this 1 μm CMOS prototype, the mixer circuit draws 4 mA from 3-V to acquire samples of a 900 MHz modulated waveform at a 50 MHz rate, which it then translates to baseband. The linearity, as measured by a +26 dBm third-order intercept, exceeds that of most continuous-time 900 MHz monolithic mixers, and for the fundamental reasons given above, the noise figure is 18 dB.

A low-power, agile frequency synthesizer with high spectral purity is required in a frequency-hopped transceiver. Conventional synthesizers based on a phase-locked loop with a variable-modulus divider in feedback suffer from limited agility, because the loop bandwidth may limit the speed of frequency switching. It is also difficult to design a VCO which both covers a wide range of frequency spreading, and produces a pure spectrum. The DDFS-DAC combination is an alternative solution to this problem, which so far has only been used by the military in spread-spectrum communication systems. A direct-digital frequency synthesizer (DDFS) [159] consists of an accumu-

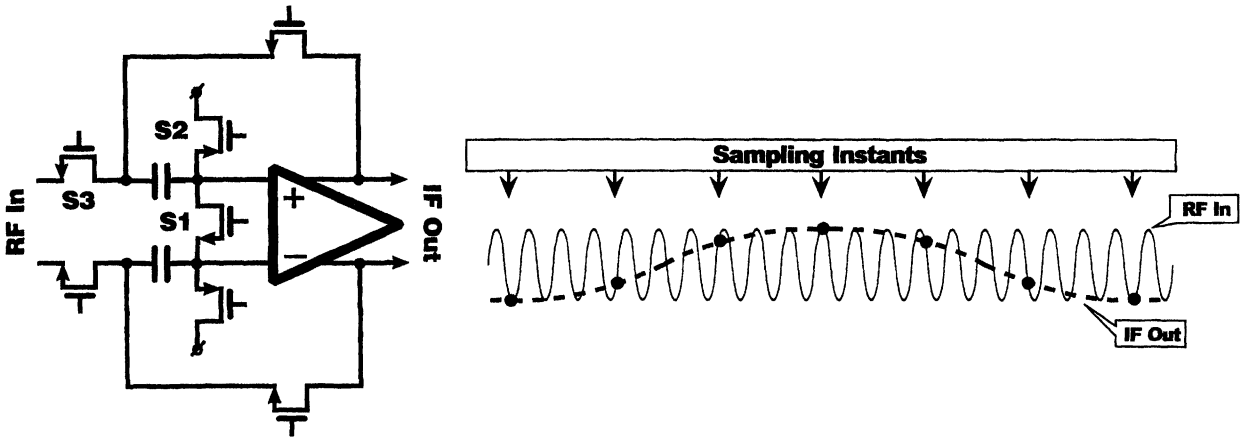


Fig. 22. A downconversion mixer based on direct sampling of RF. During track mode, switches are closed, and bandwidth of passive circuit is about 1 GHz. On receipt of sample clock, switches open within very short aperture time, capuring instantaneous value of RF waveform. Op amp removes switch charge injection, and buffers to subsequent circuits.

lator and ROM, which produces a sequence of digital words representing samples of a sinewave at a frequency set by an input control word. A D/A Converter converts the digital samples into a discrete-time analog sinewave, and a subsequent analog filter may smooth this into a continuous-time sinewave. Roundoff errors in the DDFS and nonlinearity in the DAC and filter will limit the attainable spectral purity of the synthesized sinewave [159]. In practice, DAC imperfections may contribute the largest nonlinearity in the system. A characteristic feature of digitally synthesized sinewaves is that the major imperfections do not necessarily produce harmonic tones, but instead spurious tones at rational multiples of the fundamental. These spurious tones often cluster around the fundamental and cannot be filtered. The DAC can add spurious tones of its own. We use a highly efficient DDFS combined with a high-speed, low-power charge-redistribution DAC to produce an FSK-modulated, frequency-hopped spread-spectrum at baseband, which a fixed-frequency local oscillator upconverts to RF. A CMOS implementation of a DDFS-DAC at 3 V dissipates only 40 mW when clocked at 50 MHz (of which the quadrature ROM-accumulator accounts for 35 mW), with worst-case spurious levels of -57 dBc or less across the entire spreading range (Fig. 23) [160].

The 915 MHz local oscillator is a four-stage MOS ring oscillator locked in a PLL to a lower frequency crystal reference. The quadrature outputs at 915 MHz for the image-reject mixers are tapped at diametrically opposite points [130], [134] to a phase accuracy of better than 1°. As the local-oscillator operates at a fixed frequency, it is locked to a low-frequency crystal reference in a PLL solely optimized to reduce phase noise. At a 100 kHz offset, a phase noise level of -75 dBc/Hz is measured on a prototype.

The power amplifier is a binary-weighted array of FET's biased near threshold, which is digitally selected to deliver power levels from -15 dBm to $+15$ dBm through a matching network to the antenna with a 40% conversion efficiency (Fig. 24) [161].

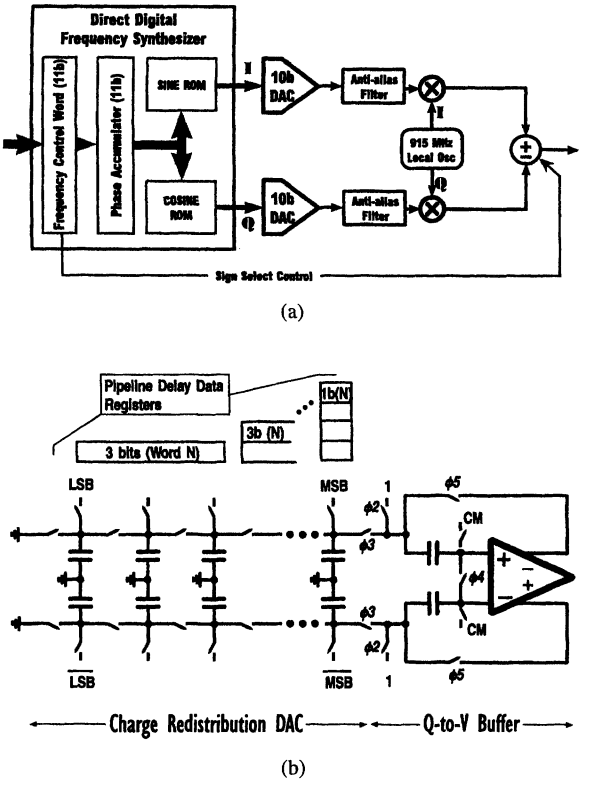


Fig. 23. (a) An agile frequency synthesizer. The DDFS produces digital samples of a sine and cosine, at a frequency set by an input word. DAC's convert these to analog domain, and after quadrature upconversion, either the upper or lower sideband is selected. Thus 0–13 MHz at baseband frequency produces output spanning 902–928 MHz. First-order anti-alias filter suffices if DDFS/DAC operates at 80 MHz. (b) DAC uses passive, pipelined architecture.

The transceiver achieves spatial diversity with two individual receive channels, which are powered-up continuously and connected to two different types of miniature antennas. Data decisions are made on an equally weighted sum of their baseband outputs. A high-order switched-capacitor elliptic lowpass filter selects the desired channel, which the on-board DDFS-based synthesizer has dehopped

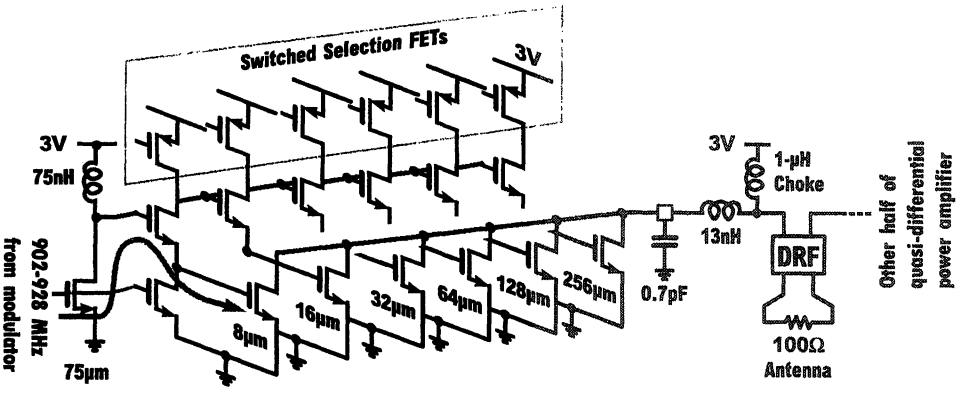


Fig. 24. A digitally controlled power amplifier. The binary-weighted array of output NMOSFET's drive the antenna load differentially, to deliver up to +15 dBm from a 3-V supply. Large on-chip inductor used as exciter load gives swings above power supply. PMOSFET's selectively activate source follower buffers, and thus total delivered power.

to dc in the course of downconversion. The capacitively coupled output is then amplitude-limited to produce a one-bit stream fed to an optimal FSK digital detector [39]. The detector quantizes the zero-crossings in time by oversampling the limited baseband data, and seeks correlations between one-bit representations of the two possible data values. A logarithmic amplifier connected to taps on the limiting amplifier chain measures the received signal-strength [162]. Operating from a 3-V supply, the 1-μm CMOS transceiver is expected to drain 70 mA in receive mode, and 100 mA in transmit mode (the power amplifier is on-chip). Considering that the transceiver communicates on a 26 MHz-wide spectrum, this is indeed a low power dissipation.

This research project is now exploring issues related to the single-chip integration of this transceiver. Such a highly integrated CMOS "VLSI radio" would represent a major step forward in the evolution of the radio integrated circuits described in this paper.

X. Conclusions

This survey has covered some of the key existing and emerging communication applications which have prompted advances in RF IC's. The emphasis was on widespread *portable consumer* applications. This has excluded coverage of integrated television tuners, for instance, which were historically the principal motivation for the development of UHF RF-IC's by the consumer electronics industry in the mid-1970's [163]. The fact that about 18 million tuners are produced every year means that there has been a steady stream of innovations in the building-block and architectures for this application [164]–[178]. Then there are emerging areas, such as personal GPS receivers, where RF integration and low-power will be the key for acceptance by consumers [179], [180]. Here, too, RF-IC designers are responding with integrated front ends [181]–[184], although the greater challenges to realize a system with an acceptable precision may lie in the baseband signal processing.

The lucrative global wireless market is attracting a great deal of attention from circuit designers across the industry. The RF range of interest spans 400 MHz to 2.5 GHz. There is a multi-pronged industry-wide assault to provide the right solutions. The solution must be low-cost, low-power, and it must give high functionality. MMIC designers bring to RF-IC's a microwave style derived from small-scale circuits which operated at much higher frequencies. On the other hand, as the frequency range lies within the capability of modern silicon IC technologies, there is a response from this community. Bipolar and BiCMOS RF-IC's are often extensions of baseband style circuits to high-frequency, often with more functionality than GaAs MMICs offer. A low transistor f_T is no longer a handicap, and experience rapidly accumulates on how to solve some of the unique problems of silicon substrates, such as high-frequency losses in the substrate [185] and on-chip coupling problems between circuit blocks. In the not too distant future, as microprocessors and memories drive the linewidths of silicon IC processes to deep submicron, RF-IC's might be designed as untuned wideband circuits, in the style of IC's for video applications today.

Small-scale GaAs MMIC's might sometimes perform better as standalone components, but embedded in a system such as a digital cellular telephone or a spread-spectrum transceiver, they require a large overhead in support circuits, and thereby lose an edge in certain specifications, such as power dissipation. Silicon RF-IC's offer higher levels of integration, but even within the silicon IC design community there are differing points of view. While integrated silicon bipolar transceivers are to be found in the next generation of products, CMOS RF solutions, albeit at an exploratory stage, now look very promising. They combine elements from well established techniques in voiceband and video IC's, and are unfettered in partitioning tasks between analog and digital signal processing, while using off-chip passive components when necessary. Digital control components and baseband signal processors are readily integrated with, indeed merged into, the RF and IF

sections. This array of competing technologies offers communication system designers more creative opportunity, and the best wireless transceiver solutions may well emerge from system design evolving together with architecture, circuits, antennas, and power-allocation plans.

What are the prospects for this multitude of approaches to low-power wireless communications? If we project on the experience gained from baseband and video telecommunications circuits, the future wireless transceiver may be only one BiCMOS or CMOS large-scale, mixed analog-digital IC, requiring one passive filter and a crystal resonator. Baseband digital signal processing may make up for imperfections in the front-end RF sections. As it will likely be used in a microcell environment at low transmit power levels, the transceiver may be encapsulated in a plastic package. There is no fundamental reason why it should need more than a single 1.5 V battery as the power source. After decades of thinking of it only as science-fiction, the electronics world is prodded forth by the communications explosion into making the two-way wristwatch-size radio a reality. A large community researchers, not trained in the classical radio art, is busy reexamining the conventions, and at time challenging the received wisdom. We are poised at a turning point in the evolution of radio-circuit engineering.

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The recent financial stringencies at UC have not so far eroded the marvellously rich Engineering Collection and online facilities at the UCLA Science and Engineering Library. It would be impossible to write this paper without ready access to these resources. Karen Andrews and Aggi Raeder, two of the expert librarians there, enthusiastically helped me in using the latest tools to peruse the literature, and amazed me with the ease with which they could track down obscure references from all corners of the world.

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Future Directions in Silicon ICs for RF Personal Communications

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Abstract

This paper presents an overview of technical challenges in achieving higher integration levels, lower power dissipation, smaller form factor, and lower cost in portable battery-powered RF transceivers for personal communications applications. Specific emphasis is placed on silicon integrated circuits for transceivers in the 800MHz-2.5GHz range of frequencies.

Introduction

Digital radio personal communications devices utilizing the bands between 800MHz and 2.5GHz will play an increasingly important role in the overall communications infrastructure in the next decade. In addition, the bands above 2.5GHz, where large, relatively untapped blocks of spectrum are available, will receive increasing use as transceiver costs in this frequency range are brought down. Compared to other types of integrated circuits, the level of integration in the RF sections of such transceivers is still relatively low. Considerations of power dissipation, form factor, and cost dictate that the RF/IF portions of these devices evolve to higher levels of integration than is true at present.

In this paper, we attempt to identify some of the key barriers to realizing these higher levels of integration, and discuss several of the avenues currently being pursued for achieving that objective for portable personal digital RF communications devices such as cellular telephones, cordless telephones, wireless PBXs and wireless LANs utilizing the bands of frequencies between 800MHz and 2.5GHz. The emergence of established standards and the rapid growth of deployment make these very attractive potential applications for high-integration dedicated integrated circuits. Other important applications include the services to be offered by a whole spectrum of providers using both unlicensed bands as well as the licensed part of the new PCS band now being allocated around 1.8 GHz. A good overview of these applications is given in [1].

Typical Present RF Transceiver Implementation

The vast majority of currently-manufactured transceivers for the applications mentioned above utilize single- or dual-conversion configuration for the receive path. Baseband channel bandwidths range from 10kHz to 1-2MHz. Good examples of systems at the current state of the art are surveyed or described partially in [2][3][4][5][6]. A typical example of such a transceiver as might be used in a frequency-hopped wireless LAN application is shown in block diagram form in Fig. 1.

The conventional architecture in Fig. 1 is not particularly amenable to higher levels of integration. Image rejection considerations usually dictate that the first intermediate frequency (IF) be on the order of 10% of the carrier frequency, with for example at least 70 MHz in 900 MHz receivers, and higher in higher frequency receivers. The use of complex signal representation at IF, as in image reject mixers, can improve image rejection by a considerable margin[47] and simplify the passive RF image reject filter, but the difficulty of phase and amplitude matching at IF usually limits the image rejection in such mixers to values on the order of 20dB, and as a result the IF must still be kept fairly high to preserve image rejection without requiring expensive and lossy ceramic RF filters. In many applications, two ceramic RF filters are required for adequate image rejection, one preceding and one following the low-noise amplifier (LNA). Depending on the modulation scheme used, the range of frequencies over which the receiver must be tuned, and the amplitude of the near-carrier interfering signals, a second frequency conversion may be performed, translating the signal down to a second IF on the order of 10-20% of the first IF.

Most current implementations also utilize external varactor-tuned LC resonators to provide the tuning element of the voltage-controlled oscillator (VCO) or VCOs which, in conjunction with a crystal reference, provides for frequency synthesis of the local oscillator (LO). The relatively high Q required for these resonators stems from phase noise considerations, discussed later.

These particular aspects of receiver architecture have fundamental implications for receiver integration level. Unfortunately, the required high-Q, low-noise, low-distortion bandpass IF filter (70-100 MHz for 900 MHz receivers, for example) is well beyond the capabilities of current low-power integrated filter technologies. As a result, external high-Q passive filters are generally used, usually implemented with SAW filters, ceramic filters, or in some cases LC filters. Because of the frequencies involved and the package parasitics usually present, considerable power dissipation is involved in taking IF signals off chip into these

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devices. Also, available on-chip spiral inductors in standard silicon technologies have Qs limited to 5-10 at the frequencies of interest, only adequate in some situations for implementation of the low-phase-noise VCO required in conventional synthesizer architectures.

In the transmit direction, the use of direct carrier modulation has become widespread[29], so that channel shaping filters can be implemented at baseband. In current practice the transmit power amplifier is usually implemented with GaAs discrete devices or simple ICs with a number of external inductors used for tuning and impedance matching. A narrowband external passive filter is usually required to limit transmit energy to the desired band.

The major challenge in RF transceiver design is to more effectively utilize scaled technologies to improve the integration level of RF transceivers, with resulting further improvements in power dissipation, form factor, and cost. Efforts are underway in industrial laboratories and universities around the world, taking various avenues toward this goal. The most promising approaches involve direct-conversion or low-IF receiver architectures that eliminate external IF filtering, new approaches to frequency synthesis that eliminate the need for external VCO resonators, and more effective utilization of on-chip spiral inductors available in near-standard IC technology to provide the tuning function essential to low-power realizations of RF functions. A hypothetical single-chip transceiver that might result from success in these areas is illustrated in block diagram form in Fig. 2.

Direct-Conversion, Quasi-direct Conversion, and Low-IF Receiver Architectures

A promising direction in architectures for higher integration in RF transceivers is the use of zero IF, low-IF, or quasi-IF configurations in the receiver, following the pager model, and the use of direct modulation in the transmit path. These configurations have been investigated intensively for many years (see for example [10][15]) but have made their way into practice in only a few specialized applications[9][11][12][13][14][15][16][17][18][19][20]. These configurations eliminate the external IF filtering function since the IF filter is replaced by two (I and Q) lowpass filters in the case of zero IF and quasi-IF receivers, or by a low-frequency, low-Q bandpass IF filter in the low-IF case.

The most severe problems in direct conversion receivers result from the fact that the baseband signal often contains low-frequency information that must be distinguished from DC and low-frequency errors that arise in the baseband signal path. One important error source is the device-mismatch-induced DC offset and 1/f noise of the signal path itself. For reasons of large-signal blocking performance, the gain of the LNA is usually restricted to the 20dB range, so that the wanted signal level reaching the mixer under weak signal conditions is on the order of 100 microvolts in amplitude. The accumulated DC offset referred to the mixer input can easily be 10mV, 100 times larger than the signal. Another important contributor is LO leakage, resulting from the fact that since the LO is at the carrier frequency, any energy from it reaching the RF path demodulates to a DC offset. Because the effects of LO leakage can be a function of the impedance seen at the antenna, these DC offsets can vary with time in an unpredictable manner. The problem is more severe in frequency-hopping receivers because the carrier leakage is different at each hop frequency, giving a time variation to the DC offset that is induced. The cumulative effect of carrier feedthrough and DC offsets is to superimpose large, possibly time-varying additive errors on the

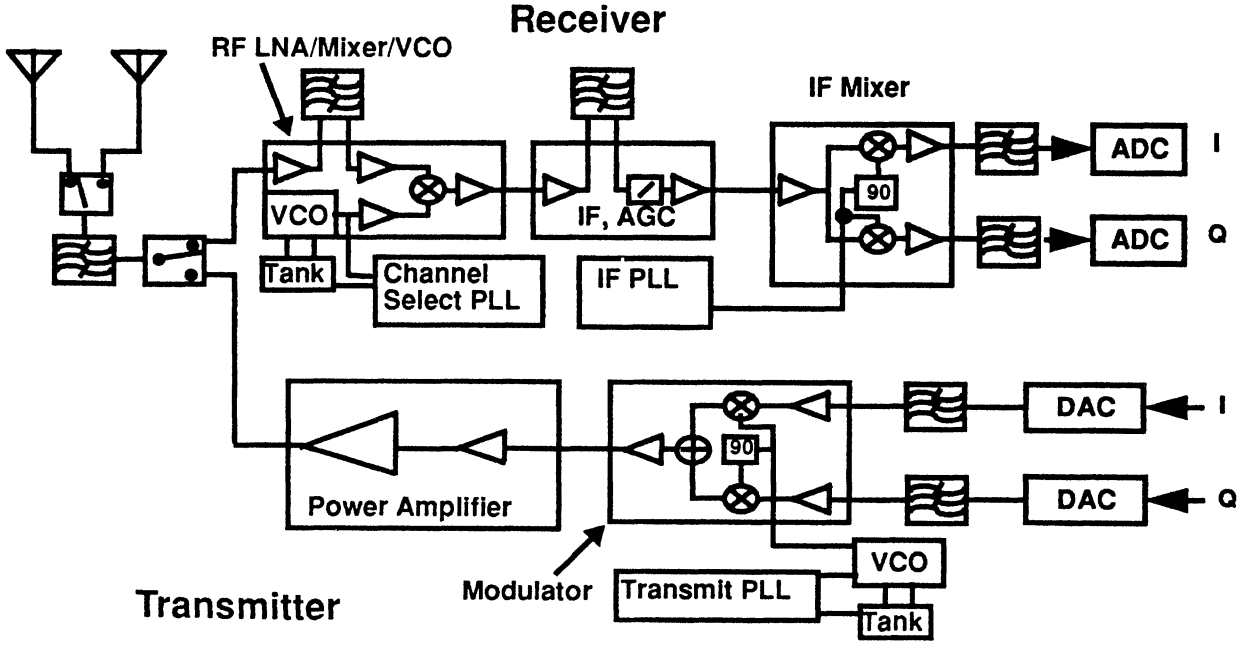

Figure 1. Block diagram of a typical multi-chip, multi-technology transceiver implementation

small wanted low-frequency AC signal in the baseband signal path.

Numerous approaches have been tried to attack these problems. Most have been attempted within the context of a more conventional, bipolar technology multi-chip receiver implementation using analog baseband filtering and demodulation. However, a closer coupling between the demodulation process and the RF and baseband analog signal path may well allow the separation of the DC offsets to be carried out using an adaptive approach that combines this function with carrier recovery, symbol timing recovery, automatic gain control (AGC), and data detection in a mixed analog-digital implementation. Most TDMA systems, for example, utilize a preamble in the frame structure which when demodulated to baseband has either zero or known DC content, allowing adaptive, frame-by-frame DC offset removal. The problem of 1/f noise can be attacked in a number of ways, one of which is to simply use correlated double sampling or chopper stabilization of the active elements in the baseband signal path. A/D conversion of the baseband signal at high resolution is a requirement for this approach.

Most of the benefits of homodyne receivers accrue if the IF is translated to a low but nonzero value instead of to DC as in homodyne receivers. The IF needs to be low enough that normal monolithic filtering techniques such as g_m/C continuous filters or switched-capacitor filters can be used. The advantage of this approach over homodyne receivers is that the problems of DC offset and 1/f noise are greatly reduced. However, a new problem of image rejection of the relatively close in image frequency is introduced. This image energy must be eliminated through the use of an image-rejection mixer configuration following the LNA. Since this mixer will have to provide image rejection on the order of 60-70dB in some applications, phase shift accuracy and path matching accuracy within the mixer must be extremely precise. Progress has been made in this area in recent research [21].

Another important variation is the quasi-IF or "vestigial IF" approach in which the entire band of frequencies to be tuned by the receiver is translated down to IF in the first mixer, and then subsequently translated directly to baseband in the second mixer with little or no IF selective filtering. The channel-select filtering is done at baseband with a lowpass filter following translation to baseband. This technique has several important advantages. The first local oscillator can be implemented as a fixed frequency oscillator, making it easier to realize the required phase noise performance. The second LO, used to tune the desired channel, is at much lower frequency and its phase noise contributions, as well as the spurs associated with the narrow channel spacing and associated low comparison frequency, can be made much smaller. The carrier feedthrough problem is also eliminated. The technique eliminates the IF filter, but retains the image reject problem at RF and also many of the DC offset and drift problems of direct conversion receivers since adjacent channel blocking signals are carried to baseband and as a result most of the gain applied to the desired signal is done at baseband. The example receiver in Fig. 2 has this configuration.

Adaptation in Receiver Implementation

Conventional mixed-technology low-integration receivers have used RF/IF signal paths with relatively fixed functionality except for AGC and one or two other parameters. Higher integration implementations offer the possibility of much greater use of adaptive blocks. This capability may allow a signal transceiver to effect large savings in power, and to interface with more than one type of RF systems.

Power-Adaptive Transceivers

Most important power-dissipating elements in high-integration communications transceivers have a minimum dissipation requirement that is a function of the distance of the transceiver from the base station. In cellular phones, for example, the transmit power of the power amplifier is routinely varied adaptively depending on distance from the base station, both to save power and to reduce interference to other users.

Improvements in overall average power dissipation could result from a wider application of the power adaptation concept. For example, the LNA power dissipation is dictated by the requirement for low noise figure and good input matching to accommodate the weakest signal that will be encountered far from the base station. When the signal is stronger, the LNA could be adaptively powered back to a lower power setting. In some current receivers a variation on this approach is now employed in which the LNA is simply bypassed and powered down for very strong signals. Similar adaptive power reductions may be possible in the mixer and baseband signal path as well. Another large dissipater is the synthesizer VCO, which must have very low phase noise for many applications. This noise is less important when the received RF signal is stronger, since the mixer-aliased VCO phase noise from the adjacent channel can be larger in absolute terms. As a result, power savings may be available by reducing VCO power and allowing larger phase noise. Similarly, the dynamic range required in the baseband signal path is greatest when the desired signal is weakest. Optimum distribution of gain and dynamic range through the baseband path is a function of both the desired signal strength and the interfering signal strength, both of which are easily detected in a digital implementation. For strong desired signal conditions, smaller filtering capacitors could be adaptively used in the path, allowing operation of the active devices at lower bias current for the same bandwidth.

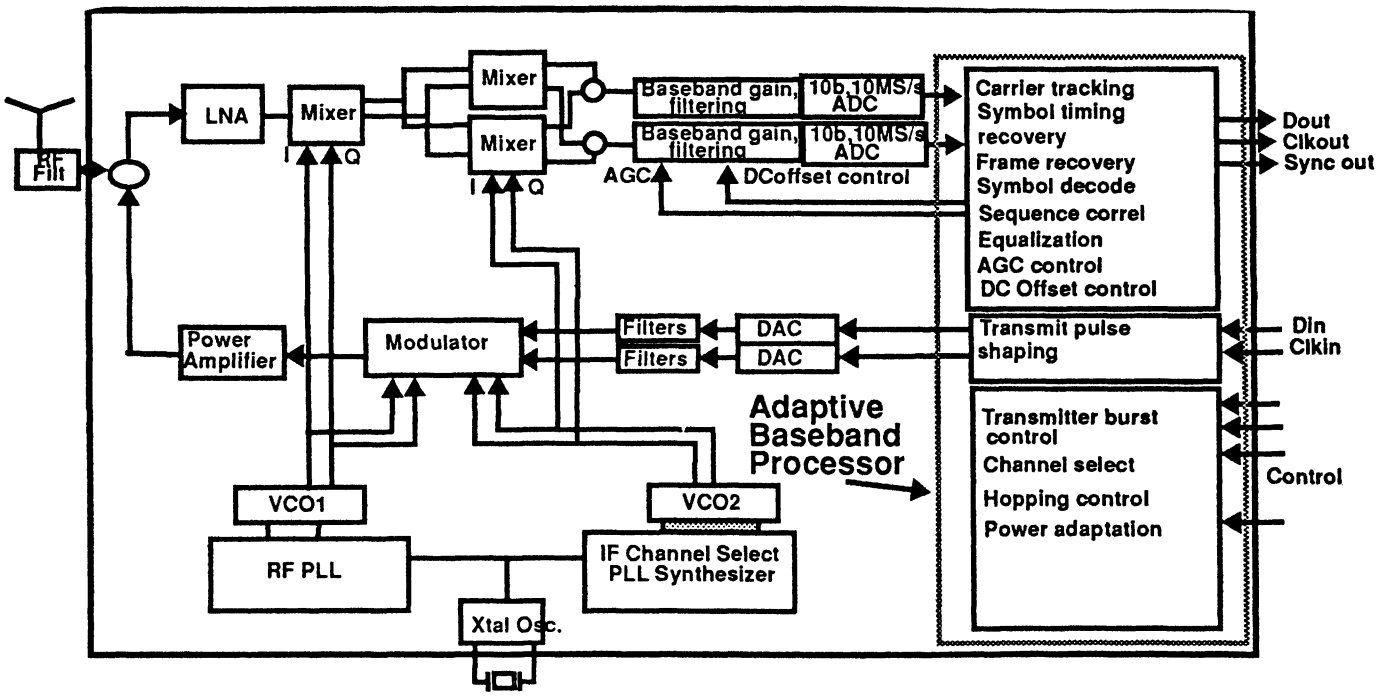

Figure 2. Block diagram of a possible future high-integration adaptive transceiver

Standard-Adaptive Transceivers

Great benefits could potentially accrue from a unification of approaches to data communications transceiver design. From an applications viewpoint, there is no fundamental reason that a single transceiver device could not provide the functionality of multiple communications standards at multiple frequencies. This might allow-for example, a single hand-held device to perform the functions of cellular phone and cordless phone compatibly with the varying standards for such service in Japan, North America, and Europe. Certainly multiple RF ports and antennas would be required for optimum performance at the different wavelengths, but following this a single transceiver should be able to adapt the different transmit power levels and modulation schemes. Central to achieving this would be an architecture in which a major portion of the IF (baseband in homodyne receivers) signal processing is performed in the digital domain, as well as carrier recovery, symbol timing recovery, equalization, DC offset control, power control, and so forth. A high-integration CMOS or BiCMOS implementation would be essential.

A secondary benefit would be a great reduction in overall engineering costs associated with development and productization of separate RF core functions for every standard and every type of device. The availability of a generic RF core function implemented in a VLSI digital compatible process such as scaled CMOS would be widely useful in implementing RF communications functions.

Circuit Approaches for Integrated Synthesizers

Most current transceiver implementations utilize external varactor-tuned resonators to implement the VCO function in one or two local oscillators that are slaved to a crystal reference through fixed or programmable divider chains in a phase-locked loop (PLL). Incorporation of these oscillators on-chip is an important goal in increasing receiver integration level and thereby reducing power. Often the divider is alternately switched between two adjacent divisor values at a high rate to achieve an effective interpolated value of division when very fine channel spacing is required (fractional-n synthesis). In the case of the US analog cellular standard, for example, the channel spacing is only 30kHz at 900 MHz, requiring the synthesizer to tune in very fine steps. This in turn requires the VCO frequency to be divided by a large integer, resulting in a low rate of comparison of current VCO phase with crystal oscillator phase. This in turn requires a low loop bandwidth.

Synthesizer PLL loop bandwidth is an important parameter in receiver design because of its influence on the local oscillator phase noise spectrum. The phase noise present in the local oscillator signal generated by the synthesizer contributes directly to phase noise on the IF or baseband signal after frequency conversion, and as a result directly degrades the effective signal-to-noise ratio (SNR) of phase-modulated signals. More importantly, LO phase noise mixes with adjacent channel signal energy, degrading overall receiver SNR and limiting receiver blocking performance. Finally, in the transmitter the phase noise of the LO contributes noise energy outside the band of the channel being transmitted. Spurious transmitted energy at adjacent channel frequencies must be closely controlled in most systems. With proper PLL loop design, the phase noise of the synthesizer is dominated by the phase noise of the crystal reference for frequencies far below the PLL loop bandwidth, and by the inherent phase noise of the VCO itself for frequencies far beyond the PLL loop bandwidth.

In conventional synthesizers realizing fine channel spacing, the phase comparison frequency is low and loop bandwidth is low. As a result, synthesizer phase noise in the regions of interest is dominated by inherent VCO phase noise. For an LC oscillator, the ratio of the internally generated VCO phase noise power to the carrier power can be shown to be directly related to the ratio of the amount of energy stored per cycle to the thermal energy kT. The energy stored is Q times the energy which must be supplied per cycle, and phase noise is directly related to the inverse of resonator Q, a fact predicted by a number of analyses of phase noise in oscillators.[31] Thus VCOs used to generate LO signals in phase-noise-critical applications almost always use some kind of external high-Q resonator.

A number of approaches show promise for realizing the VCO function on-chip. These include the use of on-chip spiral inductors[46], and the use of synthesizer configurations that allow wide PLL bandwidth so that the phase noise of the VCO is suppressed in the range of interest[27][28].

The use of on-chip inductors and varactors to implement the VCO has been demonstrated [14] using aluminum spiral inductors in standard bipolar technology. Because of the limited Q available, the phase noise achievable is not as low as required in some applications. Other alternatives with higher Q include the use of bond wire inductance [24][52]and the use of plated-up gold inductors over thick oxide [29]. Even with higher-Q inductors, the realization of a low-resistance, wide-range varactor tuning capacitance using standard IC technology is difficult. The simultaneous realization of high Q and tunability, together with either wide tuning range or high center frequency accuracy, is a very difficult task. The use of structures occurring in standard IC technology (such as bipolar base-emitter and base-collector capacitors) to perform the varactor function tends to introduce series resistance losses that reduce the Q to values below 10.

Ring-Oscillator-Based VCOs and Noise-Optimized Synthesizer Architectures

Ring oscillators are particularly attractive for LO generation because they inherently provide the quadrature clocks required for direct conversion and quasi-direct conversion receivers. Recent progress has been made in understanding the fundamental limits on noise in CMOS ring oscillator VCOs and the relationship between phase noise and power dissipation. In effect, for a given power dissipation a ring oscillator has a phase noise approximately equivalent to an LC oscillator with a Q of unity[27][28]. Each factor of 10 reduction in phase noise power with respect to the carrier requires a factor of 10 increase in power dissipation, all else being equal. The use of more advanced technology or lower supply voltages does not greatly alter this situation because of the fundamental processes involved. It appears that a phase noise level of about -106dBc per hertz should be achievable at 1MHz away from the carrier with about 50mW power dissipation in a 4-stage differential ring oscillator operating on a 3 volts supply at 1.8GHz. While this is adequate for some systems, it is inadequate for most digital radio communications applications.

The effects of close-in VCO phase noise can be minimized if PLL loop bandwidth, phase comparison frequency, and loop order can be kept high. A promising approach to achieving this is to use techniques of VCO phase interpolation in order to be able to make more frequent comparison of VCO phase with the instantaneous phase of the crystal reference. Discrete phase interpolation and noise-shaping M/N interpolation [49] are two examples of approaches to this goal. It appears likely that means can be found to increase the effective loop bandwidth by a large factor, thereby greatly reducing the effect of intrinsic VCO phase noise on the LO signal, in turn allowing the use of a ring oscillator VCO at least for some of the applications. In effect, this amounts to making the close-in VCO phase noise more dependent on the (very good) phase noise of the crystal reference and less dependent on the phase noise performance of the VCO. This approach has the additional advantage of preserving a wide loop bandwidth for frequency agility. Also, the short loop time constant potentially allows the powering down of the ring oscillator during inactive frame times in TDMA systems, resulting in power savings that offset the higher inherent active power of the ring oscillator.

The use of quasi-IF receiver architectures, in which the first VCO frequency is fixed, also relieves the phase noise problem because the comparison frequency and loop bandwidth can be kept much higher in a fixed-frequency first VCO. The second VCO/synthesizer performs the tuning function, but its impact on receiver phase noise is smaller since it operates at a much lower frequency.

Direct Digital Synthesis of the LO Signal.

Direct digital synthesis of the LO signal using a DAC, ROM, and phase-accumulation synthesizer is a very attractive alternative due to the excellent frequency agility achieved. Considerations of power dissipation and technology speed capability limit such waveform synthesis to about 100MHz and below for typical current technologies. However, the synthesized waveform can be used as a frequency offset added to a carrier generated with a fixed-frequency VCO and PLL[18][48]. Because the generated frequency is a fixed integer multiple of the crystal reference, the bandwidth of this loop can be kept high, allowing low phase noise in this fixed reference signal. This small difference frequency is used to translate the fixed carrier from the first PLL to the final carrier frequency using a quadrature modu-

lator. It appears that this will be a very effective solution for at least the subset of applications where modest phase noise and modest spurious output component requirements can be tolerated. A similar approach using a secondary PLL to generate the offset frequency has recently been proposed[29].

Low-Power Baseband Signal Conversion and Processing

Depending on the type of transceiver, baseband operations of IF filtering, equalization, timing recovery, symbol constellation decoding, signal correlation, symbol generation, quadrature modulation, frequency synthesis and so forth are required. A major body of current research is aimed at performing more of these functions in the digital domain than is currently the case, with resultant improvement performance, adaptability, and manufacturability. The principal trade-offs are the incurred penalty in power dissipation and die area of the digital implementation, and the cost and die area of the required A/D converter. Rapid progress has been made in the implementation of these types of functions in VLSI CMOS[19][37][38][39].

Many benefits accrue in pushing baseband signal processing into the digital domain, particularly for multistandard adaptive transceivers. For direct conversion receivers, the composite baseband signal contains all the large adjacent-channel blocking signals, and as a result an all-digital implementation of the baseband signal processing would require two A/D converters of greater than 80dB dynamic range and 20MHz effective sampling rate. Some combination of analog and digital filtering will be optimum. For at least the higher-frequency portions of this set of applications, low-power, high-speed approaches such as pipelining will be required. Finding techniques for reducing the power dissipation of these A/D converters is a key goal. Current state of the art for this class of converters is about 1mW/ MHz of sample rate at 10 bits [35].

Technologies for High-Integration RF Transceivers

Current transceiver implementations usually use a mix of technologies, with GaAs for the power amplifier and perhaps for the LNA, bipolar or BiCMOS for the mixer and IF functions, and CMOS for the baseband processing. High-integration implementations will require use of a single technology for most of the functions. GaAs will continue to play a very important role at the higher frequencies, but it appears likely that high-integration all-silicon solutions will evolve at the lower end of the spectrum.

Alternative technologies for a transceiver at the integration level of Fig. 2 are BiCMOS and CMOS. Bipolar and BiCMOS solutions are attractive because of the inherent capability of bipolar transistors to provide high g_m at low current, and because of the well-developed family of circuit techniques for RF design using bipolar technology[23]. There is also considerable interest in utilizing CMOS for high-integration transceivers, particularly within the university community. Because of the potentially lower cost of a CMOS implementation, efforts to overcome the poorer characteristics of CMOS for RF by utilizing alternative receiver architectures, taking advantage of the high f_{max} of the NMOS device, and using more adaptation in the receiver may pay large dividends. The continued scaling of CMOS technology, with 0.1 micron devices with f_ts of near 100GHz recently demonstrated,[42][43] should eventually allow this approach.

Silicon-germanium technologies now evolving have the potential to provide bipolar devices with substantially larger f_t and f_{max} than the best current bipolar technologies[44]. The impact of this development is likely to be felt mostly at the high end of the frequency spectrum under discussion here.

Compatible High-Q Inductors and Resonators in Silicon

For reasons explained earlier, on-chip inductors are essential to low-power RF design. Present practice makes extensive use of wirebond inductance and spiral inductors in silicon in products currently in production. Improvement of the implementation of and the modeling of integrated inductors is a key goal.

Bond Wire Inductors

Bond wires provide inductance on the order of 1-4nH, depending on length, at 2 GHz, with Q on the order of 50. Higher inductance is realizable with unusual pad placements.[24][52] While pad-pad jump bonds are possible, they are not compatible with most automated bonding equipment. Inductor tolerance is a function of die attach, bonder mechanical accuracy, and wire diameter, and is in the +/-20% range at present.Adjustments to mechanical assembly procedures could improve this significantly. Matching of bond wires on one side of the die to the same post is also better than 20%. Mutual coupling effects of adjacent wires must be accounted for through electromagnetic analysis of the configuration with a commercial package.

Creative use of bond wire inductance in SO and SSO packages with (perhaps) custom lead frames is a highly promising approach to implementing matching and tuning inductors in 1 and 2 GHz LNAs, VCOs, and power amplifiers. These elements are already widely used to perform part of the impedance matching function at LNA inputs and in power amplifiers.The tolerance is a major problem, since there is no good high-Q variable capacitive element available.

Spiral Inductors on Silicon

Extensive work has been carried out on spiral inductors on silicon[45][46]. These devices can provide implement

inductors up to about 10nH range in reasonable area, with Q limited to about 5 at 1 GHz and 10 at 2 GHz by metal series resistance for standard technologies. Self-resonance due to the large parasitic capacitance to the substrate is a substantial problem, and drops to about 2GHz for a 10nH inductor in typical technology. Since the inductor is usually being used to match impedence or tune a gate or base diffusion capacitance, the parasitic capactiance can usually be incorporated in the design process as long as the self-resonant frequency is far above the frequency of interest.

Two approaches have been described in recent work for improving the performance of spiral inductors. In one approach, [25] a pit is etched under the spiral to remove the substrate capacitance and resulting self-resonance. The resulting structures have moderate Q but good self-resonance characteristics. Another approach is the deposition of thick oxide following normal IC fabrication, and the deposition of highly conductive interconnect metallization such as gold to form a high-Q spiral with reasonable self-resonance behavior. [29] This approach has high promise because the subsequent processing is relatively non-invasive to the underlying silicon and involves only low-temperature deposition and masking steps.

Package and Substrate Modeling

Perhaps the greatest single barrier to higher integration in RF transceivers is undesired interactions through substrate and package coupling. The problem can be addressed through a number of architectural and circuit approaches, but a critical missing link is a substrate and package modeling and simulation methodology to allow accurate prediction of these coupling effects prior to fabrication. Rapid progress is being made in this area [33][41][50].

Summary

Prospects for continued progress in high-integration, low-cost RF transceivers is excellent. A key requirement for progress is close collaboration between transceiver and system designers and architects, RF and digital circuit designers, and device and package modeling engineers, so that opportunities for innovation with new architectural approaches can be identified and exploited.

Acknowledgments

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The challenges for analogue circuit design in mobile radio VLSI chips

Jans Sevenhans and Dirk Rabaey from Alcatel Bell Telephone describe the present status of mobile phone ASIC's. Radio analogue design expertise is on the move from printed circuit board to large scale silicon monolithic.

Mobile radio telephony is becoming a driving application for analogue circuit design using silicon CMOS and RF bipolar technology.

Similar things are happening for several wireless personal communication systems. Basically the cellular radio telephone, the wireless PABX and the wireless SLIC bringing the same challenges to analogue circuit design: ie maximum integration of the basic radio functions into 1 or 2 silicon chips, CMOS, Bipolar or BICMOS or GaAs. The analogue circuit designer for radio telephone applications will need all the state of the art analogue design know how available today, from RF-mixers and GHz range low noise amplifiers and local oscillator synthesizers over base band 100kHz CMOS analogue to low frequency speech analogue to digital conversion. And for all these circuits the message is: minimum power consumption for battery autonomy, minimum silicon area for maximum functional integration per die to obtain a small, low cost pocket size radio telephone.

For the asic integration of a radio transceiver the "One asic per transceiver function" approach was regarded as the optimum architecture to obtain the maximum" per die integration level". In the next generation receiver and transmitter functions operating at the radio frequency are integrated in one RF-bipolar ASIC and the baseband circuitry in a CMOS mixed analogue/digital asic doing the analogue filtering, automatic gain control and A/D conversion. The synthesizer can be partitioned with the VCO and prescaler in the RF front-end IC and the two modulus counter in the CMOS analogue baseband IC but the integration of the VCO leads to some practical problems that will be discussed further on.

The low noise radio receiver

A high performance radio receiver basically consists of the following functionalities:

A low noise amplifier (LNA) to bring the femto Watt radio input signal up to the sufficient level to cope with the thermal noise of the mixers. The challenge here for analogue radio design is to build low cost silicon bipolar low noise amplifiers with very low power consumption, about 5mA to provide +/-20dB switchable gain and a 3dB or better noise figure and an input third order intercept point above 14dBm to handle the high intermodulation radio input signals and the blocking levels specified by GSM.

One or two cascaded mixer stages bring the radio signal down from RF to baseband with sufficient gain to further process the analogue receiver signal in noisy standard CMOS technology.

The challenge in the 900MHz or 1.8GHz mixers is first to integrate the set of I and Q mixers into one silicon die together with the quadrature phase shifter that provides the 90° local oscillator signals to drive the I and Q quadrature mixers.

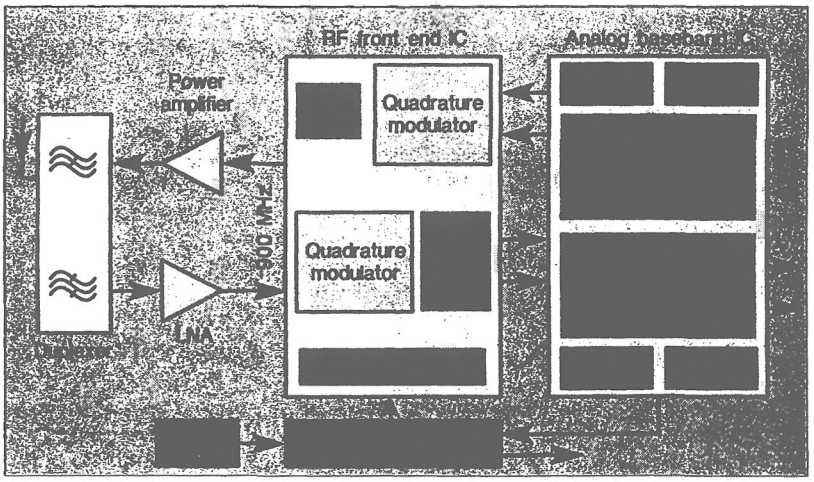

Figure 1: Block diagram of the radio analogue front end circuitry in a mobile radio telephone

In general we can say that to build a radio receiver with an acceptable Bit Error Rate, we need a low noise, low power (<25mA, 3 to 5V) analogue radio front end with 40dB total switchable gain in the low noise amplifier and the mixers before we can add 50nVHz$^{-1/2}$ CMOS thermal noise to the baseband radio receive signal.

For this low noise radio receiver the choice of technology is between advanced Silicon RF bipolar with 10 to 20GHz f_T or GaAs. The availability of those RF

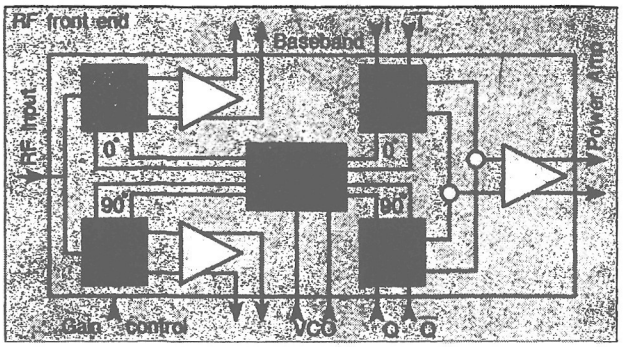

Figure 2: Monolithic silicon bipolar RF front end

Reprinted with permission from *Microwave Engineering Europe*, J. Sevenhans and D. Rabaey, "The Challenges for Analogue Circuit Design in Mobile Radio VLSI Chips," pp. 53-59, May 1993.

bipolar technologies with Silicon foundries in Europe, USA as well as in Japan has lead the majority of integrated radio designs to the use of RF-bipolar for the transceiver radio frontend of the wireless personal communication terminals.

CMOS filtering, AGC and analogue to digital conversion technique cover all the basic needs for the base band signal processing of a high performance radio receiver. Several options are open to make a compromise between filtering, AGC and A/D dynamic range. In the limit one could build a receiver out of two 0.9GHz sigma delta a/d convertors in RF-Silicon bipolar or GaAs right after the LNA operating on quadrature phases of the local oscillator. In this case you need over 80dB linear range for the a/d convertor and less than $5nVHz^{-1/2}$ equivalent input noise for the sigma delta modulator A/D convertors. In this extreme compromise another challenge is to build a 0.9GHz decimator first filter stage before the first downsampling. All of the filtering and AGC is then a job for a fast digital signal processor. Also undersampling of the radio-signal is a promising technique for futuristic radio receivers.

But today's solution is to use simple 8 bit a/d conversion and a classical rational AGC algorithm in combination with dedicated filtering between all the gain stages. The challenge of analogue radio design is to provide sufficient gain on the wanted signal to overcome the noise of the active filters that have to suppress the blocking signals and adjacent channels to protect the linear performance of the gain stage to follow, in other words a lot of delicate analogue CMOS design to provide a dB of filtering for each dB of gain until your receive signal reaches the A/D convertors input.

For accurate analogue filtering switched capacitor filters are the best as long as we have sufficient supply voltage to cover the signal amplitude and the thresholds of the switches. So with 5V supply and 1V threshold for the switches we still are 0.5V away from hard compression and signal clipping. With 3V supply voltage the trade off is a bit different. In MAD-design (Mixed Analogue and Digital) in 0.5 micron CMOS the 3V power supply is a technological maximum rating that analogue design will have to live with. The use of time continuous filters, OTA-C or MOSFET-C filters can become a solution as we go into 3V CMOS radio analogue. At least no switches threshold voltage is consuming any linear range between the supply rails. And CMOS transconductors with 60dB linear range for noise and distortion on 5V supply voltage will have to improve in the next few years to make them applicable for 3V CMOS radio analogue filter design.

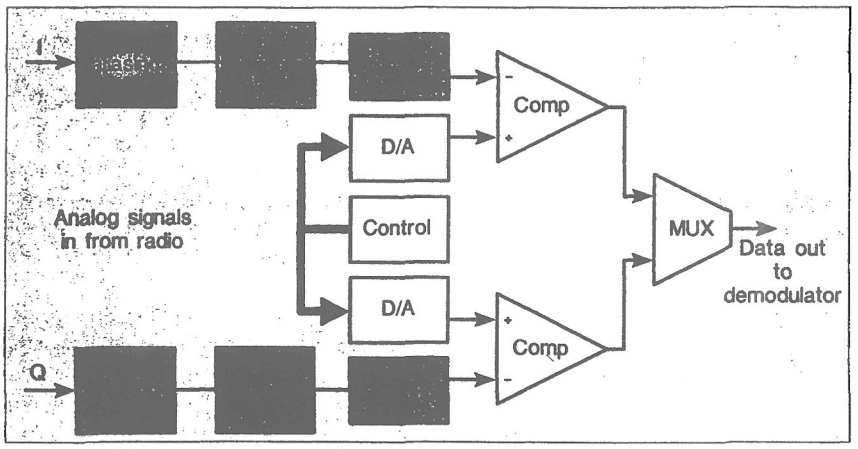

Figure 3: GSM receive channel filter and successive approximation switched capacitor A/D

For the receiver architecture the choice is between heterodyne and homodyne demodulation.

Heterodyne receivers have the advantage that the local oscillator frequency is different from the radio signal frequency on the antenna. Good design practice has lead to the choice of 71MHz as a standard for the IF (intermediate frequency) in GSM heterodyne receivers, because the 900MHz GSM band has a width of 70MHz: 890-915MHz for the base station receiver and 935 to 960MHz for the mobile terminal receiver. A second advantage of heterodyne radio receivers is the opportunity to filter the radio signal at the 71MHz IF. These IF filters can suppress the neighbouring channels and blocking signals to optimise the use of the available linear range in the rest of the receive chain. AGC amplifiers at IF have the inherent advantage that offset problems are easily solved by AC-coupling trough small (on chip) couple capacitors having transient time constants in the 10nsec range.

The only problem to integrate an IF receiver in a monolithic device is the integration of the IF filters. Passive filtering (SAW) is the solution for high Q filtering in a low noise receiver and the SAW filter drivers are very power hungry. Time continuous or sampled analogue filtering at 71MHz is very well feasibly in RF bipolar or GaAs biquads but the noise figure or a high Q active filter is going up with the Q to G ratio: quality factor to gain of one filter section.

The difficulty to integrate low noise IF band filtering is the main reason to work without an IF for a low noise radio receiver.

In a homodyne receiver, as we go directly to baseband in one mixer stage, all the filtering is well know base band filtering with low Q-factors, easy to integrate in CMOS time continuous or sampled data filters, switched capacitor or switched current circuits. Also the use of a homodyne receiver avoids the need for an image filter that prevents an IF receiver to create an unwanted response to a spurious signal at 2 times the intermediate frequency away from the wanted signal frequency.

The homodyne receiver, simple and compact as it is, with all it's advantages for low Q low pass filtering has one major draw back: OFFSET.

Demodulation of local oscillator leakage in the radio front end and self detection of high blocking levels are a major problem for radio communication systems like GSM that use a base band signal spectrum with important DC and low frequency content. In those systems the high pass action of an AC-coupling is cutting too much energy away from the signal spectrum. For this reason a homodyne receiver for GSM cellular radio mobile

communication needs a sophisticated offset cancelling algorithm to cope with 3 types of offset: static offset resulting from transistor and resistor matching errors, dynamic offset resulting from the mixer demodulating the local oscillator leaking to the antenna signal and a second dynamic offset resulting from the high blocking signals self mixing as the antenna signal is leaking to the local oscillator input of the mixers.

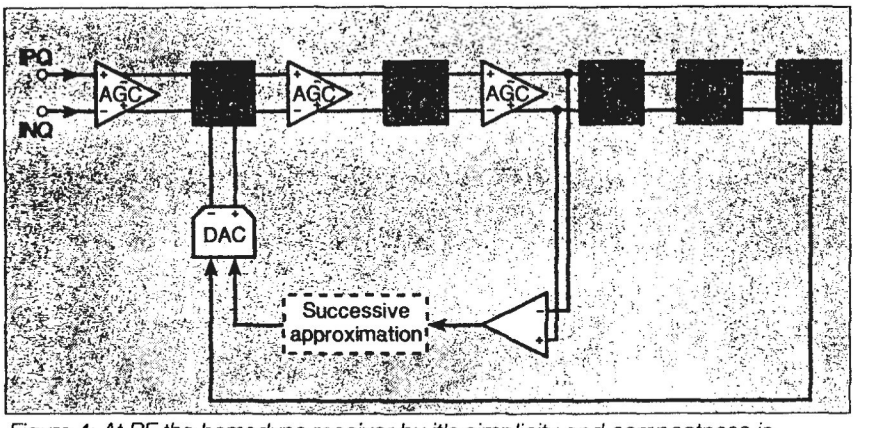

Figure 4: At RF the homodyne receiver by it's simplicity and compactness is certainly an advantageous solution for battery powered pocket radio telephones.

Over the past few years elegant solutions have been developed to overcome this offset problem by monitoring the offset in the digital base band signal, low passing it and feeding the correct offset subtraction back to the input of the CMOS AGC.

The offset problem has been the dominant reason for a lot of radio telecom companies not to use the homodyne receiver for GSM and other radiocom receivers in terminals and base stations. THe implementation of sophisticated offset algorithms in the receiver DSP, coupled with D/A convertors to subtract the correct offset value have overcome this problem.

The voice codec

The other interface of the radiotelephone is the voice interface with the microphone and earpiece. This is a classical speech interface with 8kHz speech sampling with 13 bit accuracy.

The microphone signal is going to a second order switched capacitor sigma delta a/d convertor operating at 1MHz. The 1 bit of 1MHz PDM signal is then filtered and downsampled to 32kHz in the decimator and further lowpass filtered before downsampling to the 8kHz linear speech.

The earpiece signal coming from the GSM speech transcoder is passing through a symmetrical signal path. A bandpass filter operating at 32kHz is oversampling the speech signal 4 time and a linear interpolator increases the speech sample rate up to 256kHz before the digital sigma delta modulator converts the speech signal to the 1 bit 1MHz PDM. A switched capacitor a/d convertor then provides the analogue speech signal to the earpiece.

This voice interface is very similar to the analogue interface you find in every plain old telephone. This is the reason why in today's radiotelephones you find the voice codec as a separate component usable in any voice interface. Nothing but the silicon area per die prevents us from integrating the voice interface on a single chip with the baseband CMOS radio transceiver.

The low noise radio transmitter

The noise constraints for the transmitter are very high as well: 25dB above the -174dBmHz^{-1} thermal noise floor.

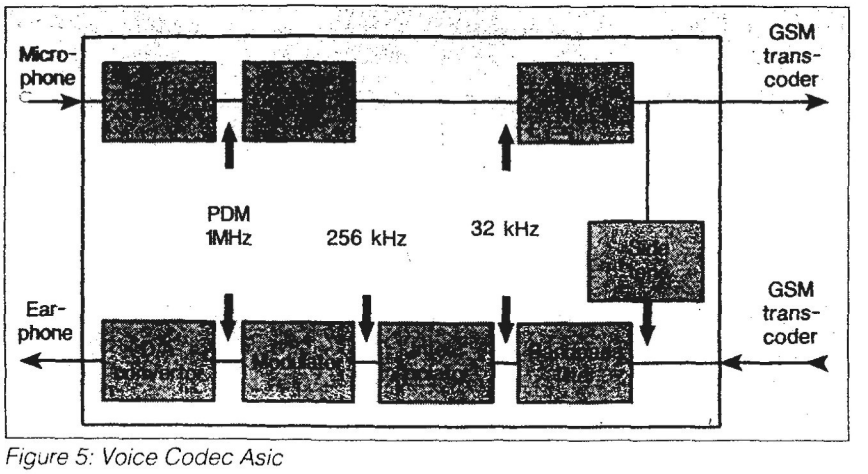

Figure 5: Voice Codec Asic

The noise constraints in the transmitter are set to prevent mobile transmitters to jam each other and the receiver of the base stations for distant users. From this point of view the homodyne transmitter was chosen: only one mixer state to contribute noise to the transmitter signal.

The quadrature phase shifter on the 900MHz local oscillator signal is a delicate aspect of the homodyne transmitter where a phase accuracy of .5° is required over the 70MHz range of the GSM receive and transmit band.

The power amplifier is still a big challenge for monolithic integration. For handportable phones the output power is between 0.8 and 2 Watt in a 1:8 burstmode duty cycle for GSM. Depending on the power efficiency of the class AB amplifier this corresponds to a power dissipation of less than half a Watt in one die, which is certainly not an obstacle for a plastic package. To provide 2W to an output transformer from a 3V supply it is clear that output currents will be in the range of ampères, forcing the designer to use 10 pins in parallel when using plastic flat packages. But the real challenge here for the analog radio design is in the efficiency of the class AB power amplifier. Today expensive hybrid modules are used for this application. But as the mobile radio telephone market will expand in the near future, RF MMIC design houses will spend the effort to develop monolithic solutions in Silicon or GaAs.

The control of the output power as a function of temperature and aging is another challenge for analogue design to measure the output power with an RF peak detector

and adjust the gain of the power amplifier in a stable feedback loop. In addition to this the loop must have sufficient bandwidth to follow the burst ramp up of the time multiplexed GSM transmit signal.

The base band signal generator in a GSM transmitter basically consists of a D/A convertor and a ROM containing the Gaussian shaped quadrature I and Q signals. The challenge for analogue design here is the low power and low voltage constraint. The use of 3V supply voltage in the digital circuitry is driving the analogue design into the 3V range as well, and the RF bipolar transmit mixers need 1V signal amplitude driven to the base band input pins of the Gilbert cell mixers to keep up the signal to noise ratio of the transmitter. A signal amplitude of 1V is easy in a 5V design, but in a 3V design you need a rail to rail amplifier for this.

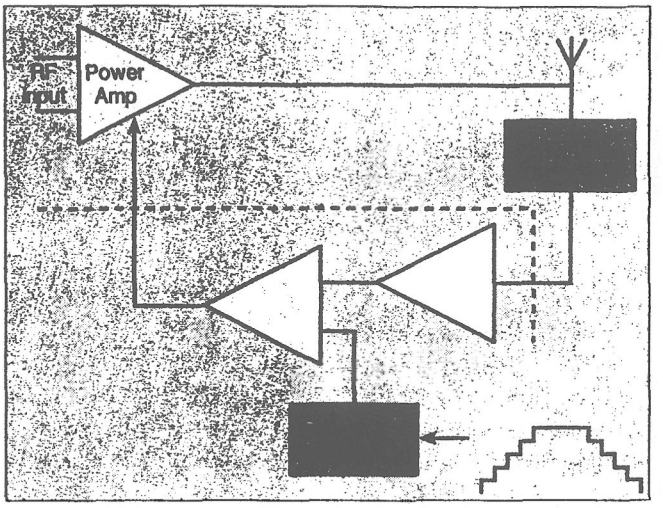

Figure 6: RF power amplifier with a feedback output level control loop.

The local oscillator synthesizer

State of the art mobile radiotelephones use phase modulation on a carrier in the lower GHz spectrum: 0.9GHz for GSM, 1.8GHz for PCN and DECT up to 3.5GHz for other wireless telephone systems in the near future. The radiotelephone terminals have to rely on temperature controlled reference crystal oscillators (TCXO) to provide the local oscillator signal with a frequency accuracy of 5ppm. These reference oscillators, operating at 13 or 26MHz for GSM are not the first candidate for further integration. The challenge for radio analogue monolithic integration is in the VCO and the prescaler.

The VCO is very difficult to integrate in an RF bipolar or GaAs front end because of the resonator. Resonators integrated on silicon have been reported with Q factors not higher than 10, which is far too low to obtain a VCO with -100dBc phase noise at 10kHz away from the carrier. The Q-factor of the spiral inductors on silicon is physically limited to very low values because in the substrate the electromagnetic field of the spiral inductor is damped in substrate currents.

This damping of RF electromagnetic fields in the bulk is a good thing to provide isolation between functional blocks on a Silicon MMIC, but for an LC resonator it is killing the Q-factor. Probably clever designers will come up one day with high Q girator solutions or biquad resonators in 20GHz RF bipolar or GaAs technology, but until then we are stuck with ceramic resonators for high Q VCO's and monolithic BICMOS synthesizers can integrate only the RF divide by 64/65 two modulus prescaler in the bipolar part and the low frequency (15 to 50MHz) CMOS two modulus divider, the charge pump and the phase comparator. An other challenge for CMOS analogue radio design is the integration of the RF prescaler in submicron CMOS.

As the f_T of submicron CMOS is well beyond a GHz, a full CMOS 0.9GHz and 1.8GHz synthesizer is the next step for analogue radio design to further reduce the cost of a mobile radio telephone.

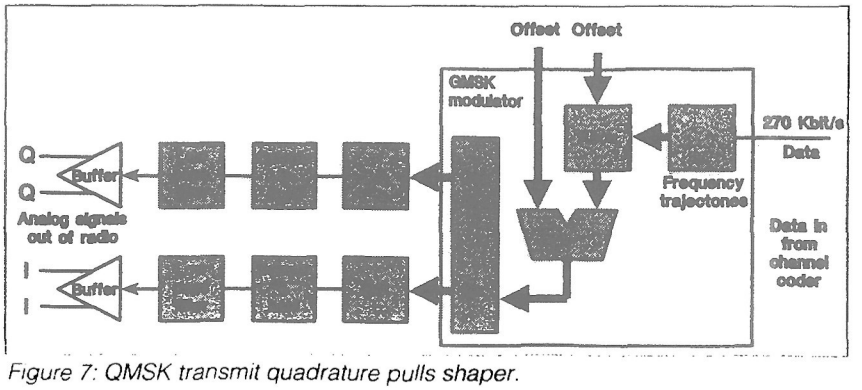

Figure 7: QMSK transmit quadrature pulls shaper.

Technology aspects

Radio analogue design is in a turbulent evolution today because of the availability of RF-bipolar technology up to 20GHz f_T. The emphasis is moving from strip line and radio board design towards single chip full radio integration. Single chip radio is still an overstatement for mobile radio telephones today and the economic aspects are not proven yet, but the experts now know that in less than 100mm^2 submicron BICMOS it is possible to integrate the analogue radio for GSM including the synthesizer with prescaler, the RF-mixers, the base band filters and AGC as well as the receive and transmit A/D and D/A converters.

For the low noise amplifier, the VCO and the power amplifier there is still some reluctance to go for silicon monolithic integration. Micromodules are certainly a valid alternative and an intermediate stage on the route towards monolithic.

The trade off between GaAs and Silicon is also a moving compromise, 3 years ago monolithic microwave integrated circuits were a GaAs monopoly, today silicon has proven to be more cost effective, at least for applications below 5GHz. But recent publications show 73GHz f_T for SiGe polysilicon emitter heterojunction bipolar transistors.

Submicron CMOS developments are more important for the digital part of the radio system because in analogue the total silicon area will not benefit from the minimum dimensions to the same extent.

Matching and other requirements in accurate analogue circuits prevent us from using minimum gate-length transistors and

minimum width poly for resistors and capacitors.

Conclusion

The challenge in analogue design for mobile telephony has a very broad spectrum: provide RF mixers for 3V supply in advanced bipolar technologies, come up with an active resonator with very low phase noise, design a monolithic 2W RF power amplifier, design CMOS 3V time continuous filters for the receive blocking and band filters. But as the silicon bipolar technology continues to catch up with GaAs for the RF building blocks and submicron CMOS trespasses the GHz border, some of the traditional compromise radio architectures will be questioned and new techniques will come up in analogue as well as digital radio design.

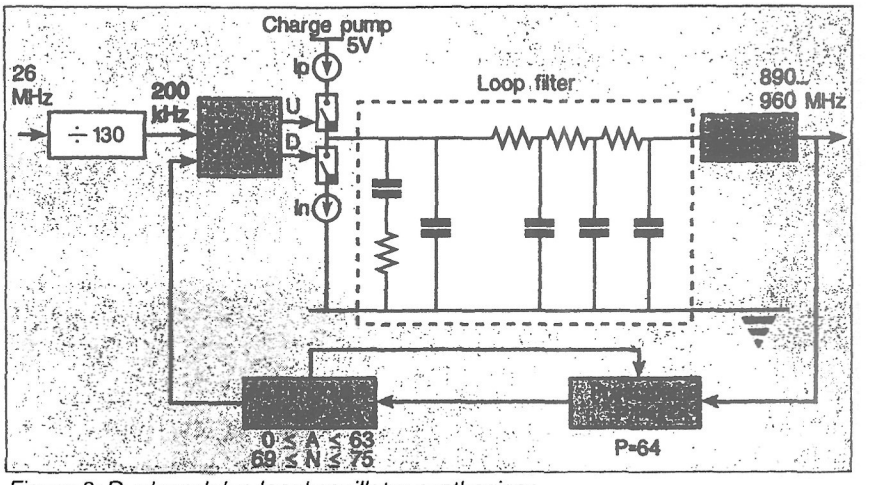

Figure 8: Dual modulus local oscillator synthesizer

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