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Introduction: The Opto-Electronic Integrated Circuit

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The history, present status and future prospects of silicon-based opto-electronic integrated circuits (OEICs) are reviewed here in order to provide a framework for the state-of-the-art discussions in this book. Before beginning the survey, let's consider some of the terminology used in opto-electronics. The Optical Society of America decided, after much debate, to replace many usages of the historic term 'optical' by the adjective 'photonic,' although 'optical' still has strong currency. The development of silicon 'photonics' is motivated largely by the desire to develop silicon-based photonic integrated circuits (PICs) since the functionality of a circuit is more diverse and significant that that of an individual photonic component. Components can be categorized as passive or active. Passive means that the optical function is fixed and constant. Active means that the function is variable and responsive to an external actuation-or-control signal. Lightwave emitters, amplifiers, detectors and modulators are active. The term 'active' is broad because it denotes a host of physical interactions such as electro-optical, thermo-optical, acousto-optical, magneto-optical, electro-mechanical-optical, chemical-optical, bio-optical and optical-optical (which includes linear and nonlinear opto-optics).

If we consider active PICs generally, we find that the actuation-and-control signals are usually applied to the silicon chip (with bonded wires, for example) from off-chip devices—at least that is how it has been done in the past. The Si-based opto-electronic integrated circuit (OEIC) is a very important special case of an active PIC in which the electronic controllers and drivers are integrated 'seamlessly' with the optical components in the same chip. This is an electronic-and-photonic integrated circuit (EPIC) in silicon: a chip-scale marriage of electronics ICs and photonic ICs. Because the 'EPIC chip' is generally associated with the EPIC program of the US Defense Advanced Research Projects Agency (DARPA), I shall favor the OEIC term in order to avoid linking the acronym to a sponsor.

The thesis of this chapter is that OEICs will, after further R&D, become the dominant form of active PICs, the one with the greatest global impact. That's why I have chosen to focus my

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attention here upon OEICs. The expectation is that OEIC chips will be very cost-effective, compact, reliable, efficient, and highly integrated—that they will solve communication problems not resolvable by optics or electronics alone. There is also the synergy speculation that new functionality will be obtained by combining optics and electronics as described here. I believe that readers of this chapter can help make this OEIC dream a reality.

1.1 A Few Words About History

Silicon photonic components were conceived in the mid 1980s [1, 2], and those early experiments dealt with waveguides and 2×2 electrooptical switches. As more people entered the field, numerous practical component structures were invented and tested. Many of the important possibilities for silicon-based photonics were recognized at the outset: that waveguides made of undoped crystal silicon could, in principle, have low propagation loss at the 1330 and 1550 nm fiber-optic telecomm bands because of silicon's transparency at wavelengths longer than its 1200 nm indirect band-gap wavelength, and that waveguided active-and-passive photonic components could be interconnected on a chip to create a PIC. To construct an active PIC, metal wires from one (or more) electrical IC chips can be joined to the PIC chip; but that arrangement is neither cost effective nor compact, and electrical parasitics are present. The OEIC provides the best photonic control technique because electrical drivers are connected internally to photonics (intra-chip) over short paths. Parasitics are low and the scale of integration is high compared with the multi-chip.

For active control of light, the 1986 paper [2] proposed the free-carrier plasma effect and acousto-optic diffraction in Si. It was suggested that plasma-related electro-refraction (ER) and electro-absorption (EA) would arise from generating electrons and holes by above-gap light (optical pumping) or from carrier injection (electrical pumping). Relatively weak EA and ER from the Si Kerr and Franz-Keldysh electric-field effects were also mentioned, and tailoring of the waveguide-core bandgap energy through the use of SiGe alloys was proposed. In the 1980s, modulation via carrier accumulation and depletion were not known and it was only in 2004 that those methods were reported.

The 1986 paper cited two motivations for silicon photonics R & D that are still valid today: (1) leveraging the infrastructure of the huge, global silicon microelectronics industry in order to make highly sophisticated silicon photonic devices, and (2) integrating silicon photonics monolithically on a chip containing fast VLSI silicon electronics so as to create an OEIC. Regarding leverage, the unstated assumption was that the knowledge, experience, capital investment, manufacturing tools, and design automation developed for silicon electronics would make possible high-volume manufacture of PICs and OEICs at low cost. This high-volume focus is very strong today.

By 1993, the vision of silicon OEICs came into sharper focus as exemplified in the superchip 'thought experiments' of Abstreiter [3] and the present author [4], who viewed OEICs as extending the reach of electronic ICs by offering new functionality with high performance. As shown in Figure 1.1, integration of photonics with CMOS was proposed, as was integration with Si bipolar, BiCMOS, and SiGe/Si heterobipolar transistors. Despite the promise, little was done on actual OE integration during 1993–2003. The turning point came in 2004 when integration experiments commenced in SOI CMOS foundries due to government investment. Progress has also been slow on photonic integration with bipolar electronics. This is both a challenge and opportunity.

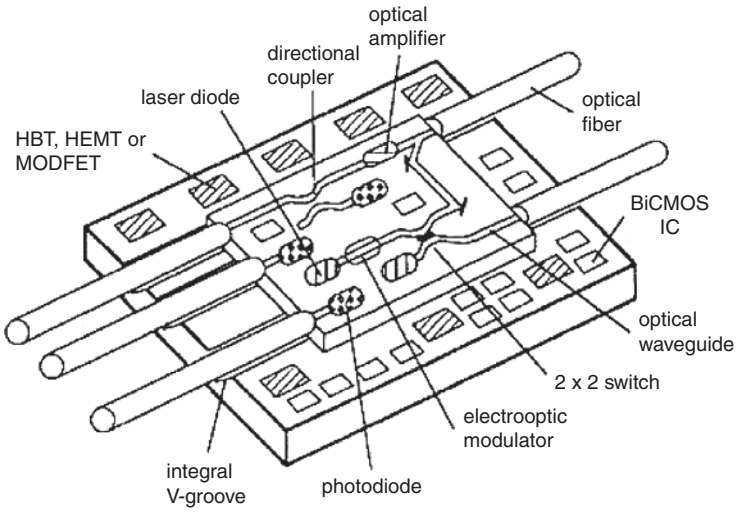

Figure 1.1 The silicon OEIC superchip as proposed in 1993 [4]

In the early years, OE integration with CMOS was felt to be important and is now viewed as supremely important. Today, CMOS captures about 90% of integrated circuit revenues, and the world-wide investment in CMOS fabrication facilities amounted to 500 billion dollars in 2005. With ingenuity, opto-electronic engineers could capture this tremendous CMOS momentum. Their hard work could spawn a huge 'CMOS photonics' industry (Luxtera's term).

For the past thirty years, Group III–V semiconductor devices have had a strong presence in photonics, and today, III–Vs are the mainstays for efficient LEDs, laser diodes, semiconductor optical amplifiers, photodetectors, electroabsorption modulators and electrooptical switches, either resonant or nonresonant. This dominance holds for the near and mid infrared. It will be difficult for silicon devices or IV–IV devices to supplant III–V devices in most of those photonic areas. In the 1980s, it was felt that devices made solely from group IV materials could not challenge the III–V dominance; however, the situation evolved during the next two decades and in 2006 it appears that IV–IVs can make real inroads into the active device scene and will eventually compete with III–Vs in some areas.

Cleverness is required to overcome the limitations imposed by the indirect bandgap of silicon Such adroitness has been the hallmark of Group IV researchers who have worked diligently towards practical LEDs, amplifiers, detectors, modulators, switches and (yes) lasers, discovering new physics in the process and/or applying known physics in novel ways. They are on the 'verge of success'. In 2006, the US Air Force Office of Scientific Research (AFOSR) launched a multi-university research initiative (MURI) to create silicon-based lasers—a project that will emphasize intrinsic approaches such as nanostructured silicon, light-from-germanium, quantum-cascade lasing and band-to-band lasing in GeSn (discussed below) as well as extrinsic approaches such as erbium-oxygen complexes in silicon.

In 1985, a 'network' made of silicon did not exist, but the component field blossomed in the ensuing 20 years. People built and tested a dozen different waveguide types (of which silicon-on-insulator is the leader) and they constructed the active devices mentioned above. They made directional couplers, optical power splitters, power combiners, TE-TM converters, TE-TM

splitters, two- and three-dimensional tapered-waveguide couplers, surface-grating couplers, echelle gratings, vertical couplers, arrayed-waveguide filters, add-drop multiplexers, resonant filters, transversal filters, variable optical attenuators, multimode to single-mode transitions, active-cladding devices, magneto-optical isolators, quantum-layered devices, self-assembled superlattices, microring resonators, slotted resonators, Si/organic composites, Si/ferroelectric composites, wavelength converters, Raman amplifiers, Raman lasers, and four-wave mixers. The goal now is to introduce standardization, to create design libraries and design tools for manufacturing the 'important set' of components—the so-called complete suite. As research goes forward, existing components become refined and new ones are invented—a virtuous cycle.

I shall close this section with a few words about OEICs that can operate in the visible and near-infrared at wavelengths shorter than the 1.2 μm indirect-bandgap wavelength of silicon. Silicon photodiodes are ideal for detecting these shorter wavelengths, and these PDs have been deployed in optical receivers which can be part of an OEIC. Although silicon waveguides are opaque over the visible and very-near IR, transmission of 0.4–1.2 μm light in 'silica-on-silica waveguides' (germania-doped-*a*-SiO_2/SiO_2/Si) and silicon-oxynitride-on SiO_2-on Si waveguides was demonstrated years ago. As to short-wavelength sources, III–V emitters are available, and even a silicon PN junction diode when reverse-biased will emit yellow light, while forward biasing of a silicon PIN diode produces 1.1 μm bandedge light. It is intriguing that a 550 nm Si P^+NN^+ avalanche emitter can be internally modulated at 10 Gb/s [5], perhaps obviating the need for lasers in short interconnects. In summary, the components needed for a short-wave OEIC are here today and there are good prospects for such a chip. In fact, we can say that the CCD and CMOS imaging chips used 'everywhere' in video cameras are one type of short-wave OEIC. It would be stretching a definition to say that an LCD display panel containing silicon thin-film transistors is an 'OEIC on glass'.

1.2 The Possibilities for OEICs

The development of OIECs is motivated by potential applications in communications (mainly optical interconnects), RF/microwave/mmw signal processing, digital signal processing, smart sensing, environmental monitoring, imaging, biomedicine, spectroscopy, lab-on-a-chip, optical logic, and transistor IC testing, among others. New 'OEIC-centric' computer architectures may include optical backplanes, optical data buses and optical clock distribution. Mario Paniccia proposed silicon micromachining (Si V- grooves, etc.) for smart OIEC packaging [6], and Cary Gunn capsulized OEIC motivation as: reduced system cost, enhanced product yields and novel system opportunities [7].

The applications are diverse, and happily there is a diversity of approaches that can be taken to implement OEICs for specific needs. The possibilities include: (1) monolithic or heterogeneous integration; (2) lasers and LEDs located on the chip or off the chip, or both on and off; (3) optical interfacing with free-space or fiber-guided lightbeams; (4) single-wavelength operation or wavelength-multiplexed operation with or without code-division multiple access; (5) operation with digital signals and/or analog signals; (6) photonic integration with CMOS or BiCMOS or SiGe CMOS or bipolar or heterobipolar; (7) use of multiple waveguiding layers or a single guide layer; (8) use of a substrate consisting of Si or SOI or strained SOI or SGOI or GOI or even SiCOI; (9) use of photonic components constructed from silicon and/or germanium and/or group IV alloys, both binary and ternary; (10) use of bulk photonic structures and/or quantum-confined structures and/or photonic-crystal structures; (11) fabrication of an

electronics layer below or above photonic layers; (12) operation at a wavelength in the visible, near IR, mid IR, long wave IR, or far IR. Let's explore these briefly.

What is monolithic and what is heterogeneous? The distinction is not entirely clear. Monolithic refers to all-silicon construction or to 'all-in-group-IV' heterostructures. III–V and II–VI devices bonded to Si exemplify heterogeneous (also known as hybrid) integration. Epitaxial III–Vs on Si 'might be' monolithic. An organic or ferroelectric cladding on a silicon waveguide is probably monolithic. Both mono- and hetero-integration are useful. Whichever is most cost-effective in a particular application is going to win. Monolithic will probably be best in the high-volume future.

Electrically pumped silicon-based lasers are the holy grail in this photonics field. But there are two issues here: demonstrating that the laser works, and showing that it can be manufactured with high yield at low cost. If not manufacturable, the glamorous device may not be widely adopted.

For the OEIC, electrically pumped and/or optically pumped lasers can be located on-chip and/or off-chip Electrical pumping on-chip would seem best, although there is a caveat here: the lasers must not consume 'too much' power, otherwise the modern VLSI chip, which is probably limited today by heat dissipation rather than transistor scaling, will tilt into a 'thermal meltdown' situation. To summarize: the useful options for future OEICs are: electrical silicon lasers on-chip, hybrid integration of electrical III–V lasers on chip, an off-chip laser that optically pumps several silicon Raman lasers on-chip, and off-chip lasers of various kinds that communicate via fiber optics with an OEIC containing no lasers.

Optical interfacing refers to the coupling of free-space or fiber-optic guided lightbeams into and out of the OEIC. Free and/or guided coupling are feasible by means of on-chip surface gratings and the tapered waveguides developed in recent years.

Digital signaling with time-division multiplexing can give high OEIC speeds; however, ultra-high data rates of, say, 50–200 Gb/s, are going to require wavelength-division multiplexing and demultiplexing in the OEIC transceiver. Code division multiple access (CDMA) is currently proposed as a useful adjunct to WDM to multiply the wavelength channel capacity. For analog situations, the broadband OEIC can perform a myriad of RF functions such as agile RF filtering. The frequency response of group IV transistors extends now into the millimeter-wave region, and Michal Shur announced emission and detection of terahertz radiation in silicon 'plasma transistors'.

The panoply of Si-based electronics now includes SiGe and SiGeC hetero bipolar transistors, SiGe BiCMOS and MOSFETs in silicon-germanium-on-insulator (SGOI). 100 Gb/s bipolar logic exists today. Although the scope of bipolar markets does not rival that of CMOS, I believe that there are application-specific niches for purely bipolar OEICs that can be exploited in the coming years. Another valuable class of OEICs will combine bipolar and CMOS electronics on-chip for mixed-signal analog-and-digital use (or all-digital application).

Presently OEICs use SOI, and there are strained-layer photonic components on the horizon to enhance OEIC capabilities. To accommodate those components, buffer layers (virtual substrates) on SOI may be required, or the OEIC could be based upon SSOI, SGOI, GOI or SiCOI.

As spelled out below, the recent advent of tin-containing alloys in group IV devices opens up possibilities for efficient monolithic lasers, LEDs, amplifiers, modulators and detectors that employ direct-bandgap valence-to-conduction transitions or intersubband transitions. It seems reasonable to speculate that Sn-alloy photonics will eventually be a major presence in OEICs.

Nanophotonics, discussed below, relies upon photonic crystals, plasmon optics, nanocrystals, carbon nanotubes, as well as alloy-based quantum wells, wires, and dots. For ULSI, there

is motivation to use photonic nanostructures in the 2010 generation of OEICs. Whether the nanostructures are truly CMOS compatible remains to be seen. That probably hinges upon the complexity of the required processing.

Described below, the multi-layer vertical three-dimensional integration of silicon waveguides and photonic devices in an OEIC is an excellent possibility currently under study. Other options are a single photonic layer above the transistors, or a subterranean photonics layer below the electronics.

The wide infrared spectrum, as mentioned below, is available for exploitation in OEICs. If and when long-wave infrared (LWIR) OEICs are implemented, they will bring new performance and economics to infrared technology.

1.3 The Present Status of OEICs

University research has consistently played a key role in silicon photonics: however, industry and governments are now spurring this field forward at an accelerated rate. An industry leader, Intel Corporation, forsees a cost-driven transition to optical interconnects in computers that could 'revolutionize future servers and enterprise networks' [6, 8, 9, 10]. Intel chose to invest in silicon photonics because they felt OEICs could alleviate electronic bottlenecks, enabling ultrafast processing in a new generation of chips-and-computers—a generation more capable and cost effective than ever before. This will be a convergence of computing and communications. 'Today, optics is a niche technology. Tomorrow, it's the mainstream of every chip we build'—(Patrick Gelsinger, Intel Sr. Vice President). Intel has already achieved excellent results in silicon photonics. Much of the Intel work is aimed toward the monolithic chip illustrated in Figure 1.2. They have the capability to fulfill that vision.

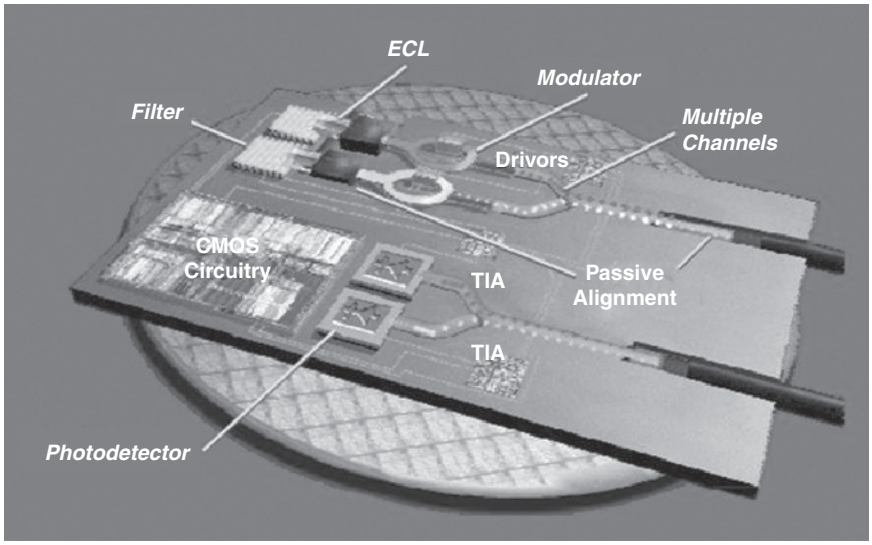

Figure 1.2 Perspective view of the future-generation monolithic silicon OEIC proposed by Intel Corporation (courtesy of Dr M. Paniccia)

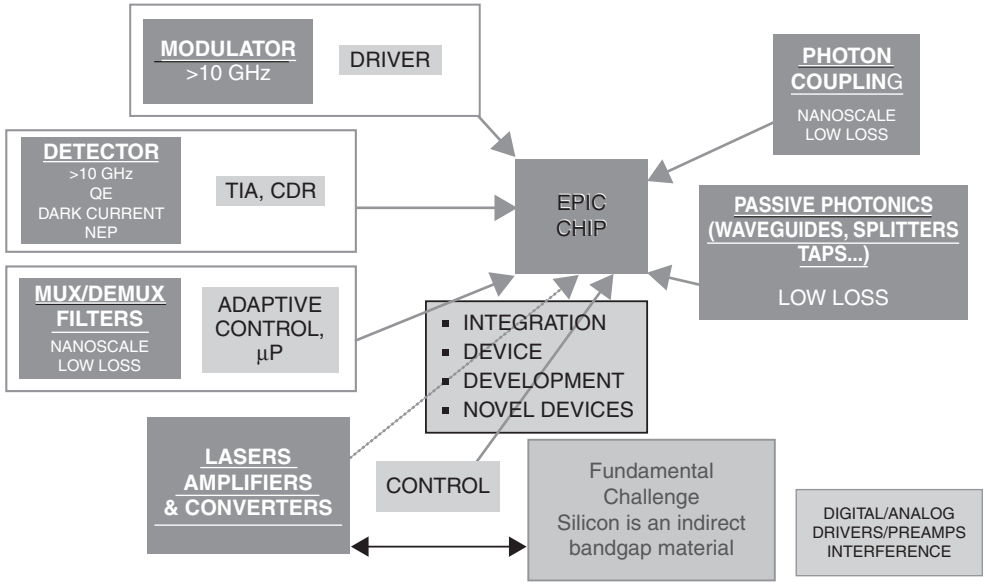

Figure 1.3 The challenge of electronic and photonic integrated circuits in silicon as envisioned on DARPA EPIC (courtesy of Dr Jag Shah)

Government agencies, especially AFOSR and DARPA, believe that highly developed Si OEICs will meet both military and commercial needs. Both organizations have invested resources to advance silicon photonics technology by sponsoring a series of research contracts. AFOSR (Dr Gernot Pomrenke) has funded small-business technology-transition research on silicon-based photonic components and is currently launching a MURI to develop silicon-based lasers. DARPA (Dr Jagdeep Shah) has selected two teams to develop OEICs in commercial state-of-the-art SOI CMOS production facilities: one team led by BAE systems, the other by Luxtera Incorporated (website: www.darpa.mil/mto/epic). The preliminary results on this four year EPIC project are quite encouraging. The reader is referred to [11–17] for more details.

The challenge of EPIC is illustrated in Figure 1.3 which shows the OE pairing envisioned for the new chip [11, 12]. A more specific EPIC goal is shown in the schematic diagram of Figure 1.4 which presents the Luxtera team's digital-signal Phase 1 OEIC fiber-optic transceiver [18–21]. Using the 130 nm Freescale production plant, the Luxtera team has created in a single layer of silicon a group of excellent components including a holographic surface-grating coupler for fibers, a carrier-depletion 10 Gb/s modulator, a trimmable three-channel demultiplexing filter and a 1×2 electrooptical switch.

For electronic warfare application, the BAE systems team is working an an analog-signal OEIC to be constructed in their rad-hard 90 nm Manassas foundry. As shown in Figure 1.5, this is a miniaturized RF-channelizer optical receiver actuated by an off-chip laser [22–23]. An incoming broadband RF signal modulates the lightbeam on-chip, and the optical filter banks pick off spectral 'slices' of the RF waveform. The inset in Figure 1.5 shows the OE layout for one slice of three in Phase I. The RF energy in each 'bin' is determined by a dedicated on-chip photodetector. BAE has already demonstrated an optical filter that has a

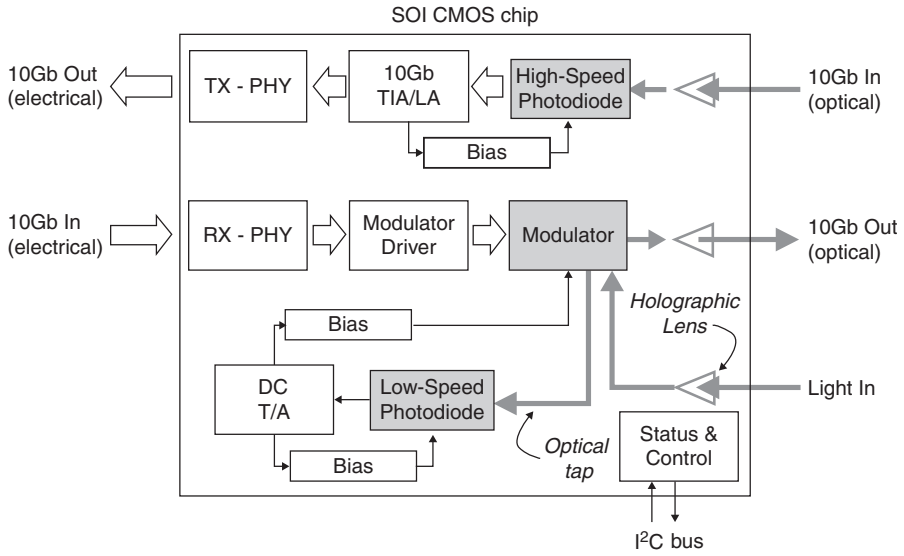

Figure 1.4 Schematic of the 10Gb/s 1.55μm silicon OEIC transceiver built by the Luxtera Inc. team for EPIC (courtesy of Dr C. Gunn)

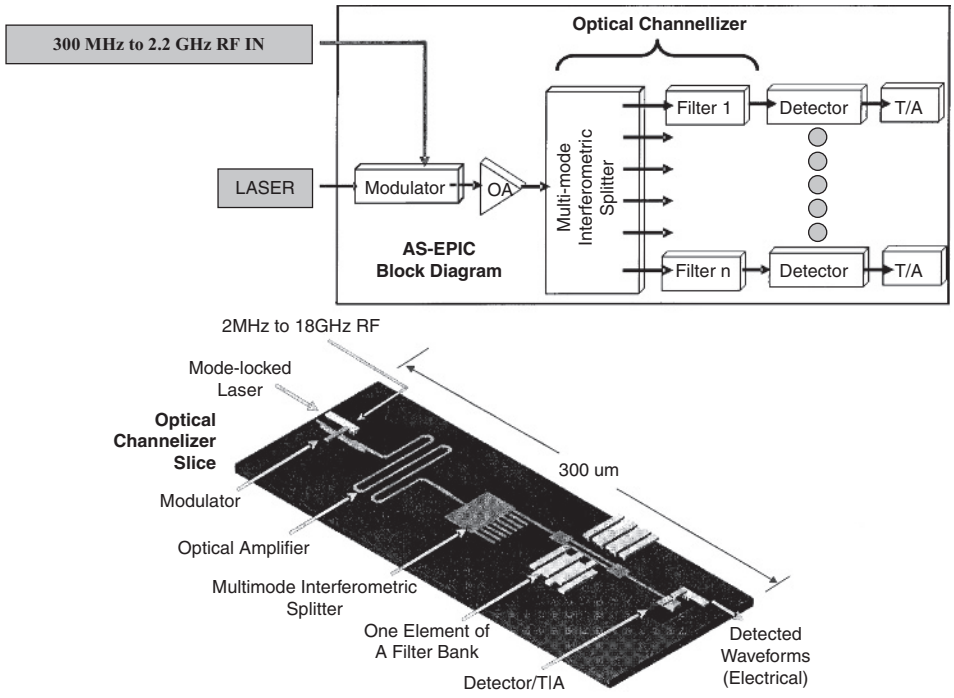

Figure 1.5 Schematic of the RF-channelizing 1.55 μm silicon OEIC receiver being built by the BAE Systems team for EPIC (courtesy of Dr M. Grove)

1 GHz electrical bandwidth (a world record), 0.35 dB/cm strip waveguides, two independent levels of Si wavguiding in a double-SOI structure, a *pin*-diode carrier-injection microring-resonator analog modulator, and a Ge-on-Si Franz-Keldysh intensity modulator. As these two projects go into Phases II and III, more sophisticated OEIC products will emerge.

1.4 Silicon-based GeSn and SiGeSn Technology

Because of the 4% lattice mismatch and thermal expansion mismatch, Ge and Ge-rich SiGe do not grow well over 'large' areas of silicon, although local-area epitaxy works well, even in Si trenches. In the past, people have grown a strain-relieved buffer of SiGe on silicon for use as a virtual substrate. This strategy can be extended to tin alloys. Since the chip of the future may contain SiGe, Ge, GeSn, SiGeSn and other column IV materials, I would rather use the term 'group IV photonics' to describe that network, rather than silicon photonics. The increased use of germanium and the advent of low-defect SiGeSn alloys are two important recent developments in group IV photonics. Currently, Arizona State University is the leader in GeSn techniques (see the references cited in [14–17]). Via low-temperature chemical-vapor deposition, a strain-relaxed buffer layer of GeSn or of SiGeSn has been grown directly upon silicon, and the layer has a relatively low defect density at its top surface, making that surface a good template for subsequent growth of coherent, strained-layer heterostructures such as Ge/GeSn multi-quantum wells (MQWs). To make thick MQWs, strain balance is employed—a new paradigm in which the wells and barriers have alternating tensile and compressive inplane strain with respect to the buffer.

The 'revolutionary' aspects are; that the QW layer in Ge/GeSn or GeSn/SiGeSn can have a direct bandgap for tin concentrations above 10%, for example, and that the QW band alignment can be Type I in the GeSn/SiGeSn system. The conduction-subband to valence-subband wavelength can be as short as 1550 nm in MQWs. More typically, in bulk heterostructures (layer thickness >10 nm), the band-to-band wavelength is in the 1.8–10 μm region. Tin-containing heterostructures can be built that mimic those in GaAs/AlGaAs, InP/InGaAsP (and related) III–V devices. The implication of the above discussion is that the group IV Ge/GeSn/SiGeSn heterodevices are (or could be) equivalent in their lasing, modulation, and detection to those of well-known III–V compound semiconductor devices. Thus, in effect, a compound semiconductor technology becomes available in group IV.

The open questions for OEICs are: whether the Sn-containing heterostructures are 'acceptable' (noncontaminating, etc) in a CMOS foundry and whether a CVD GeSn growth step can be included in the CMOS production process (as is UHV CVD SiGe). If the answer to both questions is yes, then new horizons appear in Si-based OEICs for monolithic integration of efficient sources and detectors.

1.5 OEICs for the Near, Mid and Far Infrared

In a recent paper, I identified several kinds of silicon-based waveguide structures that can, in theory, provide low-loss propagation over large portions of the wide infrared spectrum stretching beyond 1.2 μm [15]. For the near infrared, these types are silicon-on-insulator, silicon-on-sapphire and silicon-on-Si_3N_4. The near- and mid-range IR are handled by suspended silicon-membrane rib waveguides (air-clad above and below), while for mid- and

long-wave operation, the heterostructured rib of Ge-on-Si or GeSn-on-Si will do the job. To obtain coverage of the entire 1.2–100 μm wavelength spectrum, a hollow, rectangular, air-filled waveguide should work well, provided that the inner claddings are alternating layers of SiGe and Si. Proof is still needed that these structures have low loss as predicted. Assuming a favorable outcome, then I forsee that waveguided Si-based infrared networks are feasible across 1.2–100 μm.

For long-wave operation, most of the telecomm passive waveguided components can be scaled up in size from their 1.55 μm dimensions and can be fabricated with lower-resolution lithography. Narrow-gap semiconductors will serve on-chip as mid-wave/long-wave detectors and sources. Those could be monolithic GeSn/Ge structures or hybrid-integrated III–V devices. Transistor ICs can be integrated with the long-wave photonics in the same manner as for telecomm OEICs. However, the OEIC may have to be cooled when the wavelength exceeds 10 μm and the sources are on-chip. For those situations, special low-temperature transistors would be required. The inference of this discussion is that silicon-based LWIR OEICs, when properly designed, can operate anywhere within 1.2–100 μm (this is a new paradigm, awaiting demonstration). As to applications of these OEICs, some will be new and others much like known applications: free-space infrared wireless, sensor fusion, imaging and medical diagnostics, for example.

1.6 Opto-Electronic Integration with Ultimate CMOS and Post CMOS

As transistors become more nano-sized, photonic structures must shrink to 'keep pace' for OE integration. Transistor scaling has followed an electronics Moore's law with packing density doubling every 18 months. Work on nano-photonic components could, over time, produce a similar decrease in device dimensions, fulfilling a 'Moore's law for photonics', although the scaling of PICs will 'always' be behind IC scaling since the ICs 'started first'.

The semiconductor industry, currently at 130 and 90 nm Fabs, has set ambitious goals for CMOS improvements. Watkins and Bishop [24] discuss 45 nm and 'below' CMOS structures. They say that the international roadmap for silicon ULSI predicts that devices at the 45 nm node will be in production by 2010, with 32 nm devices to follow by 2013. Ultimately, CMOS is limited by quantum-confinement effects and electron tunneling through a few atomic layers of oxide. (Similarly, the minimum useable perimeter size for photonic devices is around 10 nm). CMOS represents charge-based computational electronics, and alternatives to such electronics are sought for the 2010–2020 era because CMOS will 'hit the wall' then and new types of nanoelectronic devices will be needed to fulfill the Moore's-law vision of ever-denser integration. 'Post CMOS' means that CMOS will still be ubiquitous—very much in use—but that new computing paradigms will have entered the scene. Horst Stormer points out that we shall, at the end of scaling (at the end of Moore's Law) reach the smallest silicon transistor, which will then be the standard 'brick' for all future (charge based) silicon buildings [25]. 'With the brick a commodity, it all resides with the architect (to make further progress)', and a lot of progress remains. Beyond lithography lies biology, which may mean molecular self-assembly.

1.7 Nanophotonics Integrated with Nanoelectronics

Today, we see researchers using combined microphotonic and nanophotonic techniques, with micro dominant and nano emerging strongly. Regarding micro, the passive and active versions

tend to have an elongated footprint whose length is greater than width. This differs from the 'squarish' transistor footprint. Further, the width and height of microphotonic waveguides tend to be of order λ_o/n, the wavelength in silicon—dimensions larger than transistor dimensions. However, that discrepancy does not, of itself, limit the chip-scale OE integration because, for example, the first-generation OEICs reported in 2006 [7] will contain around 50 photonic components and 100 000 transistors—implying that it is natural and acceptable to have the scale of optical integration smaller than that of electronic integration; but in the 2010 OEIC decade, nanophotonics will be the 'natural partner' of nanoelectronics.

Optical diffraction limits the mode size and device dimensions in conventional group IV waveguides; however, plasmon optics offers the chance to make devices a factor-of-ten smaller than the diffraction limit— subwavelength in size. Photonic-crystal (PhC) structures including line-defect and self-collimated waveguides also confine the infrared modal fields to deep subwavelength dimensions, and these photonic-lattice devices, together with slow-light dispersion engineering, provide electro-optical interaction lengths that are $\sim$50 $\times$ shorter than those in conventional waveguides. I imagine that group IV slow-light PhCs and plasmonics will become natural companions to nanoelectronics, allowing dense OE integration to proceed. Nanophotonics, of which photonic-crystal and plasmon-optic devices are leading contenders, requires sophisticated electromagnetic (EM) design tools to reach certain design or performance goals for OE application. Yablonovich points out that the desired design is the numerical solution of an 'inverse problem'in which one works backward from the goal [26]. A new generation of rational inverse-design algorithms and software will enable such nanophotonics.

Silicon spintronics along with plasmonics have been proposed as nano-approaches to computing for 'post-CMOS' silicon chips.. The newly formed Nanoelectronics Research Initiative (NRI) will push forward the computational power of chips. Their areas of research include phonon engineering for heat removal/diversion, directed self-assembly of nanoscale components, spintronics, plasmonics and nano modeling. Silicon spintronics would include spin transistors for logic and nonvolatile storage. Researchers from chemistry and biology will help tap into new ideas. The details of how OE integration will play out in the post-CMOS era are not clear. Conventional photonics could be used—or, one might, for example, attempt to use the same physical principles to actuate the photonics and the computing elements. That would imply a new paradigm such as opto-spintronics, a most difficult task, since silicon, without magnetic impurities, is not highly magneto-optic because its Verdet constant is relatively low. Perhaps direct-gap GeSn alloy heterostructures would be useful for spin transistors since direct-gap GaAs alloys have worked well for spin devices.

A convergence of microphotonic, photonic crystal, nanocrystal, and carbon nanotube techniques is driving the nanophotonics thrust. Plasmonics recently gained momentum due to an AFOSR MURI that was launched in 2004 (website: www.plasmonmuri.caltech.edu) Some of this work is silicon based and aimed towards CMOS compatibility. The optical mode in a silicon dielectric waveguide and the surface plasmon polariton in a plasmonic waveguide are both EM waves. That's why it is feasible to make an infrared-wave transition from the dielectric waveguide to the plasmonic waveguide, and vice versa, although phase-matching structures are needed to aid the transition. This implies that plasmonics and photonics can be monolithically integrated on silicon. Alternatively, all of the EM signal processing can be done entirely in plasmonics by utilizing a variety of plasmonic components as proposed by Brongersma [27]–an on-chip plasmonic network of the kind illustrated in Figure 1.6. The idea here is that a complete suite of active and passive plasmonic components can be interconnected on-chip.

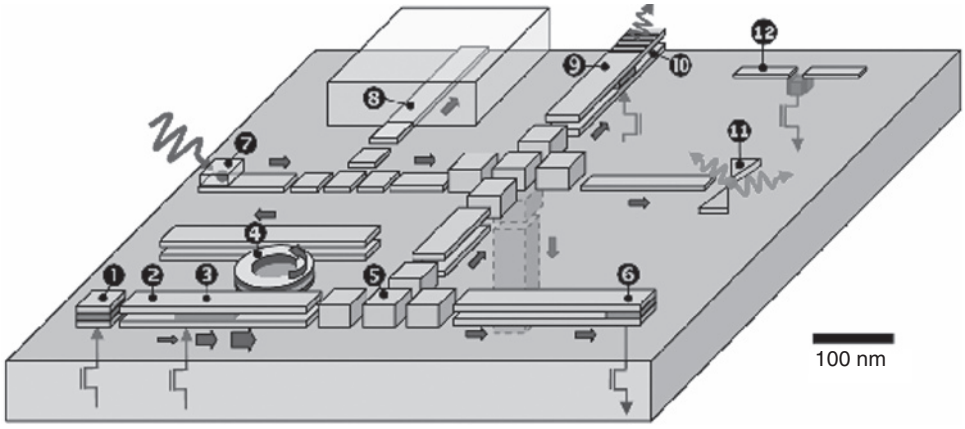

Figure 1.6 A 'futuristic' Si-based plasmonic IC chip that is proposed by the Stanford University team (courtesy of Dr M. Brongersma); transistors can be integrated here to make a PEIC

For this purely plasmonic case, the integration of transistors on the same chip would create a plasmo-electronic integrated circuit (PEIC). More likely is the combination of photonic and plasmonic components on-chip. I would call this a plasmonic-OEIC or POEIC. I suspect that plasmonics will eventually cover 1.2–100 μm.

The latest trend in plasmonic waveguides is to make strip-like composite structures consisting of a metal–insulator–metal sandwich (MIM), which could be M/Si/M. To implement such guiding, I would propose a suspended silicon membrane (such as SOI locally undercut) that could be a conventional rib guide, clad below and above by air, or the membrane could become a plasmonic guide when coated below and above by thin metal. A plasmon metal such as copper would be better than silver or gold for CMOS capatibility.

1.8 Conclusion

The era of silicon-based optoelectronic integrated circuits has just begun and will probably be long-lived. Significant OEIC progress has already been reported by teams at Intel, Luxtera and BAE Systems. Group IV nanophotonics integrated with ULSI SOI CMOS will likely dominate the OEIC field. Like computer chips, silicon OEICs do have the potential to become pervasive in everyday life. Engineers and scientists have a chance to make this potential a reality. If and when the OEIC promise is realized, it will in its course have generated a new and vigorous 'CMOS photonics industry' with considerable economic impact.

The techniques for making low-cost high-performance OEICs are varied. They include heterogeneous (hybrid) integration, and most importantly, monolithic integration. Group IV bipolar and heterobipolar electronics can contribute along with CMOS. The sources of light can be on or off the OEIC chip (or off-plus-on). Direct-gap group IV materials are becoming available. The several light beams that are processed by the OEIC chip can travel through free space, to and from the chip, or they can communicate via fiber optics linked to the chip, or they can be generated on the chip. Generally, the OEIC contains a waveguided photonic integrated circuit whose waveguides would be made of group IV semiconductor materials for wavelengths

beyond 1.2 μm. Alternatively, for transmitting visible and near IR light, the OEIC waveguides would consist of silicon oxynitride or silica. An important benefit of group IV is that the silicon OEIC can operate at a wavelength that is anywhere within the vast visible-to-terahertz spectrum that stretches from 0.4 to 150 μm.

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