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Introduction to computer relaying

1.1 Development of computer relaying

The field of computer relaying started with attempts to investigate whether power system relaying functions could be performed with a digital computer. These investigations began in the 1960s, a period during which the digital computer was slowly and systematically replacing many of the traditional tools of analytical electric power engineering. The short circuit, load flow, and stability problems – whose solution was the primary preoccupation of power system planners – had already been converted to computer programs, replacing the DC boards and the Network Analyzers. Relaying was thought to be the next promising and exciting field for computerization. It was clear from the outset that digital computers of that period could not handle the technical needs of high speed relaying functions. Nor was there any economic incentive to do so. Computers were orders of magnitude too expensive. Yet, the prospect of developing and examining relaying algorithms looked attractive to several researchers. Through such essentially academic curiosity this very fertile field was initiated. The evolution of computers over the intervening years has been so rapid that algorithmic sophistication demanded by the relaying programs has finally found a correspondence in the speed and economy of the modern microcomputer; so that at present computer relays offer the best economic and technical solution to the protection problems – in many instances the only workable solution. Indeed, we are at the start of an era in which computer relaying has become routine, and it has further influenced the development of effective tools for real-time monitoring and control of power systems.

In this chapter we will briefly review the historical developments in the field of computer relaying. We will then describe the architecture of a typical computer based relay. We will also identify the critical hardware components, and discuss the influence they have on the relaying tasks.

1.2 Historical background

One of the earliest published papers on computer relaying explored the somewhat curious idea that relaying of all the equipment in a substation would be handled by a single computer.¹ No doubt this was motivated by the fact that computers were very expensive at that time (1960s), and there could be no conceivable way in which multiple computers would be economically palatable as a substitute for conventional relays which were at least one order of magnitude less expensive than a suitable computer. In addition, the computation speed of contemporary computers was too slow to handle high speed relaying, while the power consumption of the computers was too high. In spite of these obvious shortcomings – which reflected the then current state of computer development – the reference cited above explored several protection algorithmic details thoroughly, and even today provides a good initiation to the novice in the complexities of modern relaying practices.

Several other papers were published at approximately the same time, and led to the algorithmic development for protection of high voltage transmission lines.^{2,3} It was recognized early that transmission line protection function (distance relaying in particular) – more than any other – is of greatest interest to relay engineers because of its widespread use on power systems, its relatively high cost, and its functional complexity. These early researchers began a study of distance protection algorithms which continues unabated to this day. These studies have led to important new insights into the physical nature of protection processes and the limits to which they can be pushed. It is quite possible that distance relaying implementation on computers has been mastered by most researchers by now, and that any new advances in this field are likely to come from the use of improved computer hardware to implement the well-understood distance relaying algorithms.

An entirely different approach to distance relaying has been proposed during recent years.^{4,5} It is generally based upon the utilization of traveling waves initiated by a fault to estimate the fault distance. Traveling wave relays require relatively high frequencies for sampling voltage and current input signals. Although traveling wave relays have not offered compelling advantages over other relaying principles in terms of speed and accuracy of performance, they have been applied in a few instances around the world with satisfactory performance. This technique will be covered more fully in Chapter 9; it remains for the present a somewhat infrequently used relaying application. Fault location algorithms based on traveling waves have also been developed and there are reports of good experience with these devices. These too will be covered more fully in Chapter 9.

In addition to the development of distance relaying algorithms, work was begun early on apparatus protection using the differential relaying principle.^{6–8} These early references recognize the fact that compared to the line relaying task, differential relaying algorithms are less demanding of computational power. Harmonic restraint function adds some complexity to the transformer protection problem, and problems associated with current transformer saturation or other inaccuracies continue to have

no easy solutions in computer based protection systems just as in conventional relays. Nevertheless, with the algorithmic development of distance and differential relaying principles, one could say that the ability of computer based relays to provide performance at least as good as conventional relays had been established by the early 1970s.

Very significant advances in computer hardware had taken place since those early days. The size, power consumption, and cost of computers had gone down by orders of magnitude, while simultaneously the speed of computation increased by several orders. The appearance of 16 bit (and more recently of 32 bit) microprocessors and computers based upon them made high speed computer relaying technically achievable, while at the same time cost of computer based relays began to become comparable to that of conventional relays. This trend has continued to the present day – and is bound to persist in the future – although perhaps at not quite as precipitous a rate. In fact, it appears well established by now that the most economical and technically superior way to build relay systems of the future (except possibly for some functionally simple and inexpensive relays) is with digital computers. The old idea of combining several protection functions in one hardware system¹ has also re-emerged to a certain extent – in the present day multi-function relays.

With reasonable prospects of having affordable computer relays which can be dedicated to a single protection function, attention soon turned to the opportunities offered by computer relays to integrate them into a substation-wide, perhaps even a system-wide, network using high-speed wide-band communication networks. Early papers on this subject realized several benefits that would flow from this ability of relays to communicate.^{9,10} As will be seen in Chapters 8 and 9 integrated computer systems for substations which handle relaying, monitoring, and control tasks offer novel opportunities for improving overall system performance by exchanging critical information between different devices.

1.3 Expected benefits of computer relaying

It would be well to summarize the advantages offered by computer relays, and some of the features of this technology which have required new operational considerations. Among the benefits flowing from computer relays are:

1.3.1 Cost

All other things being equal, the cost of a relay is the main consideration in its acceptability. In the early stages of computer relaying, computer relay costs were 10 to 20 times greater than the cost of conventional relays. Over the years, the cost of digital computers has steadily declined; at the same time their computational power (measured by instruction execution time and word length) has increased substantially. The cost of conventional (analog) relays has steadily increased over the same period, primarily because of some design improvements, but also because of general

inflation and a relatively low volume of production and sales. It is estimated that for equal performance the cost of the most sophisticated digital computer relays (including software costs) would be about the same as that of conventional relaying systems. Clearly there are some conventional relays – overcurrent relays are an example – which are so inexpensive that cheaper computer relays to replace them seem unlikely at present, unless they are a part of a multi-function relay. However, for major protection systems, the competitive computer relay costs have definitely become an important consideration.

1.3.2 Self-checking and reliability

A computer relay can be programmed to monitor several of its hardware and software subsystems continuously, thus detecting any malfunctions that may occur. It can be designed to fail in a safe mode – i.e. take itself out of service if a failure is detected – and send a service request alarm to the system center. This feature of computer relays is perhaps the most telling technical argument in favor of computer relaying. Misoperation of relays is not a frequent occurrence, considering the very large number of relays in existence on a power system. On the other hand, in most cases of power system catastrophic failures the immediate cause of the escalation of events that leads to the failure can be traced to relay misoperation. In some cases, it is a mis-application of a relay to the given protection task, but in a majority of cases it is due to a failure of a relay component that leads to its misoperation and the consequent power system breakdown.¹¹ It is expected that with the self-checking feature of computer based relays, the relay component failures can be detected soon after they occur, and could be repaired before they have a chance to misoperate. In this sense, although computer based relays are more complex than electromechanical or solid state relays (and hence potentially more likely to fail), as a system they have a higher rate of availability. Of course, a relay cannot detect all component failures – especially those outside the periphery of the relay system.

1.3.3 System integration and digital environment

Digital computers and digital technology have become the basis of most systems in substations. Measurements, communication, telemetry and control are all computer based functions. Many of the power transducers (current and voltage transformers) are in the process of becoming digital systems. Fiber optic links, because of their immunity to Electromagnetic Interference (EMI), are likely to become the medium of signal transmission from one point to another in a substation; it is a technology particularly suited to the digital environment. In substations of the future, computer relays will fit in very naturally. They can accept digital signals obtained from newer transducers and fiber optic channels, and become integrated with the computer based control and monitoring systems of a substation. As a matter of fact, without computer relaying, the digital transducers and fiber optic links for signal transmission would not be viable systems in the substation.

1.3.4 Functional flexibility and adaptive relaying

Since the digital computer can be programmed to perform several functions as long as it has the input and output signals needed for those functions, it is a simple matter to the relay computer to do many other substation tasks. For example, measuring and monitoring flows and voltages in transformers and transmission lines, controlling the opening and closing of circuit breakers and switches, providing backup for other devices that have failed, are all functions that can be taken over by the relay computer. The relaying function calls for intensive computational activity when a fault occurs on the system. This intense activity at best occupies the relaying computer for a very small fraction of its service life – less than a tenth of a percent. The relaying computer can thus take over these other tasks at practically no extra cost.

With the programmability and communication capability, the computer based relay offers yet another possible advantage that is not easily realizable in a conventional system. This is the ability to change relay characteristics (settings) as system conditions warrant it. More will be said about this aspect (adaptive relaying) in Chapter 10.

The high expectations for computer relaying have been mostly met in practical implementations. It is clear that most benefits of computer relaying follow from the ability of computers to communicate with various levels of a control hierarchy. The full flowering of computer relaying technology therefore has only been possible with the arrival of an extensive communication network that reaches into major substations. Preferably, the medium of communication would be fiber optic links with their superior immunity to interference, and the ability to handle high-speed high-volume data. It appears that the benefits of such a communication network would flow in many fields, and as more such links become available, the computer relays and their measurement capabilities become valuable in their own right. Where extensive communication networks are not available, many of the expected benefits of computer relaying must remain unrealized.

Other issues which are specific to computer relaying technology should also be mentioned. It has been noted that digital computer technology has advanced at a very rapid pace over the last twenty years. This implies that computer hardware has a relatively short lifespan. The hardware changes significantly every few years, and the question of maintainability of old hardware becomes crucial. The existing relays have performed well for long periods – some as long as 30 years or more. Such relays have been maintained over this period. It is difficult to envision a similar lifespan for computer based equipment. Perhaps a solution lies in the modularity of computer hardware; computers and peripherals belonging to a single family may provide a longer service life with replacements of a few modules every few years. As long as this can be accomplished without extensive changes to the relaying system, this may be an acceptable compromise for long service life. However, the implications of rapidly changing computer hardware systems are evident to manufacturers and users of this technology.

Software presents problems of its own. Computer programs for relaying applications (or critical parts of them) are usually written in lower level languages, such as assembly language. The reason for this is the need to utilize the available time after the occurrence of a fault as efficiently as possible. Relaying programs tend to be computation and input-output bound. The higher level languages tend to be inefficient for time-sensitive applications. It is possible that in time, with computer instruction times becoming faster, the higher level languages could replace much of the assembly language programming in relaying computers. The problem with machine level languages is that they are not transportable between computers of different types. Some transportability between different computer models of the same family may exist, but even here it is generally desirable to develop new software in order to take advantage of differing capabilities among the different models. Since software costs are a very significant part of computer relaying development, non-transferability of software is a significant problem.

In the early period of computer relaying development, there was some concern about the harsh environment of electric utility substations, in which the relays must function. Extremes of temperature, humidity, pollution as well as very severe EMI must be anticipated.

Another concern often raised by users of computer relays can be traced to the wide range of problems these relays can handle. It is rare to find a computer relay which does not require very large number of settings before it can be installed and commissioned. Where the organization using these devices has ample staff dedicated to working with computer relays, handling the complexity of setting these relays is not a problem. However, where the organization is small and a specialized staff for these applications cannot be justified, setting of these relays correctly and maintaining them for future modifications becomes a difficult task. Furthermore, if relays of different manufacture are in use within a single organization, it may become necessary to have experts who can deal with devices of different manufacture. Several Working Groups and Technical Committees of the Power Engineering Society of IEEE have attempted to develop a common user-interface to relays of different manufacture, but this task seems to be too complex and not much progress has been made in this direction.

1.4 Computer relay architecture

Computer relays consist of subsystems with well defined functions. Although a specific relay may be different in some of its details, these subsystems are most likely to be incorporated in its design in some form. Relay subsystems and their functions will be described next.

The block diagram in Figure 1.1 shows the principal subsystems of a computer relay. The processor is central to its organization. It is responsible for the execution of relay programs, maintenance of various timing functions, and communicating with its peripheral equipment. Several types of memories are shown in

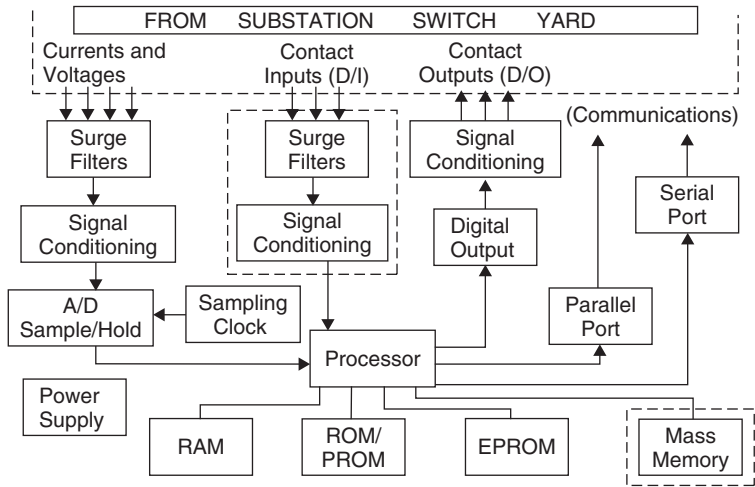


Figure 1.1 Subsystems of a relaying computer. The dashed line at the top indicates the boundary of the out-door switch yard. All other equipment is inside the control house

Figure 1.1 – each of them serves a specific need. The Random Access Memory (RAM) holds the input sample data as they are brought in and processed. It may also be used to buffer data for later storage in a more permanent medium. In addition, RAM is needed as a scratch pad to be used during relay algorithm execution. The Read Only Memory (ROM) or Programmable Read Only Memory (PROM) is used to store the programs permanently. In some cases the programs may execute directly from the ROM, if its read time is short enough. If this is not the case, the programs must be copied from the ROM into the RAM during an initialization stage, and then the real-time execution would take place from the RAM. The Erasable PROM (EPROM) is needed for storing certain parameters (such as the relay settings) which may be changed from time to time, but once set must remain fixed, even if the power supply to the computer is interrupted. Either a core type memory or an on-board battery backed RAM may be suitable for this function.

A large capacity EPROM is likely to become a desirable feature of a computer relay. Such a memory would be useful as an archival data storage medium, for storing fault related data tables, time-tagged event logs, and audit trails of interrogations and setting changes made in the relay. The main consideration here is the cost of such a memory. The memory costs have dropped sufficiently by now so that archival storage of oscillography and sequence-of-event data on a large scale within the relays has become possible.

Consider the analog input system next. At the outset it should be pointed out that Figure 1.1 is based upon using conventional transducers. If electronic CTs and CVTs are used, the input circuits may be significantly different and data are likely to be entered directly in the processor memory. The relay inputs are currents and voltages and digital signals indicating contact status. The analog signals must be

converted to voltage signals suitable for conversion to digital form. This is done by the Analog to Digital Converter (ADC). Usually the input to an ADC is restricted to a full scale value of ± 10 volts. The current and voltage signals obtained from current and voltage transformer secondary windings must be scaled accordingly. The largest possible signal levels must be anticipated, and the relation between the rms (root mean square) value of the signal and its peak must be reckoned with. It is not necessary to allow for high frequency transients in most cases, as these are removed by anti-aliasing filters which have a low cut-off frequency. An exception to this is a wave relay, which does use the high frequency (traveling wave) components. For such relays (to be discussed more fully in Chapter 9), the scaling of signals must be such that the entire input signal with its largest anticipated high frequency component must not exceed the ADC input range.

The current inputs must be converted to voltages – for example by resistive shunts. As the normal current transformer secondary currents may be as high as hundreds of amperes, shunts of resistance of a few milliohms are needed to produce the desired voltage for the ADCs. An alternative arrangement would be to use an auxiliary current transformer to reduce the current to a lower level. However, any inaccuracies in the auxiliary current transformer would contribute to the total error of the conversion process, and must be kept as low as possible. An auxiliary current transformer serves another function: that of providing electrical isolation between the main CT secondary and the computer input system. In this case, the shunt may be grounded at its midpoint in order to provide a balanced input to following amplifier and filter stages. These considerations are illustrated in Figure 1.2(a) and (b).

Figure 1.2(c) shows connections to the voltage transformer. A fused circuit is provided for each instrument or relay, and a similar circuit may be provided for the computer relay as well. The normal voltage at the secondary of a voltage transformer is 67 volts rms for a phase to neutral connection. It can be reduced to the desired level by a resistive potential divider sized to provide adequate source impedance to drive the following stages of filters and amplifiers.

Although an auxiliary voltage transformer may be used in this case to provide additional isolation, it is not a necessity. Digital inputs to the computer relay are usually contact status, obtained from other relays or subsystems from within the substation. If the other subsystems are computer based, then these signals can be input to the computer relay without any special processing. An exception to this may be an opto-isolation circuit provided to maintain isolation between the two systems. When the digital inputs are derived from contacts within the yard (or control house), it is necessary to apply surge filtering and (or) optical isolation in order to isolate the computer relay from the harsh substation environment. Surge suppression for analog and digital signals is discussed next.

Suppression of surges from wiring connected to any protection system is a specialized subject with considerable literature of its own.^{12,13} High voltage and high energy content surges are coupled into the wiring which connects current, voltage, and digital inputs to the protection system. The surges are created by faults

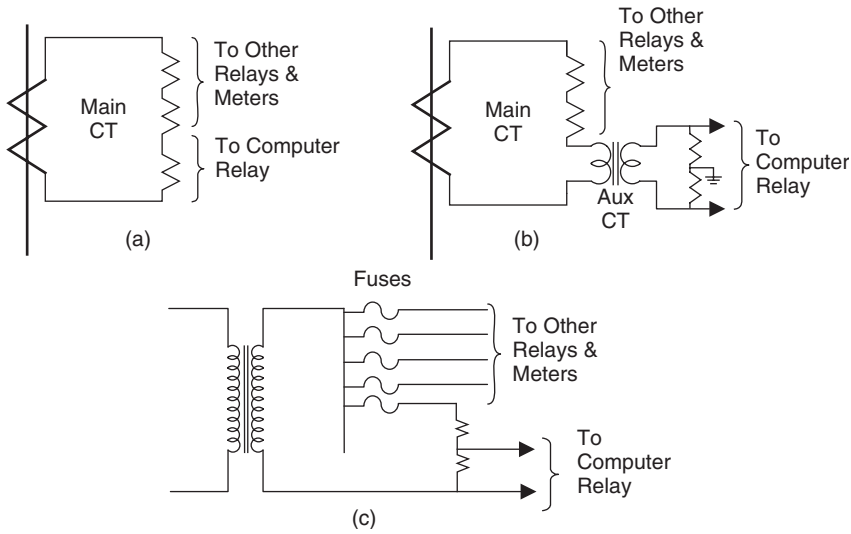


Figure 1.2 Scaling of current and voltage signals for input to the relay. (a) Direct connection in the main CT secondary. (b) Use of auxiliary CT. (c) Voltage transformer and potential divider

and switching operations on the power system, or by certain types of switching operations within the control house. For example, sparking contacts in inductive protection and control circuits within the control house have been found to be a source of very significant disturbances.¹⁴ (See Chapter 7 for additional details). Suppression of these surges requires very careful grounding and shielding of leads and equipment, as well as low-pass filtering. Nonlinear energy absorbing Metal Oxide Varistors (MOVs) may also be used. Surge suppression filters are necessary for input and output wiring, as well as for the power supply leads.¹²

The ADC and anti-aliasing filter associated with the sampling process will be considered in greater detail in Sections 1.5 and 1.6. At this stage it is sufficient to be aware of their function in the overall relaying process. The anti-aliasing filters are low-pass analog filters designed to suit a specific choice of sampling rate used. The sampling instants are determined by the sampling clock, which must produce pulses at a fixed rate. The relationship between the sampling clock and several of the measurement functions performed by a computer relay is discussed in Chapters 9 and 10. For the present, it is sufficient to understand that, at each instant defined by the clock, a conversion from the instantaneous value of an analog input signal (voltage or current) to a digital form is performed by the ADC, and made available to the processor. Since the relay in general requires several inputs, several conversions are performed at each sampling instant. It is desirable (although not essential) that all signal samples be simultaneous, which means that either the conversion and transmission to the processor of each sample be very fast, or all the signals be sampled and held at the same instant for processing by a relatively

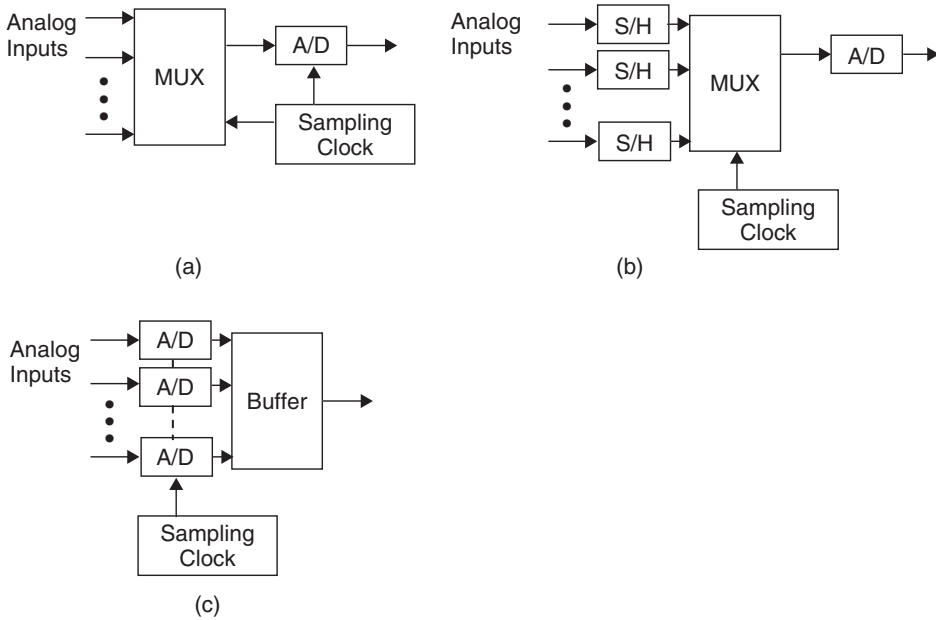


Figure 1.3 Multiple signal sampling process and its organization. (a) Single ADC with multiplexed input. (b) Sample and hold added to each channel. (c) Separate ADC for each channel

slow conversion-transmission cycle for each sample. This is typical of a multiplexed analog input system. A third option, technically feasible but expensive, is to use individual ADCs for each input channel. Trends in the ADC development and their reduced costs seem to point to the use of individual ADCs for each signal to be the preferred system. These options are illustrated in Figure 1.3.

It is well to consider this need for simultaneity in a little more detail at this point. Most relay functions require simultaneous measurement of two or more phasor quantities.

As will be seen in Chapters 3 and 8, the reference for these phasors is determined by the instant at which a sample is obtained. Thus if the phasors for signals $x(t)$ and $y(t)$ are computed from their samples beginning at instants t_x and t_y , the references for the two phasors will differ from each other by an angle θ , where

$$\theta = (t_x - t_y) \frac{2\pi}{T} \quad \text{radians}$$

where T is the fundamental frequency period of the signal. If the difference between t_x and t_y is known, then the phase angle between the two references is also known, and the two phasors could always be put on a common reference by compensating for θ . It would thus appear that simultaneous sampling of various input signals is

not necessary, as long as the difference between the two is known and compensated for. On the other hand, all computations become much simpler if θ is zero and no compensation is needed. Furthermore, when needed, the samples of different signals could be combined directly (as in the case of a differential relaying application, where all input current samples of different signals could be added directly to form samples of the differential current). To be able to combine the samples directly, it is essential that the samples be taken simultaneously – and this fact, plus the relative ease of achieving it, has led to the general practice of simultaneous sampling of all input signals by each relaying computer. Indeed, there are benefits to be gained by coherently sampling all the quantities within a station as well as at all the stations within the system. System-wide synchronization will be considered in Chapters 8, 9 and 10.

Consider the sampling scheme shown in Figure 1.3(a). In the absence of sample-and-hold circuits, the different signal samples are obtained sequentially, and are not truly simultaneous. One period of a 60 Hz wave is 16.67 milliseconds. This corresponds to about 21.6 degrees per millisecond. Thus if the entire sampling scan can be completed in about 10 microseconds, the worst error created by sequential sampling amounts to about 0.2 degree – a negligible amount of error in any relaying application. Indeed, total scan periods of about 50 microseconds could be tolerated. In fact, a tolerance of 10–50 microseconds provides a good measure for describing any data samples as being simultaneous.

It should be mentioned that if simultaneous sampling is not possible, and yet it is needed for a relaying application, one could generate approximate simultaneous samples from non-simultaneous samples. Suppose that samples $x_k = \{x_1, x_2, \dots, x_n\}$ are obtained at instants $t_k = \{t_1, t_2, \dots, t_n\}$, whereas samples at $t'_k = t_k + \Delta T$ are needed. If $x(t)$ is assumed to be suitably band-limited, x'_k can be generated by interpolation formulas. The simplest procedure would be to use linear interpolation:

$$x'_k = x_k + (x_{k+1} - x_k) \frac{\Delta T}{t_{k+1} - t_k}$$

where $k = 1, 2, \dots, n-1$ as shown in Figure 1.4. Higher order polynomials or spline functions may be used to obtain x'_k from x_k . Details may be found in any textbook on numerical methods.¹⁵ It should be remembered that, in the context of relaying applications, any but the simplest linear interpolation formula would require excessively long real-time computation.

Returning once again to Figure 1.1, digital output from the processor is used to provide relay output in the form of open or close contacts. A parallel output port of the processor provides one word (typically two bytes) for these outputs. Each bit can be used as a source for one contact. The computer output bit is a Transistor to Transistor Logic (TTL) level signal, and would be optically isolated before driving a high speed multi-contact relay, or thyristors, which in turn can be used to activate external devices such as alarms, breaker trip coils, carrier control etc.

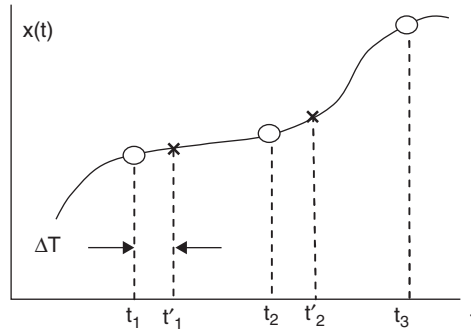


Figure 1.4 Interpolation for obtaining synchronous samples. Samples shown with x's are to be determined from samples actually obtained, which are shown by o's

Finally, the power supply is usually a single DC input multiple DC output converter powered by the station battery. The input is generally 125 volts DC, and the output could be 5 volts DC and ± 15 volts DC. Typically the 5 volt supply is needed to power the logic circuits, while the 15 volt supply is needed for the analog circuits. The station battery is of course continuously charged from the station AC service.

1.5 Analog to digital converters

The Analog to Digital Converter (ADC) converts an analog voltage level to its digital representation. The principal feature of an ADC is its word length expressed in bits. Ultimately this affects the ability of the ADC to represent the analog signal with a sufficiently detailed digital representation. Consider an ADC with 12 bit word length – which, along with the 16 bit converter – is the most common word length in commercially available ADCs of today. Using a two's complement notation, the binary number 0111 1111 1111 (7FF in hexadecimal notation) represents the largest positive number that can be represented by a 12 bit ADC, while 1000 0000 0000 (800 in hexadecimal notation) represents the smallest (negative) number. In decimal notation, hexadecimal 7FF is equal to $(2^{11} - 1) = 2047$, and hexadecimal 800 is equal to $-2^{11} = -2048$. Considering that the analog input signal may range between ± 10 volts, it is clear that each bit of the 12 bit ADC word represents $10/2048$ volts, or 4.883 millivolts. Table 1.1 shows input voltages and their corresponding converted values in two's complement and decimal equivalent for 12 and 16 bit ADCs.

The equivalent input change for one digit change in the output (4.883 millivolts in case of a 12 bit A/D converter) is an important parameter of the ADC. It describes the uncertainty in the input signal for a given digital output. Thus an output of hexadecimal 001 represents any input voltage between 2.442 and 7.352 millivolts. This is the quantization error of the ADC. In general, if the word length of the ADC

Table 1.1 Two’s complement 12 bit and 16 bit ADC input-outputs. maximum input voltage is assumed to be 10 volts

Input Volts	12 bit ADC		16 bit ADC	
	Hexadecimal	Decimal	Hexadecimal	Decimal
9.995	7FF	2047	7FFF	32767
5.0	400	1024	4000	16384
3.0	266	614	2666	9830
2.0	198	408	1999	6553
0.0	000	0	0000	0
−1.0	F33	−205	FCCB	−3277
−5.0	C00	−1024	BFFF	−16384
−10.0	800	−2048	8000	−32768

is N bits, and the maximum input voltage for the ADC is V volts, the quantization error q is given by

$$q = \frac{V}{2 \times 2^{N-1}} = 2^{-N}V$$

and normalized to the largest possible input voltage of V , the per unit quantization error is

$$\text{per unit } q = 2^{-N}$$

clearly, the larger the number of bits in a converter word, the smaller is the quantization error.

Besides the quantization error, the ADC is prone to other errors as well. In order to understand the source of these errors, it is helpful to examine the principle of operation of an ADC.

1.5.1 Successive approximation ADC

A common type of analog-to-digital converter is the successive approximation ADC. Detailed information about this type of ADC and its design can be found in the literature.¹⁶ The analog signal is amplified through an adjustable gain amplifier, as shown in Figure 1.5. A Digital to Analog Converter (DAC) converts the digital number in the output register of the ADC to an analog value. This signal is compared with the input analog signal, and the difference is used to drive up the count in the ADC output register. When the output of the DAC is within the quantization range of the analog input, the output is stable, and is the converted value of the analog signal. The amplifier is a source of additional error in the ADC. It may have a DC offset error as well as a gain error. In addition, the gain may have nonlinearity as well.

The combined effect of all ADC errors is illustrated in Figure 1.6. The offset error produces a shift in the input-output characteristic, whereas the gain error

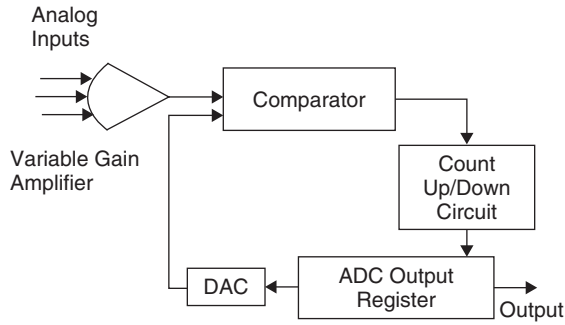


Figure 1.5 Successive approximation ADC. When the output of the comparator is positive, the ADC output register is incremented; when negative, it is decremented. When the comparator output is less than the quantization error, the output is declared valid

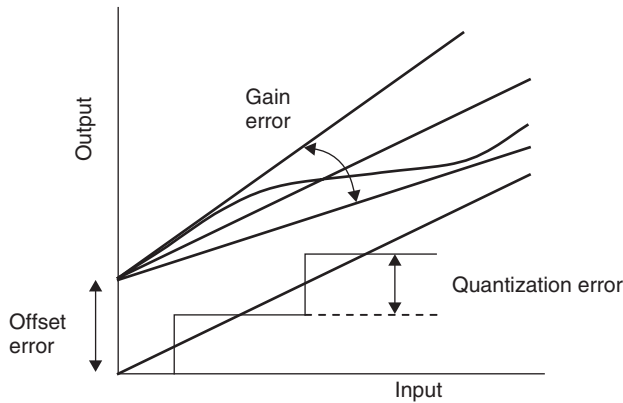


Figure 1.6 The effect of gain error, gain nonlinearity, and quantization on total error of the ADC

produces a change in the slope. The nonlinearity produces a band of uncertainty in the input-output relationship. If the gain error and the nonlinearity error are bounded by two straight lines as shown in Figure 1.6, the total error in the ADC for a given voltage input V is given by ε_v :

$$\varepsilon_v = K_1 \times FS + K_2 \times V$$

where FS is the full scale value of the input voltage, and K_1 and K_2 are constants depending upon the actual uncertainties of the conversion process.

It is possible for the gain setting to be changed between samples, although at sampling rates corresponding to relaying applications (of the order of 1 kHz), dynamic gain changing would be too time consuming. Consequently, the error model given above is fairly representative of the ADCs used in relaying applications. It should

also be clear that, when the input signal is a small fraction of the full scale value, the first error term is dominant and the error at every sample is likely to be of the same size. On the other hand, when the input signals approach the full scale, the second term may dominate and each sample error may be proportional to its nominal value.

The quantization error component of the total error is a random process, while the remaining error components are deterministic errors depending upon the gain, offset and non-linearity errors present at a given moment. If we consider the ensemble of all operating conditions under which the relay must operate, this too may be treated as a random process. The error model given for ε_v above should then be understood to represent the standard deviation σ_v of the random measurement noise. Such error models will be considered in Chapter 3.

1.5.2 Delta-sigma ADC

The Delta-Sigma analog-to-digital converter has become the ADC of choice in recent years.¹⁷ These converters use a 1 bit analog to digital converter, thus making the analog signal processing simple and inexpensive. A very high sampling rate is used (over-sampling) and the digital signal processing is used to provide appropriate anti-aliasing filters and decimation filters. The digital circuitry in these ADCs are more complex, but are relatively inexpensive to manufacture.

The block diagram of a generic delta-sigma ADC is shown in Figure 1.7(a). The signal x_1 is obtained by subtracting from the input signal x the output of the 1 bit ADC (y) converted to analog form by the 1 bit Digital-to-Analog Converter. The

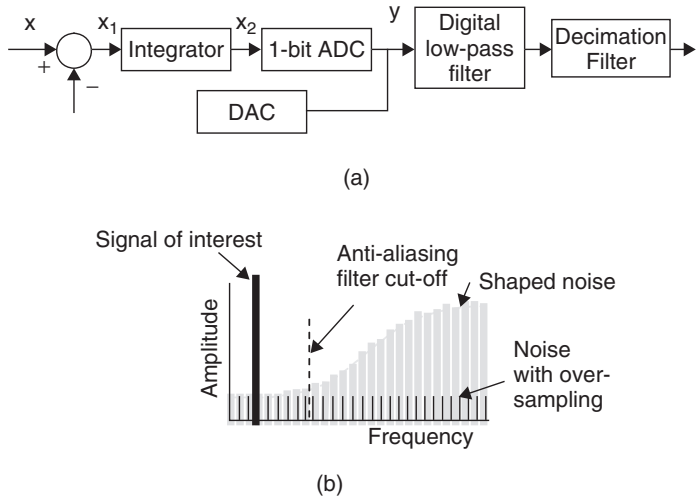


Figure 1.7 (a) Block diagram of a delta-sigma analog-to-digital converter. (b) Noise reduction in ADC output by shaping the filter characteristic

signal x_1 is integrated to produce the signal x_2 which is fed to the 1 bit ADC. The feed-back circuit ensures that the average of the analog input is equal to that of the converted signal. The output of the 1 bit ADC is a 1 bit data stream clocked at high frequency (over-sampling). A digital low-pass filter converts the 1 bit data stream to a multi-bit data stream, which is finally filtered by a decimation filter to achieve the sampling rate of interest in relaying applications. For example, with an over-sampling frequency of 40 kHz, a decimation filter output at 2 kHz could be obtained with a 16 bit resolution. The over-sampling reduces the amount of noise in the frequency band of interest, as it spreads the signal noise equally throughout the bandwidth corresponding to the over-sampling rate. A further reduction in noise in the output is achieved by shaping the digital filter characteristic so that the noise is concentrated at the high end of the spectrum, which in turn is eliminated by the anti-aliasing filter (Figure 1.7(b)).

1.6 Anti-aliasing filters

The need for anti-aliasing filters will be established in Chapter 3. For the present, we will accept that these are low-pass filters with a cut-off frequency equal to one-half the sampling rate used by the ADC. An ideal anti-aliasing filter characteristic with a cut-off frequency f_c is shown in Figure 1.8. A practical filter can only approximate this 'brick-wall' shape, as shown by the dotted line in Figure 1.8. Next, we will consider design aspects of practical anti-aliasing filters.

Anti-aliasing filters could be passive, consisting of resistors and capacitors exclusively; or active, utilizing operational amplifiers. As some buffering between the filters and the ADC is generally necessary, an operational amplifier is needed in any case, and one could use the active filter design which leads to smaller component sizes. An active filter may also be designed using the monolithic hybrid microelectronic technology providing compact packaging. The transfer function for the filter in any case is determined from considerations of sharpness of cut-off in the stop band, and the transient response of the filter.

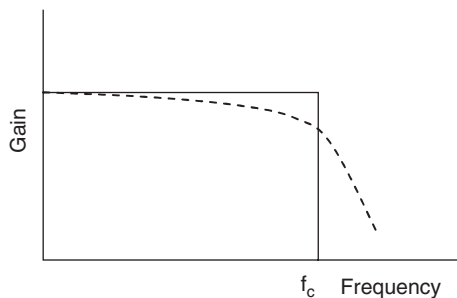


Figure 1.8 Ideal anti-aliasing filter characteristic for a cut-off frequency of f_c . Approximate realizable characteristic shown by the dotted line

In general, if filters with very sharp cut-off are employed, they produce longer time delays in their step function response.¹⁸ In most applications of computer relaying, two-stage RC filters are found to provide an acceptable compromise between sharpness of the cut-off characteristic in the stop band, and the time delay in their step input response. A second order Butterworth, Chebyshev, or maximally flat (Bessel) filter may be used to satisfy computer relaying requirements. However, these filters have a significant overshoot in their step input response. As an example, we will consider the design of a two-stage RC filter suitable for a sampling process using a sampling rate of 720 Hz (12 times the fundamental frequency for a 60 Hz power system). The filter must have a cut-off frequency of 360 Hz. We may further specify a DC gain of unity – which makes either an active or a passive design possible. An active filter can of course be designed to provide any other reasonable gain.

Two-stage RC filters are quite popular because of their simplicity, passive components, and a reasonable frequency response. They suffer from the disadvantage that they produce a rounded characteristic at the beginning of the stop band. A two-stage RC filter achieves a 12 db per octave attenuation rate when it is well into its stop band. Indeed, this is a property of an all-pole second order filter.¹⁸ The transfer function of a two-stage RC filter is given by:

$$H(j\omega) = \frac{1}{1 + j\omega(R_1C_1 + R_2C_2 + R_1C_2) - \omega^2(R_1C_1R_2C_2)}$$

R_1 , C_1 , R_2 , C_2 being the components of two stages. These components must be adjusted to provide the necessary attenuation at a desired cut-off frequency f_c . Figure 1.9(a) shows a two-stage RC circuit with this transfer function and a cut-off frequency of 360 Hz. The frequency response and step wave response of this filter are shown in Figures 1.9(b) and (c). As can be seen, the step wave response is reasonable, producing an essentially correct output in about 0.8 millisecond after application of the step wave. The phase lag at the fundamental power frequency (60 Hz) is about 11 degrees, which corresponds to a time delay of about 0.7 millisecond. Considering that this filter has been designed for a sampling frequency of 720 Hz, the phase delay produced by it is about one-half the sampling period. Recall that the sampling period at a sampling frequency of 720 Hz is 1.388 milliseconds.

Second order Chebyshev filters produce a somewhat steeper initial cut-off in their stop band. However, this is at the expense of a ripple in the pass band. The step wave response of Butterworth and Chebyshev filters is somewhat poorer, having a significant overshoot. A comparison of the frequency response and step wave response of these three second order filters with a cut-off frequency of 360 Hz is shown in Figure 1.10. Figure 1.11 shows an active realization of the two-pole Butterworth filter of Figure 1.9. Note that there are no inductors in this realization whereas a passive Butterworth filter must use inductances. This may well be one of the considerations in the final choice of active or passive filter design.

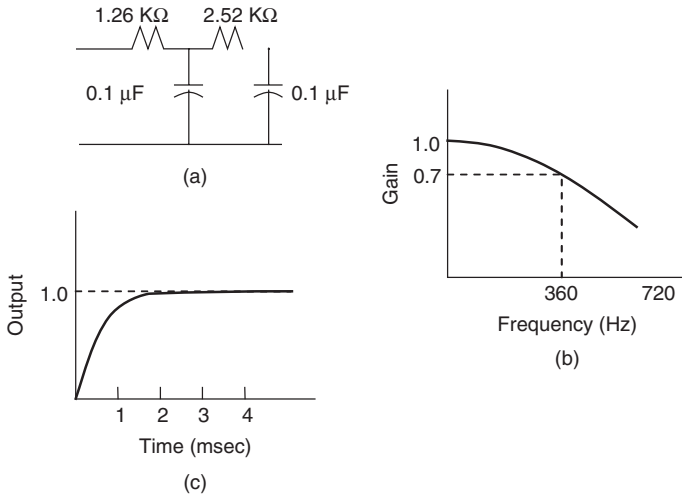


Figure 1.9 Two-stage RC filter with a cut-off frequency of 360 Hz. (a) RC ladder realization. (b) Frequency response. (c) Step wave input response

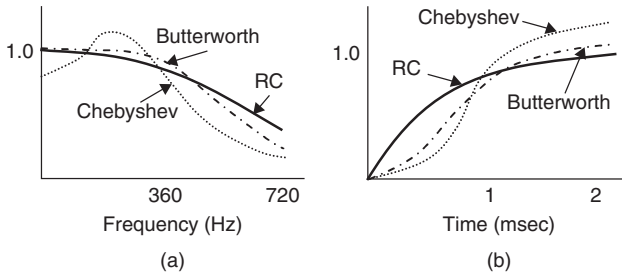


Figure 1.10 Comparison of second order RC, Butterworth, and Chebyshev filters with a cut-off frequency of 360 Hz. (a) Frequency response. (b) Step wave response

Another consideration in selecting a filter design is the stability of its transfer function in the presence of variation in component values due to aging and temperature variations. Consider the passive two-stage RC filter of Figure 1.9. Its gain and phase shift are obtained by taking the magnitude and phase angle of $H(\omega)$:

$$\begin{aligned}
 G(\omega) &\equiv |H(\omega)| \\
 &= \sqrt{\frac{1}{\{1 - \omega^2(R_1 C_1 R_2 C_2)\}^2 + \omega^2(R_1 C_1 + R_2 C_2 + R_1 C_2)}^2}} \\
 \phi(\omega) &\equiv \angle H(\omega) \\
 &= -\arctan \left[\frac{\omega(R_1 C_1 + R_2 C_2 + R_1 C_2)}{1 - \omega^2(R_1 C_1 R_2 C_2)} \right]
 \end{aligned}$$

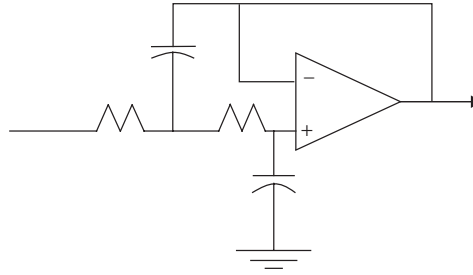


Figure 1.11 Active circuit realization of a two-pole Butterworth filter with a cut-off frequency of 360 Hz

If we consider that all four components used in the passive circuit may vary by small amounts, the variations in the gain and phase shift are given by

$$\Delta G(\omega) = \frac{\partial G}{\partial R_1} \Delta R_1 + \frac{\partial G}{\partial R_2} \Delta R_2 + \frac{\partial G}{\partial C_1} \Delta C_1 + \frac{\partial G}{\partial C_2} \Delta C_2$$

$$\Delta \phi(\omega) = \frac{\partial \phi}{\partial R_1} \Delta R_1 + \frac{\partial \phi}{\partial R_2} \Delta R_2 + \frac{\partial \phi}{\partial C_1} \Delta C_1 + \frac{\partial \phi}{\partial C_2} \Delta C_2$$

Taking the partial derivatives at the selected nominal values of R_1 , R_2 , C_1 and C_2 in Figure 1.9, we get

$$\frac{\Delta G}{G} = -0.013 \frac{\Delta R_1}{R_1} - 0.013 \frac{\Delta R_2}{R_2} - 0.004 \frac{\Delta C_1}{C_1} - 0.022 \frac{\Delta C_2}{C_2}$$

$$\frac{\Delta \phi}{\phi} = 0.493 \frac{\Delta R_1}{R_1} + 0.493 \frac{\Delta R_2}{R_2} + 0.242 \frac{\Delta C_1}{C_1} + 0.734 \frac{\Delta C_2}{C_2}$$

Often it is the relative deviation in the phase angle $\Delta \phi / \phi$ at 60 Hz due to changes in resistor and capacitor values which is of greatest concern, since this is greater in magnitude than the relative deviation in gain $\Delta G / G$. As can be seen from Problem 1.3, the gain magnitude and phase angle of an active filter are more sensitive to variations in component values as compared to those of a passive filter. Component variations can be kept small by selecting high precision metal film resistors and polystyrene or polycarbonate capacitors.

1.7 Substation computer hierarchy

Let us consider the hierarchy of various relaying and other computers in a substation. Computer relays are expected to be a part of a system wide protection and control computer hierarchy.^{19,20} Functionally the hierarchy structures that are being planned for implementation may be represented as in Figure 1.12. Relay computers and their input-output systems are at the lowest level of this hierarchy, and

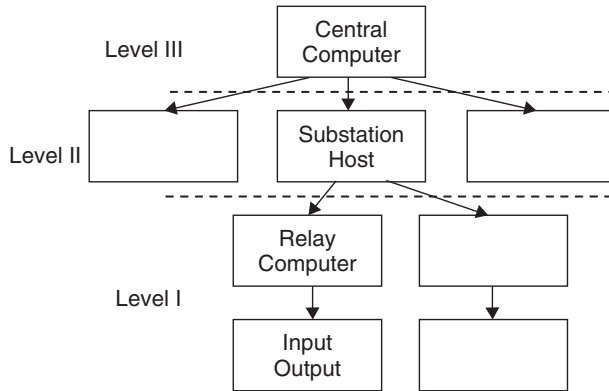


Figure 1.12 System wide hierarchical computer system. Computer relays are at the lowest level of the hierarchy. They are linked with substation host computer which in turn is linked with a system center computer

communicate with the switch yard through the relay input and output signals. As the relay outputs are connected to circuit breakers and could also be connected to remote controlled switches in the yard, the relay may serve as a conduit for supervisory control tasks at the substation. The control commands flow from the system center, through the substation host computer and to the relay computers. All the relay computers within the station are linked to the substation host computer. This host acts as a data concentrator for all historical and oscillography records collected by the relay computers. It – along with all other substation computers – transmits these data to the system central computer. The substation host computer also provides an interface between the relay computers and the station operators. Through this interface the relay settings, calibration, target interrogation, or diagnostic and maintenance functions can be performed. The substation host computer may also be used to produce some coordinated sequence-of-events for the substation as an aid to station maintenance personnel.

The role of the central computer is even less critical in the conventional relaying process. It initiates various supervisory control commands at the behest of the operator. It also collects historical data from all the substation computers and creates oscillography, coordinated sequence of event analyses, and various book-keeping functions regarding the operations performed at the station. The central computer will play a more direct role if adaptive relaying becomes accepted by the relaying community. Adaptive relaying principles and their relationship to computer relaying have been discussed in some recent publications.^{21–23}

The functions of various computers in the system wide computer hierarchy may be summarized as follows:

Level I: Relaying, input output to the switch yard, measurements, control, diagnostics, man-machine interface, communications with level II.

Level II: Man-machine interface, data acquisition and storage, sequence of events analyses and coordination, assignment for back-up in case of failures, communication with level I and level III computers.

Level III: Initiate control actions, collect and collate system wide sequence of event analyses, communication with level II, oscillography and report preparation, adaptive relaying.

1.8 Summary

In this chapter, we have traced the development of computer relaying. We have examined the motivation behind this development, and the expectations for systems of the future. Computer based relays have become the standard of the electric power industry. Their service record in field installations has been comparable to that of traditional relays, and in many respects they offer advantages which are not readily available with traditional relays. Examples of such features are adaptive relaying (to be considered in Chapter 10), oscillography records saved for post-mortem analyses, and the ability to address the relays from remote sites through available communication links. In fact, the communication capability is the single most valuable asset of computer based relays. Of course, the communication capability brings with it the concern for security from malicious intervention from unauthorized persons. As with most computer based systems, this concern can be alleviated by appropriate fire-walls and other security measures.

In this chapter we have considered in detail the functional block diagram of a computer relay and its place in the hierarchical system wide computer system. We have discussed the Analog to Digital conversion process, and the sources of errors in data conversion. We have also discussed the anti-aliasing filter design, and its contribution to the overall error in the relay input system. The Problems that follow further illustrate many of these concepts.

Problems

- 1.1 A 500 kV transmission line has a normal load current of 1000 amperes primary, and a maximum symmetrical fault current of 30 000 amperes. Determine the CT and CVT ratios and ohmic values of shunts and potential dividers in their respective secondary circuits. Assume that a full DC offset may occur in the fault current, and allow for a dynamic overvoltage of 20%. Determine the smallest load current that the input system can read if the ADC used is a 12 bit converter.
- 1.2 Consider the non-simultaneous sampling of two input signals. Assume the difference between sampling instants for the two signals to be 30% of the sampling interval. What is the error in the sample of one signal calculated to be simultaneous with the sample of the other signal using a linear interpolation formula? Assume that both input signals are of pure fundamental frequency.

Assume suitable sampling rates, and arbitrary placement of sampling instants on the waveforms.

- 1.3 A phasor is calculated from samples of an input signal taken over one period. If the samples are obtained with a 12 bit ADC, what is the error in the phasor computation due to the quantization error? Obtain the greatest upper bound for the error in magnitude and phase angle of the phasor. The phasor calculation is explained in Chapter 3. For the present, assume that the phasor is the same as the fundamental frequency component calculated by the familiar Fourier series formula.
- 1.4 Repeat Problem 1.3 for the errors introduced by an imperfect input amplifier having an offset error, a gain error, and gain nonlinearity. Assume suitable bounds for these errors.
- 1.5 Design a third order Butterworth filter with a cut-off frequency of 360 Hz. Plot its transient response to a step input function. Also plot its frequency response for a frequency range of DC to 720 Hz.
- 1.6 Design a two-stage RC filter with a cut-off frequency of 300 Hz, and compare its frequency and step input response with those of the two-stage RC filter having a cut-off frequency of 360 Hz. Often a 300 Hz cut-off frequency filter may be used for anti-aliasing purposes where sampling frequency is 720 Hz. This gives better noise immunity to the filter, but it is of course not suitable when it is necessary to calculate the fifth harmonic of the input signal – for example, in a transformer relay.
- 1.7 Complete the design of the second order Butterworth filter by finding the values of the components in Figure 1.10.
- 1.8 Verify the expressions for the relative gain and phase angle variations $\Delta G/G$ and $\Delta \phi/\phi$ given in Section 1.6 for the two-stage RC filter. Determine a general formula, and then substitute the values of the resistors and capacitors from Figure 1.8(a).
- 1.9 Derive expressions similar to those in Problem 1.8 for the two-stage Butterworth filter, and obtain numerical results for the filter design of Problem 1.5. Verify that, for the same relative variation in component values, the Butterworth filter has greater variation in its gain and phase shift when compared to the two-stage RC filter.

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