PART I

INDIVIDUAL *RF* BLOCKS

CHAPTER 1

LNA (LOW NOISE AMPLIFIER)

1.1 INTRODUCTION

In a wireless communication system, the *LNA* is the first circuit block in the receiver. It is one of most important blocks because:

- The sensitivity of the receiver is mainly determined by the *LNA* noise figure and power gain. The noise figure of the *LNA* significantly impacts the overall noise performance of the receiver. On the other hand, the power gain of the *LNA* significantly suppresses noise contributions from subsequent stages, so that it as well impacts the overall noise performance of the receiver.
- The *LNA* plays an important role in the linearity of the entire system. Its nonlinearity must be reduced as much as possible.
- In a *CDMA* (Code Division Multiplex Access) wireless communication system, the *LNA* takes care of *AGC* (Automatic Gain Control) in the entire system as well.

This chapter covers

- Typical design procedures including selection of device size, raw device testing, input and output impedance matching, stability checking, and linearity examination and improvement. This has been important subject since the advent of more advanced wireless communication systems such as 64 *QAM*.
- Cascode *LNA*. As the wireless bandwidth is raised up to *GHz* or tens of *GHz*, the performance of the *LNA* is restricted by the input Miller capacitance. Increasing the isolation between the input and output in a *LNA* would be helpful to an advanced communication system. The cascode *LNA* would improve the performance from single-ended *LNA*.

RF Circuit Design, by Richard Chi-Hsi Li

- *AGC* (Automatic Gain Control). Without *AGC* capability, it is impossible for the wireless *CDMA* communication system to operate well.

In recent years, the differential *LNA* is specially required for the direct conversion or "zero *IF*" wireless communication system. This will be discussed in Chapter 3, where the differential pair discussed applies not only to the differential *LNA* but also to other *RF* circuit blocks.

The *LNA* has been developed over several decades. However, as the progress of electronic products moved forward, *LNA* design was required to reach higher and higher goals. For example, the voltage of *DC* power supply became lower and lower, from $3V$ to $1V$ in a cellular phone design. The current drain had to be reduced as much as possible so that the standby current of the overall receiver could be just a few mA to conserve battery consumption. It must be small and the cost must be low, and the performance must be maintained at a high level. *LNA* design becomes more complicated if trade-offs must be made between size, cost, and performance.

It is well known that the *LNA* must magnify the weak signal from the antenna and intensify it up to the power level required by subsequent stages. This implies that a *LNA* must have

- A low noise block so that the weak signal will not be "submerged" by noise;
- A high power gain block so that its output can drive the following stage well.

A *LNA* with maximum gain may not be in the state of minimum noise, or vice versa. A trade-off is usually made between maximizing gain and minimizing the noise figure. In past decades, much effort has been put into designing a *LNA* to reach both maximum gain and minimum noise figure simultaneously. This is a great challenge in *LNA* circuit design. This dilemma was solved more than 10 years ago in my designs but has not been previously published. Now I am going to share it with my readers.

1.2 SINGLE-ENDED SINGLE DEVICE *LNA*

In this section, the design procedures and schemes will be illustrated through a design example, in which a *MOSFET* transistor is selected as the single-ended device (it can of course be replaced by other types of devices).

A single-end *LNA* with a single device is the simplest low noise amplifier. Nevertheless, it is the essence or core in all other types of *LNA* designs, including cascode and differential designs. The design procedures and schemes described in this section are suitable to all types of *LNA* design.

The main goals for the design example are

- $V_{cc} = 3.0\,V$,
- $I_{cc} < 3.0\,mA$,
- frequency range = 850 to $940\,MHz$,
- $NF < 2.5\,dB$,
- gain $> 10\,dB$,

- $IP_3 > 0\,dBm$,
- $IP_2 > 40\,dBm$.

1.2.1 Size of Device

The first step in *LNA* circuit design is to decide the size of the device. Many trade-offs must be taken into account between size, cost, performance, and so on. In this sub-section, only performance is counted in the selection of device size.

In digital *IC* circuit design, the *MOSFET* transistor has become dominant in recent years because the size of the device can be shrunk and the current drain can be reduced more than with other devices. Among *MOSFET* transistors, device length therefore becomes the key parameter in the selection of *IC* foundry and processing because it strongly impacts the total area of the *IC* die and therefore the cost, speed of performance, maximum data rate, current drain, and so on. The reason is simple: In digital *IC* circuit design, hundreds and even thousands of transistors are needed. The total area of the *IC* die, and therefore the cost, is significantly reduced as the device length decreases. *IC* scientists and engineers have worked very hard to shrink the size of transistors, which now approach unbelievably tiny sizes. In the 1990s, the length of a *MOSFET* device was in the order of μm; from 2000 to 2005 and the *IC* world entered the so-called "nanometers" era. Many foundries today have the capability to manufacture *MOSFET IC*s with lengths of 0.5, 0.35, 0.25, 0.18, $0.11\,\mu m$. In 2006, the length of a *MOSFET* device was further shrunk to 90, 45, $22.5\,nm$. The progress of *IC* processing is moving forward very fast, and, consequently, *IC* circuit design work becomes more and more challenging.

In the *RF* circuit design, bipolar transistors were applied to *RFIC* development in the 1990s. Meanwhile, the *MOSFET* device has been applied to the *RFIC* as well. The smaller size of *MOSFET* devices brings about the same advantages to *RF* circuit design as to digital circuit design, such as the reduction of cost and the increase in operating frequencies. It must be pointed out, however, that smaller size is not the main objective pursued in *RF* circuit design because the total number of devices applied in *RF* circuits is much smaller than the number of devices applied in digital circuits. Instead of pursuing smaller size, *RF* engineers prefer to select device lengths for which the technology of *IC* processing in the foundry is more advanced and the device model for simulation is more accurate. In addition, there are two important factors to be considered in the selection of the *MOSFET* device's size: the restriction of the device size due to the V_{gs} limitation and another due to the expectations of NF_{min}.

1.2.1.1 Restrictions of W/L *Due to Consideration of* V_{gs}

In *LNA* design, the *MOSFET* transistor is usually operated in its active region. Its *DC* characteristics can be expressed as:

$$I_d = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{gs} - V_{th})^2, \tag{1.1}$$

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th}), \tag{1.2}$$

where

I_d = drain current,
g_m = transconductance of *MOSFET* transistor,
W = width of *MOSFET* transistor,
L = length of *MOSFET* transistor,
V_{gs} = gate-source voltage for n channel *MOSFET*,
V_{th} = threshold voltage for n channel *MOSFET*, the minimum gate-to-source voltage needed to produce an inversion layer beneath the gate,
V_{ds} = drain-source voltage for *n* channel *MOSFET*,
μ_n = channel mobility, typically $700\,cm^2/V\text{-}sec$,
C_{ox} = capacitance per unit area of the gate oxide,

and

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}, \tag{1.3}$$

where

t_{ox} = thickness of the gate oxide.

From (1.1) and (1.2) we have

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_d}\,. \tag{1.4}$$

$$V_{gs} = 2\frac{I_d}{g_m} + V_{th}. \tag{1.5}$$

Equation (1.4) shows that g_m is related to the ratio W/L. The increase of the ratio W/L is equal to the increase of g_m. On the other hand, from equation (1.5), it can be seen that there are two ways to make I_d reach a certain amount, either by increasing g_m through the increase of the ratio W/L for a given V_{gs} or by increasing V_{gs} through the factor of $(V_{gs}\text{-}V_{th})$. Should the selected value of the ratio W/L be too small, V_{gs} must be increased to an unacceptable value for a given I_d.

In order to illustrate the relationships between g_m, I_d, W/L and the corresponding values of V_{gs}, Table 1.1 lists the calculated V_{gs} values when I_d and the ratio W/L are selected in different levels or amounts and when the basic parameters applied in the calculations are assumed as follows:

$$\varepsilon_{ox} = 3.45\times10^{-13}\ F/cm, \tag{1.6}$$

$$t_{ox} = 23.3\ A^{\circ} = 23.3\times10^{-8}\ cm, \tag{1.7}$$

$$\mu_n = 170\ \ cm^2/V\text{-}sec, \tag{1.8}$$

$$C_{ox} = 14.81\ fF/\mu^2, \tag{1.9}$$

$$V_{tn} = 0.49\,V, \tag{1.10}$$

TABLE 1.1 V_{gs} **limitation in the selection of device size**

I_d **(mA)**	W (μm)	L (μm)	**W/L**	g_m **(mA/V)**	V_{gs} (V)
1.00	0.9	0.09	**10.00**	**2.24**	**1.38**
1.00	9	0.09	**100.00**	**7.10**	**0.77**
1.00	90	0.09	**1000.00**	**22.44**	**0.58**
1.00	180	0.09	**2000.00**	**31.73**	**0.55**
1.00	450	0.09	**5000.00**	**50.17**	**0.53**
1.00	900	0.09	**10000.00**	**70.95**	**0.52**
1.00	1800	0.09	**20000.00**	**100.34**	**0.51**
2.00	0.9	0.09	**10.00**	**3.17**	**1.75**
2.00	9	0.09	**100.00**	**10.03**	**0.89**
2.00	90	0.09	**1000.00**	**31.73**	**0.62**
2.00	180	0.09	**2000.00**	**47.79**	**0.58**
2.00	450	0.09	**5000.00**	**70.95**	**0.55**
2.00	900	0.09	**10000.00**	**100.34**	**0.53**
2.00	1800	0.09	**20000.00**	**141.91**	**0.52**
5.00	0.9	0.09	**10.00**	**5.02**	**2.48**
5.00	9	0.09	**100.00**	**15.87**	**1.12**
5.00	90	0.09	**1000.00**	**50.17**	**0.69**
5.00	180	0.09	**2000.00**	**75.56**	**0.63**
5.00	450	0.09	**5000.00**	**11.19**	**0.58**
5.00	900	0.09	**10000.00**	**158.66**	**0.55**
5.00	1800	0.09	**20000.00**	**224.37**	**0.53**
10.00	0.9	0.09	**10.00**	**7.10**	**3.31**
10.00	9	0.09	**100.00**	**22.44**	**1.38**
10.00	90	0.09	**1000.00**	**70.95**	**0.77**
10.00	180	0.09	**2000.00**	**106.86**	**0.69**
10.00	450	0.09	**5000.00**	**158.66**	**0.62**
10.00	900	0.09	**10000.00**	**224.37**	**0.58**
10.00	1800	0.09	**20000.00**	**317.31**	**0.55**
20.00	0.9	0.09	**10.00**	**10.03**	**4.48**
20.00	9	0.09	**100.00**	**31.73**	**1.75**
20.00	90	0.09	**1000.00**	**100.34**	**0.89**
20.00	180	0.09	**2000.00**	**151.13**	**0.77**
20.00	450	0.09	**5000.00**	**224.37**	**0.67**
20.00	900	0.09	**10000.00**	**317.31**	**0.62**
20.00	1800	0.09	**20000.00**	**448.75**	**0.58**
50.00	0.9	0.09	**10.00**	**15.87**	**6.79**
50.00	9	0.09	**100.00**	**50.17**	**2.48**
50.00	90	0.09	**1000.00**	**158.66**	**1.12**
50.00	180	0.09	**2000.00**	**238.95**	**0.94**
50.00	450	0.09	**5000.00**	**354.77**	**0.77**
50.00	900	0.09	**10000.00**	**501.71**	**0.69**
50.00	1800	0.09	**20000.00**	**709.53**	**0.63**

then

$$\mu_n C_{ox} = 251.72\ \mu A/V^2. \tag{1.11}$$

In Table 1.1, the calculations are conducted for the cases of $I_d = 1, 2, 5, 10, 20$, and $50\,mA$ with the different levels of $W/L = 10, 100, 1000, 2000, 5000, 10\,000$, and $20\,000$.

The underlined values of V_{gs} in the rightmost column in Table 1.1 are unacceptable because they are higher than $0.7V$, which is considered the highest acceptable value of V_{gs} when the DC power supply is low, say, 1.0 to $1.8\,V$. Therefore, the rows containing underlined values of V_{gs} in Table 1.1 must be abandoned in the selection of the ratio W/L. Hence, the values of the ratio W/L are restricted for the given values of I_d and g_m due to the constraint on V_{gs}. All other rows and their candidates in Table 1.1 are acceptable. They will be further narrowed down in consideration of the so-called "power-constrained noise optimization."

It should be noted that Table 1.1 is an example only. The selection of the ratio W/L for the device must be conducted by designers based on the basic parameters, ε_{ox}, t_{ox}, μ_n, C_{ox}, and V_{tn}, which actually apply to the device.

1.2.1.2 Optimum Width W_{opt} of Device

Based on the theoretical derivation (Lee, 1998, pp. 230–232), the size selected for the device in *LNA* design is more reasonably considered from the expectation of a minimum of noise. By explicitly taking power consumption into account, the optimum width of a device W_{opt} for the minimum noise figure NF_{min} can be expressed as

$$W_{opt} = \frac{1}{3\omega L C_{ox} R_S}, \tag{1.12}$$

where

W_{opt} = optimum width of device (*MOSFET* transistor),
ω = operation angular frequency,
L = length of device (*MOSFET* transistor),
C_{ox} = capacitance per unit area of the gate oxide,
R_S = source resistance.

This results from the power-constrained noise optimization.

The value of the optimized width of the device is inversely proportional to the operating frequency, ω, the source resistance, R_S, the capacitance of the gate oxide area, C_{ox}, and the length of the device, L. The designer knows the first two parameters, ω and R_S. The other two, C_{ox} and L, are provided by the *IC* foundry, which may have a couple choices. For instance, device lengths of 0.25, 0.18, 0.13, 0.11, and $0.09\,\mu m$, are available in most *MOS IC* foundries at present. Based on the data that the *IC* foundry provides, the corresponding values of W_{opt} can be calculated from equation (1.12). Then, these W_{opt} and L values can be examined for a reasonable value of V_{gs} as in Table 1.1 and the best set of W_{opt} and L can be determined. Then, the final decision of *IC* processing can be made.

1.2.2 Raw Device Setup and Testing

Raw device testing is the second step in the block circuit design. It should be noted that it is a key step in a good LNA circuit design.

In the circuit design, a "device" is a general name for a transistor. The transistor can be bipolar, or a *MOSFET*, or GaAs, or some other type. The purpose of raw

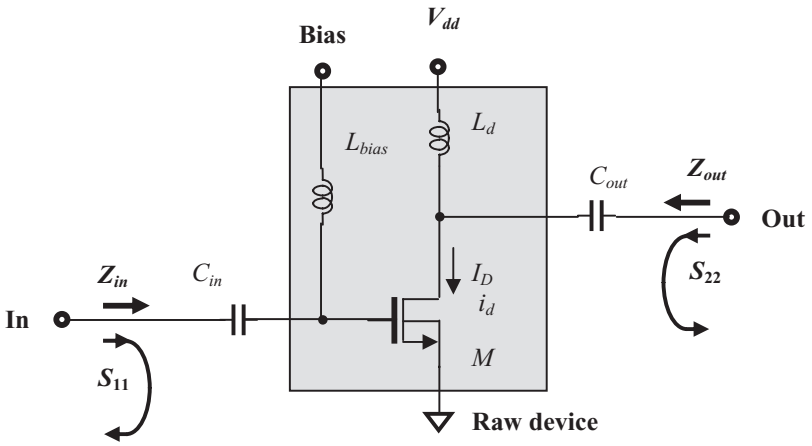


Figure 1.1 Setup for raw device testing, f = 850 to 940 MHz, $I_D = 2.6\,mA$$C_{in}$, C_{out}: "zero" capacitor; L_{bias}, L_c, L_d: "infinite" inductor.

device testing is to determine the operating characteristics only of the device, and nothing else. However, an operating transistor must be provided with the *DC* power supply and bias, and therefore, some additional parts such as the *RF* choke and *DC* blocking or *AC* by-pass capacitors must be connected. The impedance of the additional parts must therefore approach either zero when they are connected in series, or infinity when they are connected in parallel. If so, the tested characteristics of the transistor are not disturbed by the addition of those parts.

Figure 1.1 shows the setup for raw device testing. The capacitors C_{in} and C_{out} are "zero" capacitors, while the inductors L_{bias} and L_d are "infinite" inductors. They are discussed in Chapter 14 where the "zero" capacitor and "infinite" inductor are selected from discrete chip parts. In the actual simulation for *IC* circuitry, the capacitors C_{in} and C_{out} can be large capacitors with a high value of capacitance so that their impedance approaches zero at operating frequencies, while the inductors L_{bias} and L_d can be a large inductors with a high value of inductance so that their impedance approaches infinity at operating frequencies. The desired current drain of the transistor, $I_D + i_d$, can be adjusted by the bias voltage, where I_D is the *DC* current drain portion and i_d is the *AC* current drain portion of the *MOSFET* transistor.

In Figure 1.1, the device is a *MOSFET* transistor with *CMOS IC* processing. Its size has been selected based on the considerations of V_{gs} and NF_{min} as discussed in the previous section. As mentioned above, the *DC* power supply is $3V$ and the drain current, adjusted by the bias, is $2.6\,mA$.

The operating frequency range is from 850 to 940 MHz. Its relative bandwidth is

$$\frac{\Delta f}{f_o} = \frac{940 - 850}{(940 + 850)/2} = 10.05\%. \tag{1.13}$$

This is a narrow-band block. Usually, a block or a system with a relative bandwidth greater than 15% is considered a wide-band block or system. A block or a system

with a relative bandwidth less than 15% is considered a narrow-band block or system.

The purpose of raw device testing is twofold:

1) To create a starting point for impedance matching in order to continue the next design step.
2) To see if the raw device can approach a good *LNA* design. A good *LNA* design suggests that a minimum of noise and a maximum of gain can be obtained simultaneously.

It is easy to understand that the first purpose of raw device testing is to create a starting point for matching input and output impedance. The input and output impedances, Z_{in} and Z_{out}, are approximately related to the S parameters by the following equations:

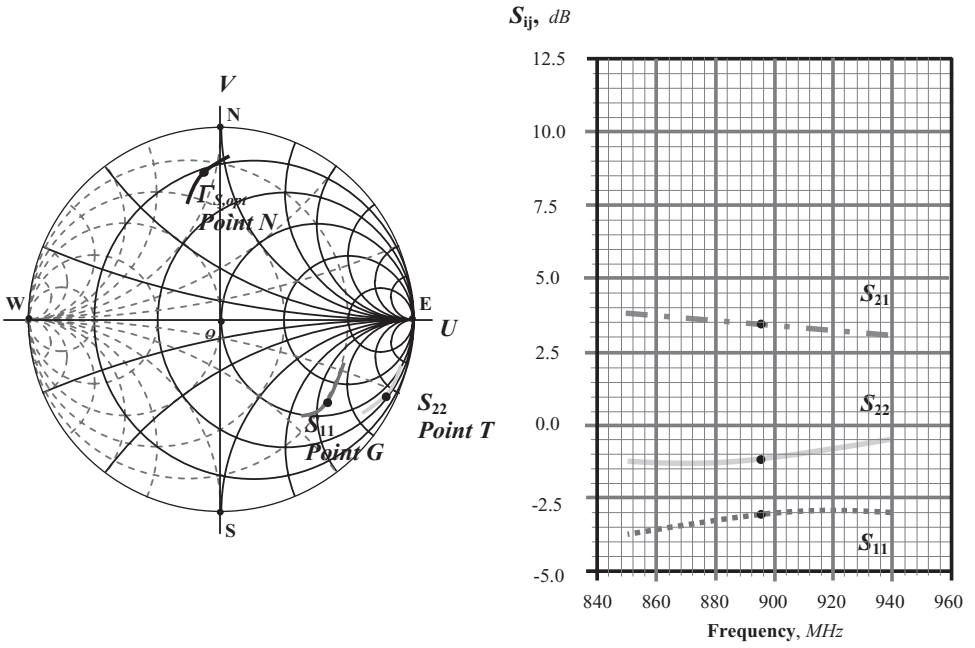
$$Z_{in} = \frac{1+S_{11}}{1-S_{11}}, \tag{1.14}$$

$$Z_{out} = \frac{1+S_{22}}{1-S_{22}}. \tag{1.15}$$

This approximation is usually correct if the transistor's isolation between input and output is good and the testing calibration is well done. Through the testing of S_{11} and S_{22}, the input and output impedances, Z_{in} and Z_{out}, can be read directly from the Smith chart at the same locations of S_{11} and S_{22}, respectively.

Figure 1.2(a) shows the test results of S_{11} and S_{22}, and hence Z_{in} and Z_{out} on the Smith chart. The input and output impedances of a *MOSFET* transistor are usually capacitive and are located in the bottom half of the Smith chart, while the input and output impedances of a bipolar transistor can be either capacitive or inductive, depending on the device size, current drain, and operating frequency. Another difference between the *MOSFET* and the bipolar transistor is that the input and output impedances of a *MOSFET* transistor are usually located in the relatively higher impedance area, while the input and output impedances of a bipolar transistor are usually located in the relatively lower impedance area. This difference implies that impedance matching is more difficult for the *MOSFET* than for the bipolar transistor, and that the isolation between input and output in the *MOSFET* is better than in the bipolar transistor.

Figure 1.2(a) also shows that the location of S_{22} is much farther from $50\,\Omega$ and is in the very high impedance area, while S_{11} is located somewhat closer to $50\,\Omega$ than S_{22}. Correspondingly, Figure 1.2(b) shows that the magnitude of S_{22} is almost close to $-1\,dB$, of S_{11} around $-3\,dB$, and of S_{21} around $3.5\,dB$, which is much lower than expected. We do not mind S_{21} too much because it is tested under an unmatched case. The magnitude of S_{12} is usually around -20 to $-30\,dB$ and therefore disappears from the plot. Likewise, we do not mind S_{12} too much because the isolation in today's devices is usually sufficient unless a feedback circuit is added. A remarkable feature shown in Figure 1.2 is that the frequency response for all the S parameters is flattened, so that one does not need to worry about bandwidth at this point.



(a) S_{11}, S_{22} and $\Gamma_{S,opt}$ on Smith chart (b) Magnitude of S_{ij}, *dB*

Figure 1.2 *S* parameters from raw device testing, f = 850 to 940 MHz, I_D = 2.6 mA. (The intermediate frequency 895 MHz is marked with a dot on each trace.)

The second purpose of raw device testing is to examine the performance of the noise figure.

Based on Haus's theory (1960), the noise figure of a noisy block can be expressed by

$$NF = NF_{\min} + \frac{R_n}{G_s}\left[(G_S - G_{S,opt})^2 + (B_S - B_{S,opt})^2\right]. \tag{1.16}$$

where

NF = noise figure of noisy block,
NF_{min} = minimum of noise figure of noisy block,
R_n = equivalent noise resistance,
Y_S = admittance of input source,
G_S = conductance of input source,
B_S = subceptance of input source,
$Y_{S,opt}$ = optimum admitttance of input source,
$G_{S,opt}$ = optimum conductance of input source,
$B_{S,opt}$ = optimum subceptance of input source.

The noisy two-port block can reach a minimum of noise figure

$$NF = NF_{\min}, \tag{1.17}$$

when

$$G_S = G_{S,opt}, \tag{1.18}$$

$$B_S = B_{S,opt}. \tag{1.19}$$

Equations (1.18) and (1.19) can be written together, that is

$$Y_S = Y_{S,opt}, \tag{1.20}$$

where

$$Y_s = G_s + jB_s \tag{1.21}$$

$$Y_{S,opt} = G_{S,opt} + jB_{S,opt} \tag{1.22}$$

On the Smith chart, the optimum condition (1.20) is usually labeled by the corresponding reflection coefficient, $\Gamma_{\text{S,opt}}$, corresponding to $Y_{S,opt} = G_{S,opt} + \text{j}\ B_{S,opt}$,

$$\Gamma_S = \Gamma_{S,opt}. \tag{1.23}$$

Of course, $\Gamma_{\text{S,opt}}$ is a complicated function mainly determined by the type, size, and trans-conductance of the raw device. It has been formularized in some technical books. Usually, an optimum source reflection coefficient, $\Gamma_{\text{S,opt}}$, is computed by the computer simulation program and can be displayed on the Smith chart as shown in Figure 1.2(a). On the Smith chart, its corresponding parameters, G_{opt}, B_{opt}, R_{opt}, X_{opt}, can be read from the same point.

Noise figure would be expected to be at a minimum if the input impedance were at point N where its input impedance corresponds to $\Gamma_{\text{S,opt}}$. Instead, in raw device testing, the noise figure is tested at point G where its impedance corresponds to its S_{11}. Therefore its value is much higher than the expected minimum. Figure 1.3 shows the tested noise figure. In the entire frequency range, it is around $8.7\,dB$.

At this point, a question may be raised: Through impedance matching, the trace S_{11} can be pulled to $50\,\Omega$, the center of the Smith chart. What would happen to the trace of $\Gamma_{\text{S,opt}}$ then? We expect that the trace of $\Gamma_{\text{S,opt}}$ would also be pulled to $50\,\Omega$, the center of the Smith chart. Can we control the change of the trace of $\Gamma_{\text{S,opt}}$ when the impedance matching network is implemented?

Let's take a look at the performance of the noise figure (*NF*) in the entire frequency range from the raw device testing. Figure 1.3 shows that the noise figure in the operating frequency range is

$$NF = 8.52 \text{ to } 8.77\,dB, \qquad \text{when } 850\,MHz < f < 940\,MHz, \tag{1.24}$$

$$NF = 8.7\,dB, \qquad \text{when} \qquad f = 895\,MHz. \tag{1.25}$$

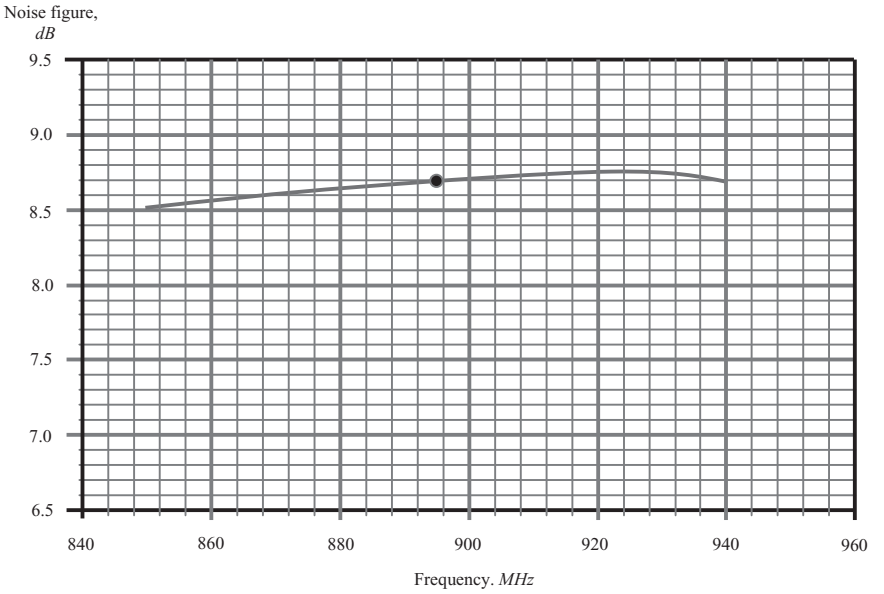


Figure 1.3 Noise figure from 850 to 940 MHz. $I_D = 2.6\,mA$, $NF = 8.7\,dB$ when $f = 895\,MHz$.

The goal is

$$NF < 2.5\,dB, \qquad \text{when } 850\,MHz < f < 940\,MHz. \tag{1.26}$$

It can be seen that in the entire operating frequency range the noise figure is unacceptable.

Now let's examine the gain circles and noise figure circles at one frequency, say, $f = 895\,MHz$, on the input reflection coefficient plane. Figure 1.4 plots both the gain circles and noise figure circles together.

The maximum of gain, $G = G_{max}$, is located at point G, which is $3.0\,dB$, as shown in Figure 1.2(b). However, its noise figure does not reach its minimum $NF_{min} = 5\,dB$ as shown at point N, that is,

At point G,

$$G = G_{max} = 3.0\,dB, \quad \text{and} \quad NF = 8.7\,dB. \tag{1.27}$$

The minimum of the noise figure, $NF = NF_{min}$, is located at point N, which is quite far from point G. Its gain is, of course, much lower than the maximum gain of $3\,dB$ at point G, that is,

At point N,

$$G = -4.8\,dB, \quad \text{and} \quad NF = NF_{min} = 5\,dB. \tag{1.28}$$

The raw device would be operating at point O, the center of the Smith chart, instead of at point G or N, if the internal impedance of the signal source is $50\,\Omega$. Its gain would be higher than $-4.8\,dB$ but lower than $3.0\,dB$, while its noise figure would be

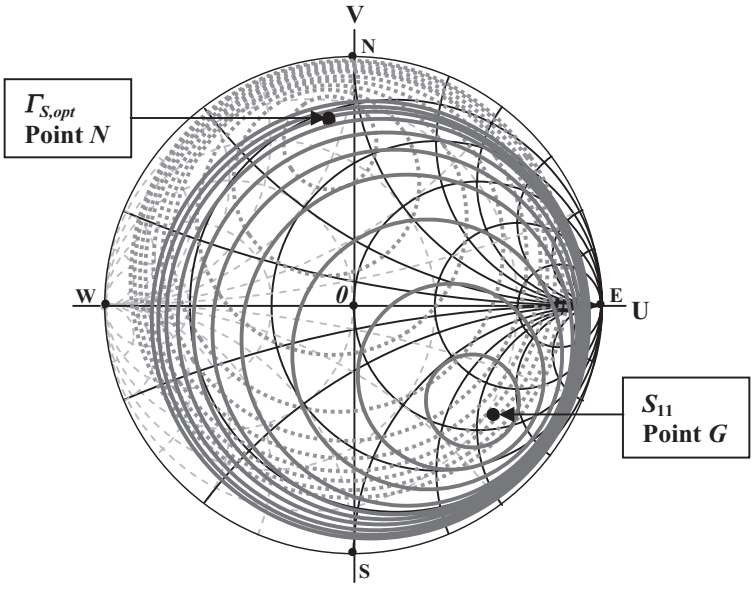


Figure 1.4 Constant gain circles and constant noise figure circles when $f = 895\,MHz$.
Gain circles: $G_{max} = 3.0\,dB$ at point G, step = $-1.0\,dB$.
Noise figure circles: $NF_{min} = 5\,dB$ at point N, step = $0.5\,dB$.

lower than $8.7\,dB$ but higher than $5\,dB$. As a matter of fact, the raw device can be operated with any source impedance. Therefore its impedance can be correspondingly adjusted to any point on the Smith chart. The actual values of gain and noise figure can be read from Figure 1.4. These gains will not be higher than $3.0\,dB$, and the noise figures will not be lower than $5\,dB$. The ideal case is to find a raw device in which the maximum of gain, G_{max}, and the minimum of noise figure, NF_{min}, come together at one point on the Smith chart. This seems almost impossible without a special scheme being involved. However, we should ask the following questions: Might this be a temporary outcome because the design work is in the preliminary stage? The next step is to build the input and output impedance matching networks based on the raw device testing. Is it possible to pull points G and N together after the input impedance matching network is built?

We will temporarily submit the noise figure to the will of heaven, take care of the gain only, and move on to the task of input and output impedance matching as shown in Figure 1.5.

Impedance matching is a special scheme and the key technology in *RF* circuit design. It is discussed in some detail in this book. Because there are many ways to do impedance matching, many different results can be found. Figure 1.6 shows one such result. The point G of maximum gain, along with its gain circles, is moved from its original high impedance location as shown in Figure 1.4 to a location near the center of the Smith chart, $50\,\Omega$. The maximum of gain is increased from the $3.0\,dB$ of Figure 1.4 to $13\,dB$ as a result of the impedance matching. However, its

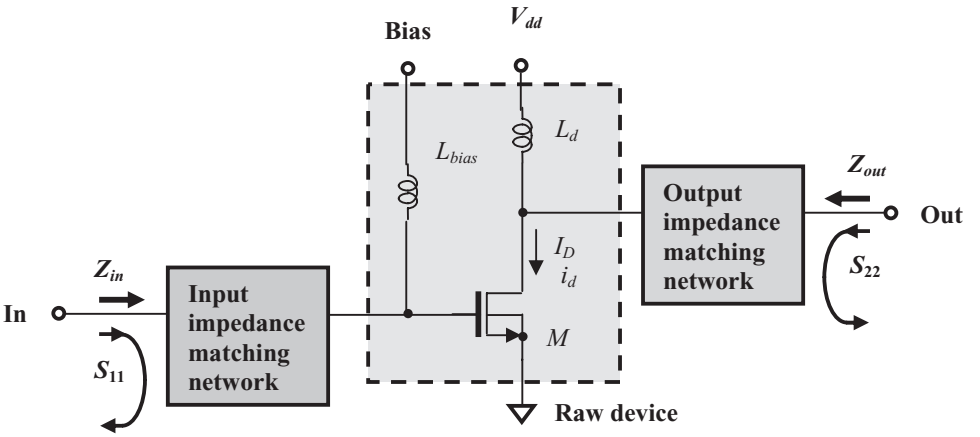
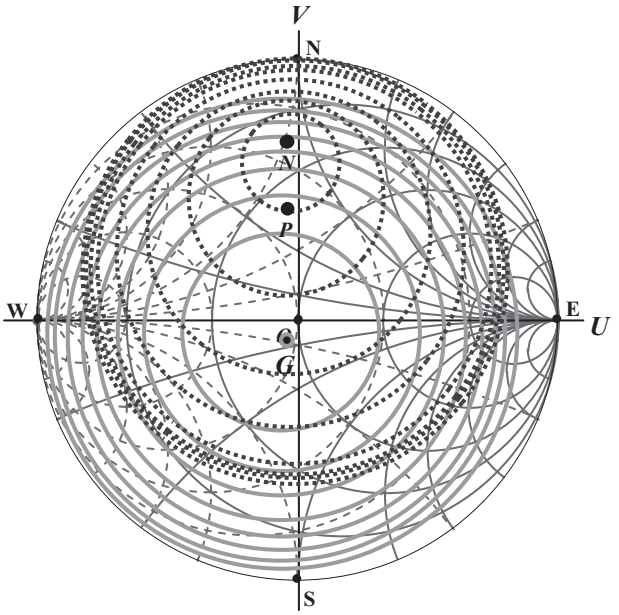


Figure 1.5 Input and output impedance matching networks are added to the raw device. $f = 850$ to $940\,MHz$, $I_D = 2.6\,mA$.



Input reflection coefficient Γ_S plane

Figure 1.6 Constant gain circles and constant noise figure circles when $f = 895\,MHz$.
Gain circles: $G_{max} = 13\,dB$ at point G, step = $1.0\,dB$.
Noise figure circles: $NF_{min} = 1.8\,dB$ at point N, step = $0.5\,dB$.

noise figure has not reached its minimum, $NF_{min} = 2\,dB$ as shown at point *N*. in Figure 1.6.

At point *G*,

$$G = G_{max} = 13\,dB, \quad \text{and} \quad NF = 3.5\,dB, \tag{1.29}$$

Also, due to the impedance matching, the point *N* of minimum noise figure, along with its noise figure circles, is moved from point *N* in the upper left area of the Smith chart in Figure 1.4 to its new location in the upper left area of the Smith chart. The minimum noise figure is dropped from the $5\,dB$ in Figure 1.4 to $1.8\,dB$ in Figure 1.6 as a result of the impedance matching. That is, at point *N*,

$$G = 8.2\,dB, \quad \text{and} \quad NF = NF_{min} = 1.8\,dB. \tag{1.30}$$

The goals as mentioned previously were:

$$G > 10\,dB, \qquad \text{when } 850\,MHz < f < 940\,MHz. \tag{1.31}$$

$$NF < 2.5\,dB, \qquad \text{when } 850\,MHz < f < 940\,MHz. \tag{1.32}$$

It can be seen that the input impedances at either point *G* or point *N* are still insufficient!

In order to satisfy these goals, a trade-off is usually made between the maximum gain, G_{max}, and the minimum of noise figure, NF_{min}. For instance, if we force the input impedance matching to point *P*, where the gain is lower than G_{max} but the noise figure is increased from NF_{min} by not too much, we satisfy the goals because at point *P*,

$$G = 11.3\,dB, \quad \text{and} \quad NF = 2.3\,dB. \tag{1.33}$$

It can be seen that the trade-off sacrifices gain to obtain low noise. This is, of course, adopted reluctantly. The probability of success without a trade-off just relies on luck, although with hard work, the probability is higher than winning a lottery. There is very little chance for a designer to obtain a maximum of gain and a minimum of noise figure at the same time.

However, this is what designers have been attempting in the past decades.

The ideal case to be pursued is that points *N G*, and hence the gain circles and noise figure circles, exactly overlap together at the center of the Smith chart when the input and output impedances are matched to $50\,\Omega$.

This is a very challenging but exciting project.

1.2.3 Challenge of a Good *LNA* Design

In order to solve the dilemma of overlapping the maximum gain with the minimum of noise figure at $50\,\Omega$ in the *LNA* circuit design, I suggest a repeated study of Haus's papers to thoroughly understand the meaning of the "optimum of source reflection coefficient, $\Gamma_{S,opt}$." In the history of the sciences of developing technology, every forward step requires a correct concept and diligent practice.

1.2.3.1 Optimum of Source Voltage Reflection Coefficient, Γ_{opt} Let's return to the raw device testing.

To clarify and distinguish the various reflection coefficients, Figure 1.7 emphasizes the directions of $\Gamma_{S,opt}$, Γ_S, S_{11}, Γ_{in}, and S_{11}^* immediately at the input and output of the raw device ($\Gamma_{S,opt}$ should not be misunderstood as the input reflection coefficient of the raw device, Γ_{in}, which is almost equal to S_{11} if S_{12} is negligible.) The following concepts are essential to solving the problem:

- In order to enable the raw device to approach the minimum of noise figure, $\Gamma_{S,opt}$ is a required optimum of source reflection coefficient, Γ_S, looking from the raw device toward the source.
- On the other hand, in order to enable the raw device to approach to the maximum gain, G_{max}, S_{11}^* is a required value of source reflection coefficient, Γ_S, looking from the raw device toward the source since the actual reflection coefficient looked from the source toward the raw device is S_{11}.

Based on Haus's theory, the minimum noise figure of the raw device will be simultaneously approached with the maximum gain if

$$\boxed{\Gamma_{S,opt} = S_{11}^*.} \tag{1.34}$$

Conversely, it is impossible to approach the minimum noise figure of the raw device with the maximum gain if

$$\Gamma_{S,opt} \neq S_{11}^*. \tag{1.35}$$

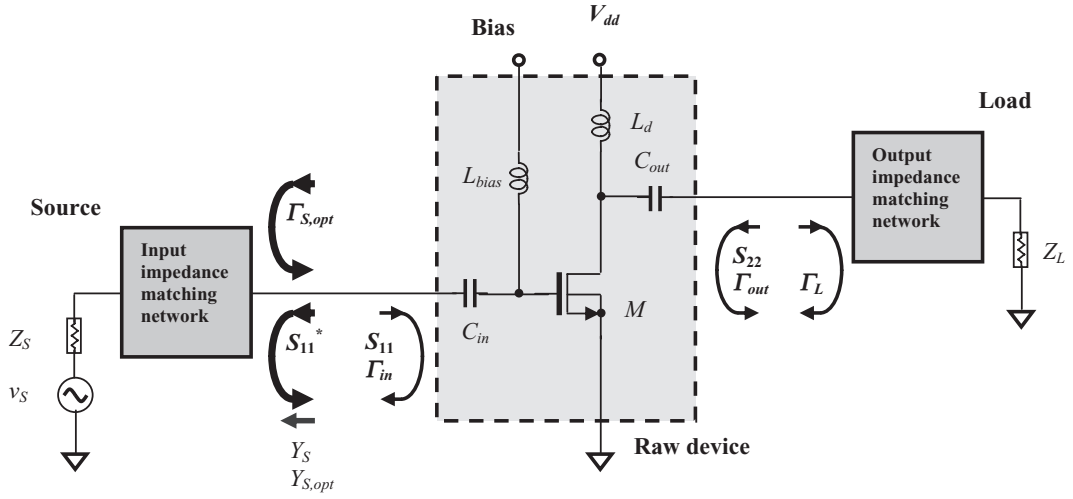


Figure 1.7 Directions of $\Gamma_{S,opt}$, Γ_{in} and Γ_{out}, S_{11} and S_{11}^* in the schematic for raw device testing.

I developed the condition (1.34) in the 1990s and have been applying it in many successful design projects, although it has not been published. We will now pursue equation (1.34). This equation represents the condition by which a perfect *LNA* with **a** minimum noise figure and maximum gain can be **simultaneously** approached after the input and output impedance matching networks are implemented.

Let's return to Figures 1.2 and 1.4 for the raw device testing. It can be found that the $\Gamma_{S,opt}$ and S_{11}^* do not satisfy condition (1.34), but are in the condition of (1.35). This is the reason for the problem in Figure 1.6, where the points *G* of maximum gain and *N* of minimum noise figure were very far apart and not in conjugate locations to each other; therefore the gain and noise figure circles did not overlap after the implementation of the input and output impedance matching networks. Consequently, in Figure 1.6, it was impossible to simultaneously achieve a maximum gain and a minimum noise figure.

It should be re-iterated that the implementation of the input impedance matching network cannot change the deviation status between $\Gamma_{S,opt}$ and S_{11}^*, since $\Gamma_{S,opt}$ and S_{11}^* are determined by the raw device only and are basically independent of the impedance matching network.

1.2.3.2 Simultaneous Approach of Both $\mathbf{NF_{min}}$ ***and*** $\mathbf{G_{max}}$ On the surface, it seems as though the purpose of raw device testing is the starting point for impedance matching. Actually, the more important purpose of this testing is to judge whether a raw device could build a good *LNA* or not, that is, to check whether condition (1.34) is satisfied or not. Should condition (1.34) not be satisfied, impedance matching design should be halted and possible means to satisfy or approach condition (1.34) should be sought.

Three major schemes are used to satisfy condition (1.34) in the step of raw device testing:

1) Increasing or decreasing the current drain, I_D;
   The *S* parameters as well as the values of $\Gamma_{S,opt}$ change as the current drain is varied. The condition $\boldsymbol{\Gamma_{S,opt} = S_{11}^*}$ could be reached with an appropriate amount of current drain.
2) Changing the device size
   The *S* parameters as well as the values of $\Gamma_{S,opt}$ change as the device size is varied. The condition $\boldsymbol{\Gamma_{S,opt} = S_{11}^*}$ could be reached with an appropriate device size. Of course, this scheme is only available to the *IC* designer and not to the designer implementing a circuit by discrete parts.
3) Addition of degeneration part
   According to empirical design experience in practical design, this is an easy way to achieve success.

Due to space limitations, we are only going to apply the third scheme to the design example. Readers are encouraged to apply the first and second in their designs since both are very effective as well. Usually, it is easier to approach the condition $\boldsymbol{\Gamma_{S,opt} = S_{11}^*}$ by the use of multiple combined schemes rather than only one.

Figure 1.8 shows a degeneration inductor, L_{degen}, applied to the source of the *MOSFET* transistor.

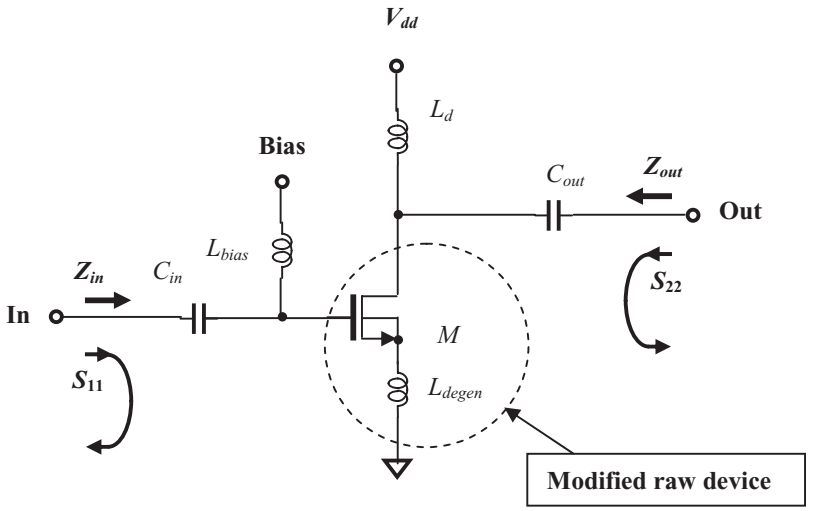


Figure 1.8 Setup for modified raw device testing by the addition of degeneration inductor. L_{degen}: degeneration inductor; C_{in}, C_{out}: "zero" capacitor; L_{bias}, L_c, L_d: "infinite" inductor.

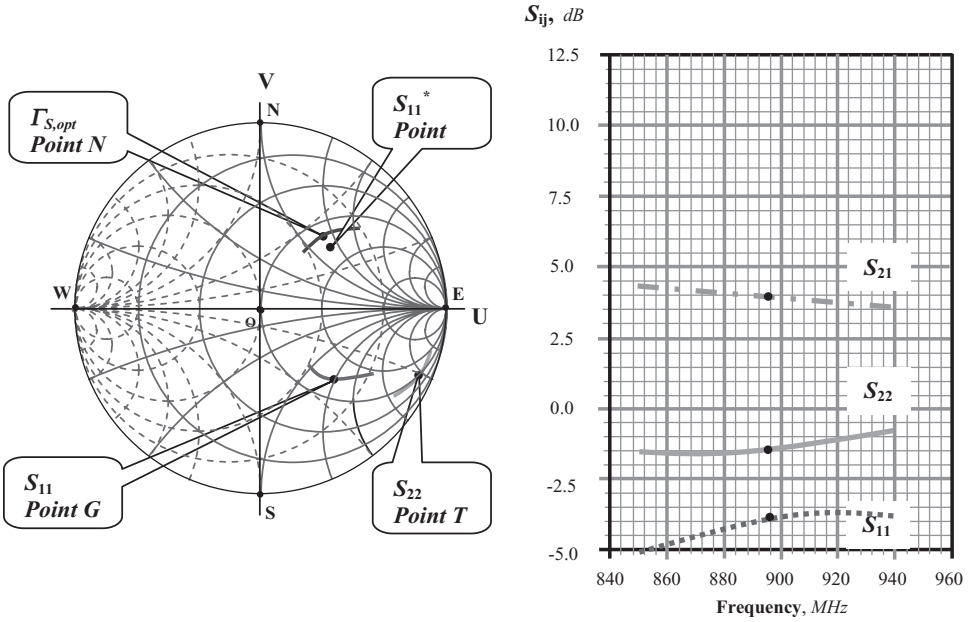
The degeneration inductor, L_{degen}, is a simple and tiny part. For example, in the *RFIC* circuit design for *GHz* of operating frequency range, it is about 0.5 to 2 turns. The actual value of the degeneration inductor applied to this design sample is $10\,nH$.

In the simulation, it is connected to the source of the device. The device, combined with the degeneration inductor, is a modified raw device. The input impedance, of course, is different from the original impedance without the degeneration inductor.

By adjusting the value of the degeneration inductor to change its input impedance, condition (1.34) could be satisfied. As the degeneration inductor is added, the trace of S_{11} is moved from its original location as shown in Figure 1.2(a) to a new location as shown in Figure 1.9(a). Consequently, the traces of S_{11}^* and $\Gamma_{S,opt}$ on the input reflection coefficient plane are close to each other as shown in Figure 1.9. The corresponding variation of impedance can be determined by the equation derived in the following sub-section 1.2.3.3, in which both resistance and reactance are increased.

Figure 1.9(a) shows that the location of S_{11} is somewhat closer to $50\,\Omega$ than in Figure 1.2(a). Correspondingly, Figure 1.9(b) shows that the magnitude of S_{11} is now around $-3.75\,dB$, which is $0.75\,dB$ improved from that of Figure 1.2(b). The magnitude of S_{21} is about $4.0\,dB$, which is $0.5\,dB$ higher than the original shown in 1.2(b). Again, Figure 1.9 shows that the frequency response for all the S parameters is flat; we need not worry about the bandwidth for now. As a matter of fact, it does not matter too much in the variation of magnitude of *S* parameters because the input and output impedances are not matched yet.

From Figure 1.9(a) it is easy to imagine that S_{11} and $\Gamma_{S,opt}$ could be pulled close together near the center of the Smith chart after impedance matching is done, although S_{11}^* and $\Gamma_{S,opt}$ are still not at the same point.



(a) S_{11}, S_{22} and $\Gamma_{S,opt}$ on Smith chart (b) Magnitude of S_{ij}, dB

Figure 1.9 S parameters from modified raw device testing, $f = 850$–$940\,MHz$, $I_D = 2.6\,mA$. (The intermediate frequency $895\,MHz$ is marked with a dot on each trace.)

Before discussing input and output impedance matching, we are going to examine the variation of the input impedance due to the addition of the degeneration inductor.

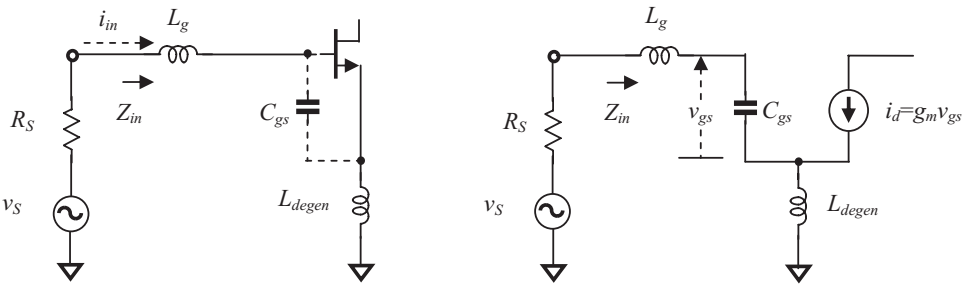
1.2.3.3 Variation of Input Impedance due to Degeneration Inductor Figure 1.10 plots the input stage of a *MOSFET* transistor and its equivalent. From Figure 1.10(b), we have

$$v_{in} = i_{in}\left(jL_g\omega + \frac{1}{jC_{gs}\omega}\right) + (i_{in} + i_d)\,jL_{\deg en}\omega = i_{in}j\left(L_g\omega - \frac{1}{C_{gs}\omega}\right) + (i_{in} + g_m V_{gs})\,jL_{\deg en}\omega, \tag{1.36}$$

$$v_{in} = i_{in}j\left(L_g\omega - \frac{1}{C_{gs}\omega}\right) + \left(i_{in} + g_m i_{in}\frac{1}{jC_{gs}\omega}\right)jL_{\deg en}\omega, \tag{1.37}$$

$$Z_{in} = \frac{v_{in}}{i_{in}} = R_{in} + jX_{in}, \tag{1.38}$$

$$Z_{in} = j(L_g + L_{\deg en})\omega + \frac{1}{jC_{gs}\omega} + \frac{g_m}{C_{gs}}L_{\deg en} = j\left[(L_g + L_{\deg en})\omega - \frac{1}{C_{gs}\omega}\right] + L_{\deg en}\omega_T, \tag{1.39}$$



(a) Input stage (b) Equivalent of input stage

Figure 1.10 The input stage of a *MOSFET* transistor with common source configuration.

where

$$\omega_T = \frac{g_m}{C_{gs}}, \tag{1.40}$$

which is called the cut-off frequency.

$$R_{in} = L_{\deg en}\omega_T, \tag{1.41}$$

$$X_{in} = (L_g + L_{\deg en})\omega - \frac{1}{C_{gs}\omega}. \tag{1.42}$$

On the other hand,

$$G_{m,eff} = g_m Q_{in} = \frac{g_m}{\omega C_{gs}(R_S + L_{\deg en}\omega_T)} = \frac{\omega_T}{\omega R_S\left(1 + \frac{L_{\deg en}\omega_T}{R_S}\right)} = \frac{\omega_T}{2\omega R_S}, \tag{1.43}$$

when the input impedance is matched, that is,

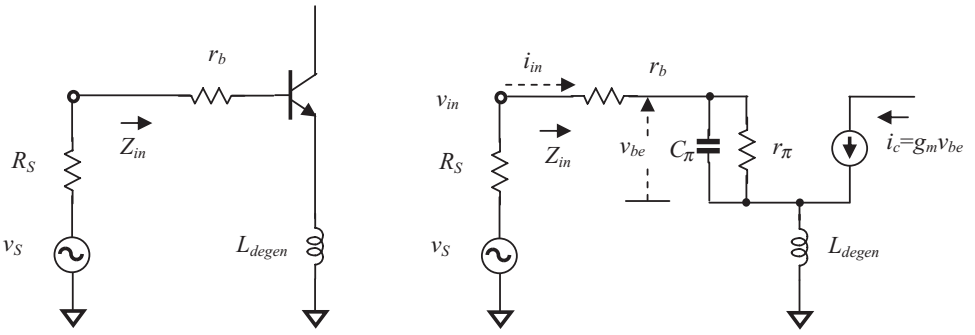
$$R_s = L_{\deg en}\omega_T, \tag{1.44}$$

where Q_{in} is the effective input Q of the circuit. Note that R_g has been neglected relative to R_s. This equation is valid at resonance where the signal voltage across C_{gs} is equal to Q_{in} times the input signal. It should be noted that the overall trans-conductance is apparently independent of g_m, the intrinsic device trans-conductance.

From equations (1.41) and (1.42) it can be seen that the input impedance is increased

$$\Delta Z_{in} = L_{\deg en}\omega_T + jL_{\deg en}\omega, \tag{1.45}$$

due to the presence of L_{degen}.



(a) Schematic of input stage (b) Equivalent of input stage

Figure 1.11 The input stage of a bipolar transistor with a degeneration inductor.

If the device is a bipolar transistor, the input portion can be drawn as shown in Figure 1.11. This figure shows the degeneration inductor connected from emitter to ground. The input impedance can be calculated as follows:

$$r_\pi // C_\pi = \frac{r_\pi}{1 + jC_\pi \omega r_\pi} = \frac{r_\pi}{1 + (C_\pi \omega r_\pi)^2} - j\frac{C_\pi \omega r_\pi^2}{1 + (C_\pi \omega r_\pi)^2}, \tag{1.46}$$

$$v_{in} = i_{in}(r_b + r_\pi // C_\pi) + (i_{in} + i_c) L_{\deg en}\omega, \tag{1.47}$$

$$i_c = g_m v_{be} = g_m i_{in}(r_\pi // C_\pi), \tag{1.48}$$

$$Z_{in} = \frac{v_{in}}{i_{in}} = r_b + r_\pi // C_\pi + j[1 + (r_\pi // C_\pi) g_m] L_{\deg en}\omega, \tag{1.49}$$

$$Z_{in} = r_b + r_\pi + \frac{L_{\deg en} C_\pi \omega^2 g_m r_\pi^2}{1 + (C_\pi \omega r_\pi)^2} + j\left[1 + \frac{\left(g_m - \dfrac{C_\pi}{L_{\deg en}} r_\pi\right) r_\pi}{1 + (C_\pi \omega r_\pi)^2}\right] L_{\deg en}\omega. \tag{1.50}$$

$$R_{in} = r_b + r_\pi + \frac{L_{\deg en} C_\pi \omega^2 g_m r_\pi^2}{1 + (C_\pi \omega r_\pi)^2}, \tag{1.51}$$

$$X_{in} = \left[1 + \frac{\left(g_m - \dfrac{C_\pi}{L_{\deg en}} r_\pi\right) r_\pi}{1 + (C_\pi \omega r_\pi)^2}\right] L_{\deg en}\omega. \tag{1.52}$$

It should be noted that
when

$$g_m = \frac{C_\pi}{L_{\deg en}} r_\pi, \tag{1.53}$$

then

$$X_{in} = L_{\deg en}\omega. \tag{1.54}$$

In cases with low frequency, the capacitor C_π can be neglected. Then (1.50), (1.51), and (1.52) become

$$Z_{in} = r_b + r_\pi + j(1 + g_m r_\pi) L_{\deg en}\omega. \tag{1.55}$$

$$R_{in} = r_b + r_\pi, \tag{1.56}$$

$$X_{in} = (1 + r_\pi g_m) L_{\deg en}\omega. \tag{1.57}$$

In cases with high frequency, R_{in} is increased while X_{in} is decreased in cases with low frequency.

From equations (1.51) and (1.52) it can be seen that the input impedance is increased

$$\Delta Z_{in} = \frac{L_{\deg en} C_\pi \omega^2 g_m r_\pi^2}{1 + (C_\pi \omega r_\pi)^2} + j\left[1 + \frac{g_m r_\pi}{1 + (C_\pi \omega r_\pi)^2}\right] L_{\deg en}\omega, \tag{1.58}$$

due to the presence of L_{degeh}.

In comparing (1.45) with (1.58), the increased resistance is almost the same while the increased reactance of the bipolar transistor has a higher slope than that of the *MOSFET* if C_π in the bipolar transistor is equivalent to C_{gs} in the *MOSFET* and $C_\pi \omega\, r_\pi >> 1$.

Based on these two equations, the designer is able to estimate how far the trace of S_{11} must be moved on the Smith chart, so as to satisfy condition (1.34), by which the maximum gain and minimum noise figure circles can be almost entirely overlapped near the center of the Smith chart.

1.2.4 Input and Output Impedance Matching

Impedance matching is a core technology in *RF* circuit design and is therefore discussed in detail in this book. The process of impedance matching for the design sample shown above will be omitted. Instead, the final input and output impedance matching networks and their performance are shown in Figures 1.12 and 1.13, respectively.

Figure 1.12 plots the impedance matching networks, which consist of parts

- In the input impedance network: $C_{S1,in} = 1\,pF$, $L_{P,in} = 20\,nH$, $C_{S2,in} = 39\,pF$, and
- In the output impedance network: $L_{P,out} = 15\,nH$ and $R_{P,out} = 1500\,\Omega$, $C_{S,out} = 1.6\,pF$.

The input impedance matching network is built with a *T* type circuitry of *C-L-C*, by which the trace of S_{11} is pulled to a location near the center of the Smith chart which corresponds to the reference impedance point of $50\,\Omega$. The capacitor $C_{S2,in} = 39\,pF$ is actually a "zero" capacitor and functions as the *DC* blocking part. By means

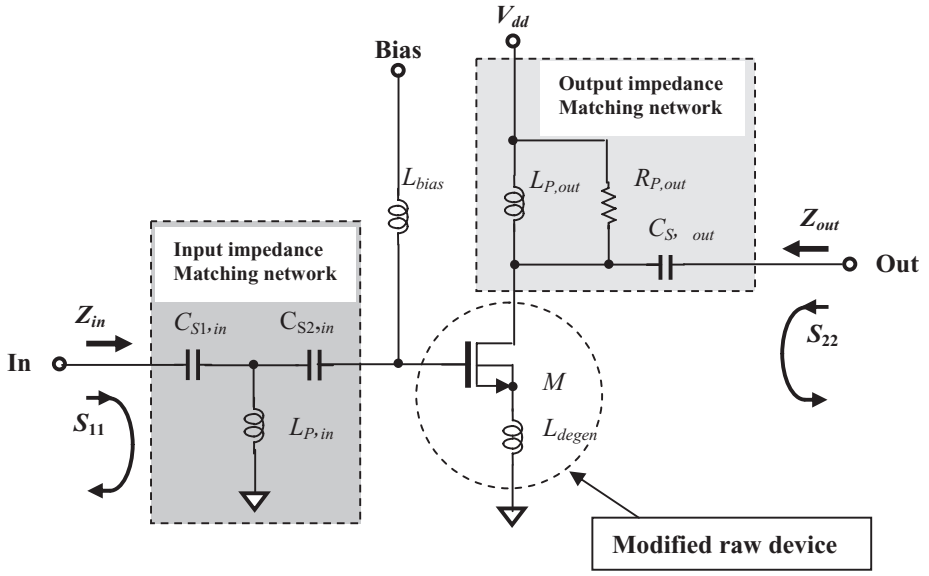


Figure 1.12 Impedance matching of modified raw device by parts. At input: $C_{S1,in} = 1\,pF$, $L_{P,in} = 20\,nH$, $C_{S2,in} = 39\,pF$. At output: $L_{P,out} = 15\,nH$, $R_{P,out} = 1500\,\Omega$, and $C_{S,out} = 1.6\,pF$.

of $L_{P,in}$ in parallel, the trace of S_{11} is pulled counter-clockwise to the resistance circle of $50\,\Omega$ along the constant conductance circle, and then, by means of $C_{S1,in}$ in series, the trace of S_{11} is pulled counter-clockwise to the area near the reference impedance point $50\,\Omega$ along the constant resistance circle.

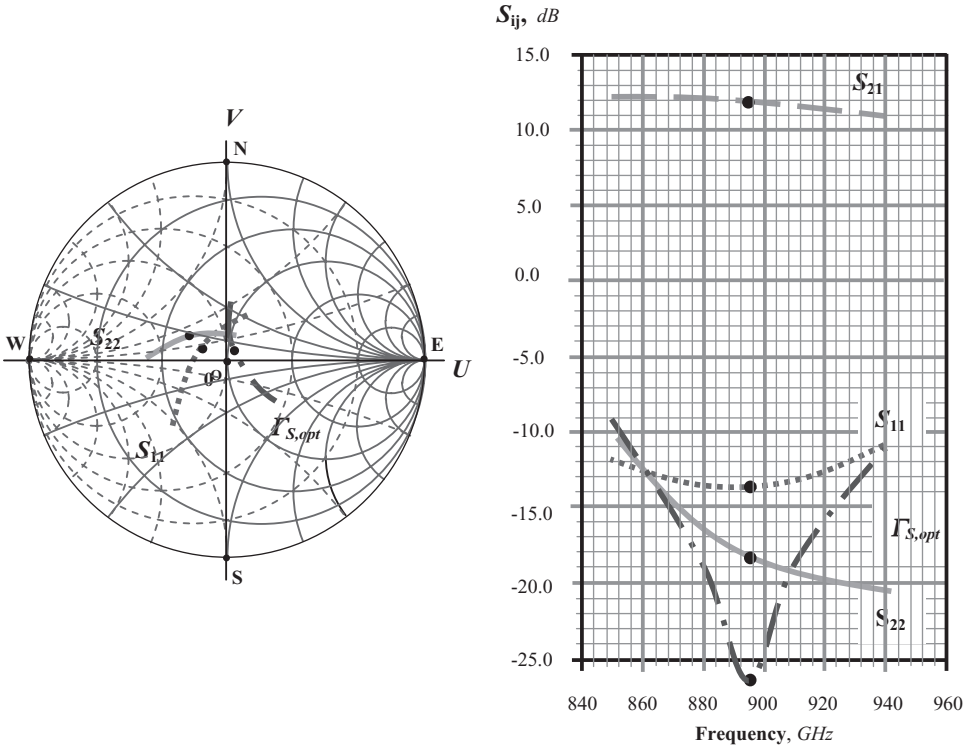
The output impedance matching network consists of an inductor, a resistor, and a capacitor. The inductor, $L_{P,out} = 15\,nH$, is the main part of the output impedance matching network, by which the trace of S_{22} is pulled counter-clockwise to a location near the $50\,\Omega$ resistance circle along the constant conductance circle. The capacitor $C_{S,out} = 1.6\,pF$ is the next part, by which the S_{22} is drawn counter-clockwise to a location near the center of the Smith chart corresponding to the reference impedance point $50\,\Omega$ along the constant resistance circle. The resistor $R_{P,\text{out}}$ is a de-Q part, by which the bandwidth is widened and the *LNA* is changed from an unstable to a stable state.

From Figure 1.13(a) it can be seen that S_{11} and $\Gamma_{S,opt}$ are not completely superimposed on each other. The deviation arises from the fact that the S_{11}^* and $\Gamma_{S,opt}$ of the modified raw device shown in Figure 1.8 are not exactly overlapped. However, this is a normal phenomenon in the actual design because all parts have tolerance and in addition, absolutely ideal cases never happen in actual engineering design. The absolute accuracy of simulation processing is never realistic. As long as the two points S_{11}^* and $\Gamma_{S,opt}$ are pulled close enough to each other, it will be sufficient to satisfy the goals of the design.
Figure 1.13(b) shows that

- Input return loss, S_{11}

$$-13.8\,dB < S_{11} < -11.0\,dB, \quad \text{when } 850\,MHz < f < 940\,MHz, \tag{1.59}$$

$$S_{11} = -13.7\,dB, \quad \text{when } f = 895\,MHz, \tag{1.60}$$



(a) S_{11}, S_{22} and $\Gamma_{S,opt}$ on Smith chart

(b) Magnitude of S_{ij}, dB

Figure 1.13 S parameters of the design example, $f = 850$–$940\,MHz$, $I_D = 2.6\,mA$. (The intermediate frequency $895\,MHz$ is marked with a dot on each trace.) The input and output impedances are matched by parts. At input: $C_{S1,in} = 1\,pF$, $L_{P,in} = 20\,nH$, $C_{S2,in} = 39\,pF$. At output: $L_{P,out} = 15\,nH$ and $R_{P,out} = 1500\,\Omega$, $C_{S,out} = 1.6\,pF$.

- Output return loss, S_{22}

$$-20.5\,dB < S_{22} < -10.5\,dB, \quad \text{when } 850\,MHz < f < 940\,MHz, \tag{1.61}$$

$$S_{22} = -18.5\,dB, \quad \text{when } f = 895\,MHz, \tag{1.62}$$

- Gain, S_{21}

$$11.0\,dB < S_{21} < 12.2\,dB, \quad \text{when } 850\,MHz < f < 940\,MHz, \tag{1.63}$$

$$S_{21} = 12.0\,dB, \quad \text{when } f = 895\,MHz, \tag{1.64}$$

- Optimum of source reflection coefficient, $\Gamma_{S,opt}$

$$-26.5\,dB < \Gamma_{S,opt} < -9.0\,dB, \quad \text{when } 850\,MHz < f < 940\,MHz, \tag{1.65}$$

$$\Gamma_{S,opt} = -26.5\,dB, \quad \text{when } f = 895\,MHz, \tag{1.66}$$

The isolation S_{12} is not shown in Figure 1.13(b) because it is lower than $25\,dB$ in the entire frequency range.

It can be seen that the gain is reasonable and the bandwidth is wide enough! In addition, the values of the parts are appropriate. Now let's check its noise performance.

1.2.5 Gain Circles and Noise Figure Circles

The noise performance of the design sample is good after impedance matching is done. This is expected because the modified raw device is designed for simultaneously approaching maximum gain and minimum noise figure. Figure 1.14 shows the performance of the noise figure in the entire frequency range, that is

$$1.37\,dB < NF < 1.97\,dB, \qquad \text{when } 850\,MHz < f < 940\,MHz, \tag{1.67}$$

$$NF = 1.5\,dB, \qquad \text{when} \qquad f = 895\,MHz, \tag{1.68}$$

The values of the noise figure shown in Figure 1.14 are denoted with two ordinates, one for simulated values and one for actual tested results. It can be seen that the actual tested values of the noise figure are $0.85\,dB$ higher than the simulated values. The good news is that the noise figure in the entire frequency range is better than the previously stated goals.

Exciting results are found from the plot of the gain and noise figure circles as shown in Figure 1.15. This is a plot for the operating frequency of $f = 895\,MHz$.

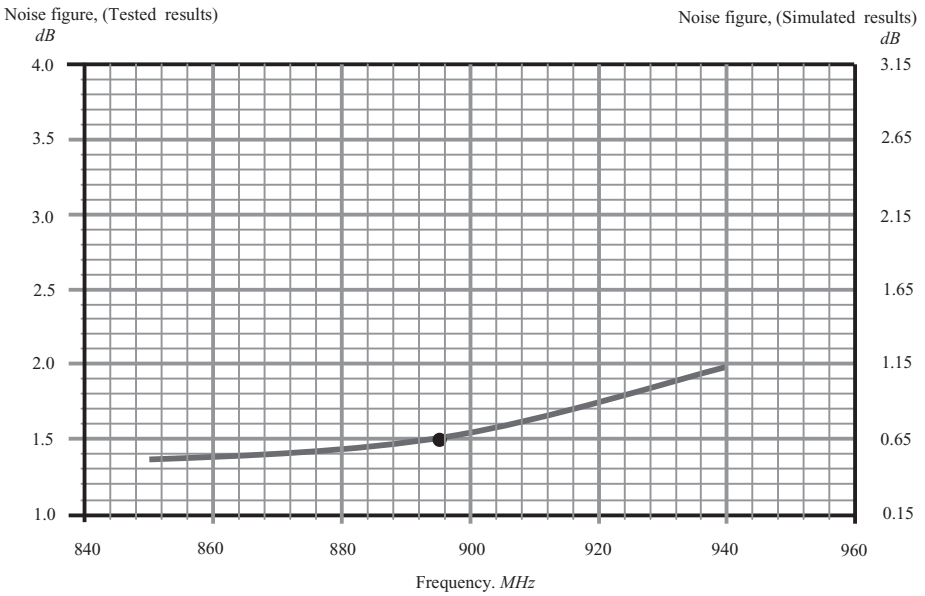


Figure 1.14 Noise figure of the design example, $f = 850$ to $940\,MHz$, $I_D = 2.6\,mA$. (The intermediate frequency $895\,MHz$ is marked with a dot on the trace.)
$NF = 1.5\,dB$ when $f = 895\,GHz$.

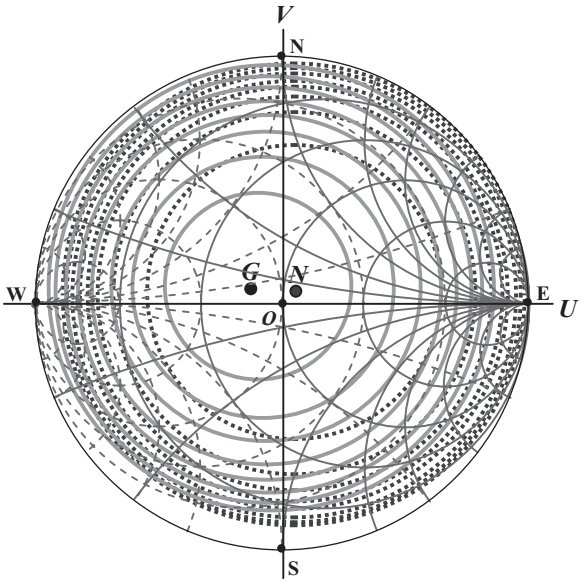


Figure 1.15 Constant gain circles and constant noise figure circles when $f = 895\,MHz$.
Gain circles: $G_{max} = 12\,dB$ at point G, step = $1.0\,dB$.
Noise figure circles: $NF_{min} = 1.5\,dB$ at point N, step = $0.5\,dB$.

After the input and output impedances are matched, the center of the gain circles is point G, which is quite close to the center of the Smith chart. The maximum gain at this operating frequency is $12\,dB$ which is consistent with the results shown in Figure 1.13(b). On the other hand, the center of the noise figure circles is point N, which is also very closed to the center of Smith chart. The minimum of noise figure at this operating frequency is $1.5\,dB$ which is consistent with the results shown in Figure 1.14. The wonderful feature of Figure 1.15 is that the gain and noise circles overlap almost perfectly. The two centers are very close to each other and near the center of the Smith chart.

As mentioned above, the deviation between point N and point O is due to the incomplete overlapping in the modified raw device so that condition (1.34), $\Gamma_{S,opt} = S_{11}^*$, is not perfectly satisfied. In reality, it is impossible to reach an ideal goal predicted by theory. Deviation between practical design and circuit theory has always existed.

1.2.6 Stability

One of the important specifications for a *LNA* design is stability. It is obvious that a *LNA* may become an oscillator if it is unstable in the circuit performance. Therefore, the designer must examine its stability after the topology of the circuit and the value of parts, such as the design sample shown in Figure 1.12, are confirmed.

It is well known that the Smith chart is a reflection coefficient plane, called a Γ plane, in which the impedance, z, is plotted by means of the following relationship,

$$z = \frac{Z}{Z_o} = \frac{1+\Gamma}{1-\Gamma}, \tag{1.69}$$

where z is a normalized impedance by the reference impedance, which is usually $50\,\Omega$.

Equation (1.69) indicates an important fact, that is,

$$z > 0, \qquad \text{if } |\Gamma| < 1, \tag{1.70}$$

Otherwise,

$$z < 0, \qquad \text{if } |\Gamma| > 1, \tag{1.71}$$

This is a universal relationship for any kind of impedance and its corresponding reflection coefficient. If an impedance looking into a two-port block or terminal is positive, then the block or terminal is stable; if an impedance looking into a two-port block or a terminal is negative, then the block or terminal is unstable. As shown in Figure 1.16, there are 4 reflection coefficients, $\boldsymbol{\Gamma_S}$, $\boldsymbol{\Gamma_L}$, $\boldsymbol{\Gamma_{in}}$ and $\boldsymbol{\Gamma_{out}}$, and 4 S parameters, $\boldsymbol{S}_{11}$, $\boldsymbol{S}_{22}$, $\boldsymbol{S}_{21}$ and $\boldsymbol{S}_{22}$.

The conditions for unconditional stability for all of the reflection coefficients shown in Figure 1.16 are

$$|\Gamma_S| < 1, \tag{1.72}$$

$$|\Gamma_L| < 1, \tag{1.73}$$

$$|\Gamma_{in}| < 1, \tag{1.74}$$

$$|\Gamma_{out}| < 1. \tag{1.75}$$

The two-port block is unstable if the magnitude of any reflection coefficient above is greater than 1. A critical case is that in which the input and output reflection coefficients are equal to 1, that is,

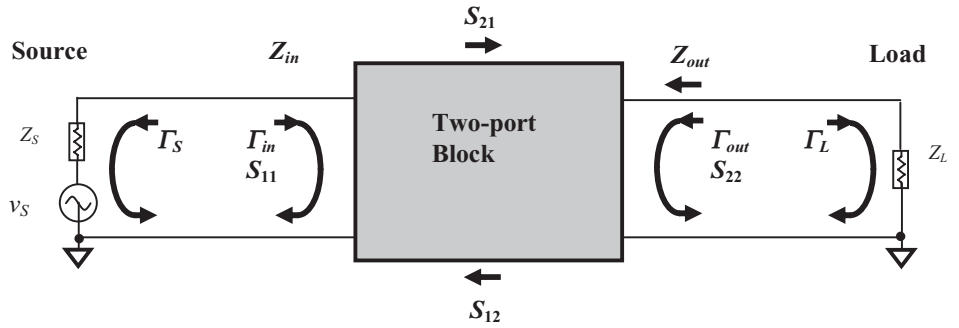


Figure 1.16 Different reflection coefficients and S parameters in a two-port block.

$$|\Gamma_{in}| = 1. \tag{1.76}$$

$$|\Gamma_{out}| = 1. \tag{1.77}$$

It is well known that

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}, \tag{1.78}$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S}. \tag{1.79}$$

The conditions in the critical case therefore are

$$\left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| = 1, \tag{1.80}$$

$$\left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| = 1. \tag{1.81}$$

The critical values of Γ_S and Γ_L can be solved from equations (1.80) and (1.81), they are

$$\left| \Gamma_L - \frac{(S_{22} - \Delta S_{11}^*)^*}{|S_{22}|^2 - |\Delta|^2} \right| = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right|, \tag{1.82}$$

$$\left| \Gamma_S - \frac{(S_{11} - \Delta S_{22}^*)^*}{|S_{11}|^2 - |\Delta|^2} \right| = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right|. \tag{1.83}$$

where

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}|. \tag{1.84}$$

On the Smith chart, they appear as two circles and are called the output and input stability circles. These two stability circles are very useful in the analysis of potentially unstable blocks. However, we are not going to repeat this analysis since it has already been discussed in great detail in many textbooks What we are interested in is how to quickly judge the stability of a designed block.

Historically, a K factor, which is a function of S parameters, has been defined as,

$$K = 1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2. \tag{1.85}$$

In terms of mathematical processing, the necessary and sufficient conditions for a two-port block to be unconditionally stable are

$$K > 1, \tag{1.86}$$

and $$|\Delta| < 1. \tag{1.87}$$

For many years, the stability of a two-port block has been judged by the K factor and the intermediate parameter Δ in terms of equations (1.86) and (1.87).

In recent years, however, they have been replaced by the μ factor, which is defined as

$$\mu = \frac{1 - [mag(S_{11})]^2}{mag[S_{22} - \Delta conj(S_{11})] + mag(S_{21}S_{12})}. \tag{1.88}$$

In equation (1.88), the symbols "mag(…)" and "mag[…]" denote the magnitude of the parameters in the parenthesis or brace, and the symbol "conj(…)" denotes the conjugated value of the parameters in the parenthesis.

The block is unconditionally stable if

$$\mu > 1. \tag{1.89}$$

Otherwise, it is potentially unstable.

Rather than the two conditions of the K and Δ factors, condition (1.89), using the factor of μ is simplest and most convenient criterion. From (1.88) it can be seen that the value of μ is dependent on the tested S parameters only. In today's simulation by *ADS* and Cadence simulation tools, the values of μ for the entire frequency range can be promptly and easily displayed on screen.

The stability of the raw device shown in Figure 1.8 is unstable because the simulation shows its μ value as

$$\mu = 0.95 < 1. \tag{1.90}$$

After the steps of raw device testing, the stability of the *LNA* block must be taken care of. One should perform analysis on the sources of instability.

In the schematic shown in Figure 1.8, the instability may come from the drain inductor, L_d, and the degenerator inductor, L_{degen}.

In order to retain as much voltage drop across the device as possible, so as to reduce intermodulation, it is preferred to use a drain inductor, L_d, rather than a resistor, although an inductor is much more expensive than a resistor. In order to satisfy the overlapping condition (1.34) for NF_{min} without a significant increase of the noise figure, it is preferred to use a degeneration inductor, L_{degen}, rather than a degeneration resistor, R_{degen}.

The drain inductor L_d in Figure 1.8 is adjusted and re-named $L_{P,out}$ as shown in Figure 1.12. The resistor, $R_{P,out}$, is used to de-Q the load inductor $L_{P,out}$, in order to prevent oscillation. On the other hand, the value of L_{degen}, should not be too high, otherwise the gain and stability both suffer.

In our design sample, $L_{degen} = 10nH$ is chosen. The resistor $R_{P,out}$ is the key part to keep the *LNA* block stable, while the lower value of the degeneration inductor L_{degen} provides good assistance.

The values of all the parts shown in the schematic as shown in Figure 1.12 are simultaneously optimized to obtain stability with a reasonable gain and noise figure level, that is,

$$\mu = 1.1 > 1, \tag{1.91}$$

when

$$G = 12\,dB, \tag{1.92}$$

and

$$NF = 1.5\,dB, \tag{1.93}$$

at $f = 895\,MHz$.

The μ value shown in (1.91) indicates that the designed *LNA* is in an unconditionally stable state.

1.2.7 Non-Linearity

1.2.7.1 Spectrum at* LNA *Output An overview of the spectrum at the *LNA* output can provide an intuitive feeling about the linearity of the design. Figure 1.17 shows that

$$P_{out} = -38.0\,dB_m, \quad \text{at } f = 895\,MHz, \tag{1.94}$$

$$P_{out} = -80.7\,dB_m, \quad \text{at } f = 1790\,MHz, \tag{1.95}$$

$$P_{out} = -119.1\,dB_m, \quad \text{at } f = 2685\,MHz, \tag{1.96}$$

...

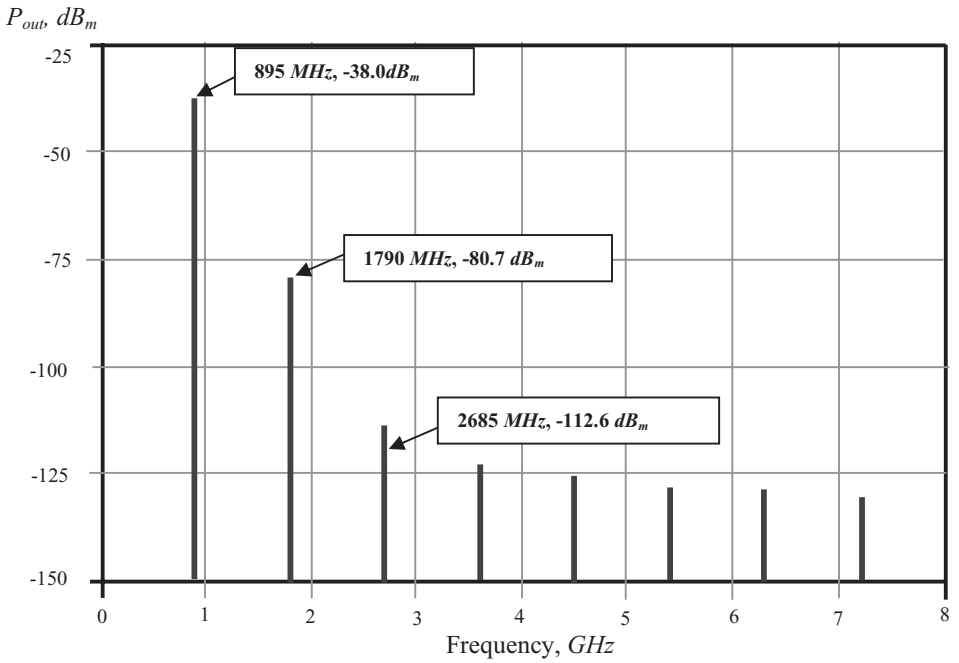


Figure 1.17 Spectrum at *LNA* output, $f_o = 895\,MHz$, $P_{in} = -50\,dB_m$.

when

$$P_{in} = -50\,dB_m. \tag{1.97}$$

Then the gain of *LNA* is

$$P_{out} - P_{in} = -38\,dB_m - (-50\,dB_m) = 12\,dB, \tag{1.98}$$

which is consistent with the gain testing shown in Figure 1.13(b).

The second harmonic is lower than the output power at the operating frequency by

$$\Delta P_{out,2} = P_{out}|_{1790\,MHz} - P_{out}|_{895\,MHz} = -80.7\,dB_m - (-38.0\,dB_m) = -42.7\,dB, \tag{1.99}$$

which implies that the spurious products at the half *IF* frequency, or the Able-Baker spurious products, would be low, and that the second order intercept point would be high. According to design experience, if the *LNA* block is applied to a popular cellular phone communication system, $\Delta P_{out,2}$ should be suppressed by $30\,dB$ at least at the operating frequency so that the distortion of the useful signal will not have conceivable distortion due to the second order spurious products. The second order non-linearity is of priority in a direct conversion or zero *IF* communication system because it produces *DC*-offset to disturb the desired signal.

The third harmonic is lower than the output power at the operating frequency by

$$\Delta P_{out,3} = P_{out}|_{1790\,MHz} - P_{out}|_{895\,MHz} = -116.0\,dB_m - (-38.0\,dB_m) = -78.0\,dB, \tag{1.100}$$

which implies that the third order non-linearity is very small, so that the probability of interference from adjacent channels will be very low or negligible.

Other harmonics higher than third order harmonic are at least $80\,dB$ lower than the output power at the operating frequency. There is nothing to worry about here.

1.2.7.2 1 dB Compression Point The $1\,dB$ compression point is the second easy method to overview the non-linearity of a circuit block. Figure 1.18 shows the $1\,dB$ compression point of our design sample, that is,

$$P_{1dB} = -1.25\,dB_m \qquad \text{when } f = 895\,MHz, \tag{1.101}$$

which satisfies the desired goal.

An intuitive feeling is that the non-linearity would be seriously hampered if the *LNA* is operated with an input power higher than $-5\,dB_m$. The $1\,dB$ compressed point looks like the demarcation point of input power. The *LNA* performs as a linear unit when its input power is below the $1\,dB$ compression point. On the other hand, the *LNA* performs as a non-linear unit when its input power is beyond the $1\,dB$ compression point.

The third order intercept point can be estimated to be 5 to $10\,dB$ higher than the $1\,dB$ compression point, which might be a value between 5 to $10\,dB_m$.

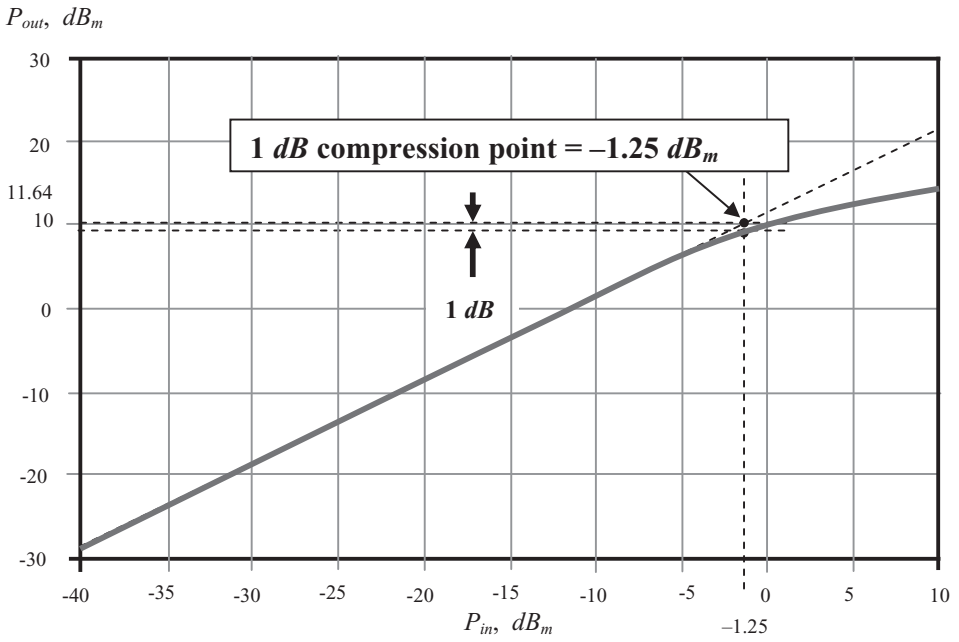


Figure 1.18 $1\,dB$ compression point when $f_o = 895\,MHz$.

***1.2.7.3 Third and Second Order Intercept Points* IP_3 *and* IP_2** Figure 1.19 shows the third order intercept point, IP_3, that is,

$$IIP_3 = 8.6\,dB_m, \quad \text{and} \quad OIP_3 = IIP_3 + G = 20.6\,dB_m, \tag{1.102}$$

In Figure 1.19, the tested values of input and output powers are plotted with bold lines. The asymptote with the expected slope is plotted with dash lines. Point ***P**** is the actual intercept point. However, point P is the expected intercept point, which is the intercept point of the lines with slopes $n = 1$ and $n = 3$. The bent portion of the dash lines indicates another non-linearity of the designed block.

Figure 1.20 shows the second intercept point, IP_2, that is,

$$IIP_2 = 38.1\,dB_m, \quad \text{and} \quad OIP_2 = IIP_2 + G = 50.1\,dB_m. \tag{1.103}$$

Testing is conducted in the input power range below $0\,dB_m$ and the intercept point is obtained by the extension of the two lines with the slopes $n = 1$ and $n = 2$.

These results satisfy the aforementioned goals. Should the tested results be unsatisfactory, extra linearization work for the *LNA* must be conducted and the simulation may have to start from the beginning.

1.2.8 Design Procedures

Based on design experience, a flow chart of *LNA* design procedures is shown in Figure 1.21. It should be noted that

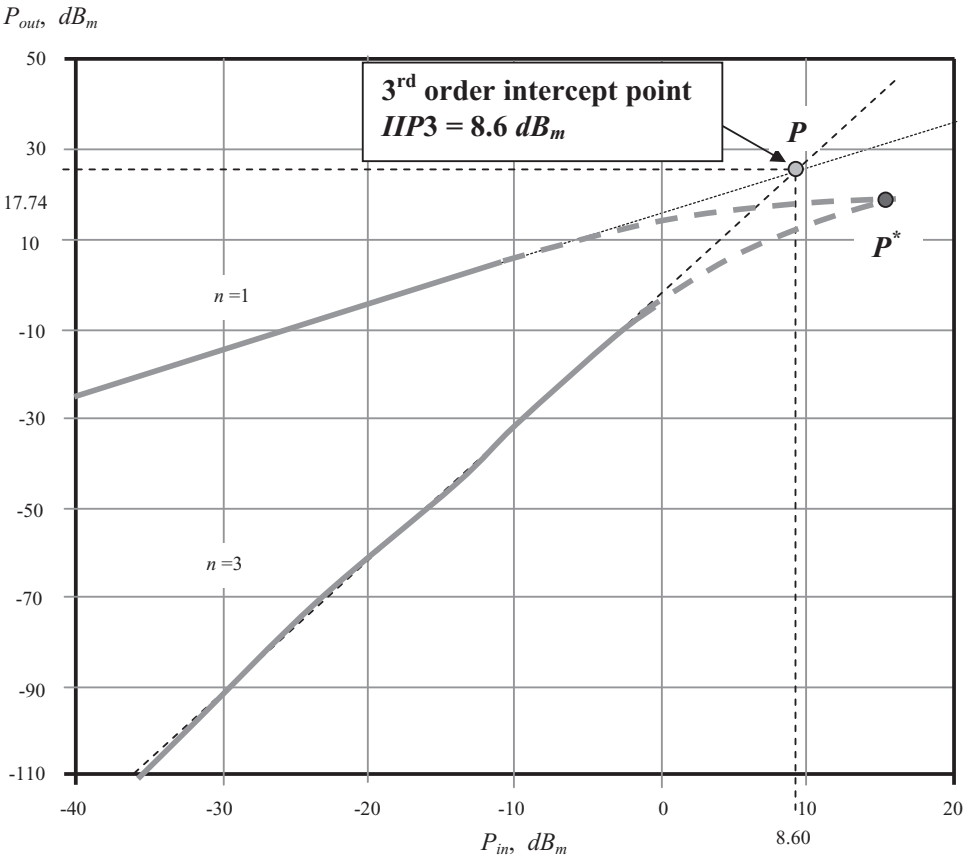


Figure 1.19 Third-order input intercept point when $f_o = 895\,MHz$.

- Raw device testing is the key step on which success or failure largely depends.
- The first iteration loop related to the raw device is judged by the condition of $S_{11}^* = \boldsymbol{\Gamma_{S,opt}}$. There are three options to choose from to satisfy this condition. If the design work in this step is executed well, a good *LNA* design should be able to obtain maximum gain and minimum noise figure simultaneously. Consequently the gain and noise figure circles should almost overlap entirely near the center of the Smith chart.
- The second iteration loop related to the raw device is to judge the stability by the condition of $\boldsymbol{\mu > 1}$.
- The third iteration loop related to the raw device is to reach or exceed all the performance parameters.
- There is another iteration loop to examine the bandwidth in the process of input and output impedance matching.

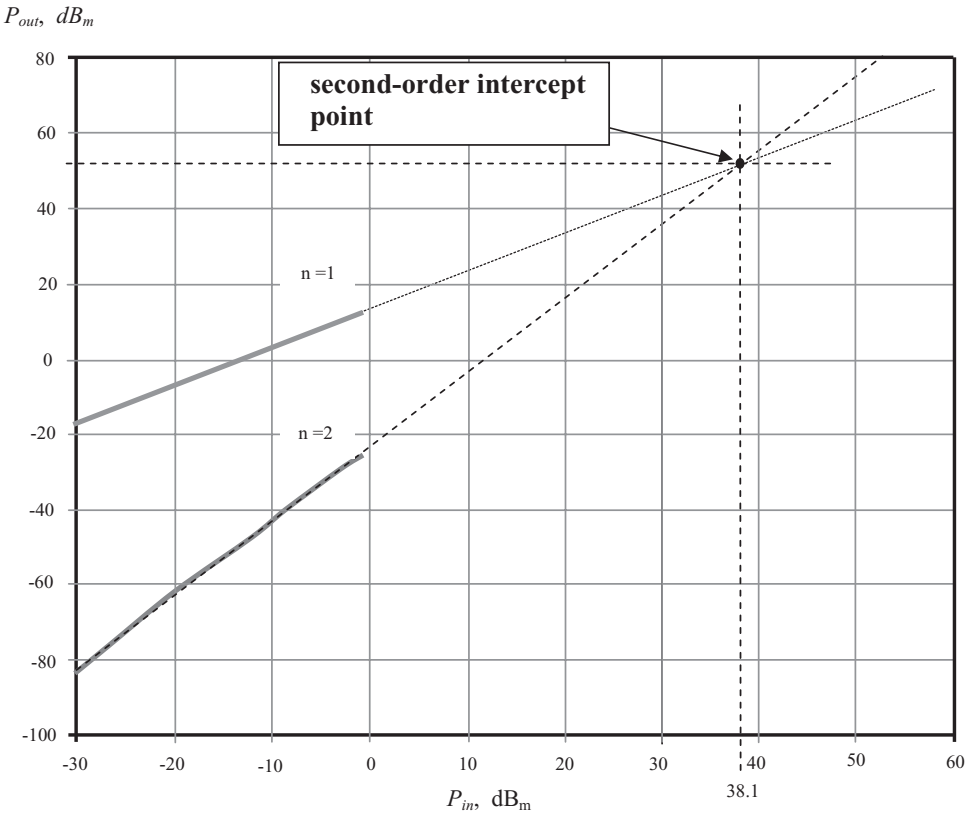


Figure 1.20 Second-order input intercept point when $f_o = 895\,MHz$.

1.2.9 Other Examples

The following three *LNA*s are actually implemented by discrete chip parts for different frequency bands. They are good examples to verify and illustrate the technology of the simultaneous approach to both NF_{min} and G_{max} as discussed in Section 1.2.3.2, even though they were designed by the author many years ago.

1.2.9.1* LNA *Design for* VHF *Frequency Band The *LNA* designed for *VHF* frequency band are outlined in the following three items:

- Electrical features (Table 1.2),
- The schematic (Figure 1.22),
- The gain and noise circles at the Γ_{in} (input voltage reflection coefficient) plane).

It should be noted that

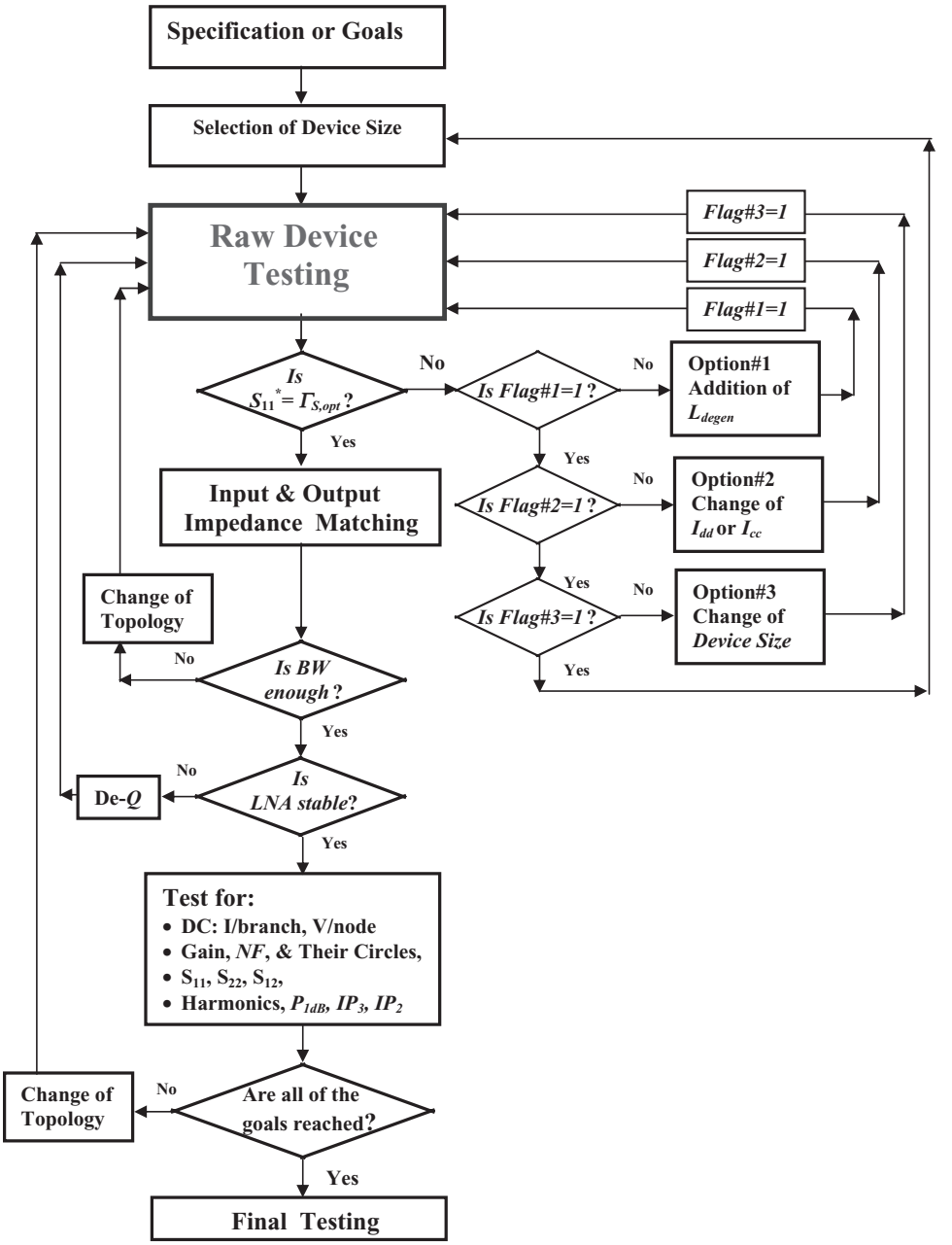


Figure 1.21 Flow chart for *LNA* design procedures.

- The inductor $L_3 = 33\,nH$ is the degeneration inductor mentioned above. The resistor $R_6 = 100\,\Omega$ is the "de-Q" resistor. The modified raw device consists of Q_1, L_3, and R_6.
- Capacitors, C_4, C_2, and C_6 are "zero" capacitors. Their specified values should be $1300\,pF$ and actual values are $1500\,pF$.

TABLE 1.2 Electrical features of *LNA* for *VHF* frequency band

	Specification		Final tested result	
Frequency range	130 *MHz* to 180 *MHz*			
Device	*BFQ67* (Manufacturer: Siemens)			
DC power supply	3	*V*		
Current drain	<4	*mA*	**3.47**	*mA*
Gain	>10	*dB*	**15.0**	*dB*
Noise figure	<2	*dB*	**1.75**	*dB*
IIP_3	>0	dB_m	**2.5**	dB_m
Input return	<–10	*dB*	**–40.0**	*dB*
Output return	<–10	*dB*	**–12**	*dB*

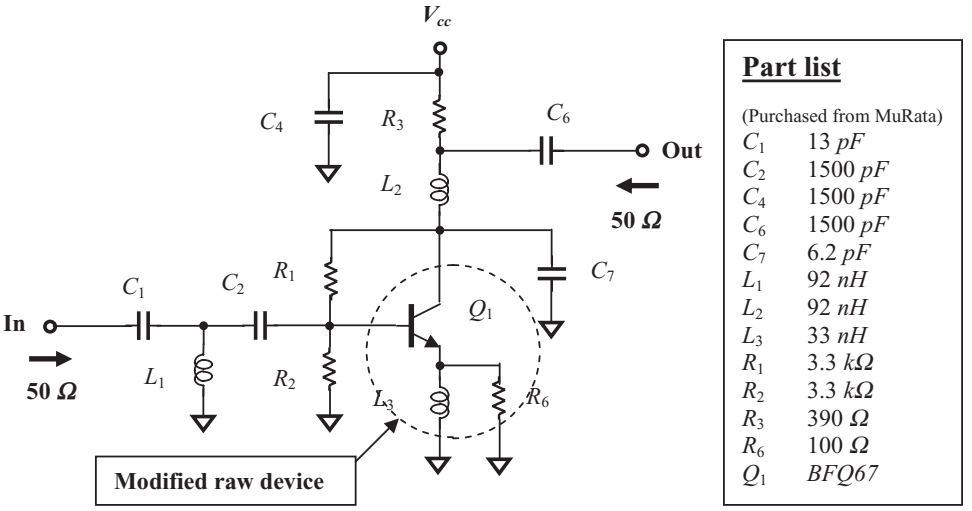


Figure 1.22 *LNA* designed for *VHF* frequency band.

- The resistors R_3 and R_6 are 390 Ω and 100 Ω respectively; they are both "de-Q" resistors.
- The resistors R_1 and R_2 are the combination of a voltage divider. They take the *DC* bias for the transistor from V_{cc}; they function as a feedback branch as well.
- The output impedance network consisting of R_3, L_2, and C_6 confers two advantages, lower part count and wider bandwidth.
- All parts in Figure 1.22 are chip parts and are purchased from MuRata.

Gain Circles and Noise Circles Figure 1.23 shows that for this circuit the noise figure circles overlap the gain circles well enough, although not perfectly. This verifies the assertion of simultaneously approaching both NF_{min} and G_{max}, because Figure 1.23 is obtained due to the satisfaction of condition (1.34).

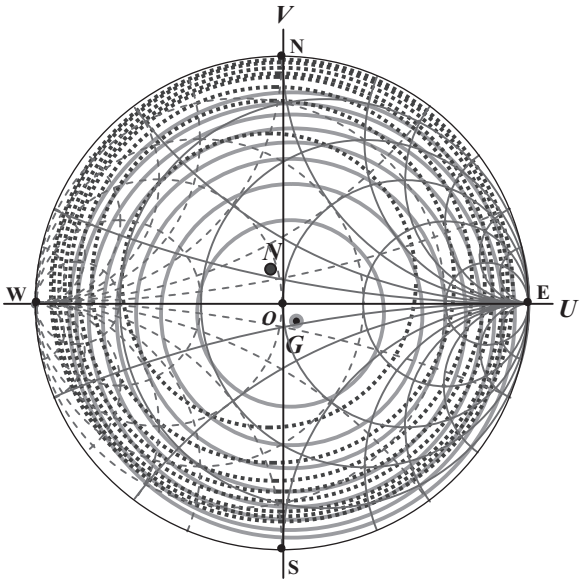


Figure 1.23 Constant gain circles and constant noise figure circles when $f = 150\,MHz$.
Gain circles: $G_{max} = 15\,dB$ at point G, step = $1.0\,dB$.
Noise figure circles: $NF_{min} = 1.75\,dB$ at point N, step = $0.25\,dB$.

1.2.9.2 **LNA *Design for* UHF *Frequency Band*** The *LNA* designed for *UHF* frequency band can be outlined in the following three items:

- Electrical features (Table 1.3),
- The schematic (Figure 1.24),
- The gain and noise circles at the Γ_{in} (input reflection coefficient) plane.

It should be noted that

- The inductor $L_3 = 5.6\,nH$ is the degeneration inductor mentioned above. The resistor $R_6 = 390\,\Omega$ is the "de-Q" resistor. The modified raw device consists of Q_1, L_3, and R_6.
- The capacitors C_4, C_2, and C_6 are "zero" capacitors. Their value is $150\,pF$.
- The resistors $R_3 = R_6 = 390\,\Omega$ are "de-Q" resistors.
- The resistors, R_1 and R_2, are the combination of a voltage divider. They take the DC bias for the transistor from V_{cc}; they function as a feedback branch as well.
- The output impedance network consisting of R_3, L_2, and C_6 confers two advantages, lower part count and wider bandwidth.
- All parts in Figure 1.24 are chip parts and are purchased from MuRata.

TABLE 1.3 Electrical features of *LNA* for *UHF* frequency band

	Specification		Final tested result	
Frequency range	400 *MHz* to 470 *MHz*			
Device	*BFQ67* (Manufacturer: Siemens)			
DC power supply	3	*V*		
Current drain	<4	*mA*	**3.43**	*mA*
Gain	>10	*dB*	**12.0**	*dB*
Noise figure	<2	*dB*	**1.5**	*dB*
IIP_3	>0	dB_m	**5.0**	dB_m
Input return	<–10	*dB*	**–17.8**	*dB*
Output return	<–10	*dB*	**–16.0**	*dB*

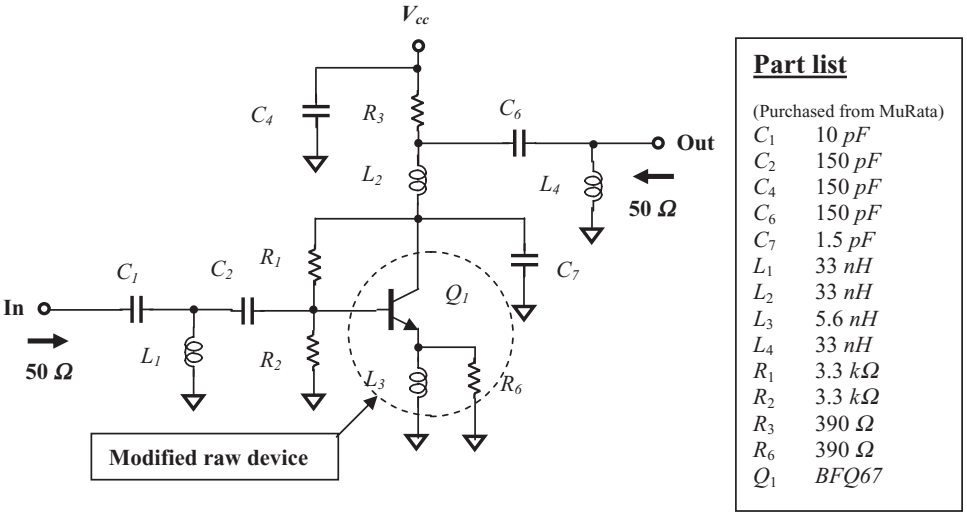
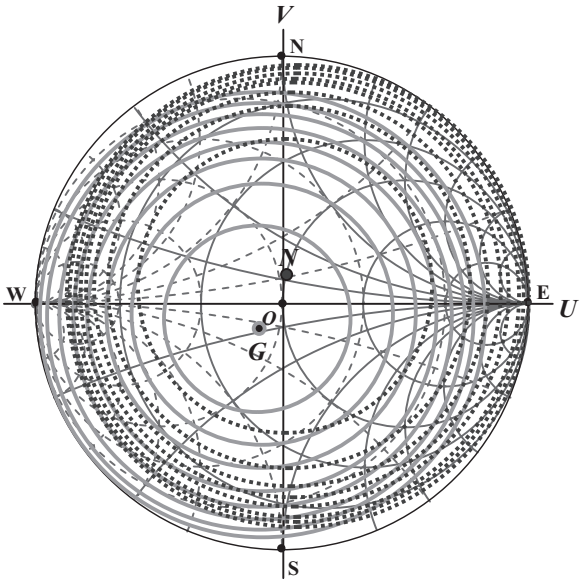


Figure 1.24 *LNA* designed for *UHF* frequency band.

Gain Circles and Noise Circles Figure 1.25 shows that for this circuit the noise figure circles overlap with the gain circles well enough, although not perfectly. This verifies the assertion of simultaneously approaching both NF_{min} and G_{max}, because Figure 1.25 is obtained due to the satisfaction of condition (1.34).

1.2.9.3* LNA *Design for 800/900* MHz *Frequency Band The *LNA* designed for 800/900 *MHz* frequency band is outlined in the following three items:

- Electrical features (Table 1.4),
- The schematic (Figure 1.26),
- The gain and noise circles at the Γ_{in} (input reflection coefficient) plane.



Input reflection coefficient Γ_S plane

Figure 1.25 Constant gain circles and constant noise figure circles when $f = 450\,MHz$.
Gain circles: $G_{max} = 12\,dB$ at point G, step = $1.0\,dB$.
Noise figure circles: $NF_{min} = 1.5\,dB$ at point N, step = $0.25\,dB$.

TABLE 1.4 Electrical features of *LNA* for 800/900 *MHz*

	Specification		Final tested result	
Frequency range		850 *MHz* to 940 *MHz*		
Device		*BFQ67* (Manufactured by Siemens)		
DC power supply	3	*V*		
Current drain	<4	*mA*	**3.48**	*mA*
Gain	>10	*dB*	**11.0**	*dB*
Noise figure	<2	*dB*	**1.8**	*dB*
IIP_3	>0	dB_m	**8.6**	dB_m
Input return	<–10	*dB*	**–11.7**	*dB*
Output return	<–10	*dB*	**–17.0**	*dB*

It should be noted that

- The inductor $L_3 = 4.7\,nH$ is the degeneration inductor mentioned above. The resistor $R_6 = 390\,\Omega$ is the "de-Q" resistor. The modified raw device consists of Q_1, *L3*, and R_6.
- The capacitors, C_4, C_2, and C_6 are "zero" capacitors. Their value is $39\,pF$.
- The resistors $R_3 = R_6 = 390\,\Omega$ are "de-Q" resistors.

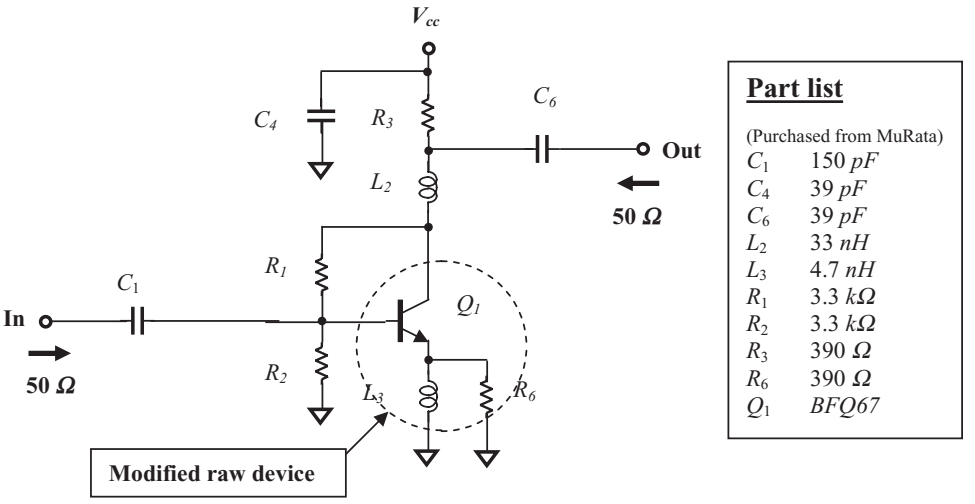


Figure 1.26 *LNA* designed for 800/900 *MHz*.

- The resistors, R_1 and R_2, are the combination of a voltage divider. They take the *DC* bias for the transistor from V_{cc}; they function as a feedback branch as well.
- The output impedance network consisting of R_3, L_2, and C_6 confers two advantages, lower part count and wider bandwidth.
- All parts in Figure 1.26 are chip parts and are purchased from MuRata.

Gain Circles and Noise Circles Figure 1.27 shows that for this circuit the noise figure circles are adequate, though not perfect, and overlap the gain circles. It verifies that the correctness of the assertion of simultaneously approach to both NF_{min} and G_{max}, because Figure 1.27 is obtained due to the satisfaction of the condition (1.34).

1.3 SINGLE-ENDED CASCODE *LNA*

1.3.1 Bipolar *CE-CB* Cascode Voltage Amplifier

Figure 1.28 shows a bipolar *CE-CB* cascode amplifier. The first stage is a voltage amplifier with a *CE* (Common Emitter) configuration because its emitter is the common *AC* and *DC* grounded terminal of the input and output. The second stage is a voltage amplifier with a *CB* (Common Base) configuration because its base is the common *AC* grounded terminal of the input and output. The collector of the first *CE* stage is connected to the emitter of the second *CB* stage. The input terminal is the base of the first *CE* stage, the output terminal is the collector of the second *CB* stage. *RF* chokes and a "zero" capacitor, C_{zero}, are connected to the devices for *DC* bias. In the operating frequency range, the impedance of the *RF* choke is assumed to approach infinity and the impedance of the capacitor C_{zero} is assumed to approach zero.

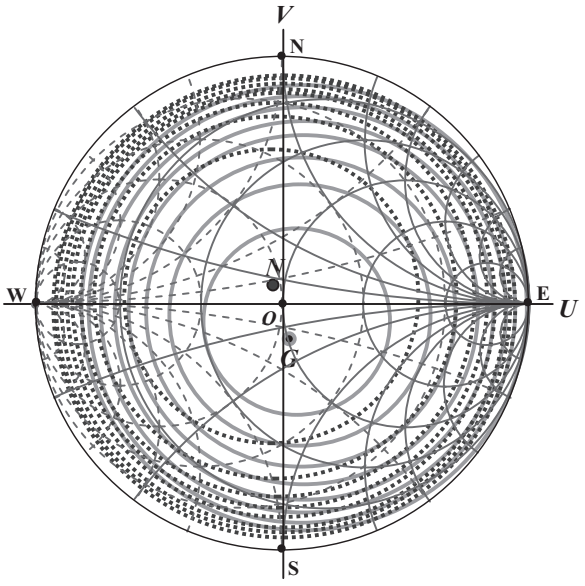


Figure 1.27 Constant gain circles and constant noise figure circles when $f = 850\,MHz$.
Gain circles: $G_{max} = 11\,dB$ at point G, step = $1.0\,dB$.
Noise figure circles: $NF_{min} = 1.8\,dB$ at point N, step = $0.25\,dB$.

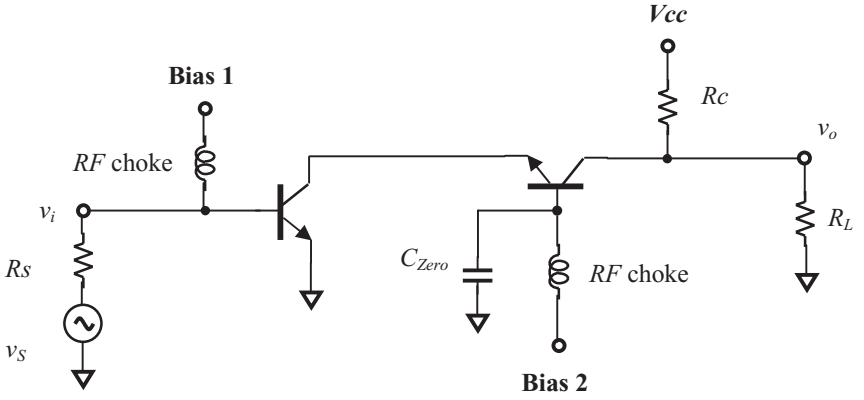


Figure 1.28 A bipolar cascode amplifier.

The equivalent of the bipolar cascode amplifier is shown in Figure 1.29(a). In order to simplify the analysis, let's consider the cases of low frequencies so as to neglect all the capacitors in the transistors, which is shown in Figure 1.29(b). Also, the resistors r_b, r_c and r_μ are neglected. In this section, the subscript "1" denotes the parameter in the first stage, the subscript "2" denotes the parameter in the second stage, the subscript "*i*" denotes the input parameter, the subscript "*o*" denotes the output parameter.

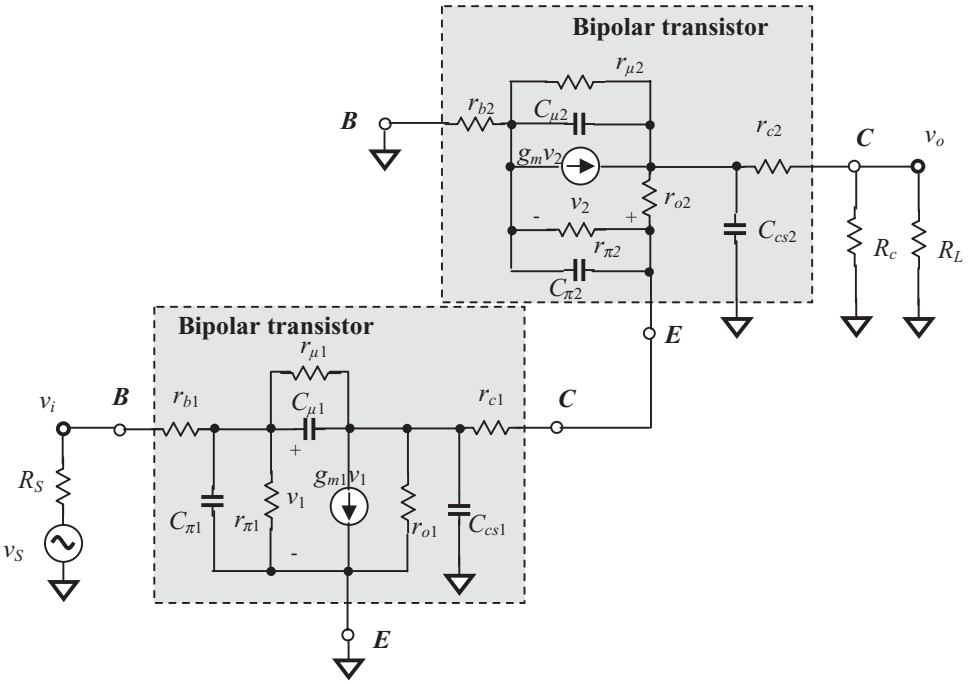


Figure 1.29(a) Equivalent circuit of bipolar cascode amplifier with *CE-CB* configuration.

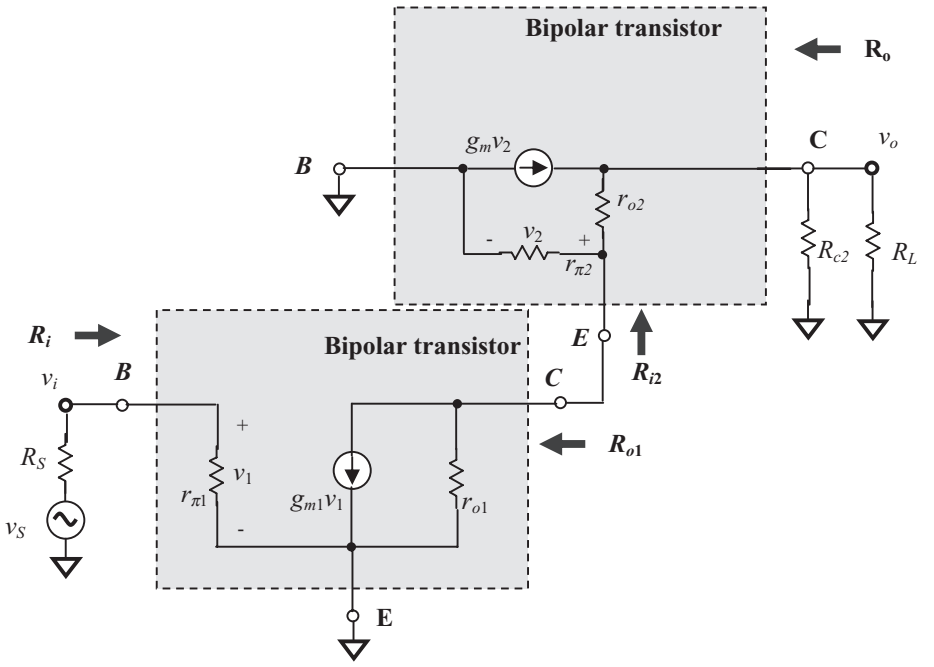


Figure 1.29(b) Equivalent circuit of bipolar cascode amplifier with *CE-CB* configuration at low frequencies, neglecting the resistors, r_b, r_μ, and r_c.

The input resistance of the cascode amplifier R_i is the input resistance of the first *CE* stage R_{i1}. Obviously, from Figure 1.29(b), it can be seen that

$$R_i = R_{i1} = r_{\pi 1}. \tag{1.104}$$

The output resistance of the first *CE* stage R_{o1} is the output impedance contributed by the first *CE* portion only when $v_S = v_1 = 0$ so that the generator $g_{m1}v_1$ is inactive. Then,

$$R_{o1} = r_{o1}. \tag{1.105}$$

The input resistance of the second *CB* amplifier is

$$R_{i2} = r_{e2} = \frac{1}{g_{m2} + \dfrac{1}{r_{\pi 2}}} = \frac{1}{1+\beta_2} r_{\pi 2} \approx \frac{r_{\pi 2}}{\beta_2}, \tag{1.106}$$

(discussed in Section 12.5, Chapter 12). It should be noted that the input resistance of the second *CB* stage is dropped by about β times from r_π in *CE* stage alone.

The output resistance is contributed by the upper *CB* portion only when $v_S = v_1 = 0$, so that the generator $g_{m1}v_1$ is inactive. The bottom portion looks just like a single resistor, r_{o1}. The entire *CE-CB* amplifier is equivalent to a *CE* stage with a degeneration resistor r_{o1} and a *AC* grounded input terminal. The output resistance has been formularized as

$$R_o = r_{o2}\left(1 + \frac{g_{m2}r_{o1}}{1 + \dfrac{g_{m2}r_{o1}}{\beta_2}}\right). \tag{1.107}$$

(Refer to: Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, John Wiley & Sons, Inc., 2004, 4th edition, pp. 197–207.)

If $$g_{m2}r_{o1} >> \beta_2 >> 1, \tag{1.108}$$

then $$R_o \approx \beta_2 r_{o2}. \tag{1.109}$$

It should be noted that in the derivation of (1.107), the resistor R_c in the second *CB* stage and the load R_L are ignored. Of course, they can never be neglected in *RF* circuit design.

From equation (1.109) it can be found that the *CE-CB* cascade amplifier displays an output resistance about β times higher than that in the *CE* stage alone.

Now let us consider the voltage and current gain.

The voltage gain of the first *CE* stage A_{v1} is not that expected from a normal *CE* stage, $A_{v1} = -g_{m1}r_{o1}$. The output resistor r_{o1} of the first *CE* stage is connected with

the input resistor R_{i2} of the second *CB* stage in parallel. As shown in equation (1.106), the input resistance of the second *CB* stage is dropped by about β times from the r_π in a normal *CE* stage; consequently,

$$A_{v1} = -g_{m1} r_{o1} \,//\, R_{i2} \approx -g_{m1} \frac{r_{\pi 2}}{\beta_2}, \tag{1.110}$$

if the input voltage v_i but not v_S is considered as the reference for the voltage gain.

Should the main parameters of the *CE* and *CB* transistor be equal, that is,

$$g_{m1} = g_{m2}, \tag{1.111}$$

$$r_{\pi 1} = r_{\pi 2}, \tag{1.112}$$

and

$$\beta_1 = \beta_2, \tag{1.113}$$

then equation (1.110) becomes

$$A_{v1} = -1. \tag{1.114}$$

The current gain of first *CE* stage A_{i1} is

$$A_{i1} = \beta. \tag{1.115}$$

The current gain of second stage A_{i2} is

$$A_{i2} \approx 1, \tag{1.116}$$

because the input current is almost equal to its output current in the second *CB* stage.

$$I_{i2} \approx I_{o2} \quad \text{and} \quad i_{i2} \approx i_{o2}, \tag{1.117}$$

where the upper case letter 'I' denotes the *DC* current and the lower case letter '*i*' denotes the *AC* current.

From (1.115) and (1.116), the total current gain is

$$A_i \approx A_{i1} A_{i2} \approx \beta. \tag{1.118}$$

The trans-conductance from the input to output is

$$G_m = g_{m1}, \tag{1.119}$$

since $A_{i2} \approx 1$ as shown in (1.116).

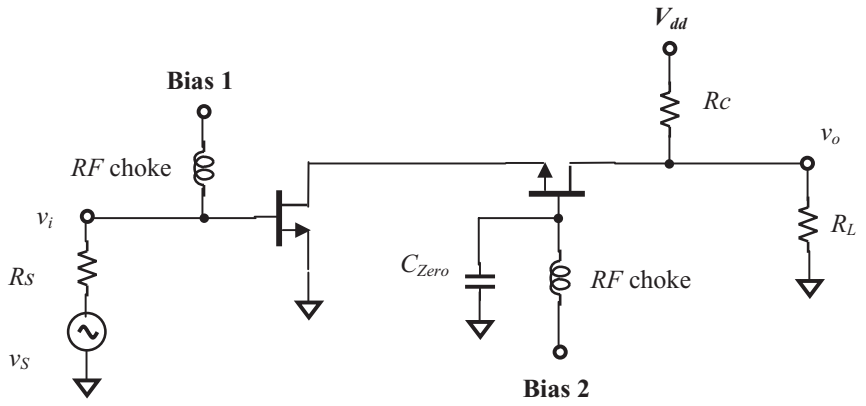


Figure 1.30 A *MOSFET* cascode amplifier.

The total voltage gain is

$$A_v = \frac{v_o}{v_i} \approx -G_m R_o \approx -g_{m1} r_{o2} \beta_2. \tag{1.120}$$

1.3.2 *MOSFET CS-CG* Cascode Voltage Amplifier

Figure 1.30 shows a *MOSFET CS-CG* cascode amplifier. The first stage is a voltage amplifier with a *CS* (Common Source) configuration because its source is the common *AC* and *DC* grounded terminal of the input and output. The second stage is a voltage amplifier with a *CG* (Common Gate) configuration because its gate is the common AC grounded terminal of the input and output. The drain of the first *CS* stage is connected with the source of the second *CG* stage. The input terminal is the gate of the first *CS* stage and the output terminal is the drain of the second *CG* stage. *RF* chokes and a "zero" capacitor, C_{zero}, are connected to the devices for *DC* bias. In the operating frequency range, the impedance of the *RF* choke is assumed to approach infinity and the impedance of the capacitor C_{zero} is assumed to approach zero.

The equivalent of the *MOSFET* cascode amplifier is shown in Figure 1.31. In order to simplify the analysis, let's consider the cases of low frequencies only so as to neglect all the capacitors in the transistors, shown in Figure 1.32. Also, the resistors r_b, r_c and r_μ are neglected. Figure 1.31 shows the equivalent circuit of the *MOSFET* cascode amplifier with a *CS-CG* configuration at low frequencies.

The input resistance of the *CS-CG* cascode amplifier is the input resistance of the first *CS* stage. Obviously, from Figure 1.32, it can be seen that

$$R_i \to \infty, \tag{1.121}$$

The output resistance of the first *CS* stage is contributed by the first *CS* portion only when $v_S = v_1 = 0$ so that the generator $g_{m1}v_1$ is inactive, then

$$R_{o1} = r_{o1}. \tag{1.122}$$

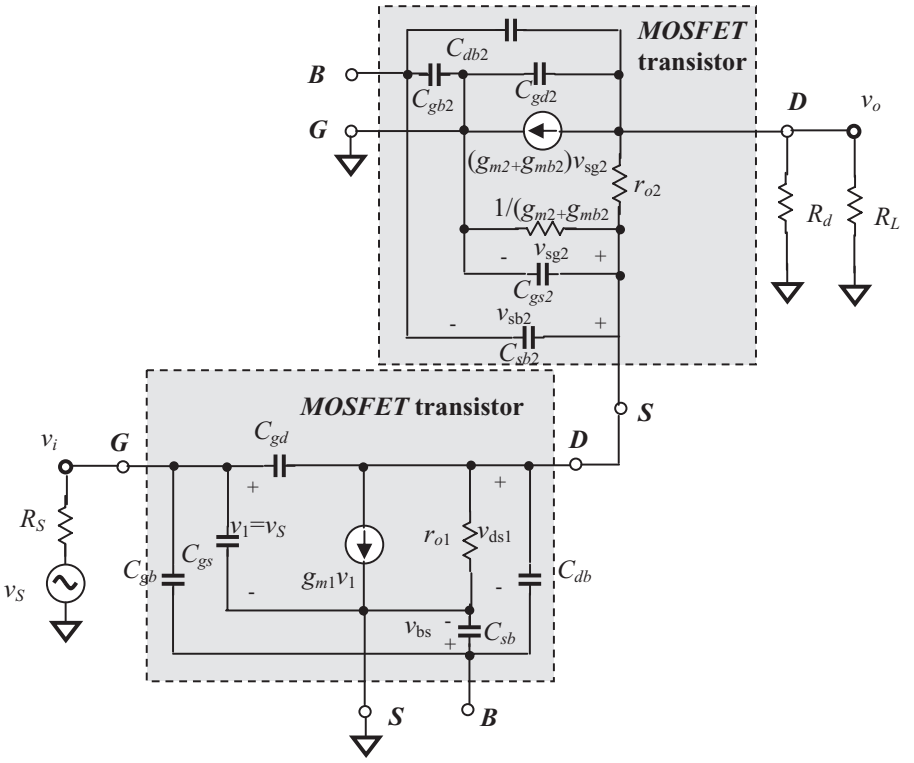


Figure 1.31 Equivalent circuit of a *MOSFET* cascode amplifier with *CS-CG* configuration.

In terms of *KCL* at the output and at the source of the second *CG* stage, the input resistance of the second *CG* amplifier is

$$R_{i2} = \frac{1}{(g_{m2} + g_{mb2})} + \frac{R'_L}{(g_{m2} + g_{mb2})r_{o2}}, \tag{1.123}$$

where

$$R'_L = R_d \,//\, R_L = \frac{R_d}{R_D + R_L} R_L, \tag{1.124}$$

and the trans-conductance is derived when $R'_L = 0$ so that $v_o = 0$, that is

$$G_m \approx g_{m1}, \tag{1.125}$$

The output resistance can be found when the g_{m1} generator is inactive, that is $v_i = 0$. Consequently the *CS* portion becomes a simple resistor r_{o1} and the entire cascode looks like a *CG* device with a source degeneration resistor. Then,

$$R_o = r_{o2} + r_{o1}[1 + (g_{m2} + g_{mb2})]r_{o2} \approx (g_{m2} + g_{mb2})r_{o1}r_{o2}, \tag{1.126}$$

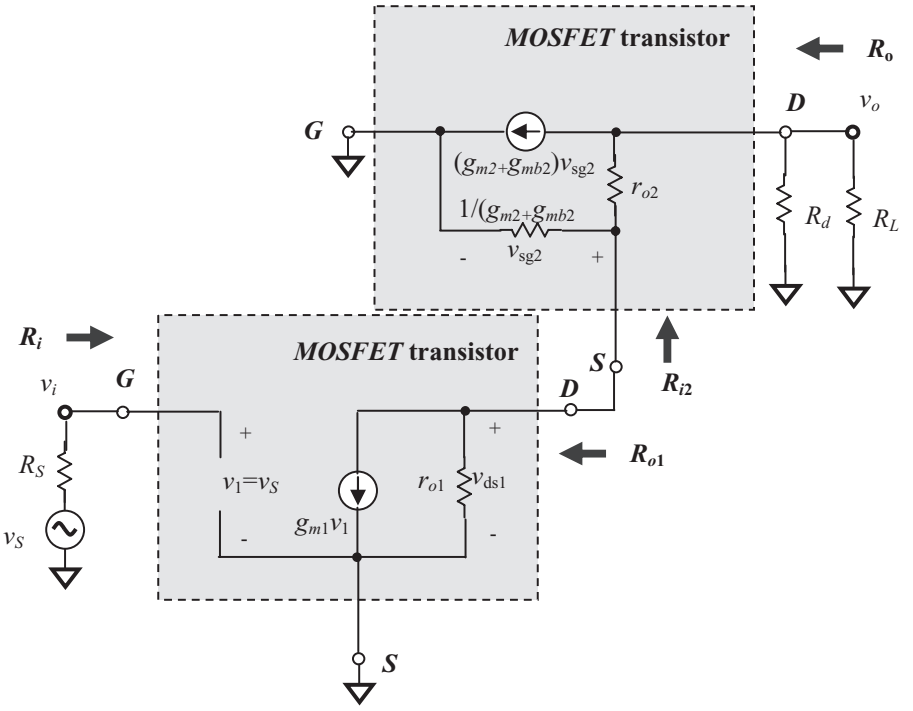


Figure 1.32 Equivalent circuit of *MOSFET* cascode amplifier with *CS-CG* configuration at low frequencies.

if

$$R_L' \to \infty, \tag{1.127}$$

(Refer to Paul R. Gray et al., *Analysis and Design of Analog Integrated Circuits*, pp. 208–209.)

Similarly to the *CE-CB* bipolar cascode amplifier, the input resistance of the second *CG* stage is quite low because the second term in equation (1.123) disappears when

$$R_L' = 0, \tag{1.128}$$

It becomes

$$R_{i2} \approx \frac{1}{(g_{m2} + g_{mb2})}. \tag{1.129}$$

which usually happens in cases where

$$R_{i2} << r_{o1}. \tag{1.130}$$

Now let us consider the voltage and current gain.

The voltage gain of the first *CS* stage is not that as expected from a normal *CS* stage, $A_{v1} = -g_{m1}r_{o1} // R_d$. The output resistor r_{o1} of the first *CS* stage is connected with the input resistor R_{i2} of the second *CG* stage in parallel. As shown in equation (1.129), the input resistance of the second *CG* stage is dropped by a good deal and is much lower than that of r_{o1} in a normal *CS* stage; consequently,

$$A_{v1} = -g_{m1}r_{o1} // R_{i2} \approx -g_{m1}R_{i2} \approx -\frac{g_{m1}}{g_{m2} + g_{mb2}}, \tag{1.131}$$

if the input voltage v_i but not v_S is considered as the reference for the voltage gain.

If the trans-conductances of the *CS* and *CG* transistors are the same, that is,

$$g_{m1} = g_{m2}, \tag{1.132}$$

then equation (1.131) becomes

$$A_{v1} \approx -1, \tag{1.133}$$

The current gain of first *CS* stage is

$$A_{i1} \to \infty. \tag{1.134}$$

The current gain of second *CG* stage is

$$A_{i2} \approx 1, \tag{1.135}$$

because the input current is almost equal to its output current in the second *CG* stage, that is

$$I_{i2} \approx I_{o2} \quad \text{and} \quad i_{i2} \approx i_{o2}, \tag{1.136}$$

where the upper case letter '*I*' denotes the *DC* current and the lower case letter '*i*' denotes the *AC* current.

Finally the total voltage gain can be evaluated from equations (1.124) and (1.126)

$$A_v = \frac{v_o}{v_i} \approx -G_m R_o \approx -g_{m1}(g_{m2} + g_{mb2}) r_{o1} r_{o2}. \tag{1.137}$$

1.3.3 Why Cascode?

Let's summarize the reasons why the cascode amplifier is superior to other amplifiers.

It increases the output impedance, which is particularly useful in desensitizing bias references from variations in power supply voltage and in achieving large amounts of voltage gain.

This is very beneficial to the digital circuit design. Digital circuits always operate under high impedances; the high output impedance of a cascode amplifier provides a powerful way to reach the goal of high voltage gain.

However, this remarkable advantage does not excite the *RF* circuit designers because RF circuits always operate under low impedances. *RF* designers pursue power gain but not voltage gain; here, high voltage gain does not make too much sense if its current gain is low.

However, both *RF* circuit designers and digital circuit designers are excited about these three advantages of the cascode amplifier.

1) It alleviates the Miller effect on a voltage amplifier.
   Unwanted capacitive feedback always exists in a voltage amplifier with a *CE* or *CS* configuration. Alleviating the Miller effect therefore allows the amplifier operation at higher frequencies than would otherwise be possible.
   The input impedance of the second *CG* stage is

$$R_{i2} = \frac{r_{\pi 2}}{\beta_2}, \tag{1.138}$$

   which is β_2 times lower than the input impedance of a *CE* stage if the same device is applied to both stages. The voltage gain of the first stage is low due to its output impedance being pulled down by the low input impedance of the second stage, that is

$$A_{v1} = -g_{m1}R'_{L1} // R_{i2} = -g_{m1}R'_{L1} // \frac{r_{\pi 2}}{\beta_2} \approx -g_{m1}\frac{r_{\pi 2}}{\beta_2} \approx 1, \tag{1.139}$$

   if

$$g_{m1} = g_{m2}. \tag{1.140}$$

   Consequently, the input Miller capacitance in the first stage is kept the same as C_μ due to the low voltage gain.

$$C_{i,miller} = C_\mu A_{v1} \approx C_\mu, \tag{1.141}$$

   Owing to the low Miller capacitance, the bandwidth in the first stage will be increased from

$$\omega_{T1} = \frac{g_{m1}}{C_{\pi 1} + C_{\mu 1}A_{v1}}, \tag{1.142}$$

   to

$$\omega_{T1} = \frac{g_{m1}}{C_{\pi 1} + C_{\mu 1}}. \tag{1.143}$$

The bandwidth of the entire *CS-CB* cascode amplifier is then mainly determined by the second stage, that is,

$$\omega_{T2} = \frac{g_{m2}}{C_{\mu 2}}. \tag{1.144}$$

It is therefore concluded that the bandwidth of the *CS-CB* cascode amplifier is approximately equivalent to the bandwidth of the single *CB* amplifier, which is much higher than that of a single *CE* amplifier.

This wide bandwidth is an outstanding advantage, which is why the cascode amplifier is widely applied in the amplifier design.

2) Better isolation
The *CB* configuration of the second stage guarantees isolation between output and input. The base of the bipolar transistor is grounded and the capacitive feedback from the output to input is reduced to an insignificant level. In addition, the low input impedance of the second stage is also beneficial to the isolation between output and input.
3) It can magnify the signal: not only the voltage but also the power of the signal as well.
In a cascade amplifier, the current is magnified in the first *CE* stage and the voltage is magnified in the second *CB* stage. Consequently, the voltage and power of signal can be magnified simultaneously, therefore satisfying both digital and *RF* circuit designers.

1.3.4 An Example

This is an *LNA RFIC* design example, which is designed for group #1, Band #2 of *UWB* (Ultra Wide Band) system. The main electrical features are

- *DC* power supply: $V_{dd} = 1.2\,V$,
- Current drain: $I_{total} < 5\,mA$,
- Operating frequency range: f = 3.696 to 4. $4224\,GHz$,
- Gain: $G > 12$ dB,
- Input return loss: $S_{11} < -10\,dB$,
- Output return loss: $S_{22} < -10\,dB$,
- Noise figure: $NF < 2.5$ dB,
- Third order input intercept point: $IIP_3 > 5\,dBm$,
- Second order input intercept point: $IIP_2 > 35\,dBm$.

In consideration of the bandwidth, it is decided to use the cascode configuration, because its relative bandwidth is

$$BW = \frac{\Delta f}{f} = \frac{4224 - 3696}{(4224 + 3696)/2} = \frac{528}{3960} = 13.3\%. \tag{1.145}$$

This can be categorized as neither a narrow- nor wide-band block. Usually, a block or a system with a relative bandwidth greater than 15% is considered a wide-band block or system; conversely, a block or a system with a relative bandwidth of less than 15% is considered a narrow-band block or system. We are hence quite hesitant to consider this design sample as a narrow-band block because 13.33% is close to 15%.

TSMC 90*nm, CMOS* is selected to be the *IC* processing, and *n*-channel *MOSFET* transistors are chosen to be the *CS-CG* device. The size of the device is calculated based on the considerations described in Section 1.2.1.

1.3.4.1 Raw Device Testing Figure 1.33 shows the setup for raw device testing. The raw device is a combination of two transistors, M_1 and M_2. All the capacitors are "zero" capacitors and all the inductors are "infinite" inductors. At the operating frequencies, the impedance of a "zero" capacitor approaches zero and the impedance of an "infinite" inductor approaches infinity.

Figure 1.34(a) shows the tested *S* parameters and the optimum input reflection coefficient $\Gamma_{S,opt}$ on the Smith chart; Figure 1.34(b) shows the frequency response of the *S* parameters. The intermediate frequency, $f = 3.96\,GHz$, is marked with a dot on each trace.

The first impression is that the *CS-CG* configuration of the raw devices exhibits wide-band behavior as expected. In Figure 1.34(a), all of the traces corresponding to the entire frequency band, 3.696 to 4.224 GHz, are squeezed to a small trace segment on the Smith chart, and in Figure 1.34(b) the trace is quite flat over the entire frequency band.

The second impression is that, unfortunately, the optimum input reflection coefficient $\Gamma_{S,opt}$ is not at the expected location, which is supposed to be conjugate to S_{11}. The raw devices must be modified so that the overlapping condition (1.34) of maximum gain and minimum noise figure can be satisfied.

The magnitudes of the *S* parameters shown in Figure 1.34(b) can be outlined as follows:

$$2.45\,dB < S_{21} < 2.58\,dB, \quad \text{when } 3.696\,GHz < f < 4.224\,GHz, \tag{1.146}$$

$$S_{21} = 2.50\,dB, \quad \text{when } f = 3.960\,GHz, \tag{1.147}$$

$$-2.75\,dB < S_{11} < -2.20\,dB, \quad \text{when } 3.696\,GHz < f < 4.224\,GHz, \tag{1.148}$$

$$S_{11} = -2.5\,dB, \quad \text{when } f = 3.960\,GHz, \tag{1.149}$$

$$-0.19\,dB < S_{22} < -0.17\,dB, \quad \text{when } 3.696\,GHz < f < 4.224\,GHz, \tag{1.150}$$

$$S_{22} = -0.18\,dB, \quad \text{when } f = 3.960\,GHz, \tag{1.151}$$

For now, we will not worry about the low gain, poor return losses, stability, or other issues, because the input and output impedances are not matched yet. Let's go ahead to modify the raw devices. This modification is usually conducted many times, depending on how much experience the designer has. Figure 1.35 shows the final attempt, which is believed the best one, in which a degeneration inductor is connected between the source of the *CS* device and ground:

$$L_{\mathrm{deg}\,en} = 0.45\,nH, \tag{1.152}$$

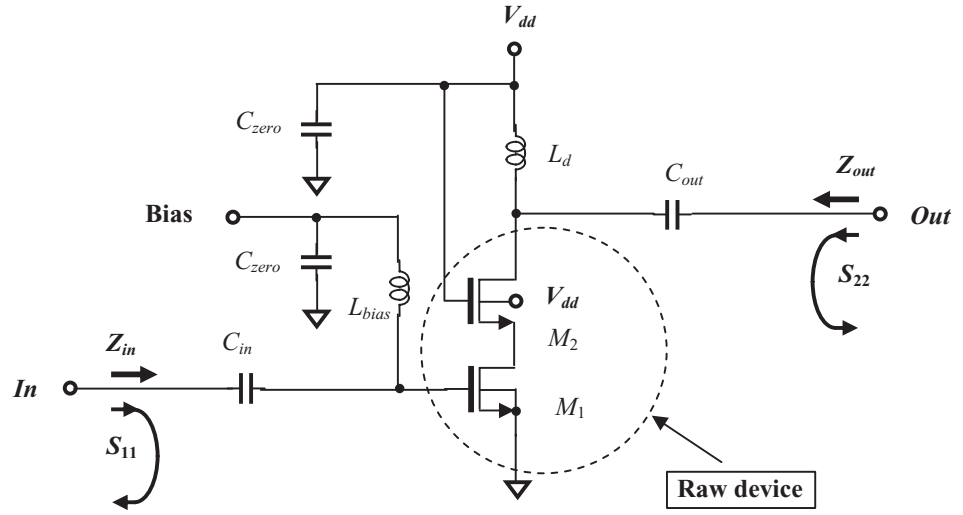
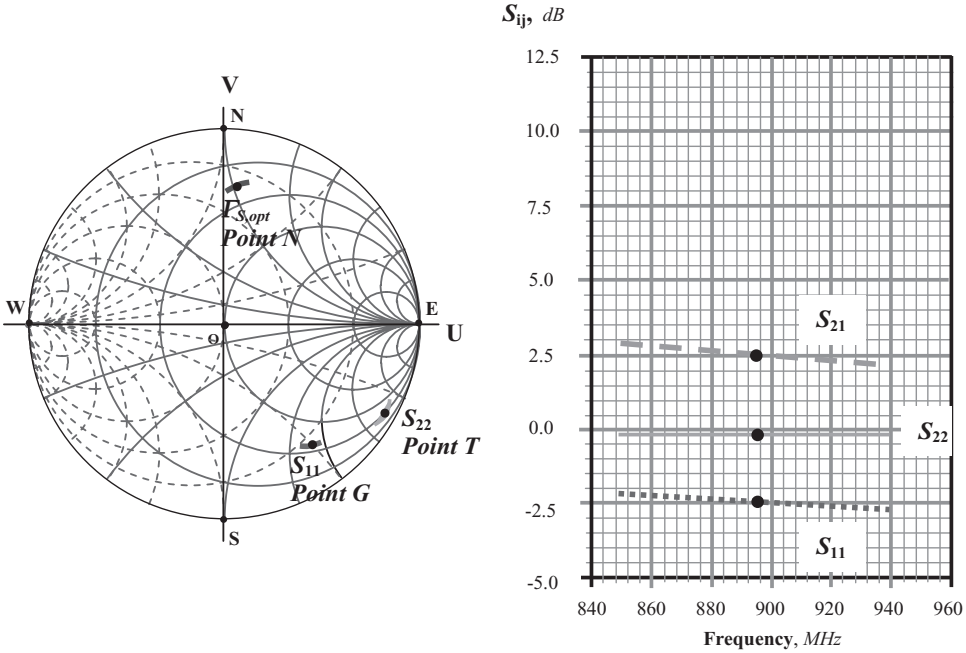


Figure 1.33 Schematic of a cascode *LNA* for raw device testing. C_{in}, C_{out}, C_{zero}: "zero" capacitor; L_{bias}, L_d: "infinite" inductor.



(a) S_{11}, S_{22} and $\Gamma_{S,opt}$ on Smith chart

(b) Magnitude of S_{ij}, *dB*

Figure 1.34 *S* parameters from raw device testing. (The intermediate frequency $f = 3.96\,GHz$ is marked by a dot on each trace.)

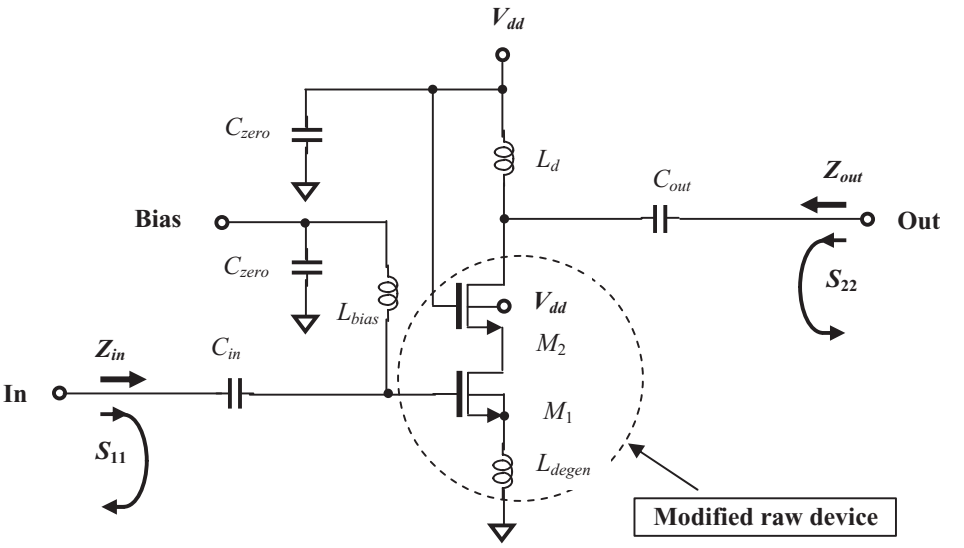


Figure 1.35 Schematic of setup for modified raw device testing. C_{in}, C_{out}, C_{zero}: "zero" capacitor; L_{bias}, L_d: "infinite" inductor.

The degeneration inductor, L_{degen}, is a simple and tiny part. In the *RFIC* circuit design for the operating frequency range of GHz, it is about 0.5 to 2 turns, with approximately a tenth to a couple nH of inductance.

Figure 1.36(a) shows the tested S parameters and the optimum input reflection coefficient $\Gamma_{S,opt}$ on the Smith chart from the modified raw device testing. The optimum input reflection coefficient $\Gamma_{S,opt}$ is at the expected location, which is very close to S_{11}^*. This means that the raw devices are quite close to fitting the overlapping condition of maximum gain and minimum of noise, (1.34), although $\Gamma_{S,opt}$ does not exactly overlap S_{11}^*. A little deviation is inevitable, mirroring a philosophy of life: "Nobody is perfect and nothing is perfect!"

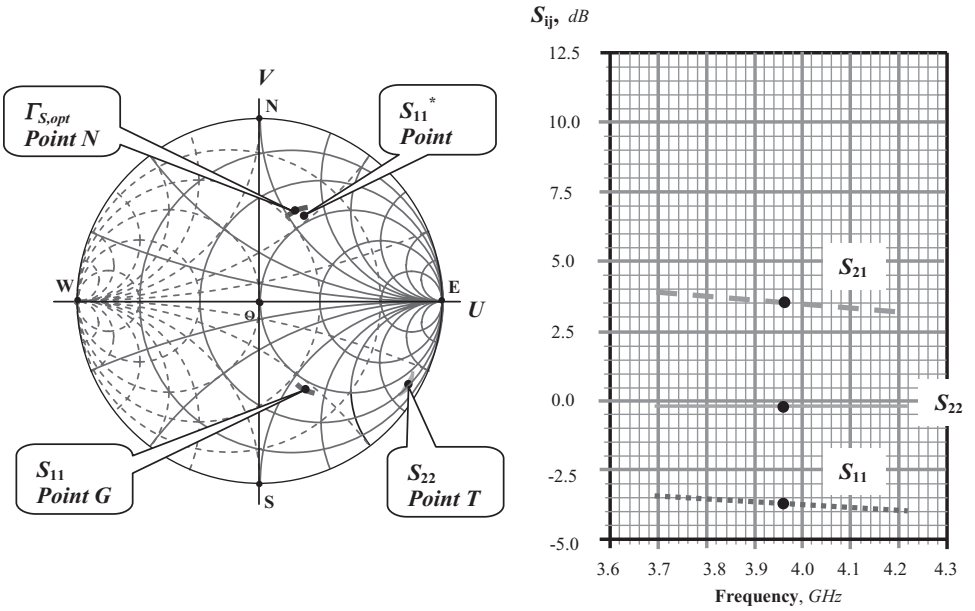
Again, at this point, we are not worrying too much about the magnitude of the S parameters shown in Figure 1.36(b) which is far from the stated goals, because the input and output impedances are still not matched.

1.3.4.2 Gain and Bandwidth Impedance matching is one of the key issues in *RF* circuit design. A new designer without *RF* circuit design experience might need to spend a lot of time on it. Let's spend some time demonstrating the process of impedance matching in this example.

The first try to implement the impedance matching network is shown in Figure 1.37: it consists of parts

- In the input impedance network: $L_{S,in} = 4\,nH$, $C_{S,in} = 10\,pF$;
- In the output impedance network: $L_{P,out} = 10\,nH$ and $R_{P,out} = 500\,\Omega$, $C_{S,out} = 1\,pF$.

The inductor $L_{S,in} = 4\,nH$ is the main part in the input impedance matching network, by which the trace of S_{11} is supposed to be pulled to a location near the center of



(a) S_{11}, S_{22} and $\Gamma_{S,opt}$ on Smith chart (b) Magnitude of S_{ij}, *dB*

Figure 1.36 *S* parameters from modified raw device testing. (The intermediate frequency $f = 3.96\,GHz$ is marked by a dot on each trace.)

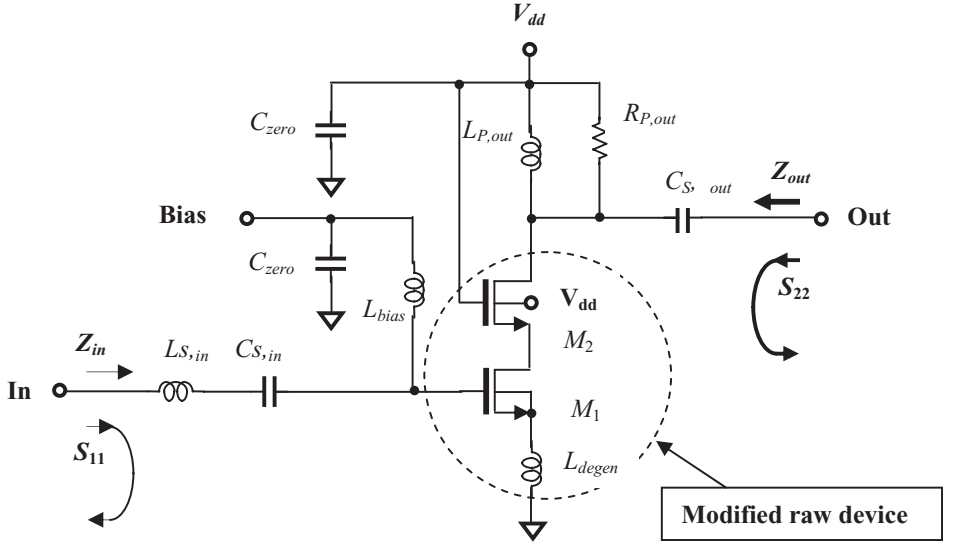


Figure 1.37 Impedance matching by parts. At input: $L_{S,in} = 4\,nH$, $C_{S,in} = 10\,pF$. At output: $L_{P,out} = 10\,nH$, $R_{P,out} = 500\,\Omega$, and $C_{S,out} = 1\,pF$.

the Smith chart, which corresponds to the reference impedance point $50\,\Omega$. The capacitor $C_{S,in} = 10\,pF$ functions as the DC blocking part because at the operating frequency range its impedance is very low, such that

$$Z_{10\,pF} = \frac{1}{j\omega C} = -j\frac{1}{2\pi fC} = 4.02\,\Omega, \qquad \text{when } f = 3960\,MHz. \tag{1.153}$$

The inductor $L_{P,out} = 10\,nH$ is the main part in the output impedance matching network, by which the trace of S_{22} is supposed to be pulled counter-clockwise up to a location near the $50\,\Omega$ resistance circle along the constant conductance circle; then, the capacitor $C_{S,out} = 1\,pF$ is the next part, by which the S_{22} is drawn counter-clockwise to a location near the center of the Smith chart, which corresponds to the reference impedance point $50\,\Omega$ along the constant resistance circle. The difference between these two inductors, $L_{S,in}$ and $L_{P,out}$, should be noted. One is in series and the other is in parallel. By means of $L_{S,in}$ in series, the trace of S_{11} is pulled clockwise to the area near the reference impedance point $50\,\Omega$ along the constant resistance circle, while by means of $L_{P,out}$ in parallel, the trace of S_{22} is pulled counter-clockwise to the area near the reference impedance point $50\,\Omega$ along the constant conductance circle.

The raw device shown in Figure 1.35 is unstable because the simulation shows its μ value as

$$\mu = 0.95 < 1. \tag{1.154}$$

Looking at the schematic shown in Figure 1.35, the instability may come from the load inductor, $L_{P,out}$, and the degenerator inductor, L_{degen}. However, in order to retain as much voltage drop across the device as possible, so as to reduce the intermodulation, I prefer to use a load inductor, $L_{P,out}$, rather than a resistor, even though an inductor is much more expensive than a resistor. On the other hand, in order to satisfy the overlapping condition (1.34) for NF_{min} without significant increase of the noise figure, I prefer to use a degeneration inductor, L_{degen}, rather than a degeneration resistor, R_{degen}. The value of L_{degen}, however, should not be too high, otherwise the gain and stability would both suffer. In design sample, $L_{degen} = 0.45\,nH$, the resistor, $R_{P,out}$, is used to de-Q the load inductor $L_{P,out}$ so as to prevent oscillation. It is the key part in keeping the *LNA* block stable, while the low value of the degeneration inductor L_{degen} provides good assistance.

The values of all the parts shown in the schematic in Figure 1.37 are simultaneously optimized to obtain stability with a reasonable gain and noise figure level, that is,

$$\mu = 1.23 > 1, \tag{1.155}$$

when

$$G = 8.0\,dB, \quad \text{and} \quad f = 3.960\,GHz. \tag{1.156}$$

The μ value shown in (1.155) indicates that the unconditionally stable condition is satisfied.

In summary, the input impedance matching network in this example basically consists of only one part. It is a simple impedance matching network indeed. The output impedance matching network consists of three parts, which is a typical part count in an *LNA* design. In general, impedance matching is difficult and it is one of the main tasks of an *RF* circuit designer. In the chapters about impedance matching, some useful schemes and technologies are presented for more complicated impedance matching networks.

Figure 1.38 displays the tested *S* parameters after the input and output impedance matching networks are implemented.

In the entire operating frequency range, the results are:

$$7.2\,dB < S_{21} < 8.8\,dB, \quad \text{when } 3.696 < f < 4.224\,GHz, \tag{1.157}$$

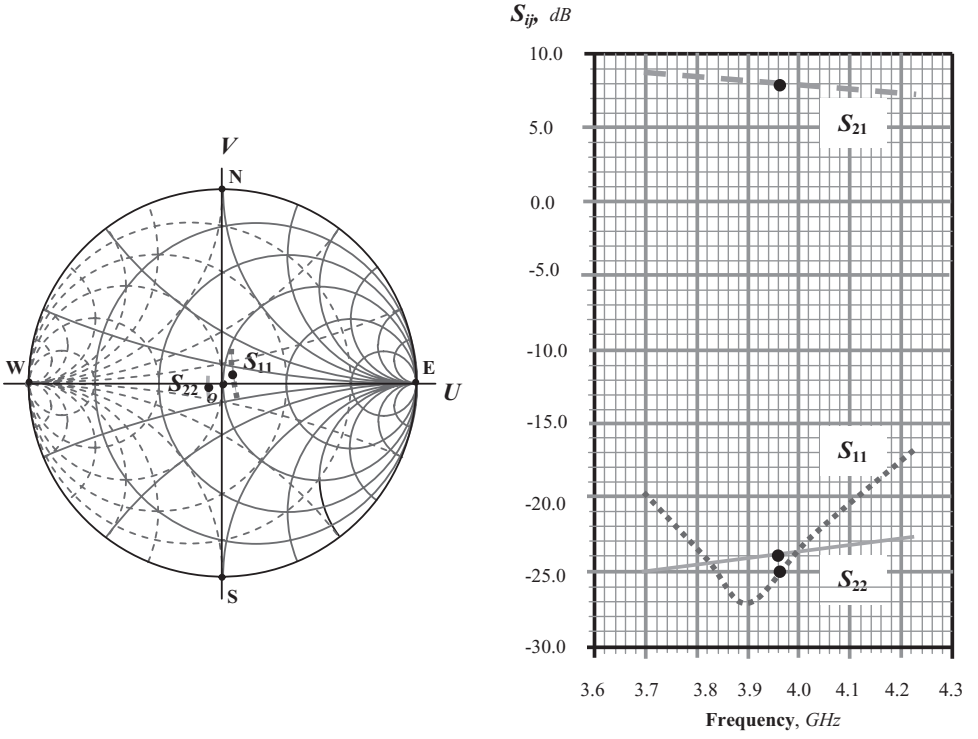
$$S_{21} = 8.0\,dB, \quad \text{when } f = 3.960\,GHz, \tag{1.158}$$

$$-27.1\,dB < S_{11} < -16.9\,dB, \quad \text{when } 3.696 < f < 4.224\,GHz, \tag{1.159}$$

$$S_{11} = -25.0\,dB, \quad \text{when } f = 3.960\,GHz, \tag{1.160}$$

$$-25.0\,dB < S_{22} < -23.7\,dB, \quad \text{when } 3.696 < f < 4.224\,GHz, \tag{1.161}$$

$$S_{22} = -23.9\,dB, \quad \text{when } f = 3.960\,GHz. \tag{1.162}$$



(a) S_{11} and S_{22} on Smith chart

(b) Magnitude of S_{ij}, *dB*

Figure 1.38 *S* parameters after input and output impedances are matched by parts. (The intermediate frequency $f = 3.96\,GHz$ is marked by a dot on each trace.) At input: $L_{S,in} = 4\,nH$, $C_{S,in} = 10\,pF$. At output: $L_{P,out} = 10\,nH$, $R_{P,out} = 500\,\Omega$, and $C_{S,out} = 1\,pF$.

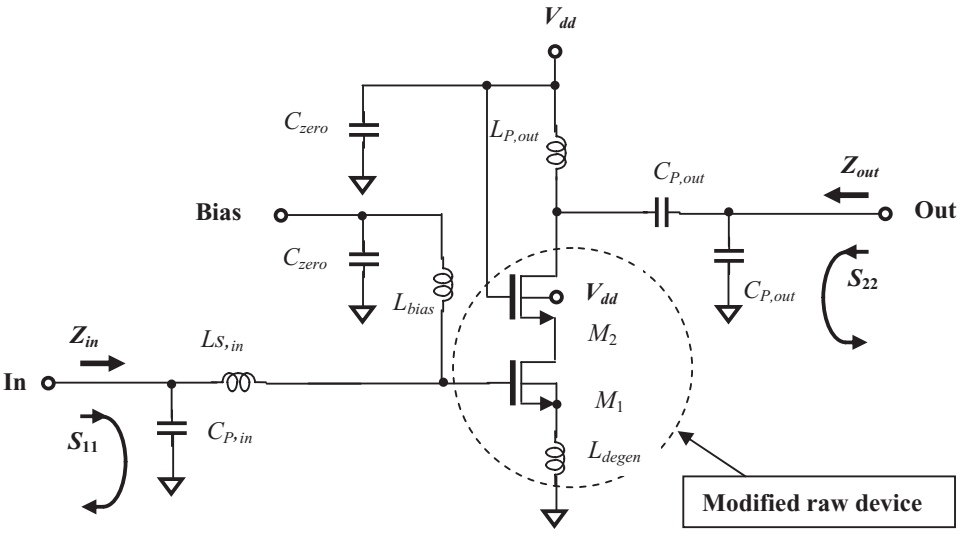


Figure 1.39 Modified impedance matching by parts. At input: $C_{P,in} = 0.3\,pF$, $L_{S,in} = 3.3\,nH$. At output: $L_{P,out} = 5\,nH$, $C_{P,out} = 0.13\,pF$, and $C_{S,out} = 0.3\,pF$.

By comparing the locations of S_{11} and S_{22} shown in Figures 1.36 and 1.38, it can be found that either the S_{11} or S_{22} traces are not moved exactly along the resistance or conductance circles. Both traces are moved to the location with higher resistance. In other words, the corresponding resistances of S_{11} and S_{22} as shown in Figure 1.38 are increased from those in Figure 1.36. This is due to the inductors $L_{S,in}$ and $L_{P,out}$, which are low Q parts and bring about additional resistance. The Q value of inductors applied in this section is assumed to be 10, which is a reasonable value in today's *RFIC* design.

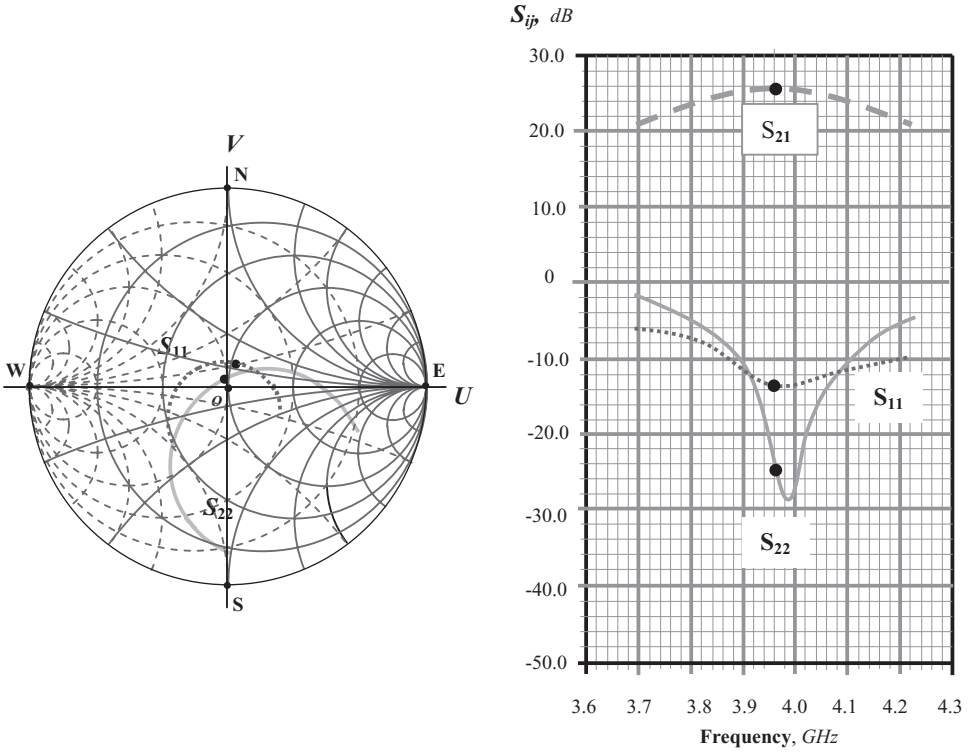
The input and output impedances are matched well and the *LNA* is in a stable state. **However, the gain, S_{21} = 8.0 to 9.0 *dB*, is too low!**

One solution might be to change the topologies of the input and output impedance networks, even though they are quite simple, as shown in Figure 1.37, and have the feature of wide-band performance, as shown in Figure 1.38.

Figure 1.39 plots the modified impedance matching networks, which consists of parts

- In the input impedance network: $C_{P,in} = 0.3\,pF$, $L_{S,in} = 3.3\,nH$;
- In the output impedance network: $L_{P,out} = 5\,nH$ and $C_{S,out} = 0.13\,pF$, $C_{P,out} = 0.3\,pF$.

The topologies of the input and output impedance matching networks shown in 1.39 are different from those shown in Figure 1.37. In the input impedance network of Figure 1.39, the inductor $L_{S,in} = 3.3\,nH$ plays the same role as the inductor $L_{S,in} = 4\,nH$ in the input impedance network of Figure 1.37. However, after the inductor $L_{S,in} = 3.3\,nH$ is attached to the gate of the device, the location of S_{11} still does not exactly overlap with the center of the Smith chart. This implies that further improvements could be made if the trace S_{11} is made to exactly overlap the center of the Smith chart. This is the our clue or motivation to apply a capacitor, $C_{P,in} = 0.3\,pF$, to



(a) $\boldsymbol{S_{11}}$ and $\boldsymbol{S_{22}}$ on Smith Chart (b) Magnitude of $\boldsymbol{S_{ij}}$, *dB*

Figure 1.40 *S* parameters after input and output impedances are matched by parts. (The intermediate frequency $f = 3.96\,GHz$ is marked by a dot on each trace.) At input: $C_{P,in} = 0.3\,pF$, $L_{S,in} = 3.3\,nH$. At output: $L_{P,out} = 5\,nH$, $C_{S,out} = 0.13\,pF$, and $C_{P,out} = 0.3\,pF$.

the input impedance network, so that the trace S_{11} can be pulled clockwise toward the center of the Smith chart along the constant conductance circle. This will definitively help enhance the power gain of *LNA*.

In the output impedance network shown in Figure 1.37, the de-Q resistor, $R_{P,out} = 500\,\Omega$, is removed. The *DC* blocking capacitor in Figure 1.37, $C_{S,out} = 1\,pF$, is replaced by a smaller capacitor, $C_{S,out} = 0.13\,pF$, and an additional capacitor, $C_{P,out} = 0.3\,pF$, is added at the output terminal as shown in Figure 1.39. By the addition of $L_{P,out} = 5\,nH$, the trace S_{22} is pulled counter-clockwise to somewhere in the upper portion of Smith chart along the constant conductance circle. Then, by the addition of $C_{S,out} = 0.13\,pF$, the trace S_{22} is drawn counter-clockwise to somewhere in the upper portion of the Smith chart along the constant resistance circle. Finally, by the addition of $C_{P,out} = 0.3\,pF$, the trace S_{22} is pulled clockwise toward the center of the Smith chart along the constant conductance circle.

The resulting *S* parameters are plotted in Figure 1.40:

$$20.8\,dB < S_{21} < 25.5\,dB, \qquad \text{when } 3.696 < f < 4.224\,GHz, \tag{1.163}$$

$$S_{21} = 25.5\,dB, \qquad \text{when } f = 3.960\,GHz, \tag{1.164}$$

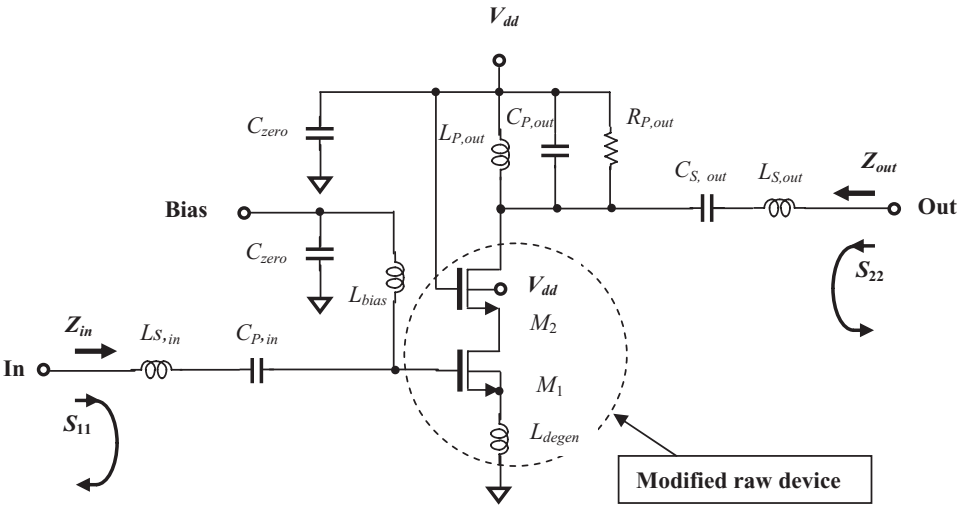


Figure 1.41 Re-modified impedance matching by parts. At input: $L_{S,in} = 3.8\,nH$, $C_{S,in} = 5\,pF$. At output: $R_{P,out} = 200\,\Omega$, $L_{P,out} = 2\,nH$, $C_{P,out} = 0.97\,pF$, and $C_{S,out} = 10\,pF$, $L_{S,out} = 3.3\,nH$.

$$-13.8\,dB < S_{11} < -6.2\,dB, \quad \text{when } 3.696 < f < 4.224\,GHz, \tag{1.165}$$

$$S_{11} = -13.6\,dB, \quad \text{when } f = 3.960\,GHz, \tag{1.166}$$

$$-28.8\,dB < S_{22} < -1.8\,dB, \quad \text{when } 3.696 < f < 4.224\,GHz, \tag{1.167}$$

$$S_{22} = -25.0\,dB, \quad \text{when } f = 3.960\,GHz. \tag{1.168}$$

In the entire frequency range, the gain, $S_{21} > 20.8$ dB, is satisfactory!

Unfortunately, from the frequency response of S_{11} and S_{22}, the bandwidth becomes narrow and does not cover the desired frequency range: $3.696\,GHz < f < 4.224\,GHz$.

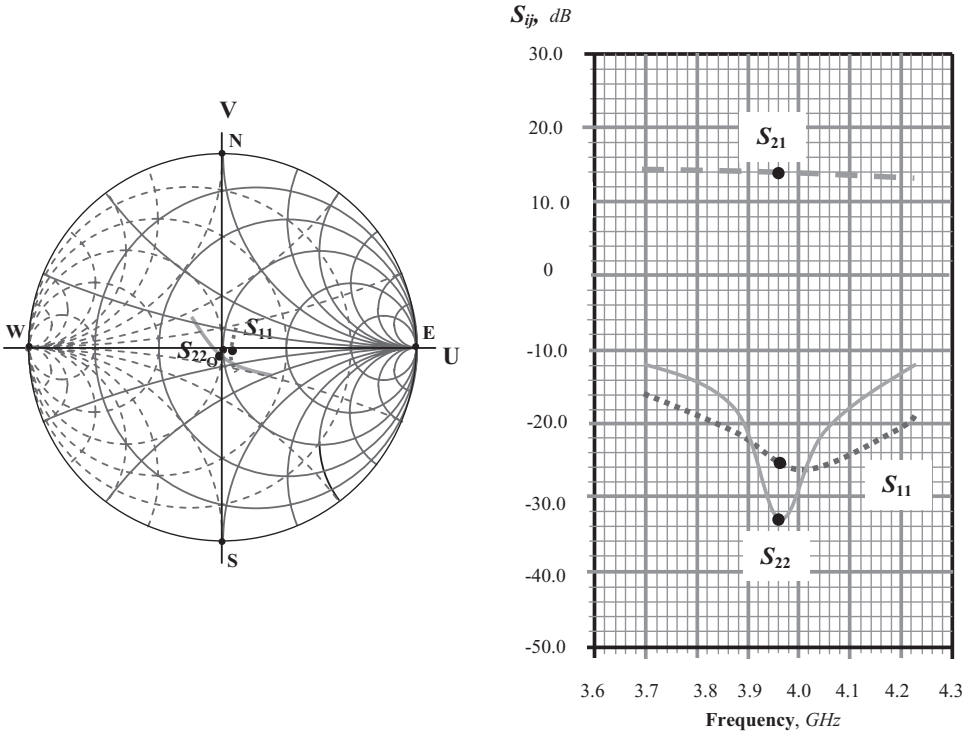
Another issue concerns the capacitors $C_{S,out} = 0.13\,pF$ and $C_{P,out} = 0.3\,pF$. Their capacitances are too small and therefore unrealistic! One cannot find any discrete capacitor with $0.13\,pF$ of capacitance on the market at all. A $0.3\,pF$ capacitor is in the same order as the parasitic or spray capacitance which exists in the circuit layout. These capacitors are therefore unacceptable parts in this circuit implementation.

So, more effort must be put into the impedance matching work! Let's try again!

In general, it is expected that input and output impedance networks can be constructed to satisfy the goals both of power gain and the bandwidth of *LNA*. Figure 1.41 shows a successful attempt, which consists of the parts:

- At input impedance matching network: $L_{S,in} = 3.8\,nH$, $C_{S,in} = 5\,pF$,
- At output impedance matching network: $R_{P,out} = 200\,\Omega$, $L_{P,out} = 2\,nH$, $C_{P,out} = 0.97\,pF$, and $C_{S,out} = 10\,pF$, $L_{S,out} = 3.3\,nH$.

Special topologies are applied to both input and output impedance matching networks.



(a) $\boldsymbol{S_{11}}$ and $\boldsymbol{S_{22}}$ on Smith chart

(b) Magnitude of $\boldsymbol{S_{ij}}$, *dB*

Figure 1.42 *S* parameters after input and output impedances are matched by parts. (The intermediate frequency $f = 3.96\,GHz$ is marked by a dot on each trace.) At input: $L_{S,in} = 3.8\,nH$, $C_{S,in} = 5\,pF$. At output: $R_{P,out} = 200\,\Omega$, $L_{P,out} = 2\,nH$, $C_{P,out} = 0.97\,pF$, $C_{S,out} = 10\,pF$, and $L_{S,out} = 3.3\,nH$.

The input impedance network is an *LC* "arm," in which two parts, $L_{S,in}$ and $C_{S,I}$, are connected in series. The output impedance matching network consists of one "branch" and one "arm". The "branch" is built by three parts, $L_{P,out}$, $C_{P,out}$, $R_{P,out}$, which are connected in parallel, while the "arm" is built by two parts, $C_{S,out}$ and $L_{S,out}$, which are connected in series. As discussed in Chapter 11, either the arm or branch is a special part, which is effectively applied in the wide-band impedance matching network. Readers are encouraged to read Chapter 11 about wide-band impedance matching so as to understand more schemes on wide-band impedance matching. Figure 1.42 shows its performance:

$$13.0\,dB < S_{21} < 14.3\,dB, \quad \text{when } 3.696 < f < 4.224\,GHz, \tag{1.169}$$

$$S_{21} = 14.0\,dB, \quad \text{when } f = 3.960\,GHz, \tag{1.170}$$

$$-26.2\,dB < S_{11} < -15.9\,dB, \quad \text{when } 3.696 < f < 4.224\,GHz, \tag{1.171}$$

$$S_{11} = -25.5\,dB, \quad \text{when } f = 3.960\,GHz, \tag{1.172}$$

$$-33.2\,dB < S_{22} < -11.9\,dB, \quad \text{when } 3.696 < f < 4.224\,GHz, \tag{1.173}$$

$$S_{22} = -33.1\,dB, \quad \text{when } f = 3.960\,GHz. \tag{1.174}$$

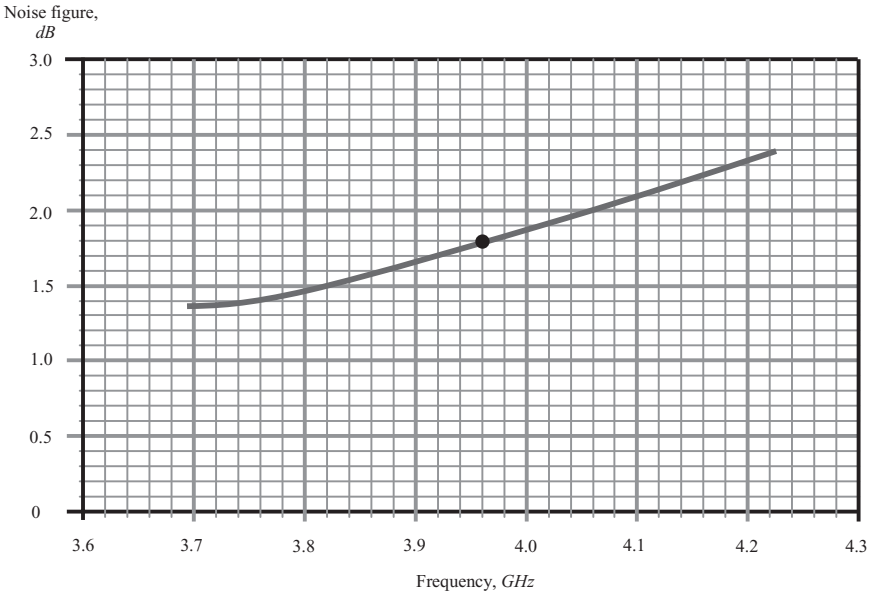


Figure 1.43 Noise figure from 3.696 to 4.224 GHz. $NF = 1.8\,dB$ when $f = 3.960\,GHz$.

Now the gain is reasonable and the bandwidth is wide enough! In addition, the values of the parts are appropriate!

From the demonstrations above, we recognize that impedance matching is not an easy task. Not only the gain but also the bandwidth needs to be taken care of. Additionally, there are many solutions to the same problem. The designer must select one of the possible solutions with the least part count, smallest size, lowest cost and current drain, and best performance.

1.3.4.3 Noise Figure The noise performance of the design sample is good after impedance matching is completed. This is expected because the modified raw device is designed to satisfy the condition (1.34) to simultaneously approach maximum gain and minimum noise figure. Figure 1.43 shows the performance of the noise figure over the entire frequency range:

$$NF = 1.37\,dB, \quad \text{when } f = 3.696\,GHz, \tag{1.175}$$

$$NF = 1.80\,dB, \quad \text{when } f = 3.960\,GHz, \tag{1.176}$$

and

$$NF = 2.40\,dB, \quad \text{when } f = 4.224\,GHz. \tag{1.177}$$

The exciting results can be seen on the plot of the gain and noise figure circles as shown in Figure 1.44. This is a plot for the operating frequency $f = 3.960\,GHz$. After the input and output impedances are matched, the center of the gain circles is point G, which is very close to the center of the Smith chart. The maximum gain at this operating frequency is $14\,dB$, which is consistent with the results shown in Figure 1.42(b). On the other hand, the center of the noise figure circles is point N, which

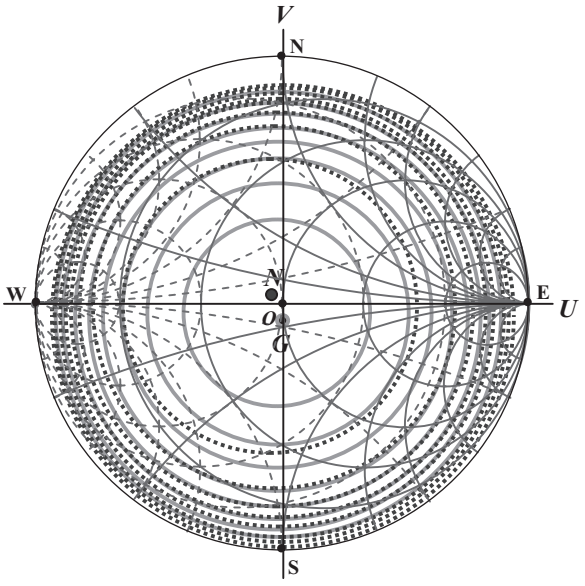


Figure 1.44 Constant gain circles and constant noise figure circles when $f = 3.96\,GHz$.
Gain circles: $G_{max} = 14\,dB$ at point G, step = $1.0\,dB$.
Noise figure circles: $NF_{min} = 1.8\,dB$ at point N, step = $0.5\,dB$.

is also very close to the center of the Smith chart. The minimum noise figure at this operating frequency is $1.8\,dB$, which again is consistent with the results shown in Figure 1.43.

The wonderful feature in Figure 1.44 is that the circles and noise circles overlap each other almost completely. The two centers are very close to each other near the center of the Smith chart. The deviation between point N and point O is due to the tolerance existing in the condition (1.34), $\Gamma_{S,opt} = S_{11}^*$; the deviation between point G and point O is due to the tolerance of parts existing in the impedance matching networks. In practice, it is impossible to reach the perfect goal predicted by theory. Deviation between the practical design and the circuit theory always exists.

1.3.4.4 Non-linearity The frequency spectrum at the output of the *LNA* is shown in Figure 1.45. The first (the desired signal), second, and third harmonics are

$$P_{out} = -35.9\,dB_m, \qquad \text{at } f = 3.96\,GHz, \tag{1.178}$$

$$P_{out} = -91.7\,dB_m, \qquad \text{at } f = 7.92\,GHz, \tag{1.179}$$

$$P_{out} = -119.1\,dB_m, \qquad \text{at } f = 11.78\,GHz, \tag{1.180}$$

$$\ldots$$

when $P_{in} = -50\,dB_m$.

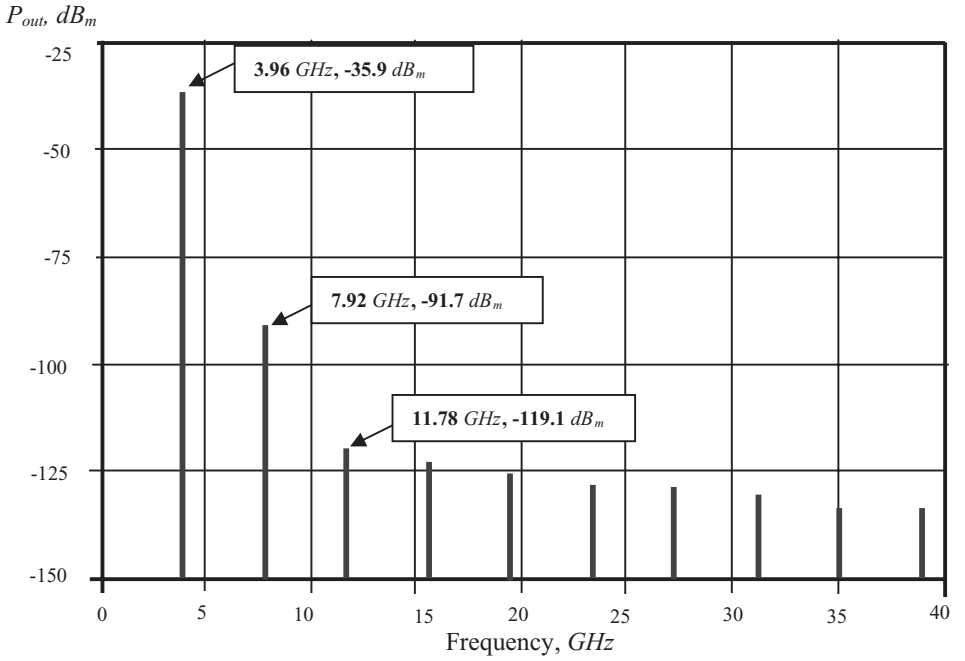


Figure 1.45 Spectrum at *LNA* output, $f_o = 3.96\,GHz$, $P_{in} = -50\,dB_m$.

The gain of the *LNA* is

$$P_{out} - P_{in} = -35.9\,dB_m - (-50\,dB_m) = 14.1\,dB, \tag{1.181}$$

which is approximately consistent with the gain testing of $S_{21} = 14.0\,dB$ as shown in Figure 1.42(b).

The second and third harmonics are lower than the output power at the operating frequency by

$$\Delta P_{out,2} = P_{out}|_{7.92\,\mathrm{GHz}} - P_{out}|_{3.96\,GHz} = -91.7\,dB_m - (-35.9\,dB_m) = -55.8\,dB, \tag{1.182}$$

$$\Delta P_{out,3} = P_{out}|_{11.78\,\mathrm{GHz}} - P_{out}|_{3.96\,GHz} = -119.1\,dB_m - (-35.9\,dB_m) = -83.2\,dB, \tag{1.183}$$

respectively, which implies that low value spurious products existed in this *LNA* block. The good news is that we need not worry about *DC* offset considerations and the interference of adjacent channels anymore.

Figures 1.46, 1.47, and 1.48 show the $1\,dB$ compression point, third order intercept point, and second order intercept point respectively. The $1\,dB$ compression point is

$$P_{1dB} = -3.64\,dB_m, \qquad \text{when } f = 3.96\,GHz, \tag{1.184}$$

The third order and second order intercept point are

$$IIP_3 = 3.74\,dB_m, \qquad \text{when } f = 3.96\,GHz, \tag{1.185}$$

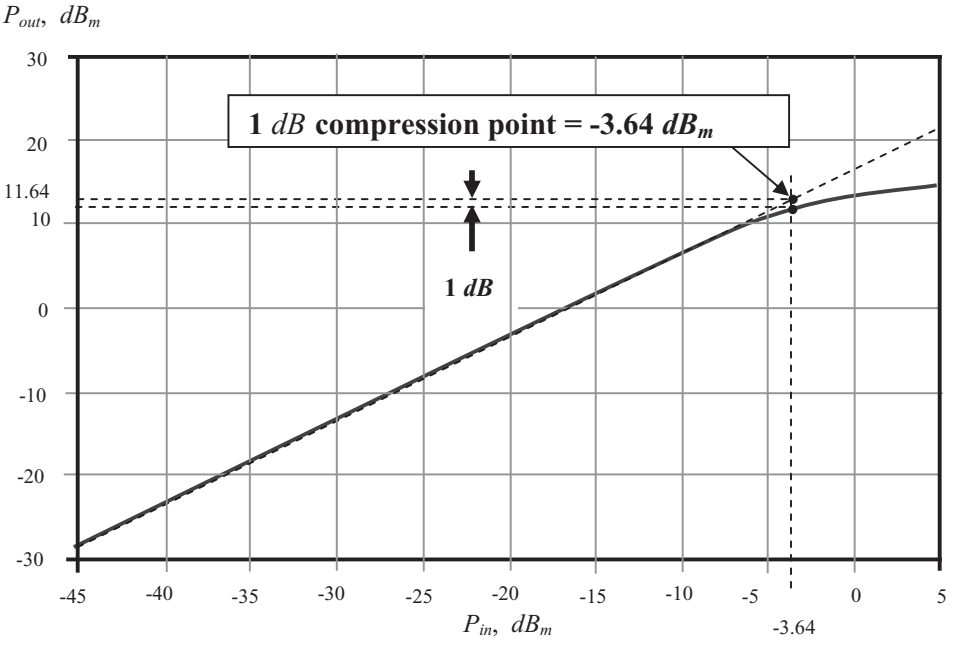


Figure 1.46 $1\,dB$ compression point when $f_o = 3.96\,GHz$.

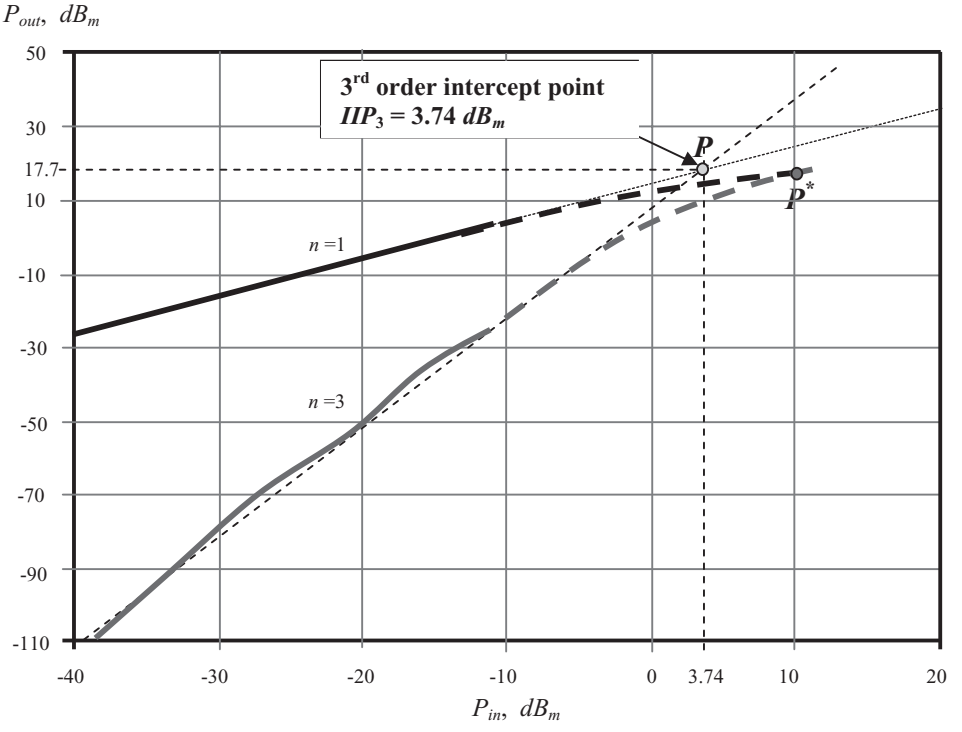


Figure 1.47 Third-order input intercept point when $f_o = 3.96\,GHz$.

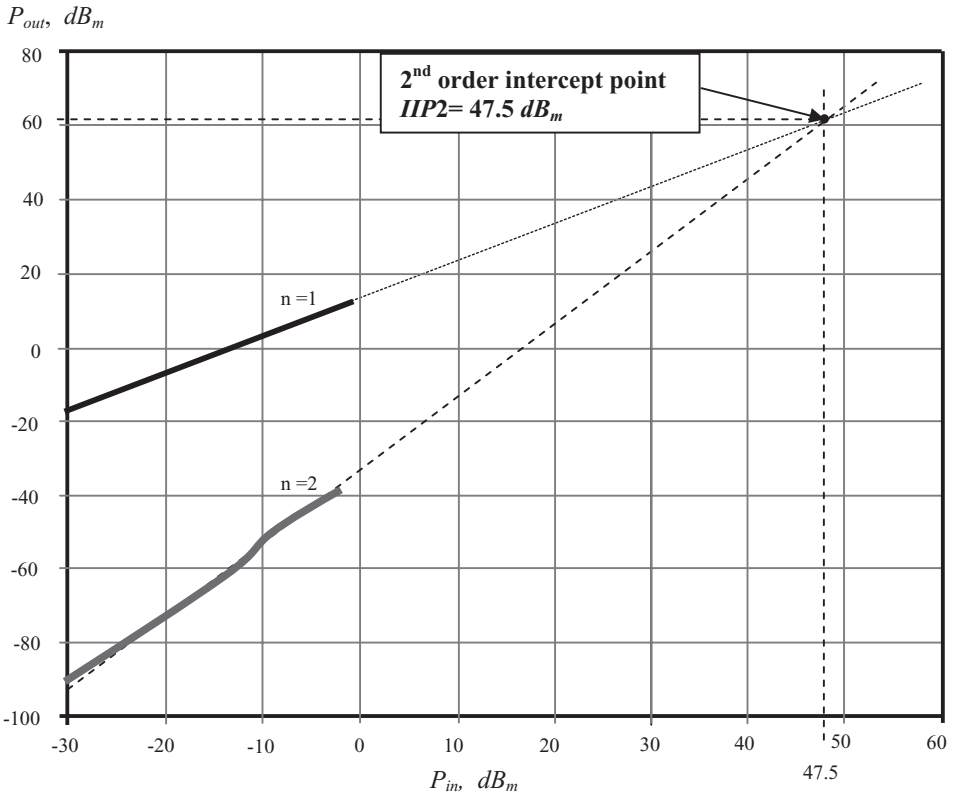


Figure 1.48 Second-order input intercept point when $f_o = 3.96\,GHz$.

$$IIP_2 = -47.5\,dB_m, \qquad \text{when } f = 3.96\,GHz, \tag{1.186}$$

respectively.

1.4 *LNA* WITH *AGC* (AUTOMATIC GAIN CONTROL)

1.4.1 *AGC* Operation

Received signals very often suffer from fading, so that fluctuation of the field strength of radio signals at the receiver antenna always exists. In order to maintain a relatively constant output to the sensor, such as the speaker, it is necessary to detect the strength of the received signal and then adjust the gain of the receiver automatically. This is the subject of *AGC* operation.

In the early development stages of portable radios and cellular phones, modulation technology was relatively simple and therefore it was not necessary to apply *AGC* technology. As advanced modulation technology develped, *AGC* technology became required and sometimes played a decisive role in the receiver.

In the early development stages of cellular phones, a $20\,dB$ dynamic range of *AGC* control in *LNA* design was occasionally required. However, in today's *CDMA* or *WCDMA* receivers, a *AGC* control range of up to $90\,dB$ is required. This is really an astronomic number! It is well-known that every $3\,dB$ variation corresponds to a 50% or double power variation. $90\,dB$ of variation implies that the received power or field strength around the antenna could vary by as many times as

$$2^{\frac{90}{3}} = 1,073,741,824!$$

The wide dynamic range of *AGC* control is indeed a challenge to circuit designers.

It is well known that the amount of power gain in a receiver is mostly contributed by the back-end after the de-modulator. In order to be able to set up $90\,dB$ of *AGC* in the back-end, the total power gain in the back-end must be higher than $90\,dB$. This will easily and inevitably bring about oscillation in those amplification blocks due to the high gain required. Eventually, the $90\,dB$ of power variation cannot rely on the *AGC* control in the back-end only. The front-end or *RF* designers must share the task of *AGC* control for a $90\,dB$ power variation. At present, the task of *AGC* control in a radio or a cellular phone is distributed to both front-end and back-end in an approximately 50 to 50% ratio. The *LNA* at the front end must then have an *AGC* control of 40 to $50\,dB$, as other blocks in front-end are difficult to work with for *AGC* control.

An *LNA* with *AGC* control is sometimes called a *VGA* (Variable Gain Amplifier).

An important concern is that the *LNA* with *AGC* control should not produce additional distortion on the modulated signal. At the present, *AGC* requirements for *AM* receivers are usually more stringent than those for *FM* or *PM* receivers.

The *AGC* control loop is usually implemented in the receiver of a wireless communication system, illustrated in Figure 1.49. There is a special block called the *RSSI* (Received Signal Strength Indicator) for *AGC* control in the receiver. It detects the received signal from the *IF* amplifier output and compares it with a reference signal, V_R, in a comparator. The difference between these two signals is the output of the *RSSI*, V_{agc}, which is used to control the gain of the *LNA*.

The analysis and design of the *AGC* control loop must be conducted at the system level. Here we will focus on the *LNA* with *AGC* block only. The characteristics of the *LNA* with an *AGC* block are shown in Figure 1.50. For low input received signals the *AGC* control is inactivated, so that the output of *LNA*, $V_{S,out}$ or $P_{S,out}$ is linearly related to the input received signal V_i. When the input received signal is increased above V_{i1}, the *AGC* loop is activated and will maintain the output level at a constant value or with a tiny increase until the input received signal increases above V_{i2}. The minimum and maximum output voltages from the *RSSI* block, $V_{agc,min}$ and $V_{agc,ma}$, correspond to V_{i1} and V_{i2} respectively. When the input received signal is stronger than V_{i2}, the *AGC* loses its control capability and the *LNA* output, $V_{S,out}$ or $P_{S,out}$, returns to the linear relationship with the input received signal V_i. Instead of a suddenly activating or inactivating of the *AGC* control, the actual performance of the *AGC* produces a somewhat smooth curve as shown in Figure 1.50.

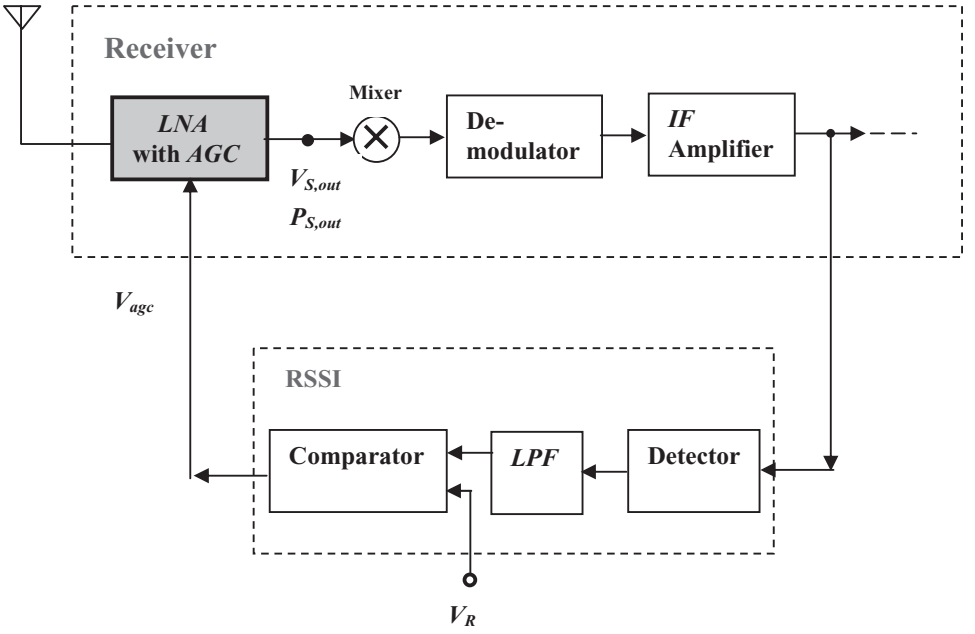


Figure 1.49 An *AGC* control loop in the receiver of a communication system.

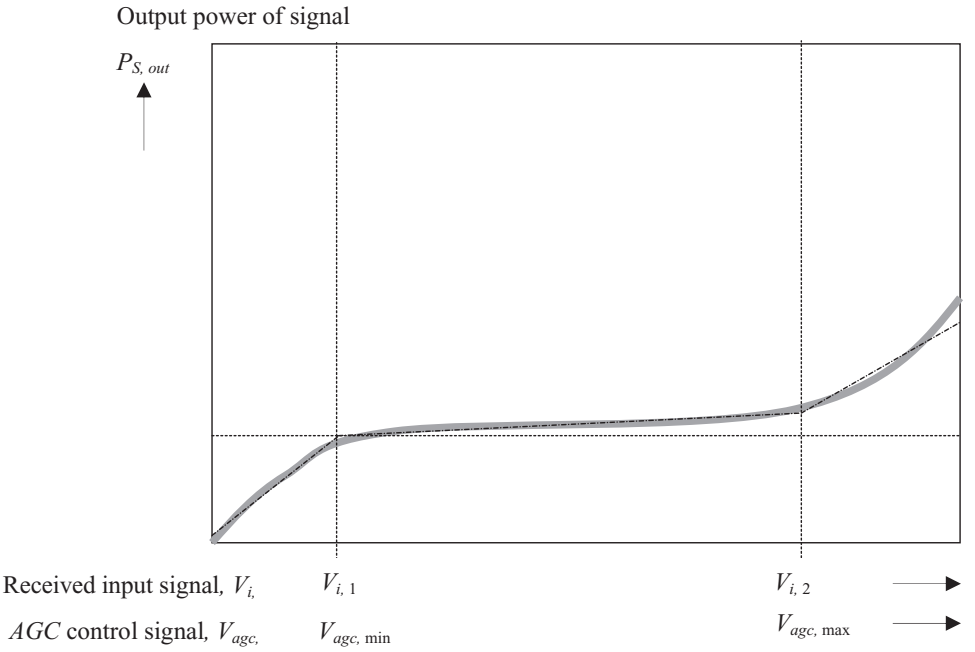


Figure 1.50 Expected characteristics of *AGC* control.
Ideal
Actual performance

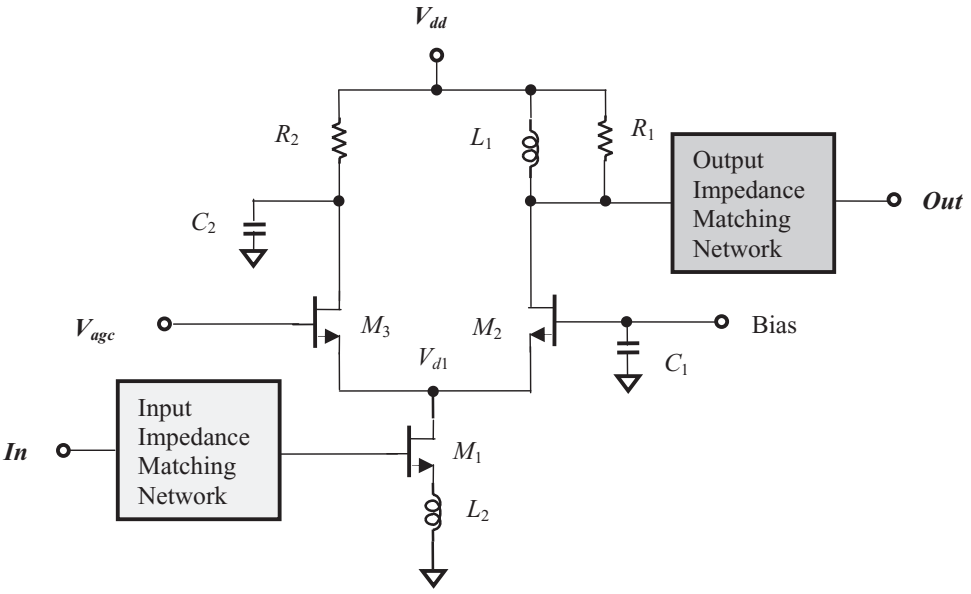


Figure 1.51 Traditional *LNA* with *AGC*.

The dynamic range of the *AGC* control voltage is

$$DR_{agc} = V_{i,2} - V_{i,1} = V_{agc,\max} - V_{agc,\min}, \tag{1.187}$$

in which the power variation of received signal at antenna, say, 40 to 50 dB, can be "swallowed."

1.4.2 Traditional *LNA* with *AGC*

Figure 1.51 shows a traditional *LNA* with *AGC*. Its configuration is a differential-type with a cascode *LNA* branch, which consists of M_1 and M_2, and an *AGC* control branch, which consists of M_1 and M_3. The function of each part is as follows:

- M_1, M_2: cascoded devices;
- C_1, C_2: *AC* short-circuited or "zero" capacitor;
- L_1: load inductor;
- R_1: stability resistor;
- L_2: degeneration inductor;
- M_3: *AGC* effective device;
- R_2: Current control resistor.

The input to the gate of the transistor M_3, V_{agc}, is a *DC* voltage from the *RSSI* output in the radio. When the *RSSI* voltage is lower than $V_{agc,min}$, the M_3 is turned off and *AGC* function is not activated. However, if the *RSSI* output voltage, V_{agc}, is increased above $V_{agc,min}$, the M_3 is turned on and shares the *AC* current from the M_1–M_2 cascode

LNA branch. As the *RSSI* voltage continuously rises, the M_3 will share more *AC* current. The *AC* current shared by M_3 is shorted to the ground by the capacitor C_2. Consequently, the gain of the cascode *LNA* branch M_1–M_2 will be reduced because the *AC* current is partially shared and shorted to the ground by the *AGC* control branch M_1–M_3. Intuitively, the higher the *RSSI* control voltage V_{agc}, the more the reduction of *LNA* gain.

The normal gain of the *LNA* is defined as the gain when the *AGC* branch is not activated, that is the *RSSI* voltage V_{agc} is lower than $V_{agc,min}$. The *LNA* gain can be reduced when the *AGC* branch becomes effective.

As mentioned above, the *AGC* dynamic range is required to be at least $40\,dB$. However, with the traditional *LNA* with *AGC* control design shown in Figure 1.51, the *AGC* dynamic range only approaches $20\,dB$. This limitation is due to the restrictions of the topology. Let's take a look at Figure 1.51. Should the drain voltage of M_1, V_{d1}, always trace the variation of *RSSI* output voltage V_{agc} at the gate of M_3, the *LNA* gain might be continuously reduced as the *RSSI* output voltage V_{agc} at the gate of M_3 is increased. Then the *AGC* dynamic range could be much higher than $20\,dB$.

Unfortunately, owing to the existence of the M_1–M_2 branch, the variation of voltage V_{d1} is not as expected. At the beginning, V_{d1} increases as the *RSSI* voltage increases, so that the *AC* current is shared by the *AGC* control branch and the *LNA* gain is lowered. However, as the increased *RSSI* output voltage V_{agc} reaches a certain value, V_{d1} stops increasing, or even inversely decreases. This leads to the increase of *LNA* gain back in the direction toward its normal gain without *AGC* control. That is why the *AGC* dynamic range is limited.

1.4.3 Increasing of *AGC* Dynamic Range

In order to increase the *AGC* dynamic range, there are three improvements to be adapted:

1) **Diode clamping**
   In order to force the voltage V_{d1} to trace the variation of the *RSSI* voltage, a device M_4 with a diode-connection is added to the gate and source of M_3 as shown in Figure 1.52.
2) **Avoiding *RSSI* operation as a current sink or source**
   Without the additional resistor R_3 and the additional device M_4 as shown in Figure 1.52, the gate of M_3 is the load of the *RSSI* output, which is extremely light since the input impedance of M_3 is quite high. Now, the addition of the device M_4 brings about a problem for the *RSSI* output. The device M_4 is *DC* connected from *RSSI* output to the source of M_3 and the rest of the circuit. This makes the *RSSI* output port a *DC* source or sink. The current from or into the *RSSI* output could be in the order of *mA* or more, which the *RSSI* output terminal cannot usually afford.

   The solution is to add a resistor R_3 between the V_{dd} and the gate of M_3 as shown in Figure 1.53. An appropriate adjustment of the value of R_3 can make the current either flowing from or into the *RSSI* output less than $0.5\,mA$.
3) **Selection of big device M_3**
   In the design of *LNA* with *AGC*, the selection of the device M_3 is very important. From a system design viewpoint, it is desirable to reduce the current drain

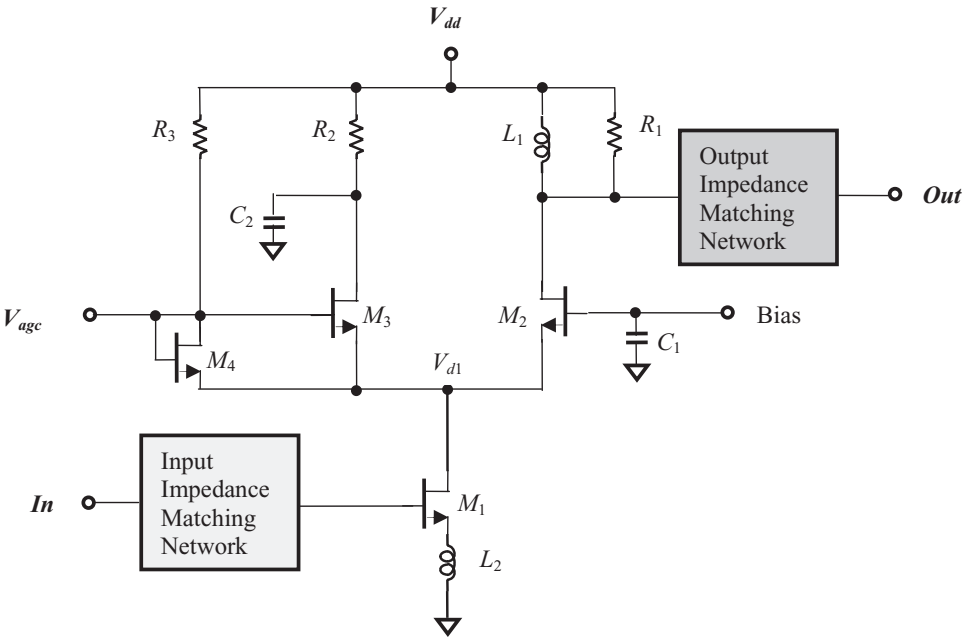


Figure 1.52 *LNA* with large dynamic range *AGC*.

as much as possible. Therefore, the I_{ds} current of M_3 should not be too high when it is turned on. On the other hand, its I_{ds} current should be very low when it is turned off. In order to satisfy these two requirements simultaneously, one must select a big device M_3 with a large number of "fingers.".

1.4.4 An Example

The schematic as shown in Figure 1.52 has been simulated with the *CMOS* process and the corresponding work on the bench has been done.

In this design, the number of fingers is 8 and 16 for M_1 and M_2 respectively, whereas the number of fingers for M_3 is selected as 100. (In the *CMOS* processing, the width of one finger is 16 microns.) The *DC* characteristics of M_3 are shown in Figure 1.53 and can be outlined as follows.

$$I_{ds} \approx 0.02\,mA \text{ or } 20\,\mu A, \qquad \text{when } V_{agc} = 1.2\,\text{V}; \tag{1.188}$$

$$I_{ds} = 1.25\,mA, \qquad \text{when } V_{agc} = 1.2\,V. \tag{1.189}$$

Table 1.5 lists its parts and Table 1.6 lists its performance.

This *LNA* with a large dynamic range of *AGC* design has been integrated with a 1 *watt PA* in an *IC* chip, which has been successfully applied to a radio production line.

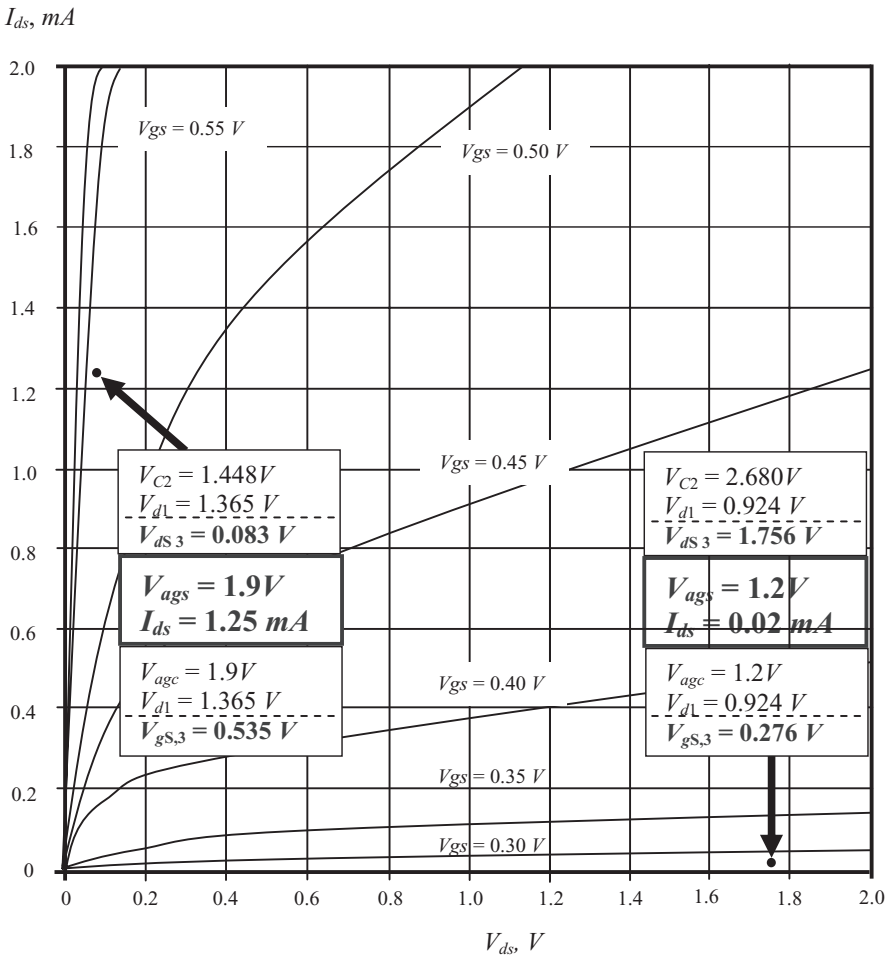


Figure 1.53 *DC* characteristics of transistor M_3.

TABLE 1.5 Part list of LNA with AGC

Part		Value.
M_1	Fingers = 8	$W_{total} = 128\,\mu m$
M_2	Fingers = 16	$W_{total} = 256\,\mu m$
M_3	Fingers = 100	$W_{total} = 1600\,\mu m$
M_4	Fingers = 16	$W_{total} = 1256\,\mu m$
R_1	$700\,\Omega$	
R_2	$1\,k\Omega$	
R_3	$10\,k\Omega$	
C_1	$20\,pF$	
C_2	$40\,pF$	
L_1	$50\,nH$	
L_2	$30\,nH$	

TABLE 1.6 Goals, simulation, and performance of an *LNA* with *AGC*

	Goal		Simulation		Performance		
DC power supply, *V*	3.0		3.0		3.0		*V*
Frequency, *f*	460 to 470		460 to 470		460 to 470		*MHz*
RSSI control voltage, V_{agc}	1.2	1.9	1.2	1.9	1.2	1.9	*V*
***AGC* dynamic range, DR_{agc}**	**0.00**	**–40**	**0.00**	**–43.7**	**0.0**	**–42**	***dB***
Current drain, I_{ds}	2.0	*	1.87	1.48	2.0	1.4	*mA*
Gain, *G*	1.0	–28	1.6	–31.1	15.0	–27.0	*dB*
Noise figure, *NF*	2.0	*	1.26	29.4	2.7	*	*dB*
3rd order intercept point, IIP_3	–15.0	*	–10.2	–7.5	–10.5	–8.0	dB_m
Input Return Loss, S_{11}	*	*	–15.3	–10.4	*	*	*dB*
Output Return Loss, S_{22}	*	*	–23.2	–11.7	*	*	*dB*

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