CHAPTER 1

Introduction to Solution-Deposited Inorganic Electronics

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1.1 BACKGROUND AND MOTIVATION

1.1.1 Electronics Technologies

Two thrusts currently dominate efforts in electronics research. In both thrusts, the business opportunities stem from society's desire for a more pervasive and integrated electronics environment. However, the technical methods and strategies for achieving this goal are fundamentally different. The first and most widely discussed thrust focuses on what is popularly referred to as Moore's Law and the seemingly endless progression to smaller device feature sizes and the increasing numbers of transistors integrated onto a chip.[1] These chips (i.e., microelectronics) have enabled everything from laptop computers to cell phones, from smart cards to smart toys. The essence of the success of Moore's Law is that by creating technology to make devices smaller, the density and performance increases and the functionality goes up, whereas cost/function goes down. This amazingly successful thrust has created a technological revolution and has been an engine for worldwide economic growth because it results in faster and more compact products for computing and communications.

While over the last 40 years microelectronic integrated circuits based predominantly on silicon technology have made possible our current capabilities in everything from computers and phones to appliances and toys, even greater opportunities would exist if the circuits could be made more lightweight,

Solution Processing of Inorganic Materials, edited by David B. Mitzi

flexible, and inexpensive. Everything from flexible displays, to radio frequency identification (RFID) tags that conform to a product's shape, to large and pliable "sensor sheets" that are integrated into airplanes, bridges, or even people to monitor and augment their physical condition, could become possible.[2] This concept is much newer, and the required technology is not nearly as mature. The distinguishing feature of this newer approach is that small device size is not a critical factor. Rather than fabrication of smaller devices and circuits, described below are two microelectronics-related electronics technologies that have become successful by fabricating modest-sized devices over larger and larger glass substrates (large-area electronics). This work is just now being extended to plastic substrates to provide reduced weight and novel form factors.

Given that microelectronics and large-area electronics are both electronics technologies, it might be assumed that the second is derived from and will evolve with the mainstream semiconductor industry. However, microelectronics is driven to produce smaller feature sizes and higher complexity chips. There are, however, many applications where microelectronics is not an appropriate technology, and in fact, it represents too complex or costly of a solution. Thus, the requirements and drivers are so different that few, if any, of the mainstream integrated circuit (IC) technologies are applicable to this second and newer thrust. While sharing many concepts with microelectronics, the second thrust is NOT for the most part derived from the IC industry and does not really benefit from its learning curve, but rather it originates from needs not adequately addressed by conventional microelectronics. It has different drivers, product attributes, and metrics and will be successful in its own product space, or by complementing conventional ICs to create solutions that neither could provide individually. Because of this distinction, varieties of names have been used to describe this non-microelectronic, large-area electronics technology. Because the device dimensions are generally large compared with microelectronics and product applications are physically large compared with microchips, one popular name for this form of electronics is "macroelectronics."[3]

1.1.2 Commercial Macroelectronic Technology

The most successful application of macroelectronics, the flat panel display (FPD) industry,[4,5] now rivals the microelectronics industry in revenue; yet, from an electronics perspective, it is based on nothing more than manufacture of modest-sized transistor switches distributed over glass substrates as large as a meter on a side.[6] Within 10 years, the FPD industry has almost reached the $100B mark (see Figure 1.1), whereas more traditional semiconductor industry growth has become relatively mature with slowing growth prospects. Another interesting aspect of the FPD story is that it has been accomplished while undergoing rapid changes in the manufacturing technologies. As shown in Figure 1.2, the size of the glass panels used have progressed rapidly through multiple manufacturing generations, which means that the panel size has

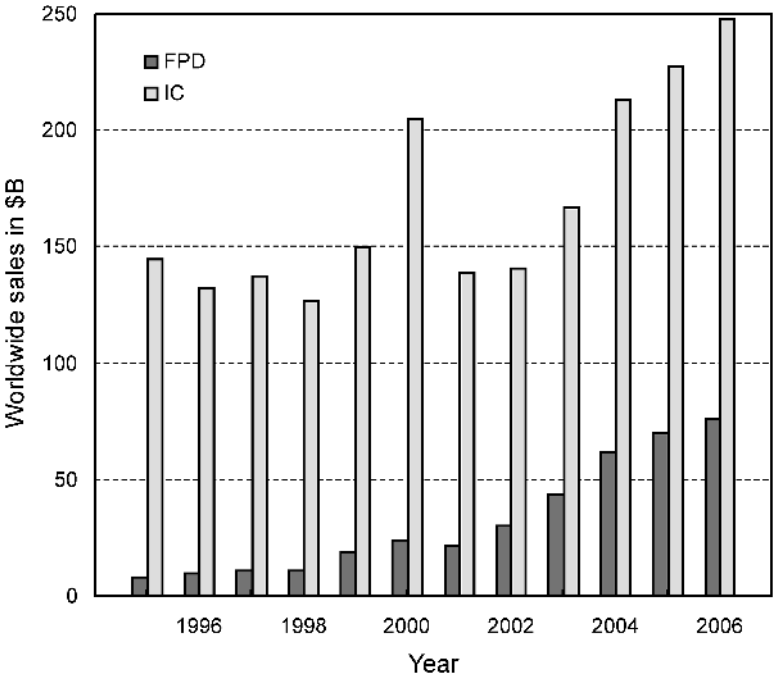

Figure 1.1. Growth of semiconductor and flat panel display industries. [Data Source: Semiconductor industry sales data from Semiconductor Industry Association (SIA) and flat panel display data from Displaysearch Corp, San Jose, CA.]

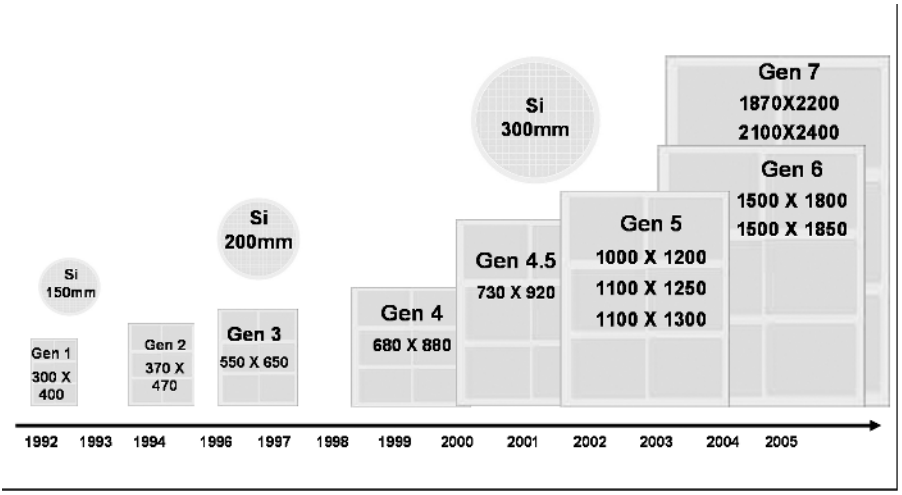

Figure 1.2. Substrate size comparison between Si wafers and glass substrates used in flat panel displays.

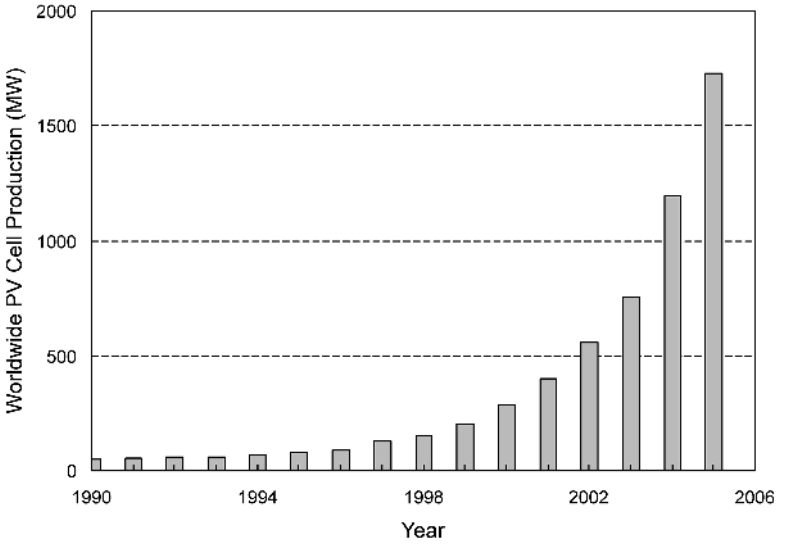

Figure 1.3. Worldwide production volume of photovoltaic modules. [Data source: European Photovoltaic Industry Association, 2006.]

increased by more than 30 times to more than 2 m × 2 m for the current eighth-generation production facilities. In contrast, most semiconductor fabrication has been limited to wafer sizes of 300 mm or smaller.

The second large-area electronics technology to reach high volume and revenue, photovoltaics (PV), which is based on "simple" diodes distributed over many hundreds of square centimeters, is also now poised to grow into a major industry as new energy sources become more essential.[7,8] With the declining stock of fossil fuels and worries about global climate change, solar energy using photovoltaics has become increasingly attractive. The cumulative installed capacity of PV systems has reached over 4 GW and is expected to double every year over the next three years. The annual production volume of PV modules reached the 1-GW milestone in 2004 (see Figure 1.3). With the commencement of a number of a high-volume PV manufacturing facilities over the last two years, production volumes have been growing rapidly ever since, with worldwide manufacturing capacity reaching more than 5 GW in 2007.[9] Most expansion in photovoltaics is based on crystalline and multicrystalline silicon materials.[10] With the rapid growth of the solar energy market, the availability of reasonably priced silicon feedstock has become a major barrier for future growth. Thin-film technologies offer efficient materials utilization and opportunities for large-area processing. Several companies are building thin-film silicon PV production lines based on large glass substrates (e.g., 4-m^2 glass sheets), which are similar to those employed by the FPD industry. The main barriers for thin-film PV technologies, which need to be overcome in order for thin-film PV to become pervasive, are improved conversion

efficiencies (approaching that of crystalline Si devices) and lower capital cost of some production equipment, especially vacuum deposition tools.[11]

To overcome these barriers, the industry is aggressively pursuing both alternative materials and manufacturing methods. Although the major focus of the PV industry is on silicon-based devices, several companies have developed products based on thin-film chalcopyrite and cadmium telluride, as these materials offer opportunities for lower cost production through solution-based processing. Chalcopyrite, or more specifically the $Cu(In,Ga)(Se,S)_2$ family of compounds, has achieved the highest conversion efficiencies (~20%) of any polycrystalline thin-film material.[12] Several companies have commercialized the technology and are approaching volume production.[13] Several companies have started producing CdTe in volumes beyond pilot production. Small-area efficiencies of 16% together with simple production technologies make this material very attractive. State-of-the-art commercial CdTe PV modules that have efficiencies in the 9% range are in volume production.[14]

1.1.3 Macroelectronics Potential

The success of the FPD industry and the rapidly developing PV industry are testaments to the potential for large-area electronics for other system solutions. For example, conformal and flexible form factors are very desirable attributes to provide either portability and/or the ability to install large-area electronics in a variety of locations. These needs are receiving much attention, although fulfilling them is proving to be difficult. Moreover, despite the success of microelectronics, there are applications where it has not been good enough to meet all requirements. Specifically, applications where very low cost is the product driver, rather than performance, can prove challenging for conventional microelectronics. As much as microelectronics has reduced the cost/transistor, the costs are still not low enough to meet the few pennies/item targets for electronic applications that are intended to be disposable, such as RFID tags and product expiration sensors. Similarly, although the number of microelectronic transistors per square centimeters (areal density) has remarkably increased over the last 40 years, the ability to distribute even moderate numbers of transistors over large areas onto a variety of substrates is just beginning to be commercialized for applications such as flexible displays.[15] Transistors at low density can be fabricated over large pieces of glass, but at great sacrifice to performance characteristics compared with mainstream "Moore's Law" devices.

Although initial applications of large-area electronics have focused on displays and PV, future product opportunities are expected to include sensors, imagers, distributed lighting, electronics that are embedded into clothing or gear already carried (radios, computers), and health monitoring/control of vehicles and even people (Figures 1.4– 1.7).[3,16,17] Figure 1.4 captures a concept long championed by many display manufacturers. It proposes that at some point in the future, the display manufacturing capability will be able to provide

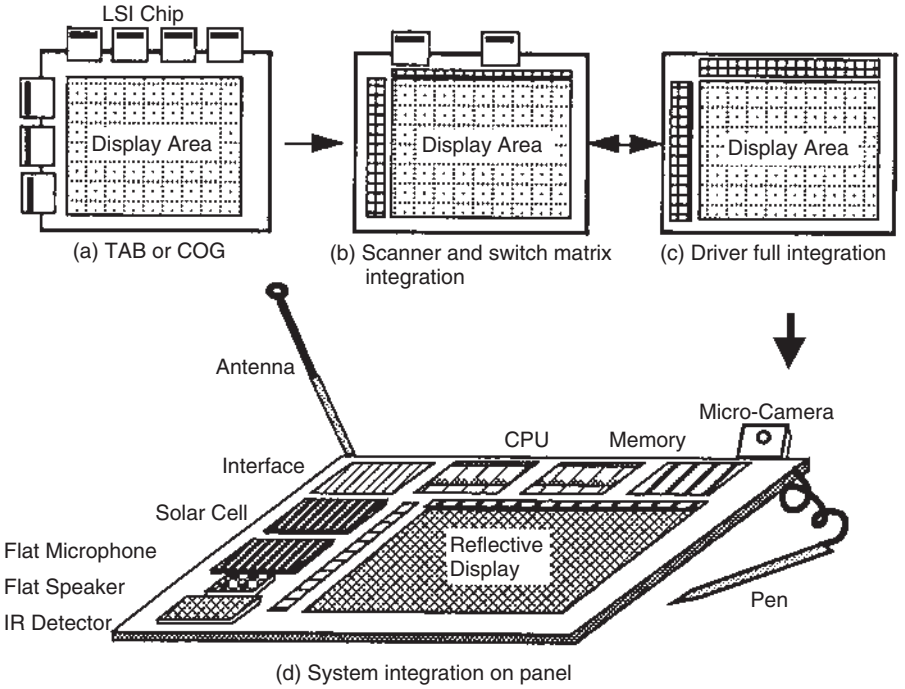

Figure 1.4. Schematic showing the evolution of displays toward a system on a flexible panel. (a) Direct chip on glass attachment technology, moving toward (b) partial display driver integration, (c) fully integrated drivers on glass, followed by (d) a fully integrated "system on a flexible panel," showing how high-performance thin-film transistors enable display drivers and other system components to be integrated on a flexible metal foil. [Schematic courtesy of Sharp Corp, Osaka, Japan.]

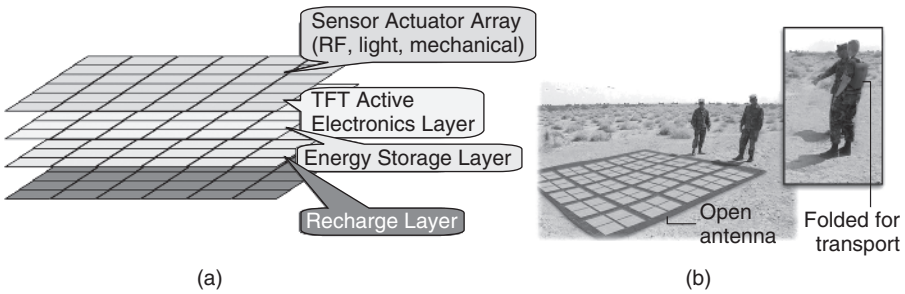

Figure 1.5. Schematic of a fully integrated macroelectronic system and an example of an application concept for macroelectronic systems. (a) Building blocks for a generic macrosystem. (b) Mockup of a large-area antenna array. [Figure courtesy of Sarnoff Corporation. Used with permission.]

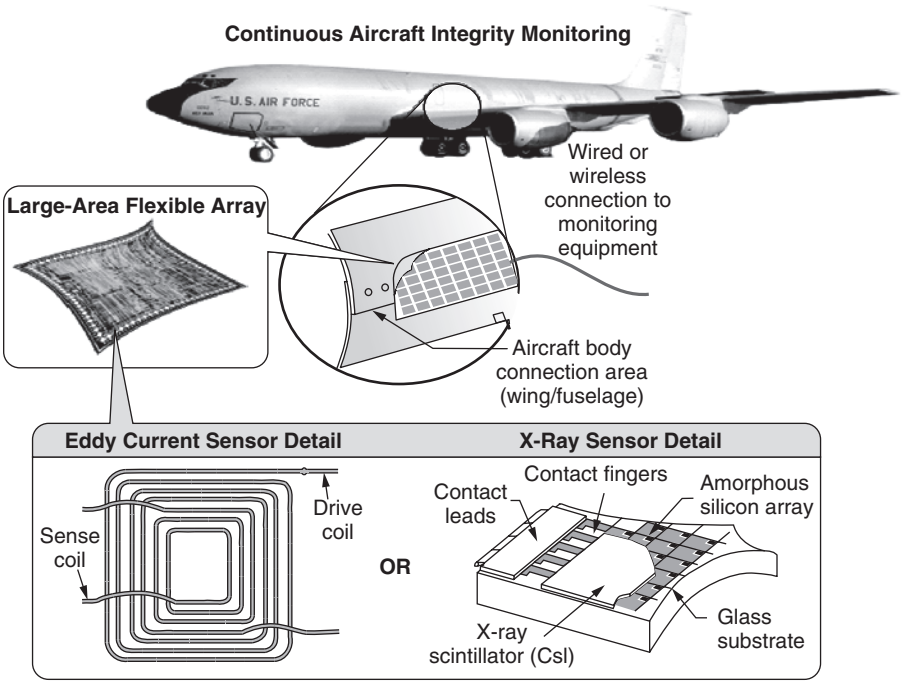

Figure 1.6. Application of large-area embedded flexible control electronics includes structural health monitoring of large objects such as airframes.

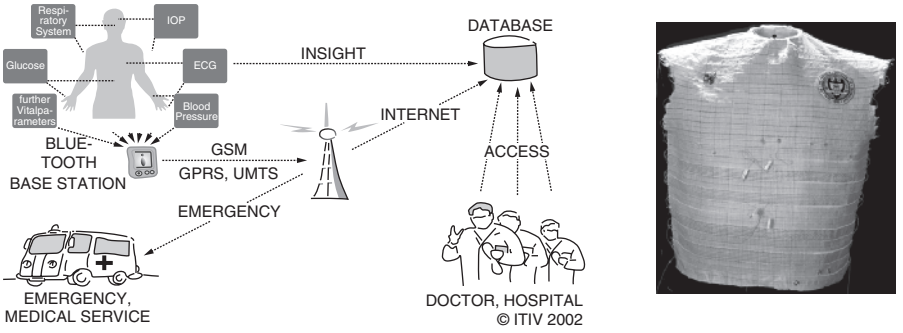

Figure 1.7. Large-area electronic fabrics and health monitoring systems for soldiers and personnel employed in high-risk field operations. (a) Operation of a personnel health monitoring system. (b) Example of a vest with integrated sensors for monitoring body temperature, respiration rate, and other bodily parameters.

not just a display, but also an entire wireless laptop tablet complete with camera, microphone, and solar cell for power. It is unclear when, or even if, such a vision will ever make technical (let alone economic) sense. Nevertheless, the point is that this is one example of a vision that is driving the creation of macroelectronics technology. Figure 1.5 shows yet another large-area concept. Here, the notion is a sensor system that comes integrated with control electronics, energy storage mechanism, and energy harvesting layer, all made via yet-to-be-determined manufacturing technology. Figure 1.6 takes this idea one step further and suggests how a conception suggested in Figure 1.5 might be implemented into an aircraft for structural health monitoring, active flight control and multifunctional applications such as load-bearing structural antennas. Finally, in Figure 1.7, the personal health status application involves a range of sensors, processors, and transmitters integrated within composite materials or mounted on/in human biomaterials (skin/tissues). This assembly is then able to sense and report faults to ensure proper drug usage, or to continuously sense, modify, and transmit physiological and cognitive status. The weight and material integration issues with conventional ICs make these applications impossible or unlikely with a purely microelectronics approach. The major challenge for macroelectronics technology is to enable applications beyond displays that involve large areas and applications that cannot be cost-effectively achieved through traditional packaged-chip fabrication followed by pick-and-place assembly. Nonetheless, these applications will still require sophisticated, high-functionality circuits. The large-scale applications envisioned give rise to the requirement for properties heretofore not associated with IC applications, including the thinness, ductility, and elasticity of electronic components, even during operation. Potentially, cofabrication of electronics and physical structures might be possible. This process would enable the electronics to be built directly onto or within the structure from which it controls, senses, or communicates. Ideally, the electronics would be synergistic with and inseparable from the system. A conceptual model might be the human nervous system. However, the opposite is true for traditional microelectronics, in which passive devices, packaged chips, boards, and boxes are each fabricated separately and only later integrated into the final structure. This difference in manufacturing approach creates major differences for the materials, electronic design, and fabrication methods for macroelectronics versus microelectronics.

1.2 IMPORTANCE OF SOLUTION PROCESSING

Researchers have many obstacles to overcome in the quest to make macroelectronics the “next big thing.” The keys to achieving the desired levels of functionality for a wide range of large-area electronic functions are advances in materials and processes and device structures that can get cost down to pennies (rather than dollars) per square centimeter. Tools and process methods

that provide these devices and their interconnections, at adequate levels of integration and in high yield on a wide range of substrates, must be developed. Some of the required advances in processing and tools will be adopted from the display and photovoltaic industry. However, to achieve the device/circuit performance for more demanding electronic functions, significant improvement in materials and device characteristics must be achieved.

To manufacture flexible integrated circuits, it is not the transistors themselves that are inflexible; it is the relatively thick, bulk wafer on which that the transistors are manufactured. Thinning the wafer to harvest just the upper active circuits is possible but also time consuming, difficult, and expensive. Therefore, in the macroelectronics thrust, the focus is on developing techniques for depositing semiconductors very inexpensively and, in most cases, over a large area on a variety of substrates (to include even plastics and fabrics). The result is a different transistor structure known as a thin-film transistor (TFT; see Section 1.3.1).[2] The ideal method for fabrication of TFTs for macroelectronics requires that the materials used to create the devices be directly deposited on a thin (and ideally, flexible) substrate. In contrast to microelectronics, with TFTs for macroelectronics, the feature size and level of performance are not the primary drivers. Rather, the processing cost, compatibility with diverse substrates, and attributes of the end item (area, weight, bendability, durability/ruggedness) represent the critical factors. These challenges generally require mild processing conditions not significantly different from the ambient (in contrast to the temperatures and chemicals associated with microelectronics fabrication). Processing under such conditions is much more conducive to a variety of electronic substrates and to the integration of diverse functionality, including computational devices, sensors, photovoltaics, and displays. Therefore, fabrication technologies that promise lowest possible cost while delivering at least adequate electrical performance are of great interest.

Because cost/square centimeter is such a major driver for macroelectronic applications, established methods for low-cost manufacture are of great interest. Solution processing for all manner of printed products has a long history and well-developed infrastructure that addresses multiple applications with a wide range of inexpensive materials and patterning methods. Therefore, solution processing has received significant attention, because the essential steps of macroelectronic TFT circuit fabrication can (in principle) all be accomplished using the ordinary, relatively cheap, and widely available technologies used to print ink.[18–20] One method is a modification of ink-jet printing, and another adapts roll-to-roll processing, which is commonly used to print fabrics and newspapers (for a more detailed discussion, see Chapter 12). Unfortunately, to date, the problem with both of these approaches is the ability to produce transistors that can operate fast enough for potential applications of interest. Although adequate for displays, the TFTs produced easily with these printing methods are much too slow for many applications. Thus, macroelectronics research seeks to exploit this rich printing infrastructure, but with

incorporation of materials required to fabricate higher performance TFT-based electronics.

One means that has been pursued to achieve low-cost, multi-material processing is based on organic semiconductors, because of the well-established potential for compatibility with printing technology.[21–24] However, to date, inorganic semiconductors have achieved the highest and most stable TFT performance.[25] Recent results have provided encouraging results based on solution deposition of inorganic materials rather than requiring the standard vacuum deposition methods. Because of the relatively mature theoretical understanding of inorganic semiconductor devices, and the difficulty of obtaining organic-based TFTs with adequate device characteristics, new ways to solution-deposit and fabricate inorganic semiconductors have received increasing attention, as will be explored in subsequent chapters.

Macroelectronics thus seeks to create a new fabrication methodology based on techniques that are currently alien to microelectronics processing. Ideally, roll-to-roll substrate handling will replace wafer batches, with material deposition via solution processing replacing vacuum evaporation, and material patterning by printing eliminating the need for etching. Given the diversity of materials, devices, and applications that may eventually encompass "large-area electronics technology," it may well be that no "standard process" and "standard equipment" will ever exist for macroelectronics, as it does for mainstream CMOS IC manufacturing. However, Figure 1.8 provides some idea of

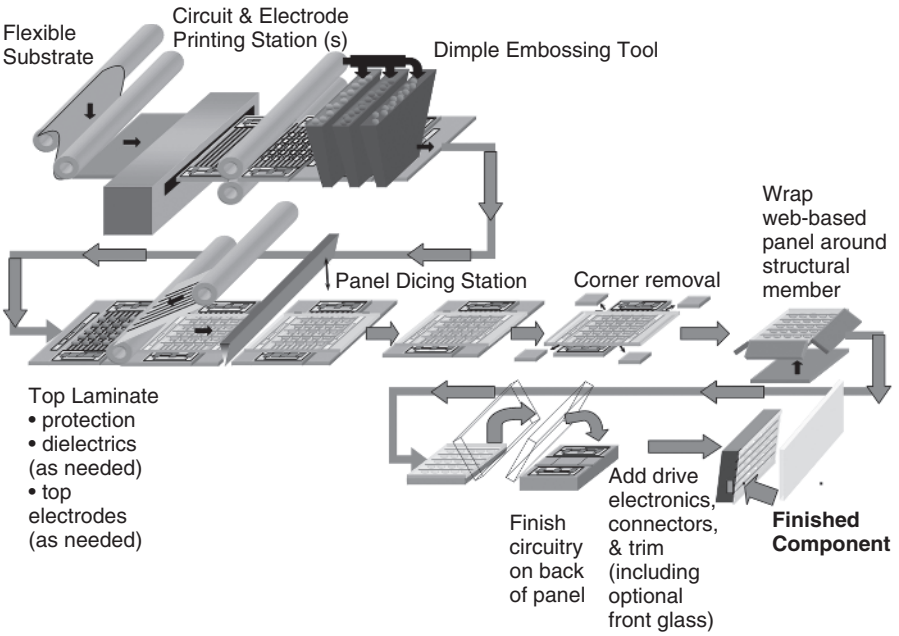

Figure 1.8. Conceptual roll-to-roll manufacturing process.

what a future "printed electronics" manufacturing line might look like. As much research in this field is still in its infancy, it is difficult to forecast what the technology will actually look like. Whatever the final details are, tools and methods will be chosen for their ability to handle large areas at a low cost/square centimeter. The end result of this new manufacturing paradigm is expected to provide electronics solutions inexpensive enough to be "thrown away" or to cover a vast area (e.g., pervasive PV arrays).

This shift in the means of production can be appreciated as follows. The capital required to build a microelectronics state-of-the-art 300-mm wafer fabrication facility is more than $3B, whereas macroelectronics facilities are anticipated to cost at least an order of magnitude less. Furthermore, the cost per unit area of product is expected to drop from the order of $\$10{,}000\,ft^{-2}$ for microelectronics to $\$100\,ft^{-2}$ for macroelectronics.[16] Of course, the cost of making electronics with a roll-to-roll process is not expected to be as inexpensive as conventional ink printing. However, by eliminating the high-temperature, high vacuum steps used in the conventional chip manufacturing, a significant reduction in the manufacturing cost for macroelectronic circuits is expected. Perhaps of more significance, less demanding, lower cost macroelectronics fabrication technology may lead to its integration into the manufacture of a wide range of products, which would provide additional functionality not possible today.

1.3 APPLICATION CHALLENGES: TFT DEVICES AND CIRCUITS

Macroelectronics is a key enabler for several platform technologies.[3] Now, after a decade of fundamental materials and device research, the area is witnessing the first major push toward commercialization for products other than PV and displays. However, productization requires device architectures and materials processes that are reliable and well qualified for high-volume manufacturing (i.e., additional maturization is needed in these areas). Although there has been tremendous progress in device development, future advances need to occur not only at the device level, but also at the circuit and systems level. With continued progress, the technology could provide a practical means for delivering unique application solutions that are otherwise not possible. Some key applications that are expected to benefit and derive enhanced functionality through printed large-area electronics include flexible displays, new imaging devices, transparent electronics, RF tags, photovoltaics, solid state lighting, electronic textiles, robotics, and several unique applications in distributed electronics, including large antenna arrays and structural health monitoring of buildings, ships, and airframes.[26]

Unfortunately, TFT circuit performance has been limited by relatively poor device characteristics compared with bulk Si. Existing amorphous Si and organic TFT devices are constrained by materials and/or substrate process limitations and result in TFTs with low mobility (less than $1\,cm^2/V\text{-}s$). Thus,

applications that require even modest computation, control, or communication functions cannot be addressed by today's TFT technology. To achieve the desired ability to implement diverse electronic functions, it will be necessary to develop a transistor technology that can switch at least millions of times a second, rather than only thousands of times a second as is possible with today's technology. Doing so requires balancing process parameters and resulting electrical parameters suitable for intended applications.

1.3.1 TFT Device Fundamentals

A detailed discussion of TFT device operation is outside the scope of this chapter. Comprehensive review of TFT design parameters and related electrical characteristics is available in the published literature.[27,28] The actual performance of a TFT is determined by a wide range of interacting characteristics that depend on material parameters and dimensions of the device. Here we will focus on the critical first-order parameters that must be significantly improved as the minimum first step in achieving enhanced performance. Although the detailed description is complex, the fundamental features that dominate macroelectronic device performance are simple as shown in Figure 1.9. To first order, the higher the mobility (μ) and the shorter the channel (L), the higher is the transit frequency (f_T, a measure of the speed of the device). f_T is a key parameter that determines maximum frequency performance of a device in both digital and RF applications. The mobility is a measure of the ease of movement of charge carriers from the source across the channel to the drain. A low number indicates that there are many impediments to charge transport. The channel length is simply the distance that separates the source

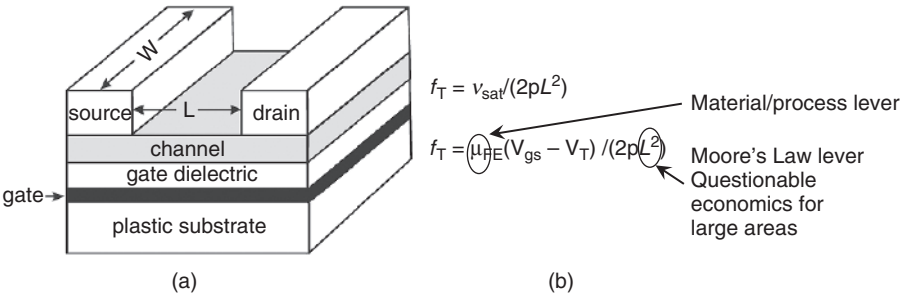

Figure 1.9. Device, materials, and process parameters to achieve high-performance thin-film transistors. (a) Thin-film transistor structure. TFTs consist of a substrate (in this case, a plastic sheet), a conducting "gate"; a semiconducting "channel" layer; a "gate dielectric," which separates the gate from the semiconductor; and source/drain contacts. The device operates by modulating the current flow in the channel (between source and drain) by applying a voltage to the gate. (b) Equations governing the performance (i.e., speed) of a TFT.

of carriers (source) from the collection point (drain). Although shorter channels are an obvious means for faster device operation, they also can be important because the shorter distance means that the charge carriers will interact with fewer impediments when crossing the channel.

One reason macroelectronic TFTs have significantly degraded performance is because, in microelectronic crystalline semiconductor TFTs, there are relatively few impediments and the device mobilities are in the range of hundreds to thousands of centimeters squared/volt-seconds. In comparison, macroelectronic TFTs, which comprise amorphous or polycrystalline materials, have many impediments, particularly at grain boundaries or surface discontinuities. Thus, these devices have mobilities of about 1 cm^2/V-s or even less. Therefore, for a given feature size, a macroelectronics TFT could have performance degraded by two or even three orders of magnitude compared with conventional crystalline semiconductors, simply as a result of intrinsic materials properties. Therefore, as will be described in detail in subsequent chapters (e.g., see Chapters 3 and 5), a major macroelectronics device development emphasis has been on finding materials and processing techniques that offer significant improvement in mobility, with little or no cost impact compared with amorphous silicon. Organic semiconductors devices (OFETs) tend to be consistent with the cost objectives, but they have mobilities about the same (or worse) than amorphous silicon. As noted, polycrystalline, rather than amorphous, silicon provides a significant performance improvement. But its increased processing cost becomes an important issue.

Since f_T increases exponentially with shorter channel length, all other factors being equal, the best way to achieve higher performance is to make devices with shorter channels. This is essentially responsible for the major advances in semiconductor microelectronics technology for the last several decades. Channel lengths are now in the 100 nm or less regime, which results in transistors with operating frequencies of >100 GHz and digital circuits that operate at 1 GHz or more. However, typical printing technology aimed at macroelectronics provides feature sizes of 100 μm or larger, with advanced methods capable of about 20 μm. Thus, for the same materials, a microelectronics device (channel = 100 nm) would have a f_T 40,000 $[(20/0.1)^2]$ times larger than a macroelectronic device (channel = 20 μm). The difference in potential performance between the two types of devices can be appreciated as follows. Even if a macroelectronics TFT is fabricated with a channel length of around 1 μm (very difficult/expensive in a commercial process), it could be as much as 100 times slower than the corresponding deep submicron microelectronics transistor (channel < 100 nm). Obviously, because shorter channels and overall smaller devices can provide so much performance improvement, many printing methods capable of smaller and smaller features are being explored and developed for adaptation to macroelectronics. The scope and limitations of several of these will be described in detail in later chapters.

Although the above discussion addresses the major concerns associated with the semiconductor component of high-performance macroelectronic

TFTs, other issues must also be satisfactorily addressed. The gate dielectric (see Figure 1.9), for example, must be deposited via a method that results in no pinholes and ensures the integrity of the dielectric layer between gate and channel. Ideally, the deposition process will also be able to provide a thin dielectric film so that the gate voltage that must be applied to start current flow is not too high for practical circuits. In addition, the deposited dielectric must have very little trapped charge or other defects, especially near the semiconductor interface. Such defects are another source of degraded mobility, as they also impede the smooth flow of charge carriers across the channel. Besides the dielectric and semiconductor components, other device features can also have significant impact. For example, low-resistance, ohmic contacts are also essential to minimize the effects of parasitics on device performance.[29]

The capability to fabricate an individual high-quality thin-film transistor with attributes as described above is certainly important. However, from a circuit perspective, high device yield and uniformity also must be achieved. Furthermore, the device characteristics must remain reasonably constant and metal interconnects must provide both low resistance and durable, rugged performance when the substrate is flexed.[30–33] Promising technology capable of yielding resistivity comparable with bulk metals, but rugged enough for thin, flexible substrates has been achieved using directed self-assembly[34] and thermal spray deposition.[35,36] Both methods provide a means for room temperature deposition of a variety of metals and insulators for fabrication of passive electronic components. The directed self-assembly technique is adapted from the well-known laboratory technique, but it has been scaled to process large glass plates and fabrics. Thermal spray is somewhat similar to a variety of vacuum deposition techniques except that it operates in an ambient atmosphere and the vaporized material can be shaped to provide a beam size of about 100 μm.

In summary then, current macroelectronic device technology results in devices with mobility of $<10\,cm^2/V\text{-}s$ and channel lengths of $>10\,\mu m$. Research is being aggressively pursued to improve both of these key metrics significantly. However, it needs to be understood that unless low-cost methods are developed to provide micrometer-sized channel length devices and semiconductor materials with mobility more than $100\,cm^2/V\text{-}s$, macroelectronic transistors will suffer a significant performance penalty and limitations on the applications that can be addressed. System designers will need to deal with this issue to increase overall functionality without the benefit of the best device performance.

1.3.2 Next-Generation TFTs

If amorphous Si TFTs and OFETs are adequate only for lower performance, lower cost applications, what are the options for more advanced applications? To achieve the higher performance that is desired while keeping process technology consistent with the goals of macroelectronics, several different fabrica-

tion methods and materials are being explored. Primarily, work in this area has focused on crystallization of vacuum-deposited amorphous silicon to create polysilicon (known as LTPS) device islands at low processing temperatures, which are compatible with glass and even plastics. This advance has resulted in devices with mobilities of 100 cm^2/V-s and even higher.[37–39] Devices and circuits have even been produced on polyimide with operation at 100 MHz, which shows the potential for good device performance even on flexible substrates.[40] Significant literature is already available that describes efforts at improving the device/circuit characteristics of conventional polysilicon-based TFTs. The interested reader is referred to several review articles[27,37,39] and to several excellent reference volumes[41] that describe the efforts to circumvent process temperature issues by fabrication of LTPS devices via laser-induced crystallization. We note that display manufacturers are now introducing products with on-display LTPS driver and demux circuits, with built-in memory expected in the near future.[6,42]

Rather than laser processing, another approach for solving process temperature limitations is to look for new substrates that are less sensitive to heat. In particular, plastics made from liquid crystals or silicone resins are showing some promise.[43–45] For applications that do not need transparent substrates, thin metal foils can replace the plastic.[39] LTPS circuits on stainless steel foil that switch at rates of several hundred megahertz up to a gigahertz have been fabricated. Devices fabricated with this approach also provide performance that is satisfactory for operation of analog circuits.[46] A key issue here is the surface roughness of the foil. Planarization is critical for avoiding defects caused by pinholes in the over-layers and resulting low yields of LTPS circuits because of shorting to the metal substrate.

Although LTPS technology has made great strides for display applications as noted above, deposition and crystallization of semiconductors on flexible, low-temperature substrates remains a significant problem, with currently only relatively expensive solutions. Therefore, researchers have turned to solution deposition as a means of providing high-mobility semiconductors at relatively low cost. Promising results in the range of 10–100 cm^2/V-s have been reported.[47,48] These approaches include TFTs made from a variety of polycrystalline materials. The end objective is the capability to provide polycrystalline semiconductor materials by a variety of printing/deposition methods that do not require vacuum deposition and/or high-temperature thermal processes to achieve high-quality TFTs. Note also that a variety of semiconductors can be used such that optimum material for a given function can be employed. Subsequent chapters will describe the range of materials and processes being developed (see Chapters 3–5 and 7).

1.3.3 Technology for RF TFTs

As summarized, significant advances have been made with LTPS from a performance and cost perspective. In addition, lower cost solution-based

processing of inorganics as an alternative to LTPS is progressing. However, even these advances have limitations, and therefore, one of the most important and most challenging applications for the proposed macroelectronics technology remains unsolved. TFT technologies able to reach the level of RF Performance needed to support sensor-based consumer electronics and electronically scanned antennas for government communication and radar systems, must be found. Many next-generation radar systems require very large, electrically scanned antenna arrays, which are flexible and conformal.[49] Antenna sizes of up to 5000 square feet or more are needed for some applications. A extremely low weight is critical for airborne or space-borne applications, and a low cost is required to attain system affordability goals. The goal is RF circuit performance at over 500 MHz or even several gigahertz if possible. Flexible plastic antennas incorporating active circuitry at each element of the array (to include low-noise amplifiers, RF switches, active RF combiners, and digital control circuits) are ideal candidates to meet these requirements. The challenges here include not only gigahertz-type switching, but also low noise figure operation for adequate amplifier operation. In addition, an ideal solution is a transceiver, which requires that the TFT technology provide at least milliwatt levels of output power at an efficiency of more than 10% to achieve practical solutions.

The challenges for application of macroelectronic TFTs for RF are significant and the available technical solutions are limited.[3] As described in Section 1.3.1, high f_T devices required for RF can be most effectively achieved "simply" by reduction of the channel length. Unfortunately, production of such short channels is both expensive and difficult, as is well known from microelectronics experience. This is even more so for macroelectronic devices because it is difficult to generate such small features reproducibly over the large substrates desired for production. Furthermore, the large substrates may be glass or various plastics, which tend to have rougher and undulating surfaces (compared with semiconductor wafers), making it even more difficult to control small feature sizes.

However, the benefit of smaller geometries is significant. Thus, if all other factors were the same, a lithographically defined device at 1 μm would have a theoretical f_T 400 times higher than the corresponding ink-jet-fabricated device with a 20 μm channel. For high-performance TFTs, an improvement of several orders of magnitude over existing technology can be expected by simultaneously increasing mobility and decreasing device dimensions. For example, using values consistent with modest semiconductor technology, for mobility (>100 cm^2/V-s) and channel length (1–2 μm), Figure 1.9 indicates that the theoretical maximum f_T is in the 5–15 GHz range. Real devices, of course, have parasitic elements that degrade the performance and practical circuits do not operate at the peak performance of an individual device. Therefore, a realistic expectation for a macroelectronics TFT RF circuit is probably about 1 GHz, possibly as high as 3 GHz. This is, obviously, very mediocre when compared with hundreds of gigahertz achieved by microelectronic devices and circuits.

But, it is substantially better than the tens of kilohertz that classic amorphous silicon or OFETs can achieve. It is also in frequency ranges of interest for many mobile communication systems and radar detection bands and, therefore, would provide sufficient capability for a range of RF opportunities.

High-resolution lithography is usually associated with microelectronics. However, a promising solution to the production of small feature sizes for TFT fabrication even on flexible substrates is available, but it has not yet received widespread use. It is based on scanning laser projection lithography with resolution and alignment capability in the 1–2-micrometer range.[50] If this approach can be successfully integrated into a solution-based fabrication approach, it should provide a significant advantage over available printing methods. Microcontact printing (see Chapters 12 and 13) is expected to also play a major role here in the future.[51]

Although significant reduction in feature size is essential, other advances will also likely be required. In the next section, we describe results that promise to improve the semiconductor materials significantly and to provide dramatic improvement over existing LTPS TFT technology. Of course, achieving these material and lithography advances in a cost-effective manner is yet an additional challenge that must be overcome.

1.3.4 Exploratory TFT Concepts

Because of the desire to address increasingly more demanding electronic functions, approaches that employ crystalline semiconductors may be required. However, a successful solution will also require that low-cost manufacturing, potentially available via printing methods, be achieved. Recently, approaches that use micro/nanoscale objects—e.g., nanotubes, nanowires, ribbons, disks, and platelets—of high-quality, single-crystal semiconductors have been reported.[52] A collection of these building blocks constitutes a type of material that can be deposited and patterned, by dry transfer printing or solution casting, onto plastic substrates, thereby forming an effective semiconductor layer to yield mechanically flexible thin-film transistors that have excellent electrical properties.[52–54] Because this approach separates the semiconductor growth process from the device substrate, it is independent of traditional requirements for epitaxy, thermal budgets for processing, and other considerations. As a result, it is well matched not only to flexible electronic systems on plastic substrates but also to devices that require heterogeneous or three-dimensional integration (see Chapter 13 for more details). This type of approach has been successfully demonstrated for highly bendable device arrays of modest size and should be scalable to large areas.[52,53,55] Devices fabricated with microstructured GaAs and 2-μm channels, with an f_T of almost 2 GHz, have been reported.[54] An interesting alternative technical approach here may be the application of direct laser transfer to move desired materials or devices from a temporary carrier transfer sheet onto the host substrate.[56]

Another strategy to integrate thin, high-quality semiconductor materials involves printing nanowires onto a low-temperature substrate.[57,58] In this approach, the nanowires, which may possess a core-shell structure, including a thin outer layer of high-quality silicon dioxide, are grown in an offline reactor. The nanowires are then suspended in a solution and printed onto the substrate. Work to date indicates that performance approaching that of bulk Si devices can be achieved with hole mobilities of >200 cm^2/V-s demonstrated. Non-RF optimized devices fabricated with the nanoribbon/wire approach with gate lengths of 2 μm have shown f_T of over 100 MHz. Perhaps of greater interest, not only Si nanowire devices can be fabricated. Other semiconductor nanowire devices, including those fabricated from GaAs, InP, and CdS via the same approach, have been reported.[58] A detailed discussion of nanowire structures and synthesis, as well as their use in fabrication of electronic devices, will be given in Chapters 10 and 11.

Although both nanostructured and nanowire approaches can avoid the need for high-temperature processing of the gate insulator to facilitate fabrication on low-temperature substrates, these methods may not always be applicable. Another promising approach to achieve low-temperature, yet high-quality, gate oxides is the development of solution-deposited, self-assembled nanodielectrics.[59,60] These dielectrics can be solution-deposited at thicknesses of 15 nm or less. The resultant films have leakage currents of less than 10^{-8} A/cm^2 and breakdown voltages of 6–7 MV/cm. Device mobility is several times higher and on-current is about 10 times higher compared with values achieved from devices with a conventionally deposited SiO_2 dielectric. A more complete description of solution-deposited dielectrics is presented in Chapter 4.

Although not a classic semiconductor material, single-wall carbon nanotube (SWNT) based TFTs have also received significant attention for microelectronic applications recently. Because of their unique properties, including potential mobilities of 10,000 cm^2/V-s or higher, as well as the ease and low expense of producing them in large quantities, they provide significant promise for a variety of device applications. These properties have also made them attractive for large-area electronics because of the possibility of achieving extremely high field-effect mobilities via printing a nanotube suspension onto substrates.[61,62] Because of the extremely high intrinsic per-tube mobilities, it is expected that very high device mobilities will be possible by increasing the fill factor of tubes from the current relatively low values of 1–2%.

Several major challenges must be overcome in order to take full advantage of carbon nanotubes as an electronic material. A major barrier to very low-temperature processing is the gate dielectric; it is difficult to form low-temperature deposited dielectrics with high dielectric integrity and with low hysteresis for the SWNT devices. A promising solution for this problem may also be the nanodielectrics mentioned previously.[63] Perhaps a bigger issue is that as-grown carbon nanotubes can be either semiconducting or metallic. Therefore, a means must be found either to remove the metallic tubes selectively or to render them insulating; otherwise, the metallic tubes will act as

electrical shorts. Laboratory methods to achieve this have been reported,[62] but, to date, no method adequate for manufacturing has been reported. Finally, for maximum device performance, it is desirable to have a large density of nanotubes aligned in parallel between source and drain. Just as in the case of semiconductor nanowires, a reliable means must be developed to orient and position the nanotubes (see Chapter 11). Here again, not only would a successful approach provide a means to high-performance devices for large-area electronics, but also as with the nanowire-type approach, "printing" of carbon nanotubes may also be a viable route to three-dimensional (3D) and heterogeneous integration.

1.3.5 Technology Computer Aided Design for TFTs

For either conventional polycrystalline semiconductors or nanotubes and nanowires to be successful, the development of model and simulation tools that can be used for device and circuit design as well as for predictive engineering must be available. Since these devices are not necessarily based on single "wires" or single crystals, but rather on an ensemble of particles, the aggregate behavior must be considered. Initial efforts to provide the necessary physical understanding and device models using percolation theory have been reported.[64,65]

Although computer-aided design technology is highly developed for microelectronics, there is much that that needs to be modified, extended, or developed for macroelectronic devices. Design requirements, tools, and techniques have not been evaluated, optimized, or even defined for many of the materials, structures, and applications in the frequency ranges of interest. For more demanding applications like RF devices, advanced modeling capabilities will be required to simulate RF circuits accurately. Ideally, two-dimensional models should be available to provide a higher level of model fidelity and assistance in improving TFT reliability.[66]

1.4 APPLICATION CHALLENGES: OPTOELECTRONICS

Although high-performance TFTs are needed for several electronic applications, the potential for printed, inorganic electronics encompasses other devices and applications. A major opportunity is in optoelectronic applications, which impose different requirements, challenges, and opportunities (see Chapters 6, 7, 9, and 11 for discussion of solution-processed solar cells and other printed optical devices).

1.4.1 Photovoltaics

As discussed previously (e.g., see section 1.1.2), photovoltaics is already a commercially successful application of macroelectronics and appears poised

to expand even further with solution-based inorganic materials and large-area, roll-to-roll processing reaching maturity. Just as TFT-based flat panel displays have become successful based on a relatively simple electronic switch, PV's success is also based on a relatively simple device, i.e., a pn junction photodiode. Comprehensive descriptions of the specifics of junction diodes and their use in PV technology are available elsewhere.[67,68] Here, we will focus on the key challenges to the development of a successful solution-based manufacturing technology. From this perspective, the focus is on the following material properties: energy band gap, quantum efficiency, photo-efficiency, and suitability for solution-based processing.

The band gap is important because it determines the energy of the incident photon required to create an electron in the semiconductor diode. When light is absorbed, an electron–hole pair is created and the charge carriers are swept away and collected at the respective diode electrodes. If the band gap of the material is small, a large percentage of the incident photons can generate an electron. However, because the band gap (difference in energy between valence and conduction bands) is small, the electrons that are produced are relatively low voltage and of limited utility in an external circuit. If the band gap is large, then the electrons have higher and more useful voltages. Unfortunately, the percentage of incident photons that have high enough energy to create an electron falls off at shorter wavelength/higher energy. Therefore, selection of the material with the optimum band gap for the intended PV application must be done carefully.

The next challenge is quantum efficiency. This is a measure of what percentages of absorbed photons are converted to electrons. Energy from absorbed photons that is not converted to electrons is dissipated as heat. Such nonradiative processes are more of a problem for solution-processed inorganic materials because the noncrystalline or polycrystalline nature of the solution-deposited film tends to create more locations where electron-hole pairs can relax back to the ground state without production of an electron, thus reducing the efficiency of the cell. Here, as in TFTs, defects can trap electrons and prevent efficient collection of the generated carriers (electrons/holes), thus degrading the efficiency of the PV device. The problem that solution processing must successfully address is, therefore, to find deposition and post-processing conditions that produce devices with quantum and overall efficiency comparable with those fabricated with vacuum deposition technology (i.e., to achieve comparable film quality for the active layer).

Finally, the materials must be readily suited for solution-based deposition on large areas, either on large glass plates or on flexible metal foils. Although solution-based processing is potentially economical in the use of materials, achieving throughput comparable with large vacuum deposition processes is a major challenge.

Although this discussion has focused on challenges for solution-based processing for PV, the fundamentals apply to other optoelectronic applications to be discussed in the following sections. First, the material characteristics

must be achieved to maximize absorption (or transmission depending on the application). Next, the efficiency of the photo process must be maximized so that the absorption energy is not dissipated as heat, and finally, the electrons created by the photo process must be efficiently collected at the electrodes (or vice versa for emissive devices).

1.4.2 Transparent Conductive Oxides

Transparent conductive oxides (TCOs) of various types have been used in a wide range of applications, such as conducting electrodes for displays, solar panels, and electroluminescent lamps; as materials for electromagnetic interference (EMI) / radiofrequency interference (RFI) shielding applications; and in architectural and automotive window glasses.[69] The major considerations and development activity has been focused on maximizing both conductivity and transmissivity. Although there is a large class of TCO materials, such as CdO, Cd_2SnO_4, $CuAlO_2$, $CuGaO_2$, $BaCu_2S_2$ and $SrCu_2O_2$, the most commonly used transparent conductors are simple binary oxides, such as SnO_2, In_2O_3, and ZnO, or ternary alloys, such as $In_2O_3SnO_2$.[70]

For more than half a century, indium tin oxide, commonly referred to as ITO, has been the transparent conductor of choice for display applications, whereas SnO_2 and doped ZnO have been the most widely used materials in solar cells, architectural glass, and RFI/EMI applications. Although several other transparent oxides and their respective alloys have been explored as possible alternatives, the ease of processing for large-area applications and superior electrical and optical properties of ITO, SnO_2, and ZnO have made them the most widely used. These materials are highly transparent within the near-ultraviolet (UV)and visible range. Appropriate electrical conductivity values are achieved through the proper selection of material processing and the introduction of native (controlling the stoichiometry within the film) or substitutional dopants. The obvious challenge here for solution-processed inorganic systems is to achieve comparable performance to these well-established vacuum-deposited materials.

1.4.3 Transparent Transistors

Although transparent diodes (of interest for PV and "smart windows" applications) were fabricated over a decade ago, successful demonstration of transparent TFTs using various group IV oxide semiconductors are also beginning to show promise. Although these device demonstrations are scientifically interesting, the technology is far from offering significant performance improvement over existing TFT technology. Researchers have reported fabricating TFTs using sputtered ZnO on Si substrates but with field-effect mobilities of only ~–2 cm^2/V-s.[71,72] Improved device performance using epitaxial $InGaO_3(ZnO)_5$ has been reported.[73] However, neither of these material

systems is desirable for commercial applications, especially when considered from a solution-based deposition perspective.

1.4.4 Light-Emitting Diodes

Optoelectronic applications such as blue and near-UV light-emitting diodes (LEDs) and detectors are well established in microelectronics. Equivalent macroelectronic devices may become feasible, if suitable p-type materials become available. The most fundamental problem is in finding p-type TCOs that can be used to form efficient pn junctions. P-type TCO materials such as $CuAlO_2$, $CuGaO_2$, and $SrCu_2O_2$ are in early development. What is really needed is a ZnO-based p-type semiconductor to create a transparent analog of a Si pn diode. Additional discussion on low-temperature solution processing of oxide electronic materials is presented in Chapter 4 (although in this case focusing on dielectric applications). Here, we simply note that the initial challenges are the fundamental electrical and material properties required for adequate electrical characteristics. After this will come the challenge of maintaining adequate optoelectronic performance using solution-deposited materials and methods.

1.4.5 Solid-State Lighting

An area of significant technological interest is solid-state lighting and its application to distributed light sources. Although general lighting technology options may seem straightforward, the cost of ownership is a significant issue that adds considerable complexity. A 100-W incandescent light bulb costs less than $1. With an efficiency of 15 lm/W, this represents a lamp cost of less than $1 per kilolumens. The cost for fluorescent lighting is approximately a factor of two higher. However, the average lifetime of an incandescent bulb is about 1000 hours, whereas that of a fluorescent tube is approximately 20,000 hours. Therefore, the cost of ownership calculated over the life of the lamp is much lower for a fluorescent lamp compared with an incandescent lamp. Thus, cost of ownership is particularly important in understanding market penetration of alternative technologies in the commercial and industrial markets.[74]

Although there has been tremendous progress in conventional microelectronic III–V-based LED technology, the major commercialization challenge for penetration into the general lighting market is achieving the cost targets that will be required to compete with existing incandescent and fluorescent lamps.[75] As these LEDs are manufactured on small (2–3″ typical), expensive substrates and are point sources, system integration costs, including backend packaging, light, and thermal management issues, pose a significant barrier to cost reduction over the next decade. Healthy penetration in automotive exterior lighting as well as niche architectural lighting applications are expected[76] and will continue to push down the cost of this technology. Since manufacturing cost is such a significant issue, a printed electronics-based solution could

be attractive. Unfortunately, currently, the technical challenges coupled with the highly competitive cost structure seem to be too difficult for a viable point source lighting solution based on solution processing.

In contrast, extended (distributed) light sources, by their nature, circumvent such issues and are more consistent with printed electronics technology. Organic LEDs (OLEDs) represent another technology platform suitable for large-area solution processing.[77] However, the improvements in the reliability of organic semiconductors required to meet general lighting requirements continues to be very challenging. More environmentally stable thick-film inorganic electroluminescent devices have been used to fabricate flexible and thin illumination sources for LCD backlights, some automotive applications and novelty applications such as night lights. Even though this technology is well suited for solution-based large-area processing, efficiency, and lifetime remain as major problems. Because of a short lifetime, low luminance, and high operating voltage, this technology has found only limited applications in general illumination or displays. However, the attractive features of LEDs for lighting and the solution processability of OLEDs and inorganic electroluminescent materials, coupled with the importance of lighting in overall energy consumption, suggests that this may be an active area for future research.

1.4.6 Si-Based Integrated Emitters

Nanocrystalline silicon presents opportunities for integrating optoelectronic functionality on large-area substrates. Recent reports of light emission from silicon represent an exciting and innovative area of research that combines advances in nanoscale silicon and silicon oxides and rare earth materials.[78] Adoption of methods that have been developed in the flat panel display industry for silicon-based solid-state lighting provide the advantage of having manufacturing processes that are compatible with CMOS and flat panel display processing. Therefore, this technology can be integrated with existing silicon devices, or be fabricated on large-area glass substrates (similar to those used in FPD fabs) with great potential for cost improvement as compared with III–V-based LEDs. In addition, this approach offers the possibility for developing large-area light sources.

One of the most exciting and promising recent areas of research has been the development of silicon nanocrystals embedded in a silicon oxide matrix. This activity initially focused on the development of high-density-embedded memories.[79] More recently, it has led to interesting applications in silicon microphotonics. Although much of the current effort is on synthesis of nanocrystals with proper size and passivation, in order to achieve saturated emission color and high luminescent efficiency, several other technological advances need to occur. These include the development of efficient and low-cost methods to insert and activate rare earth ions. Downstream use of nanocrystals for fabrication of efficient electrically pumped devices is in the early stages of development. As the technology matures, adaptation of printing and solution

deposition techniques would allow exploitation for novel large-area applications.

Innovative technologies that consist of highly efficient emitters, compatible with CMOS production processes and inherently large area, so as to be manufacturable on flat glass panel substrates, present significant potential as they cut across several markets (e.g., display, telecom, and lighting) and offer a paradigm shift in manufacturing cost. Furthermore, the increase in substrate size that can be used for product manufacture represents a major factor in reducing production cost even more dramatically, especially if FPD infrastructure can be leveraged. What has been demonstrated is based on traditional semiconducting processing methods; adoption of methods similar to what is discussed in Chapter 5 (Liquid Silicon Materials) to silicon nanophotonics would offer exciting possibilities for large-area silicon-based optoelectronics.

1.5 APPLICATION CHALLENGES: POWER SOURCES, SENSORS, AND ACTUATORS

Although a wide range of potential electronic and optoelectronic applications have been described, at least one more component must be considered to achieve a truly integrated macroelectronic system. Perhaps the most difficult of the major challenges for macroelectronics is providing adequate power (and power storage), especially for systems that are field portable such as large-area PV and antenna arrays. Although existing lithium ion batteries are well suited for conventional microelectronic portable device applications, thin-film batteries offer possibilities for device level integration into macroelectronic systems. What would be truly innovative would be the integration of thin-film microbatteries as power sources for macroelectronics (flexible displays, large-area electronics, and integrated flexible photovoltaic modules). This could lead to new applications in autonomous sensor units, miniature remotely piloted vehicles, self-powered 3D circuits, and power modules with integrated batteries and photovoltaic layers. Unlike commercial lithium ion batteries, which are fabricated using solution-based processing methods, existing thin-film battery technology is based on vacuum deposition methods.[80] Even though large-area, thin-film batteries on flexible Kapton films have been commercialized,[81] for them to become primary sources of energy for macroelectronics, energy capacity needs to be increased significantly along with methods to fabricate these devices at lower temperatures to facilitate integration with other components and multiple substrate types. Rather than lithium-based technology, much older electrochemical cell technology has been successfully converted to roll-to-roll manufacturing for integration into various large-area applications. Zinc/MnO_2 is a well-known and well-understood technology. Several companies are now making it available in thin-film format (Figure 1.10).[82,83]

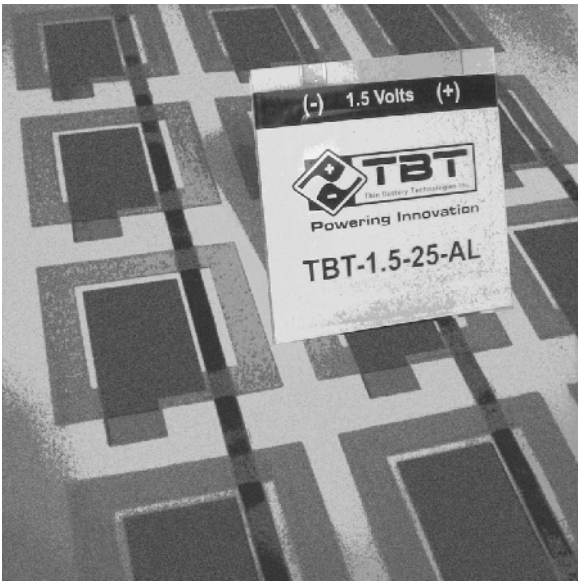

Figure 1.10. Example of fully integrated battery and electronics. [Figure courtesy of Thin Battery Technologies, Inc. Used with permission.]

Of course energy storage is just part of the power source problem. If the battery cannot be replaced or recharged readily, then energy harvesting must be considered. Even though the technology for stand-alone PV is well established and progressing at a rapid pace, integration of PV cells with other electronic functions as suggested earlier is still some years and several research breakthroughs away. Currently, printed organic-based PV technology has shown promise for this type of application.[84] However, solution-deposited inorganics (see Chapters 6 and 7) are a more attractive solution because of the demonstrated higher conversion efficiency and greater stability to oxygen, water, and light. The same can also be said for various other energy scavenging mechanisms, which are reasonably well understood as a discrete component, but will likely need considerable effort to integrate into a complete macroelectronics system.

There are more issues and complexity to be considered if various microelectromechanical (MEMS)-type devices are included in the macroelectronics tool kit. As described previously, the materials and devices required for TFTs and circuits can provide adequate electromagnetic (visible and RF) sensitivity for many image-type applications. These materials may also provide satisfactory performance in pressure and strain sensors. Nanotube/nanowire-based devices look promising for various chem-bio sensors.[85] However, there is little that is known about the ability to integrate printed microfluidic devices (and other such devices with moving parts) into a roll-to-roll-type process.

Questions regarding applicability of particular technologies to particular applications must, of course, be resolved eventually. However, mainstream focus has been on achieving adequate TFT device and circuit performance to support the control, computation, and communication functions for a wide range of potential applications. As satisfactory electrical circuit performance is attained for additional functionality, questions that relate to the quality of other device types, their integration into an overall process flow, and perhaps most importantly, the robustness and stability of the final product, will receive much more attention.[86–88]

1.6 CONCLUSIONS

In this introductory chapter, the intent has been to identify and describe the two major electronics technologies, with an emphasis on why and how Macroelectronics is related to, but yet very different from microelectronics. The differences in intended product applications drive macroelectronics to have very different requirements in terms of manufacturing technology and required electrical performance. In contrast to microelectronics, the main objectives for macroelectronics are very low cost and processing on large-area, preferably flexible substrates. These attributes, when achieved, will allow a wide range of interesting and novel applications ranging from surface conformal electronics to rollable/foldable multi-meter-area distributed electronics.

The display and PV industries are the first examples of commercially successful macroelectronics. Research is being aggressively pursued to extend these initial successes into a wide range of new areas that require lower cost, higher performance, and compatibility with a variety of substrates. Existing solutions based on amorphous silicon, LTPS and organic TFTs have not been successful because of either cost and/or performance limitations.

To achieve more aggressive cost and performance objectives, new materials, devices and manufacturing methods must be developed and combined into an integrated, cost-effective macroelectronics solution. One of the most promising approaches for this next generation of macroelectronics technology is solution deposition of inorganic materials. This class of approaches should provide the means to deposit the key electronic materials—metals, semiconductors, and insulators. Furthermore, the methodology is scalable from wafer-sized, to sheet-sized, to roll-sized substrates. It also offers the potential to enable high-performance devices, with mobilities of more than $50\,cm^2/V\text{-}s$ or even as high as several hundred, approaching that of crystalline silicon used in current microelectronic devices. Just as critical, numerous inorganic materials can be solution deposited to facilitate high-throughput, low-cost processing and multifunction systems. It can be accomplished at near-ambient temperature so that many substrate types can potentially be used. Finally, inorganic materials tend to be stable to light, oxygen, and water, all of which create problems for the TFTs currently used in manufacturing.

Another critical challenge is combining the materials and device structures with a patterning technique that is consistent with the low-cost objectives, but still providing resolution and alignment features in the less than 10 μm range (preferably in the 1-μm range). Furthermore, this capability must be achievable over substrate sizes of meters and/or in a roll-to-roll format. Achieving both good materials characteristics and small feature sizes will be necessary if significant RF applications (at least several gigahertz) are to be addressed.

Although adequate materials and devices are essential, successful manufacturing will require other capabilities as well. First, the process must have high yield, which implies low variability, and provide robust stability to environmental factors. To produce the envisioned products, there must be readily available electronic design tools that can adequately simulate both device and circuit performance. Although some of these computer-aided design tools are available from microelectronics technology, others must either be modified, because of the differences in the thin-film devices, or created anew because the devices have no equivalent (nanowires and nanotubes).

Since macroelectronics will be most successful if it can integrate diverse materials and devices, the above statements also apply to the creation of technology for solution-deposited inorganic optoelectronic devices, batteries, and sensors, deposited on a wide range of substrate types (including those that are flexible). The fabrication process must be nimble enough to adjust for many product types and many manufacturing variables. As the remaining chapters describe, there is good reason to believe that solution-based deposition of inorganic materials will ultimately provide the necessary device performance and manufacturing capability.

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