1

Introduction to Signal Integrity and Radiated Emission in a Digital System

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This is an introductory chapter in which the motivations for studying the subjects of *Signal Integrity* (SI) and *Radiated Emission* (RE) are discussed.

Signal integrity is a very important task and deals with the need to ensure that electrical signals are of sufficient quality for proper operation. Signal integrity affects all levels of electronics packaging, including, but not limited to, the *Integrated Circuit* (IC). For high-speed digital products, at the level of an IC package or *Printed Circuit Board* (PCB), the main issues of concern for SI are reflections occurring because of interconnect discontinuities, noise induced by neighbouring connections (crosstalk), and noise on power distribution, produced by switching of the digital devices. All these noises can cause functional problems if they are not mitigated by controlling parameters such as the characteristic impedance and spacing of interconnects, which, owing to fast switching of the actual digital devices, should be considered as transmission lines. An overview of the noises affecting SI is given in this chapter, leaving a detailed discussion to the following chapters where the different noises are introduced and investigated separately.

The interest in radiated emission is due to the fact that an apparatus or system must be electromagnetically compatible with its environment. Electronic devices generate electromagnetic fields that unintentionally propagate away from the device's structure, and they may interfere with their normal operation or the normal operation of other devices in close proximity. For this reason, the allowable radiated emissions from electronic modules are regulated by mandatory standards which must be complied with before marketing the apparatus or system. In this chapter, FCC part 15 and CISPR 22, relating to emission from digital systems, are highlighted, and the sites for measurements are discussed. Particular emphasis is given to the new EMC European Directive 2004/108/EC which makes it possible to demonstrate conformity of a product to the essential requirements of emission and immunity by using calculations and therefore computer simulations instead of measurements. The three main sources of emissions of a complex digital system (traces, integrated circuits, and cables) are investigated.

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An example of a complex system that complies with the RE requirements is reported, and its emission spectrum with and without shielding is discussed. The difficulties in mitigating radiated emission are shown by using simple radiating structures.

In the third part of this chapter, signaling parameters significant for SI are defined. Some examples of data errors when the voltage and current specifications of the devices are not met owing to reflections on the interconnects are provided. An example of an eye diagram for jitter signal evaluation is provided.

Finally, the last part of the chapter offers an overview of the methodologies suitable for developing prediction models of SI and RE problems. Advantages and drawbacks regarding mathematical, circuit, and numerical codes for simulation are discussed. A list of problems solved by simulation and reported in the book is provided.

1.1 Power and Signal Integrity

Power and signal integrity addresses two concerns in electrical design aspects: the timing and the quality of the signal. The goal of power and signal integrity analysis is to ensure reliable high-speed data transmission. This can mainly be done by setting up design rules in order to mitigate the delays and distortions of digital signals due to reflections, *crosstalk*, and switching noise (*ΔI-noise*):

- Reflection refers to signal waveform distortion caused by discontinuities along the interconnects of the digital devices, such as impedance mismatch, stubs, vias, and other line discontinuities.
- *Crosstalk* refers to the noise produced in a signal line by other lines as inductive and capacitive coupling.
- Switching noise refers to the disturbances induced in a signal line by the voltage drop along the inductive path of the power supply network for the IC and its packaging. This noise is also called *ground bounce*, *ΔI-noise* or *Simultaneous Switching Noise* (SSN).

Power and signal integrity are not regulated by standards because the associated disturbances are considered as internal noises of the system and therefore they do not interfere with the environment or other nearby equipment or systems. It is the task of the PCB designer to prepare a set of design rules to limit these types of noise which affect both timing and quality of the signal. To accomplish this goal, circuit and numerical simulations are used.

The first step to evaluate these types of problem consists in modeling by an equivalent electrical circuit the physical structure of the PCB where the digital devices are located. The physical parameters of the PCB to be considered are: the width, thickness, and spacing of the interconnects (traces); the dielectric constant of the substrate; the via or hole diameter and spacing. The modeling is usually performed by means of closed-form expressions when available, or by using field-solver programs to calculate the desired inductances, capacitances, and resistances. Once these linear network parameters are known, any required quantity, such as the characteristic impedance of the line Z_0 (ohm), the line propagation delay time T_D (seconds), and the line coupling coefficients, can be calculated. The first two parameters are defined as

$$Z_0 = \sqrt{\frac{L}{C}} \tag{1.1a}$$

$$T_D = \sqrt{LC}\,l = t_{pd}l \tag{1.1b}$$

where L is the per-unit-length inductance of the line (H/m), C is the per-unit-length capacitance of the line (F/m), l is the length of the line (m), and t_{pd} is the per-unit-length propagation delay time of the line (s/m).

The key parameters defined by Equations (1.1) are nominal and frequency independent in the frequency range of interest. They refer to a lossless interconnect and depend on the interconnect geometry. For typical stripline and microstrip trace structures used in multilayer PCBs, Z_0 and T_D can be computed with closed-form expressions as reported in *Appendix B*. These two parameters greatly affect the performance, the net design, and the noise limits of power and signal distribution, as will be shown in the following sections [1].

1.1.1 Power Distribution Network

The *Power Distribution Network* (PDN) for a typical PCB is depicted in Figure 1.1a. A *Voltage Regulator Module* (VRM) (i.e. DC/DC converter) provides the required power supply to the digital device by a pair of bus bars or solid copper planes indicated as *Power* and *Ground*. At points P and G, a digital device (i.e. IC) is connected. In this representation, the device has a gate switching from low to high level, and a step voltage ΔV_S with a rise time t_r is launched onto the line (trace) towards a receiver placed somewhere in the PCB. The traveling signal is given by

$$\Delta V_S = Z_0 \Delta I_S \tag{1.2}$$

where Z_0 is the characteristic impedance of the line (trace) and ΔI_S is the variation of current in line before and after the switching. This happens every time the double delay of the trace $2T_D$ is much higher than the switching rise time t_r or fall time t_f of the output voltage. Considering a typical per-unit-length delay time of about 6 ns/m, and rise and fall times (i.e. t_r and t_f) of about 1 ns or less, which is a common situation in a PCB, it is easy to deduce that traces must be modeled as transmission lines. When this situation does not occur, the line is said electrically *short*, and the load of the driver can be modeled by a lumped capacitance which is the sum of the trace capacitance and the receiver input capacitance. For short lines, the inductive effect can be neglected. In any case, at the output of the driver there is a current variation ΔI_S that must be provided by the PDN. When the gate switches, another impulsive current, denoted by ΔI_t, could be sunk by the gate. This current is caused by the momentary simultaneous switch-on of the two output transistors in the typical totem-pole configuration characteristic of TTL and CMOS devices that, with their complementary condition on or off, determine one of the two (high or low) logic levels (see *Chapter 2*). Therefore, the total switching current that the PDN must provide to the IC is given by

$$\Delta I = \Delta I_t + \Delta I_S \tag{1.3}$$

Denoting by Z_{PDN} the characteristic impedance of the PDN or the impedance looking back from the points P and G where an IC is connected, the voltage drop between these two points is given by

$$\Delta V_{PG} = Z_{PDN} \Delta I \tag{1.4}$$

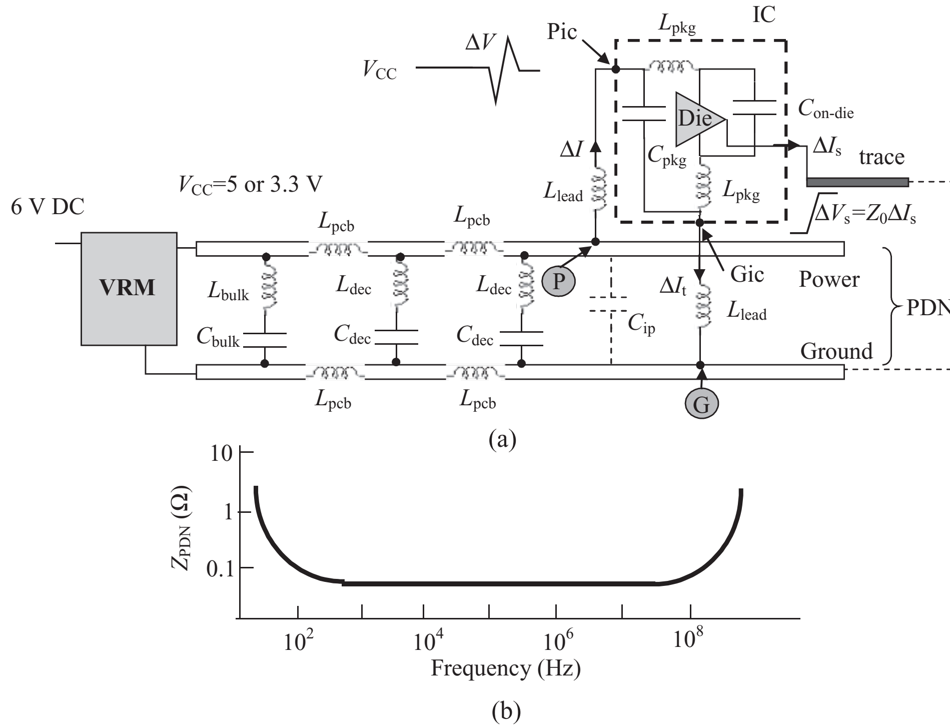

Figure 1.1 Power distribution network in PCBs: (a) equivalent circuit; (b) impedance versus frequency at points P and G

This is an impulsive disturbance, indicated as ΔI-*noise*, that sums to the DC power supply V_{CC} of the device. As many gates can switch simultaneously, this noise, known also as *Simultaneous Switching Noise* (SSN), could rise to dangerous values for the functionality of the system. Therefore, the main task of an electrical designer is to make the parameter Z_{PDN} as low as possible. This goal can be pursued by increasing the capacitance term in Equation (1.1a) by means of decoupling capacitors, and by using power and ground planes instead of bus bars in order to have a higher interplane capacitance C_{ip} and a lower PDN inductance L_{pcb}. This is usually accomplished as shown in Figure 1.1a.

At the VRM output, a large decoupling capacitor, indicated as bulk capacitance C_{bulk}, is inserted for filtering the lower-frequency components of low- and high-level changes caused by circuit switching throughout the PCB. For filtering the higher-frequency components, a number of decoupling capacitors with capacitance C_{dec} are distributed at regular intervals along the PDN and located near the devices. Between each pair of capacitors there is a power/ground effective inductance L_{pcb}. The problem with decoupling capacitors is that their action as capacitance is affected by the inductance associated with the component itself, plus the inductance associated with the component connections to the power and ground conductors, denoted by L_{bulk} and L_{dec}. The effect of these parasitic inductances is shown in Figure 1.1b, where a typical impedance Z_{PDN} is plotted versus frequency. At very low frequencies the network appears

to be capacitive, while at very high frequencies the network appears to be inductive. In the mid-range, capacitances compensate for inductances, yielding a very small impedance for the PDN. The goal is to design the PDN so that the curve is flat and resistive throughout the frequency range required by the speed of the circuits.

To achieve this goal, two strategies can be applied: (1) choose an appropriate number of decoupling capacitors, located in order to minimize their parasitic inductances; (2) make the interplane capacitance large by increasing the dielectric constant ε_r and, above all, by minimizing the distance between the two power and ground planes. All this will be discussed in *Chapter* 8.

Actually, ensuring a low Z_{PDN} curve could not be sufficient for preserving the IC from malfunctions. In fact, the connection of the power and ground pins to the PDN must be realized with care taken to minimize the loop inductance associated with the connections. Looking at points Pic and Gic in Figure 1.1a, which correspond to the power and ground pins of the IC respectively, a further voltage drop on the path of the power supply between points P and Pic must be considered. This is indicated as *power bounce noise* and is given by

$$V_{\text{lead}} = L_{\text{lead}} \frac{\Delta I}{\Delta t} \tag{1.5}$$

where L_{lead} is the effective inductance associated with connection between points Pic and P. This concept of effective inductance associated with a segment of the loop, known as *partial inductance*, is very useful for package modeling, and it will be defined in *Chapter* 3 starting from the loop inductance definition.

Up to this point, it is a task of the PCB designer to minimize all these inductive effects. However, looking within the IC towards the die where the circuitries are allocated, it is important to consider the package inductance L_{pkg} associated with the pins–die connection (between points Pic and die). This inductance also produces a voltage drop on the power supply. It is a task of the device manufacturer to minimize L_{pkg} and to provide a die capacitor $C_{\text{on-die}}$ in order to have an on-die filtering that permits less impulsive current to be required from the PDN. This will be considered in depth in *Chapter* 8 by circuit simulations.

1.1.2 Signal Distribution Network

The *Signal Distribution Network* (SDN) for a high-speed digital system accounts for a considerable part of the total path delay. To minimize this delay, it is very important to examine the role that the characteristic impedance Z_0 plays in designing a SDN. The choice of an appropriate characteristic impedance Z_0 is important to all aspects of the SDN, as it affects net design, net performance, and disturbances such as reflection, crosstalk, and Δ*I-noise*. By superimposing these effects, a design space can be generated for selecting Z_0, as will be shown in the next section.

Consider the interconnect shown in Figure 1.2 where a driver, represented by its Thévenin equivalent circuit, sends a signal onto a line with a receiver R1 along the line (trace), and a cluster of receivers, R2–R4, at the end of the line. The reference plane could be the power plane or the ground plane of the PCB in accordance with the fact that the PDN impedance Z_{PDN} is extremely low in the frequency range typical of signals, as shown in Figure 1.1b, and the AC return current tends to flow along a path that ensures less loop impedance. Each

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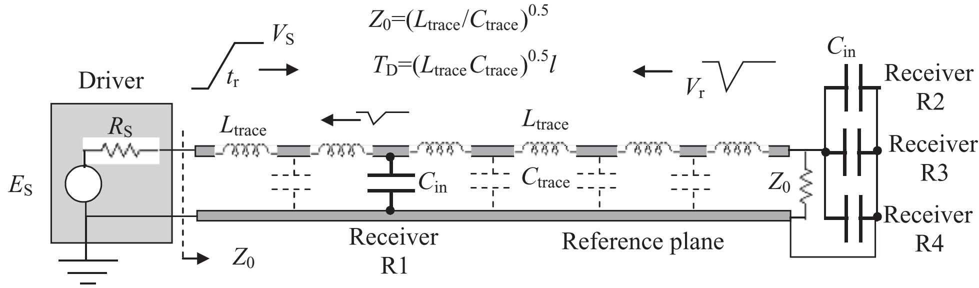

Figure 1.2 Interconnect (trace in PCB) of length l, with receivers concentrated at the end of the line causing large reflections

receiver is represented by its input capacitance C_{in} of some pF, and the line is terminated with its characteristic impedance Z_0 in order to avoid resistive mismatching which could generate large reflections. The inductance L_{trace} and the capacitance C_{trace} are parameters associated with a segment of the trace and determine the line characteristic impedance Z_0 and the delay time T_D according to Equations (1.1). Dangerous reflection peaks are generated by excessive capacitive loads. The mechanism can be explained in this way. When a signal V_S is sent out by the driver, a fraction of the unloaded voltage swing E_S enters the line because of the voltage divider consisting of R_S and Z_0. The signal V_S is given by

$$V_S = \frac{Z_0}{R_S + Z_0} E_S \tag{1.6}$$

From Equation (1.6), two important facts must be observed. To maximize the sending signal in order to ensure switching of the receivers at the first step with a suitable margin, the driver resistance R_S should be minimized and the characteristic impedance Z_0 should be maximized. The upper bound of Z_0 is dictated by the fact that, above certain values, undesired capacitive reflections and excessive coupling effects between traces could occur. While the signal propagates along the line, reflections are generated at each capacitive discontinuity. When the lines are long and the losses can be neglected, the signal travels with unchanged rise time t_r. For a line to be considered long, each segment between two loads should have a propagation delay time T_D that exceeds one-half of the rise time t_r. At each capacitive discontinuity a negative reflection is generated that has maximum value and width given by [2]

$$V_r = -\frac{C_D Z_0 V_i}{2t_r} \tag{1.7a}$$

$$t_{w50} = t_r \tag{1.7b}$$

$$t_{w0} = t_r + 1.5 C_D Z_0 \tag{1.7c}$$

$$T_\Delta = \frac{C_D Z_0}{2} \tag{1.7d}$$

where C_D is the capacitance of the discontinuity, V_r is the peak voltage of the reflection, $V_i = V_S$ is the incident voltage magnitude, t_{w50} is the width of the reflection at the 50 %

points, t_{w0} is the width of the reflection at the baseline, and T_Δ is the delay added to the main line incident signal because of the discontinuity.

Thus, as C_D and Z_0 increase, the reflections V_r defined by Equation (1.7a) become larger and the delay time T_Δ given by Equation (1.7d) becomes longer. Limits should be set on these parameters. If they are not, the reflection from the load at the end of the line, where a large capacitance is formed by the cluster of the receivers, could be so large when it hits the receiver R_1 that it transiently switches into its down state, causing a logical error in a downstream latch. The discontinuity capacitance C_D associated with the load at the end of the line is the sum of the receiver input capacitances C_{in} and the capacitances associated with the connection of the receivers to the line.

A way to avoid this problem is to distribute the receivers along the main line at regular electrically short intervals, or, in other words, so that the delay of the line between two loads is less than one-half of the rise time t_r. In this case, the reflections merge together and the load capacitance is now combined with the line capacitance and treated as if it were uniformly distributed along the line. The additional line capacitance acts to lower Z_0 and increases the propagation delay time T_D. The new line parameters are expressed as

$$Z_{0eq} = \sqrt{\frac{L_{trace}}{C_{trace} + (C_{in} + C_{stub})n/l}} \tag{1.8a}$$

$$T_{Deq} = \sqrt{L_{trace}(C_{trace} + (C_{in} + C_{stub})n/l)}l \tag{1.8b}$$

$$T_{\Delta eq} = T_D(Z_0/Z_{0eq} - 1) \tag{1.8c}$$

where n is the number of receivers distributed for the line length l, C_{stub} is the capacitance associated with the trace connecting the receiver to the main line, and $T_{\Delta eq}$ is the added delay due to loading.

Treating each discontinuity as a lumped capacitance is helpful for understanding fundamental dependencies. However, for actual design work, the effective partial inductance associated with the leads and IC package must be accounted for as done for PDN in Figure 1.1a. Once inductances are introduced into the model, the analytical approach becomes unwieldy and circuit simulators based on SPICE must be used to predict the desired signal waveforms. Reflections will be investigated in detail in *Chapter 5*, where circuit models for their predictions will also be presented.

1.1.3 Noise Limitations and Design for Characteristic Impedance

Three types of noise generally concern the electrical PCB designer: reflection, switching noise, and *crosstalk*. Very often, reflections may be treated separately, while the other two noises can interact. An example of PCB where ΔI*-noise* and crosstalk generated by the digital devices switching can sum, causing a false switching, is shown in Figure 1.3. The upper gate of chip 1 switches and sends onto line 1 a voltage step $\Delta V_1 = Z_0 \Delta I_1$, where Z_0 is the characteristic impedance of line 1, and ΔI_1 is the current difference at the driver output before and after the switching. Recall that Z_0 depends on the trace geometry and on the dielectric constant of the PCB substrate. If line 1 is not matched or terminated with a resistance equal to Z_0, the voltage step ΔV_1 can return in part as reflection towards the driver, causing waveform

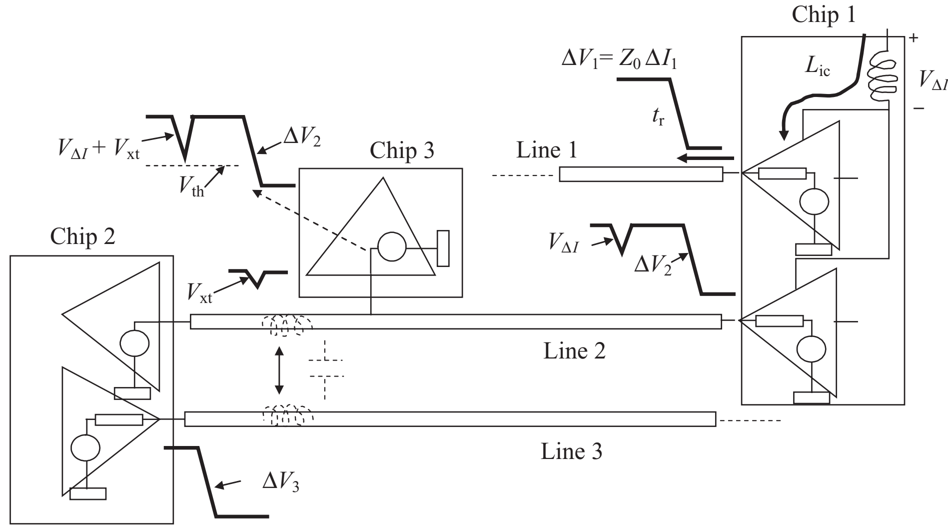

Figure 1.3 Illustration of a PCB where reflection, crosstalk, and switching noises sum

distortions. The current ΔI_1 causes the voltage drop (ΔI-*noise*) given by $V_{\Delta 1} = L_{ic}\Delta I_1/\Delta t_1$, where $L_{ic} = L_{lead} + L_{pkg}$ is the effective power supply inductance of chip 1, and $\Delta t_1 = t_r$. In this example it is assumed that the voltage drop caused by the PDN of Figure 1.1a can be neglected, and only the voltage drop on the effective inductances associated with the lead and package conductors of the IC are significant (*power bounce*). This voltage drop becomes a disturbance for the signal sent by the lower gate of chip 1 just some nanoseconds before, and superposes on the step voltage ΔV_2.

The lower gate of chip 2 switches from a high to a low state with a swing ΔV_3 and, owing to inductive and capacitive coupling between line 2 and line 3 (*crosstalk*), induces a disturbance V_{xt} on line 2. The total disturbance $V_{xt} + V_{\Delta I}$ can cause a false switching at the input of chip 3 if the voltage of the signal plus the total disturbance is lower than the threshold voltage V_{th} of the receiver. The threshold voltage is the nominal level where the receiver changes state. It is important to point out that all three kinds of noise (reflection, *crosstalk*, and ΔI-*noise*) depend on the parameter Z_0. The dependency of crosstalk on Z_0 will be investigated with suitable modeling and measurements in *Chapter 6*. Superimposition of crosstalk and disturbance in line, produced by ΔI-*noise*, happens frequently when a large number of simultaneous switchings occur in the same IC. This will be investigated by modeling and measurements in *Chapter 8*.

The aim of the designer is to find a range of values for Z_0 where the immunity of a generic receiver is maximized, as illustrated in Figure 1.4. The receiver noise immunity V_{NI} is the margin that a designer must preserve to ensure functionality of the system in the presence of other internal and external disturbances, and is defined as

$$V_{N1} = (\Delta V - V_{th}) - (V_{xt} + V_{\Delta I}) > 0 \tag{1.9}$$

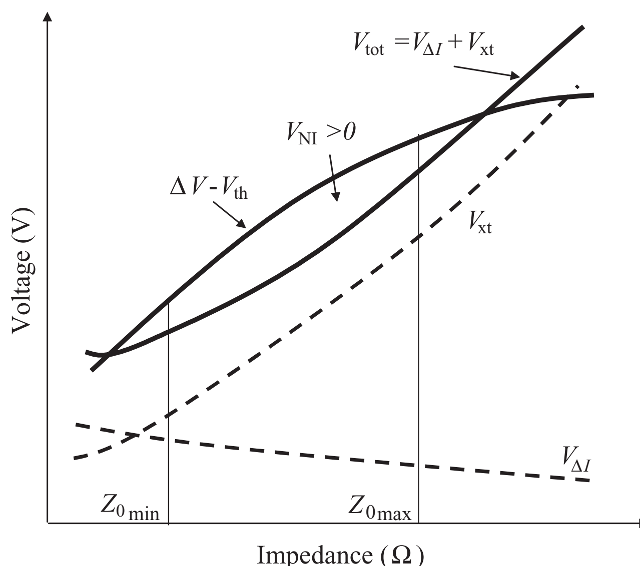

Figure 1.4 Total noise versus the characteristic impedance Z_0 of a PCB trace

where ΔV is the step signal, V_{th} is the threshold voltage of the receiver, V_{xt} is the crosstalk disturbance, and $V_{\Delta I}$ is the ΔI-*noise*.

The condition defined by Equation (1.9) must be verified for both low-to-high and high-to-low switching. As the characteristic impedance Z_0 increases, the step signal ΔV increases and the disturbance $V_{\Delta I}$ decreases because the driver requires less switching current, but, unfortunately, the disturbance V_{xt} increases more than the decrease in $V_{\Delta I}$. This is due to the fact that, to have higher Z_0 values, the traces must be positioned more distant from the reference return plane, and therefore the inductive and capacitive coupling parameters are more significant. To quantify signals and noises, it is very important to have circuit models of the digital devices and their interconnects. How to build up these models will be one of the main purposes of the following chapters.

1.2 Radiated Emission

In this book, radiated emission is considered together with signal integrity because they are strictly correlated. Reflections of signals have the effect of increasing the radiated emission from PCBs, while the switching noise produced by the digital devices generates strong radiations from cables attached to PCBs.

1.2.1 Definition of Radiated Emission Sources

Radiated Emission (RE) regards the unwanted electromagnetic field produced by PCBs and cables of an equipment or system. Radiated emission is regulated by standards because the associated disturbance is considered as an external noise that can interfere with the environment

or other nearby equipment or systems. Experience, measurements, and computer simulations are the tools for preparing a set of design guidelines that take into account the technologies used. Several possible sources and different types of emission can be distinguished. This task is generally very difficult because high values of emission are often due to the unwanted *common-mode* (CM) currents on PCBs and cables. *Common-mode* currents are produced by voltage drops in power and ground planes, caused by impulsive noises flowing through parasitic inductances. The noise voltages across the parasitic inductances feed the cables attached to the PCB which act like antennas. Another source of *common-mode* current on cables is the dissymmetric structure of I/O devices which is difficult or impossible to predict. Although the *common-mode* current is much lower than the signal or *differential-mode* (DM) current (μA versus mA), it produces very high levels of emission, as it returns to the source in the form of electrical and displacement currents making large loops and often uncontrolled paths.

In a PCB, three types of emission source can be identified, as illustrated in Figure 1.5: *Integrated Circuits* (ICs), traces, and cables attached to the PCB.

- Emission from ICs is due to the switching current that flows within the device and forms a small loop. The radiated field can be calculated as radiation by a small loop antenna once the current spectrum is known.
- Emission from traces is due to the signal current. A trace and its reference conductor, generally a plane in a high-speed digital system, form a *Transmission-Line* (TL) structure.

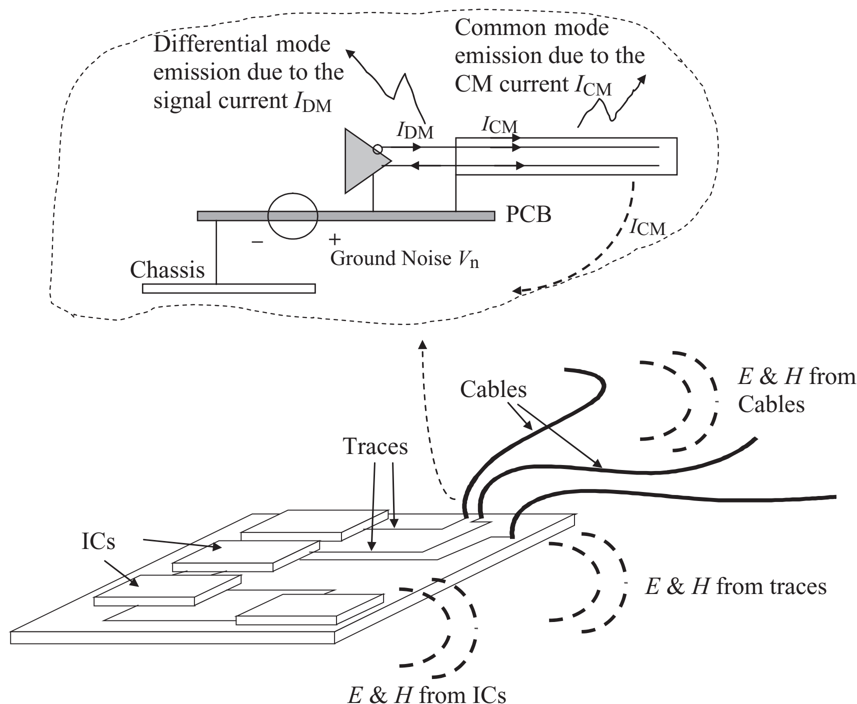

Figure 1.5 Illustration of emission sources from a PCB

Removing the plane and using as the return path a conductor with a distance twice the height of the trace from the plane (image theory), the radiated field can be calculated by segmenting each conductor in electrically small dipoles (length much smaller than the minimum wavelength of interest) and calculating the current in each segment by the TL model, and by accounting for the input/output characteristics of the drivers/receivers.

- Emission from cables is due to the wanted *differential-mode* current I_{DM} used for signaling (often this type of emission can be neglected owing to the cancellation effect that occurs in the pair of signal wires), or due to the unwanted *common-mode* current I_{CM} on the cable which can be caused by the noise V_{n} in the power and/or ground planes of the PCB, as well as by the unbalance of the driver. The radiated emission from cables can be calculated by combining the transmission-line model (i.e. *differential-mode* emission) and the long monopole or dipole antenna models (depending on the position of the cable), fed by the noise in the PCB, and having the cables as branches (i.e. *common-mode* emission). With attached cable, it is intended that an I/O cable, because of the low output impedance of its line driver device, behaves like a wire connected to the ground of the PCB. Even if the driver does not transmit any signal, the cable emits like an antenna fed by the voltage noise V_{n} occurring in the PCB.

The mechanisms of emission and the relative models will be described in detail in *Chapter 9* and throughout this book, starting from signal integrity considerations.

1.2.2 Radiated Emission Standards

There are three classes of radiated emission requirements that are imposed on digital systems:

1. Those mandatory for selling a product.
2. Those imposed by some organizations as proof of quality.
3. Those imposed by the product manufacturer.

The mandatory requirements cannot be avoided for the products to be marketed. An example is given by the European Community which obliges manufacturer to demonstrate the conformity of their products to the limits of emission imposed by the relevant standard. An example of the second type are the requirements imposed by Telcordia Technologies to the manufacturers of network telecommunications equipment [3], in which the emission limits that must be complied with are extended up to 10 GHz instead of the usual upper limit of 1 GHz. On the other hand, the emission requirements that manufacturers voluntarily impose on their products are intended to result in customer satisfaction. This section will be devoted to a brief illustration of requirements of the first type for commercial products. For more details regarding commercial and military standards, and the measurement sites and instrumentations, the reader is referred to Paul's textbook [4].

1.2.2.1 FCC and CISPR Standards

The most popular emission standards for commercial products are the FCC and CISPR standards. The *Federal Communications Commission* (FCC) published, under Part 15 of its Rules

and Regulations, a requirement that has had, and will continue to have, an impact for digital products to be marketed in the United States [5]. The FCC standard sets limits for the radiated and conducted emissions of a digital device which is defined as '*any unintentional radiator (device or system) that generates and uses timing pulses at a rate in excess of 9000 pulses (cycles) per seconds and uses digital techniques* ...'. Therefore, the range of frequency to be considered starts from 9 kHz. Any product that does not meet the limits imposed by this standard is illegal in the USA. The FCC classify digital device products into Class A and Class B. Class A devices are those that are marketed for use in a commercial, industrial, or business environment, while Class B are those that are marketed for use in a residential environment. The Class B limits are more stringent than those of Class A, as the susceptible devices are likely to be in closer proximity to the product seen as a source of emission. Another reason is that owners of sensitive devices do not have knowledge of how to protect their products from the interference of other products. Examples of Class B products are personal computers and their peripherals. Examples of Class A products are items of telecommunication equipment to be installed in telecommunication centers.

The FCC limits are presented in the remainder of this section, while the measurement procedures to verify compliance will be discussed in the following subsection. The frequency range considered by FCC for conducted emissions extends from 150 kHz to 30 MHz. The frequency range for radiated emissions begins at 30 MHz and extends up to 40 GHz. Radiated emissions concern the electric and magnetic fields radiated by a digital system that may be received by other electronic devices which would be victims of interference. The FCC, as well as other regulatory agencies such as the European Community, requires the radiated electric field to be measured in terms of field strength in dBμV/m (i.e. $20\log_{10}(E \times 10^6)$, with E in V/m). This enables very low and very high levels of electric fields to be plotted in the same graph. Compliance is verified by measuring the radiated electric fields from the product either in a *Semi-Anechoic Chamber* (SAC) or at an *Open Area Test Site* (OATS). The radiated emissions must be measured with the antenna in both vertical and horizontal polarizations with respect to the test site ground plane, and the product must be compliant for both the polarizations.

The upper frequencies of applicability for radiated emissions are given in Table 1.1 and are based on the highest frequency of use in the product. For example, for a personal computer having a clock frequency of 3.4 GHz, its radiated emissions will be measured up to 17 GHz.

Table 1.1 Upper limit of measurement frequency

Highest frequency generated or used in the system or on which the system operates or tunes (MHz)	Upper frequency of measurement range (MHz)
<1.705	30
1.705–108	1000
108–500	2000
500–1000	5000
>1000	5th harmonic of highest frequency or 40 GHz, whichever is lower

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Table 1.2 FCC radiated emission limits

Frequency (MHz)	Class A measured at 10 m (dBμV/m)	Class B measured at 3 m (dBμV/m)
30–88	39	40
88–216	43.5	43.5
216–960	46.4	46
>960	49.5	54
>1 GHz	49.5 (AV)	54 (AV)
	69.5 (PK)	74 (PK)

The limits of radiated emissions for both FCC Class A and B products are given in Table 1.2. Up to 960 MHz, the level refers to a quasi-peak detector in the measurement receiver. For measurements above 1 GHz, the limits are referred to an average (AV) or peak (PK) detector. The distances for radiated emission measurements are 3 m for Class B and 10 m for Class A products.

A common practical method for comparing the limits for Class A systems with those for Class B systems is to add about 10 dB to the Class A limits according to the assumption that the emissions fall off linearly with increasing distance of the measurement antenna. Thus, the emissions at 3 m are assumed to be reduced by a factor of 3/10 if the measurement distance is moved to a farther distance of 10 m, and vice versa, and therefore $20\log_{10}(10/3) = 10.46 \cong 10$ dB. According to this extrapolation, it can be observed in Table 1.2 that the Class A limits are some 10 dB less stringent than the Class B limits. This assumption of 10 dB is affected by two errors. The first error is that the emissions from antennas fall off inversely with distance only if the measurement points are in the farfield zone where there are no components of the fields along the direction of propagation, and the ratio between the orthogonal electric and magnetic fields is constant and equal to 377 Ω. An approximate criterion for evaluating the farfield boundary is $d = 3\lambda_{\mathrm{m}} = 3 \times 300/f_{\mathrm{MHz}}$, where d is the distance between the *Equipment Under Test* (EUT) and the antenna (in meters) [4]. Therefore, the near-to-farfield boundary at the lowest measurement frequency of 30 MHz is 30 m, but it is 90 cm at 1 GHz. The second error is the presence of a metallic reference plane in both possible test sites, SAC and OATS. This plane causes electromagnetic reflections that algebraically sum with the direct emissions. This will be discussed in *Section 11.3*. In conclusion, the comparison appears somewhat approximate.

The majority of the governmental emission requirements for markets outside the USA are based on the work carried out by the *International Special Committee on Radio Interference* (CISPR), which is a committee of the *International Electrotechnical Commission* (IEC). Although CISPR writes standards, they are not mandatory. However, most countries adopt the CISPR recommendations. The most widely used standard is CISPR 22 [6]. This sets limits for the radiated and conducted emissions of *Information Technology Equipment* (ITE), which basically includes digital systems as described for FCC. By analogy with FCC, limits are provided for Class A and Class B equipment. CISPR 22 has been adopted by the *European Economic Area* (EEA). This includes the members of the *European Union* (EU), which was formerly known as the *European Community* (EC) or the *European Economic Community* (EEC). The new European EMC Directive 2004/108/EC, published on 31 December 2004 (the former directive was 89/336/EEC) took effect on 20 July 2007 [7] and applies to members

P1: OTA/XYZ P2: ABC
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Table 1.3 CISPR 22 radiated emission limits for ITE equipment

Frequency (MHz)	Class A measured at 10 m (dBμV/m)	Class B measured at 10 m (dBμV/m)
30–230	40	30
230–1000	47	37

of the EEA. Although the directive refers to a large number of electromagnetic compatibility standards, the primary one is the European Norm EN 55022 [8] often mentioned in this book. This is essentially the CISPR 22 standard published by the IEC.

The radiated emission limits of CISPR 22 (EN 55022) are tabulated in Table 1.3 for both classes of ITE equipment. Note that, in this case, both Class A and Class B emissions refer to a distance of 10 m from the EUT. Moreover, similarly to FCC, the emissions are to be measured with a CISPR 16 receiver having a quasi-peak detector (QP) [4]. Whereas it is straightforward to compare FCC and CISPR emission limits for Class A equipment or systems, it is not as simple to perform comparisons for Class B, as the measurements for FCC compliance are to be carried out at a distance of 3 m, while a distance of 10 m is adopted in CISPR compliance. With the limitations discussed above in using the approximation of about 10 dB according to the inverse distance rule, the FCC limits at 3 m are scaled at -10.45 dB for comparison with CISPR limits, and the deviations between CISPR 22 and FCC limits are reported in Table 1.4. From this comparison it can be observed that CISPR 22 limits are slightly less restrictive up to 88 MHz, more restrictive in the range 88–230 MHz (up to 6.4 dB for Class A in the range 216–230 MHz), and again slightly less restrictive in the range 230–960 MHz. Above 960 MHz the CISPR 22 limits revert to being more restrictive.

CISPR standards are in continuous evolution. The basic standard for instruments and measurement procedures is CISPR 16, which is summarized in Table 1.5. For instance, CISPR-16-1-4 describes the test sites for measurement of radio disturbance field strength not only in the frequency range 30 MHz–1 GHz but also for the range 1 GHz–18 GHz. Alternative test sites such as reverberating chambers for total radiated power measurement are also considered. An example of evolution for products is CISPR 32 on multimedia equipment, which is still in preparation and will replace CISPR 13 (*Sound and television broadcast receiver and associated equipment – limits and method of measurement*) and the CISPR 22 [6] standards.

As this book is mainly focused on providing suitable models for signal integrity and radiated emission predictions, attention is directed towards the set of CISPR 16 documents that concern specifications for radio disturbance and immunity measuring apparatus, including the

Table 1.4 Deviation of CISPR 22 radiated emission limits from FCC radiated emission limits. To allow Class B comparison, a scale factor of -10.5 dBμV/m has been applied to the FCC limits of Table 1.2

Frequency (MHz)	Class A measured at 10 m (dBμV/m)	Class B measured at 10 m (dBμV/m)
30–88	−1	−0.5
88–216	+3.5	+3
216–230	+6.4	+5.5
230–960	−0.6	−1.5
960–1000	+2.5	+6.5

Table 1.5 Some CISPR publications

CISPR 16-1-1	Measuring apparatus
CISPR 16-1-2	Ancillary equipment – Conducted disturbances
CISPR 16-1-3	Ancillary equipment – Disturbance power
CISPR 16-1-4	Ancillary equipment – Radiated disturbances
CISPR 16-1-5	Antenna calibration test sites for 30 MHz to 1 GHz
CISPR 16-2-1	Conducted disturbance measurements
CISPR 16-2-2	Measurement of disturbance power
CISPR 16-2-3	Radiated disturbance measurements
CISPR 16-2-4	Immunity measurements
CISPR 16-3	CISPR technical reports
CISPR 16-4-1	Uncertainties in standardized EMC tests
CISPR 16-4-2	Measurement instrumentation uncertainty
CISPR 16-4-3	Statistical consideration in the determination of EMC compliance of mass-produced products
CISPR 16-4-4	Statistics of complaints and model for the calculation of limits

uncertainties associated with the measurement instrumentation and test site. This last item is very important in order to validate the models experimentally (this will be discussed in *Section 11.3*).

Modeling has recently become very important not only for designing but also for demonstrating conformity with essential requirements of the new European EMC Directive 2004/108/EC. *Essential requirements* means conformity to the emission and immunity limits for a specific product. One important novelty of the new directive is that the conformity can be demonstrated by technical documentation that includes the following information (see Annex IV – Technical documentation and EC declaration of conformity [7]):

> *'The technical documentation must enable the conformity of the apparatus with the essential requirements to be assessed. It must cover the design and manufacture of the apparatus, in particular:*
> – *a general description of the apparatus;*
> – *evidence of compliance with the harmonized standards, if any, applied full or in part;*
> – *where the manufacturer has not applied harmonized standards, or has applied in part, a description and explanation of the steps taken to meet the essential requirements of the Directive, including a description of the electromagnetic compatibility assessment set out in Annex II, point 1,* ***results of design calculation made****, examination carried out, test reports, etc.;*
> – *. . .'*

This means that, contrary to the previous EMC directive, it is no longer mandatory to carry out all the measurements required by the standards applicable to the product, but conformity can also be demonstrated, always referring to the standards, by calculations such as simulations performed with suitable and validated models.

1.2.2.2 Radiated Emission Set-Up for Verification of Compliance

FCC and CISPR 22 require that the radiated emission measurements for compliance should be carried out at an *Open Area Test Site* (OATS) or in a *Semi-Anechoic Chamber* (SAC). In

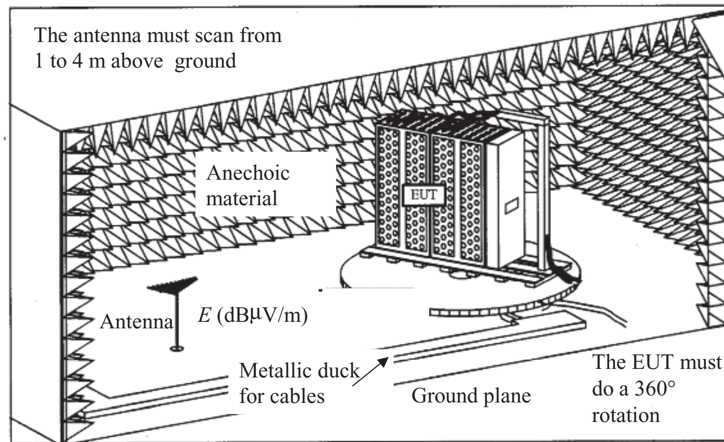

Figure 1.6 Set-up for radiated measurement in a semi-anechoic chamber

CISPR, alternative test sites such as reverberation chambers (CISPR 16-1-4) are also considered. While the OATS should be preferred, especially for FCC, SAC provides an all-weather measurement capability as well as security. An SAC consists of a shielded room lined with radio-frequency absorber material on the sides and at the top of the room to prevent reflections and simulate free space. A schematic representation is shown in Figure 1.6 where the *Equipment Under Test* (EUT) is a standing-floor system. The equipment is positioned on a turntable. The ongoing signal and power cables are to be arranged in order to maximize emissions. The radiated emissions must be measured with the measurement antenna in both horizontal and vertical polarizations with respect to the ground plane of the test site. The antenna must be elevated at a distance above the ground plane in the range 1–4 m, and the maximum emission must be recorded for each frequency. Portable products such as computers are to be placed 1 m above the floor of the chamber. The floor of the room constitutes a ground plane without an absorber, and this causes reflections that must be accounted for when performing simulations by models.

For an accurate measurement, the preferred antenna should be a tuned, half-wave dipole. A half-wave dipole is a linear antenna whose length is 0.5λ at the measuring frequency. If the frequency is changed, the dipole physical length must also be changed in order to maintain an electrical length of 0.5λ. Since this procedure is very time consuming, antennas having large bandwidth covering the whole range from 30 to 1000 MHz are used [4]. This fact must be taken into account when making comparisons with results obtained by simulations because some uncertainty should be associated with the measurements. This will be discussed in *Section 11.3*.

The main reason for choosing an SAC is to prevent external electromagnetic emission which could interfere with the measurements. An example is given in Figure 1.7, which shows the measured electric field from 30 MHz to 1000 MHz in an industrial area. It can be noted that the maximum measured electric field is due to radios and TV broadcast transmitters: they are much higher than the CISPR 22 limit for Class B equipment scaled at 3 m by the +10 dB factor, so that measurements with the EUT powered are unpredictable. In fact, as

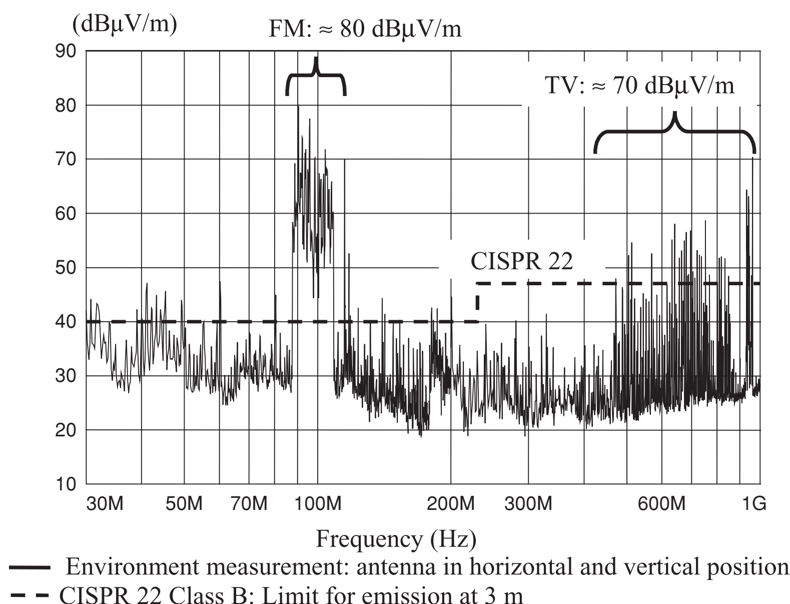

Figure 1.7 Radiated emission measurements of environment outside the semi-anechoic chamber in an industrial area. The CISPR 22 limit is indicated by the dashed line

will be shown later on, the emission profile of a typical digital system without fixes such as shielding is around 70 dBμV/m, that is, approximately of the same order of magnitude as the electromagnetic environment.

1.2.3 Radiated Emission from a Real System

As an example of a typical digital equipment emission profile, the radiated emission measured in the case of a switching telecommunication rack is shown in Figure 1.8. The system consists of several parts: a power voltage regulator (−48 V DC/logic power supply) located on a board, distributed microprocessors, memories, nets for telecommunication switching, and I/O devices for data transmission. The PCBs have several logic families with a maximum clock frequency of 155 MHz.

The equipment was designed to comply with the CISPR 22 Class A limits at 10 m. It was tested for precompliance verification in an SAC for 3 m measurements, taking CISPR 22 Class B as the design goal, with the *E*-field limit reported to 3 m by the scale factor of 10 dB, as previously discussed. Although design rules to minimize the levels of emission were applied, the equipment was too complex, and shielded racks and cables were required to meet the limits. In fact, with open doors and unclamped cables (which means that the shield of the cables is not connected to the metal frame of the rack), the emission profile is well above the limits of up to 25 dB and comparable with the *E*-fields present in the environment outside the semi-anechoic chamber. With closed doors and clamped cables (which means that the shield of the ongoing cables is well connected at 360° to the metallic frame of the rack),

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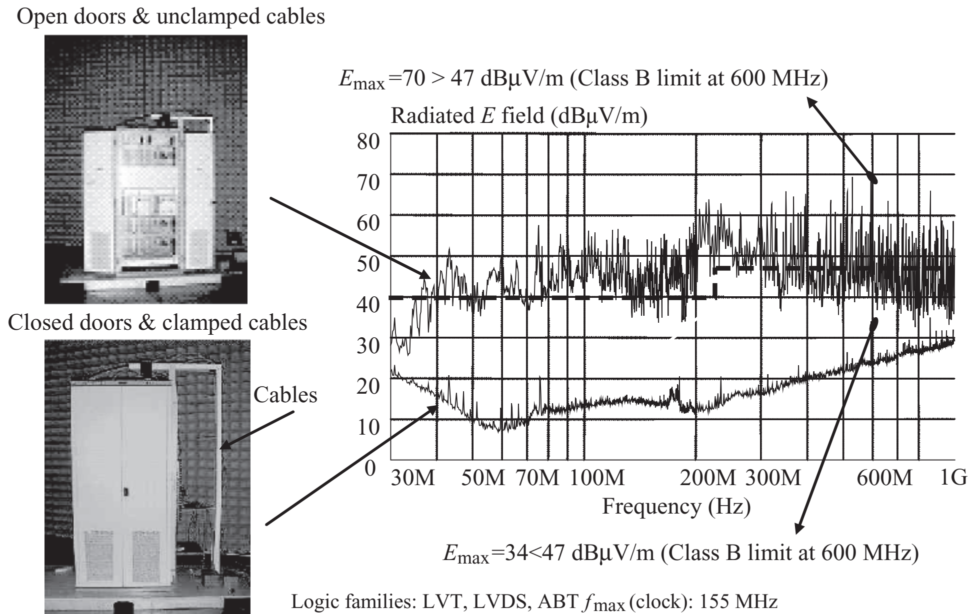

Figure 1.8 Radiated emission measurements at 3 m in a semi-anechoic chamber of switching equipment for telecommunication. The CISPR 22 limit is indicated by the dashed line

the emission profile is much less than the CISPR limit. A maximum measured field of 34 dBμV/m was measured, with 13 dB of margin with respect to the limit. From Figure 1.8 it can be noted that the emission profile has maximum values in the upper frequency range owing to the very fast switching time of the logic devices. Therefore, the apertures and the contacts of the cable shield with the metallic part of the rack must be designed with care. The numerous peaks of emission measured without shielding are due to the harmonics of the clocks and are present in the whole frequency range. Lower, random, continuous levels of emission are caused by data signaling. To meet the limit, as required by FCC and CISPR, it is necessary to check whether all the peaks are under the required level using a peak detector. If some peaks are above the limit, the measurement must be repeated using a quasi-peak detector in order to verify whether the peak is persistent. When this occurs, very often the emission is due to a harmonic of the clock, as will be discussed in *Section 9.1*. To achieve a trade-off between performance and cost of the shielding, it is very important to have design rules to mitigate emission from PCBs. One of the main tasks of this book is to outline methods and models to achieve this goal.

The emission profile of a complex system is not generally due to the sum of the contribution of many sources of emission, it could be mainly the result of one source only if this source has not been properly designed. In order to demonstrate this important issue, two simple experiments were performed with the same PCB consisting of two parallel wires of length $l = 20$ cm and diameter $d = 1$ mm, and separated by a distance $s = 2$ cm, as schematically shown in Figure 1.9a. An 8 MHz oscillator drove an inverter ACMOS device that, by an output resistance of 50 Ω, sent a periodic digital signal to a load of 100 Ω attached to the other end

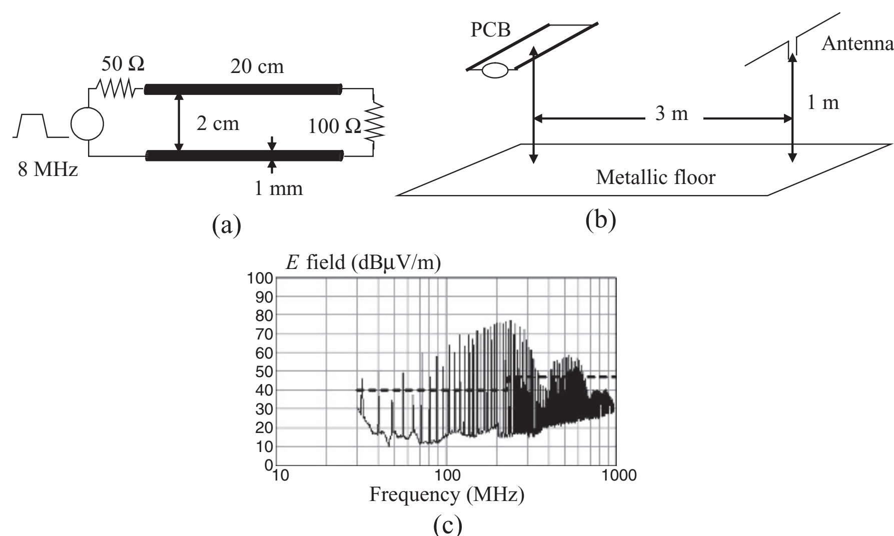

Figure 1.9 A simple experiment to demonstrate the difficulty in meeting the radiated emission limits: (a) schematic and dimensions of the tested device; (b) set-up for measurements; (c) measured radiated emission. The CISPR 22 limit is indicated by the dashed line

of the pair of wires. In order to measure the contribution of the wires only, the active device was placed within a small shielded box that also contained a voltage regulator driven by a 9 V battery. The power supply was very compact and had no connection to a commercial power system. The set-up for measurement is shown in Figure 1.9b, and the measured horizontal radiated emission is shown in Figure 1.9c. Observe that the horizontal emission exceeds the CISPR 22 Class B limit by as much as 30 dB, as in a complex system!

The second experiment was carried out with the same PCB within a shielded rack and with a cable attached to the return wire. The cable goes out by a small hole, as shown in Figure 1.10a. Without the cable, no emission was measured. With the cable, the emission rose to the levels shown in Figure 1.10b. Observe that, in this case also, the horizontal emissions exceed the CISPR 22 Class B limit by as much as 35 dB, and the peaks are mainly located in the low-frequency range, as previously found for a complex system with power and I/O signal cables. These two experiments will be considered in more detail in *Sections 9.2* and *9.6*. Moreover, the radiation mechanism will be investigated and models to predict the emission profiles will be provided.

1.3 Signaling and Logic Devices

In this subsection, the fundamental parameters concerning signaling with digital devices are defined. Digital devices belonging to different logic families will be presented in detail in *Chapter 2*. Anyway, they are all characterized by the following static parameters:

- V_{OHmin} – minimum output high (OH) voltage of the driver for a defined sourced current to ensure a high level;

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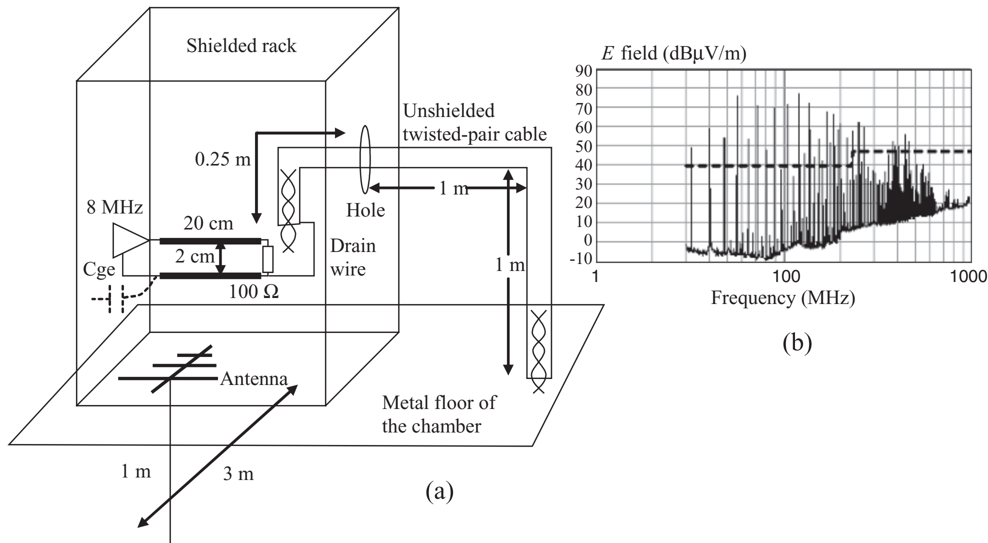

Figure 1.10 PCB with an attached cable: (a) schematic and set-up for measurements; (b) measured radiated emission with the antenna in the horizontal position. The CISPR 22 limit is indicated by the dashed line

- V_{IHmin} – minimum input high (IH) voltage of the receiver to recognize a high level;
- V_{th} – threshold switching voltage of the receiver;
- V_{ILmax} – maximum input low (IL) voltage of the receiver to recognize a low level;
- V_{OLmax} – maximum output low (OL) voltage of the driver for a defined sunk current to ensure a low level;
- $\text{NM}_{\text{Lmin}} = V_{\text{ILmax}} - V_{\text{OLmax}}$ – minimum noise margin (NM) at low level;
- $\text{NM}_{\text{Hmin}} = V_{\text{OHmin}} - V_{\text{IHmin}}$ – minimum noise margin (NM) at high level.

These parameters are guaranteed by the component manufacturer in order to ensure functionality of the device under defined conditions regarding power supply, temperature, and loading. The data sheet provides these parameters. Other parameters significant for *Signal Integrity* (SI) are:

- overshoot, undershoot, and plateau;
- noise immunity;
- set-up and hold time;
- data jitter and clock skew.

These parameters are defined and discussed in detail in the following.

1.3.1 Overshoot, Undershoot and Plateau

Overshoot and undershoot are positive and negative ringing with respect to the steady-state voltage levels. The plateau is a constant step voltage on the signal waveform that lasts twice the time delay T_{D} of the interconnect. Some examples are provided to clarify these definitions.

Consider the equivalent circuit of an interconnect with CMOS devices, as shown in Figure 1.11a. The driver and receiver devices are three inverter gates in cascade (see *Section 8.1* for more details). The driver is excited at its input by a voltage source of trapezoidal waveform with steady-state low and high levels of 0 and 5 V respectively, a rise and fall time $t_r = t_f = 0.2$ ns, and a period $T_p = 50$ ns with a duty cycle $D = 50$ % (where D is the portion of time during which the device is operated at a high level with respect to the period). At the output of the driver there is a series resistance $R_S = 30\ \Omega$ to mitigate reflections. The device and package capacitances are represented in the equivalent circuit by $C_{in} = 3$ pF and $C_{out} = 10$ pF. The receiver threshold $V_{th} = 2.4$ V. The interconnect is represented by a lossless *Transmission Line* (TL) of characteristic impedance $Z_0 = 60\ \Omega$ and time delay $T_D = 2$ ns. This last value corresponds approximately to a microstrip trace of length $l = 30$ cm. The simulated voltage waveforms at the points $D1_{out}$ (driver output after R_S) and $R2_{in}$ (receiver input) are shown in Figure 1.11b, where the overshoot and undershoot due to mismatching at both ends of the line can be observed. For a logic high level, the oscillations should be above the guaranteed V_{OHmin} voltage level with specified load and converge rapidly to the associated steady-state value. If this happens, the noise margin $NM_{Hmin} = V_{OHmin}–V_{IHmin}$ is preserved, as V_{IHmin} is the specified minimum voltage level for the receiver to recognize a logic high level. The same considerations hold for the logic low level, where the noise margin to preserve is

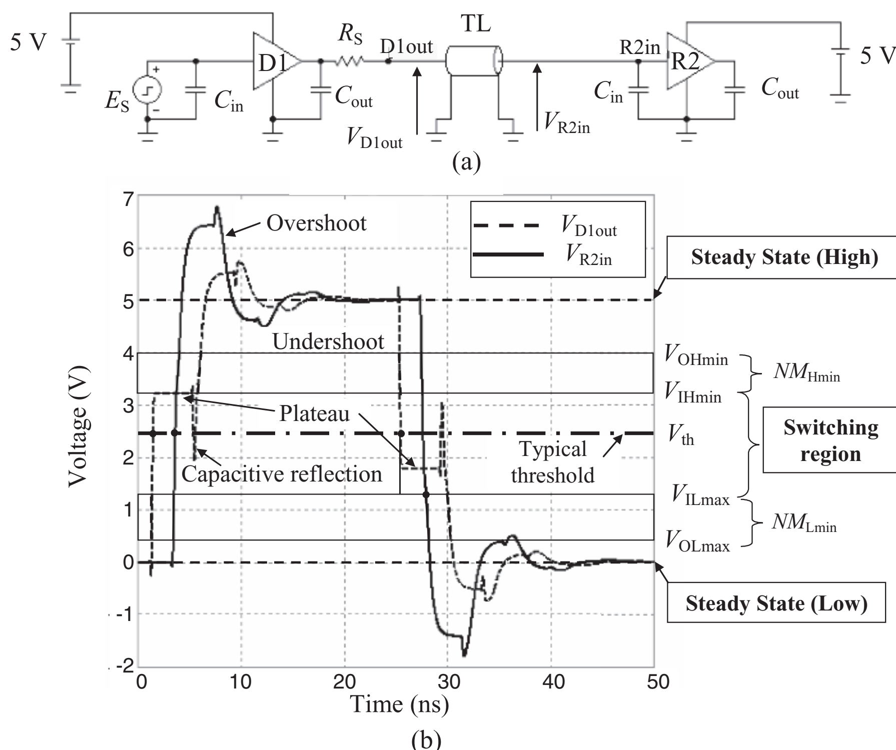

Figure 1.11 Interconnect with CMOS devices with series termination R_S: (a) equivalent circuit; (b) simulated waveforms with definitions of fundamental signaling parameters

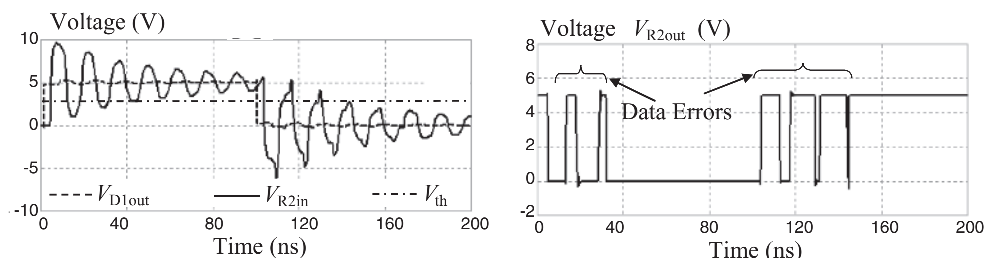

Figure 1.12 Interconnect with CMOS devices without series termination: simulated waveforms in line and data errors at the receiver

$NM_{Lmin} = V_{ILmax}–V_{OLmax}$. The values of these parameters for some popular logic families will be given in *Section 2.1*.

A very important signal distortion to consider is the plateau that can occur when the driver does not provide sufficient current to drive lines with low Z_0. This plateau lasts twice the line delay time and, if it stays in the region $V_{IHmin}–V_{ILmax}$, can cause data error. This concept will be clarified by the following examples.

Figure 1.12 shows what happens when the series resistance termination R_S is omitted. The overshoots and undershoots are so high that several data errors occur at the receiver output, as the oscillations cross the voltage threshold $V_{th} = 2.4$ V several times. For this example and the others that follow, the line has a delay time $T_D = 3$ ns, corresponding to a trace length $l =$ 50 cm.

In many cases, especially for CMOS devices, two clamping diodes are used to mitigate reflections, as shown in Figure 1.13a: one is connected between the receiver input and the ground, the other between the receiver input and the power supply. The simulated waveforms

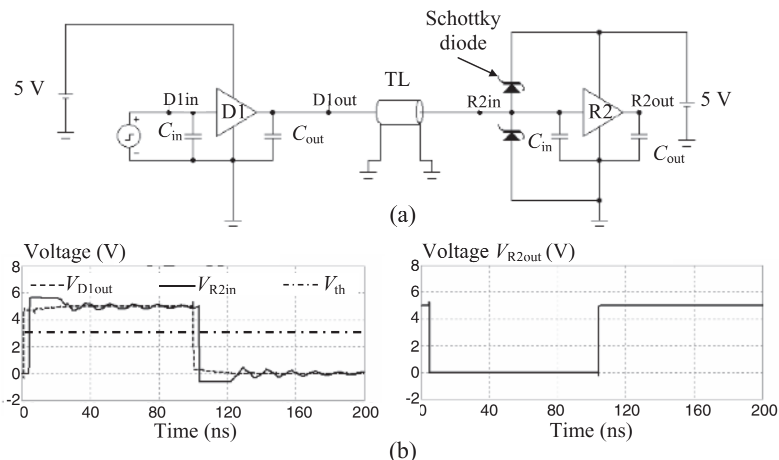

Figure 1.13 Interconnect with CMOS devices with clamping diodes: (a) equivalent circuit; (b) simulated waveforms in line and at the receiver

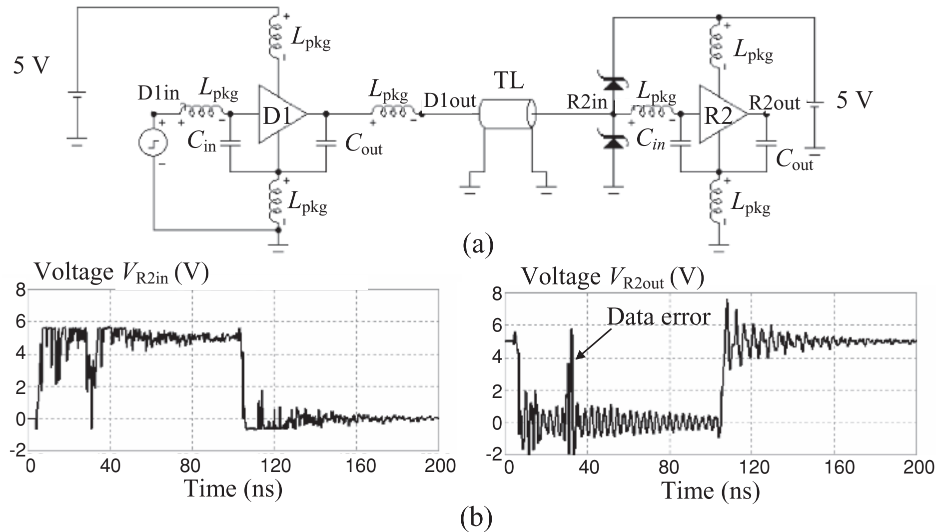

Figure 1.14 Interconnect with CMOS devices where parasitic package effects are considered: (a) equivalent circuit; (b) simulated waveforms in line and data error at the receiver

are shown in Figure 1.13b. In this case, errors do not occur, as the overshoot and the undershoot are far away from the threshold voltage $V_{\text{th}} = 2.4$ V.

A high-speed circuit is defined as 'a circuit for which the parasitic elements (resistance, inductance, and capacitance) of the PCB and its components play a significant role in performance'. The following classification is also used:

- low speed: frequency <10 MHz, edge rates >5 ns;
- high speed: frequency >10 MHz, edge rates <5 ns.

To see the importance of parasitic elements in SI performance, simulation of the structure with clamping diodes was repeated, introducing the inductance L_{pkg} associated with the package of each pin of the device, as shown in Figure 1.14a. It was verified that, with increase in the parasitic inductances to a value of 13 nH, data failure occurs. These device inductances must be minimized to avoid data errors.

Last but not least, to see the plateau effect on the line delay, consider the interconnect structure shown in Figure 1.15a, where a second receiver was added just after the series resistance $R_{\text{S}} = 30\ \Omega$. Since the sending waveform depends on the characteristic impedance Z_0, the simulations were repeated, adopting different values of Z_0 in the range 30–60 Ω with a step of 10 Ω in order to assess its effect. The simulated waveforms in line and at receiver output R1 are shown in Figure 1.15b. Note that for lower Z_0 an extra delay occurs for the data owing to the plateau effect. This does not occur at the input of receiver R2 because the arriving signal step doubles. Of course, if receiver R1 is positioned before the series resistance, just at the output of the driver, the extra delay does not occur because there is no partitioning

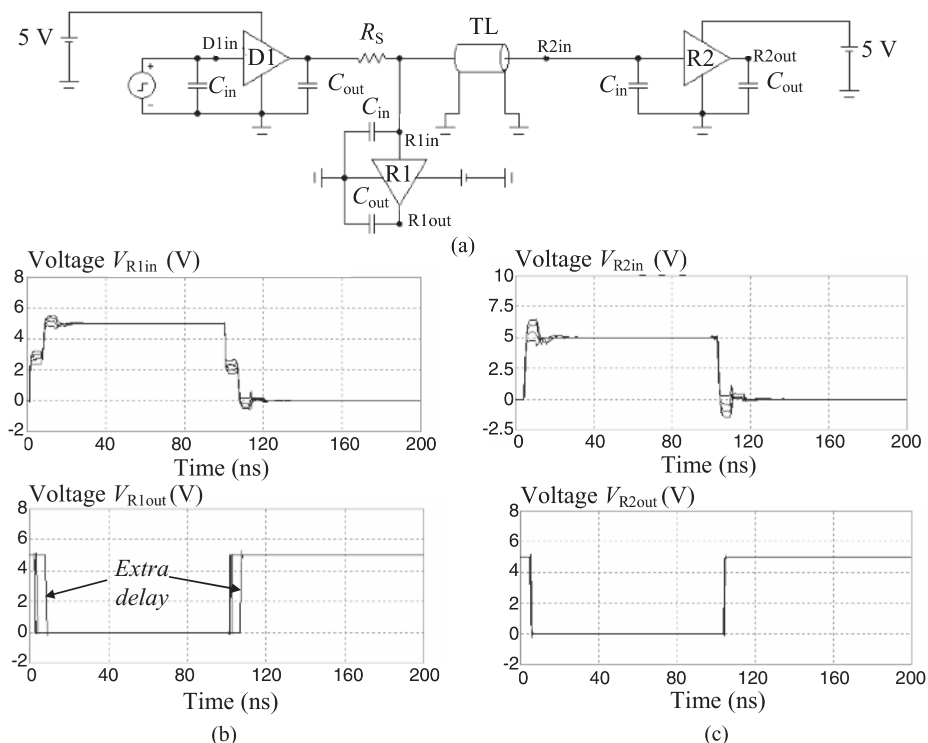

Figure 1.15 Interconnect with CMOS devices with a second receiver located at the driver end: (a) equivalent circuit; (b) simulated waveforms in line and extra delay at receiver R1 for variable Z_0; (c) simulated waveforms in line and correct data at receiver R2. Z_0 varies from 30 to 60 Ω with a step of 10 Ω

effect between the series resistance and the line characteristic impedance. Recall that, when a high-speed digital device switches, it sees at its output the characteristic impedance of the line and not the receiver located at the interconnect end. In *Chapter 5*, methods for coping with reflection problems will be provided.

1.3.2 Noise Immunity

Any signal applied to a receiver must have sufficient width t_w and amplitude V_p to be recognized from the receiver. It is possible to distinguish a '*static noise immunity*' when the receiver recognizes the input signal from its level only, regardless of the time width t_w. Generally, when the width of the spike t_w is smaller than the delay of the receiving device, the capability of the receiver to recognize the input signal depends on its width and level. In particular, the ability of a receiver to ignore very narrow signals (i.e. spikes) is called '*receiver dynamic noise immunity*' [9]. In general, very narrow pulses require more amplitude to trip the receiver, and faster logic families are more sensitive to a given spike than slower families are.

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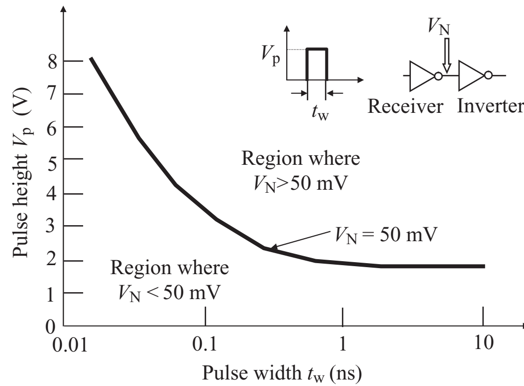

Figure 1.16 Example of dynamic noise immunity, showing the dependence of the dynamic immunity noise, defined as $V_N < 50$ mV, on pulse width t_w and height V_p

To avoid unwanted switching, the noise V_N passing through a receiver could be required not to exceed some value such as 50 mV. A simple example is shown in Figure 1.16 [9] for a 3.3 V inverter-based receiver with feedback. In the region of static noise immunity defined for t_w >1 ns, the maximum pulse height $V_p = 1.65$ V ensures a noise level within the fixed 50 mV. When the width of the spike t_w is less than 0.1 ns, a pulse height V_p of more than the supply voltage 3.3 V is required to cause $V_N > 50$ mV.

1.3.3 Timing Parameters

The reflection effects and other interferences such as crosstalk and ΔI-*noise* can affect the following timing parameters essential for defining the performance of a digital system in terms of speed.

Timing parameters are defined according to the common-clock timing scheme shown in Figure 1.17, where a single clock is distributed to a driver and to a receiver by traces having

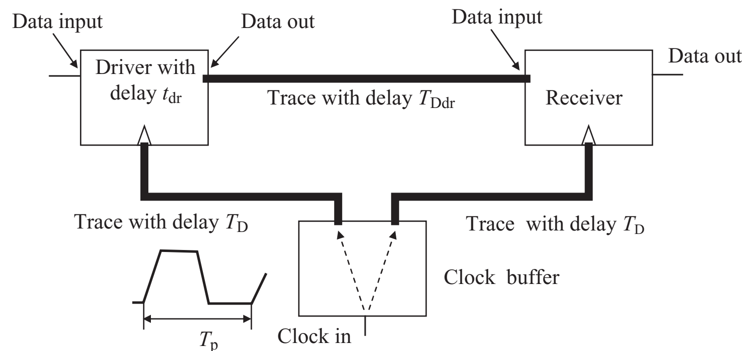

Figure 1.17 Block diagram of a common-clock bus

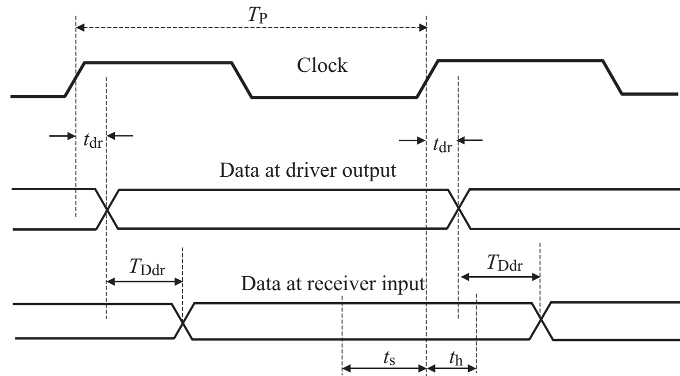

Figure 1.18 Timing diagram of a common-clock bus

the same delay time T_D [10]. The driver sends bits of data to the receiver by a trace of delay time T_{Ddr}. A complete data transfer requires two clock pulses, one to latch the data into the driver flip-flop and one to latch the data into the receiving flip-flop. Data transfer takes place in the following sequence:

1. Data are provided by the circuit core to the input of the flip-flop driver.
2. The clock to the driver is provided by the clock buffer through a trace of delay time T_D, and data transfer from the driver input to its output occurs with delay t_{dr}.
3. The bit propagates down the trace with a delay time T_{Ddr} and is latched by the clock edge coming from the clock buffer to the receiver by a trace of delay time T_D.

This process is shown as a timing diagram in Figure 1.18, where:

- The set-up time t_s is the time for which the input waveform at the receiver is settled, in other words, the bit must meet the input voltage specifications previously defined as static parameters before the clock edge acts on the receiver.
- The hold time t_h is the time after the clock edge during which the waveform must still meet input voltage specifications previously defined as static parameters.

Assuming that the data are sampled on the rising clock edge, it must be true that

$$T_p > t_{dr} + T_{Ddr} + t_s \tag{1.10}$$

Therefore, under the condition that $t_h < t_{dr} + T_{Ddr}$, the maximum clock rate is

$$f_{max} < 1/(t_{dr} + T_{Ddr} + t_s) \tag{1.11}$$

The timing diagram in Figure 1.18 implies that the clock and data edges fall at precise times. In a real system this does not occur, and many factors, such as reflection, crosstalk, and simultaneous switching noise, influence the times. The uncertainty in the arrival time

of a signal edge is the '*signal jitter*', while '*clock skew*' refers specifically to skew from all sources on the clock line in a synchronous system. Clock generators inherently produce some variation in the timing of clock edges at their output, and this variation is called '*clock jitter*'. In a system driven by a single clock generator, clock jitter is included in the timing budget as uncertainty in the clock period.

The maximum clock rate is given by

$$f_{\max} < 1/(t_{\mathrm{dr}} + T_{\mathrm{Ddr}} + t_{\mathrm{s}} + \Delta T_{\mathrm{Ddr}} + \Delta t_{\mathrm{clock}} + \Delta t_{\mathrm{jitter}} + \Delta t_{\mathrm{margin}}) \tag{1.12}$$

where ΔT_{Ddr} is the signal jitter, $\Delta t_{\mathrm{clock}}$ is the clock skew, $\Delta t_{\mathrm{jitter}}$ is the clock jitter, and $\Delta t_{\mathrm{margin}}$ is the margin chosen by the designer.

Eye diagram simulations can help in calculating the signal jitter precisely, as we will show in *Chapter 7* for lossy lines. Further consideration of digital timing analysis can be found in work by Hall *et al*. [10].

1.3.4 Eye Diagram

For a long stream of bits at high rate launched onto a lossy line, it could be difficult to tell if the signal meets the design specifications by monitoring the data waveforms. An example is shown in Figure 1.19, where the distortion on the edge of the signal is due to the losses in the line (see *Chapter 7* for details). To overcome this problem, the technique is to translate rise and fall waveforms of each bit in just one time window. Superposing all the bits builds an eye diagram [11]. A good plot results when the waveform is plotted for one clock period before and after the edge. In this case, the full data bit plus a half of the one before and a half of the one after are captured. In doing so, it is assumed that the data are sampled on the rising edge of the clock.

The eye diagram is a very useful method for accurate drawing of the timing diagram for determining the maximum clock frequency not only in the case of lossy lines but also for all types of signaling where reflection, crosstalk, and switching noise can cause jitter. The eye diagram gives an indication of the signal quality: the larger the eye opening, the better is the signal quality. The data sequence can be generated by a pseudorandom sequence generator, which is a digital shift register with feedback connected to produce a maximum length sequence. Ideally, the entire bit edge should cross the threshold voltage at the same time. On

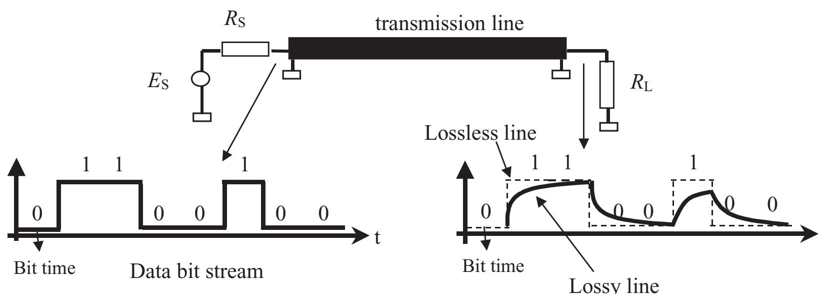

Figure 1.19 Data bit stream transmission with a lossy line

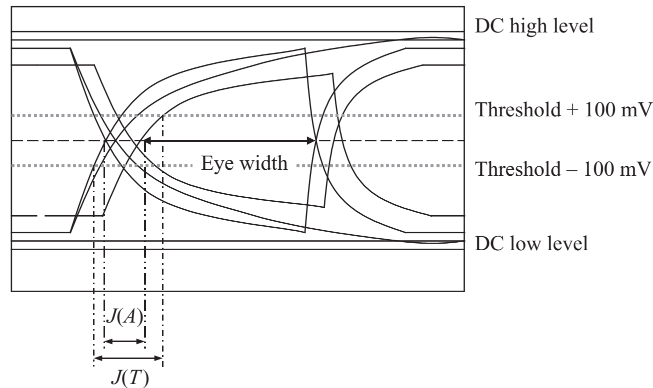

Figure 1.20 Fundamental parameters of an eye diagram

account of lossy lines, noises, and spread in threshold, this does not happen. The parameter that quantifies this fact is called 'signal jitter', whereas the vertical thickness of the line in the eye diagram is indicative of the AC voltage noise.

Figure 1.20 shows a typical eye diagram with differential signaling, where a '*zero crossing*' jitter $J(A)$ is defined together with a '*worst-case jitter*' $J(T)$. It is assumed, as an example, that the uncertainty of the threshold is between 100 mV and −100 mV.

An example of a measured eye diagram is given in Figure 1.21. A data stream at 311 Mb/s is injected onto an AWG28 twinax cable having LVPECL devices as the driver/receiver. Two measurements are shown: one with a cable length of 6 m and the other one with a cable

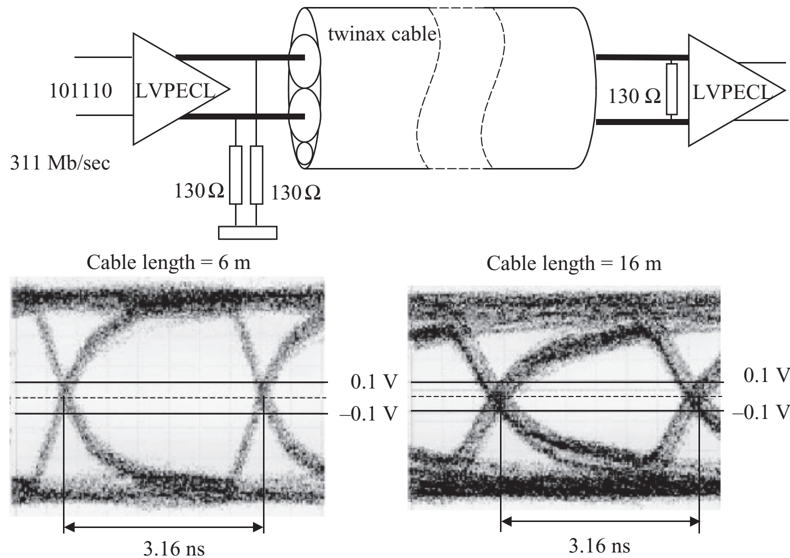

Figure 1.21 Example of eye diagram measurements with LVPECL devices and a twinax cable

length of 16 m. For the longer cable, the eye tends to close, as there are more losses in line. Another fact that determines eye closure is increase in the frequency of the data rate. Models for predicting the step response and eye diagrams directly in the time domain with lossy lines will be presented in *Section 7.2*.

1.4 Modeling Digital Systems

Modeling is very important for the design of complex digital systems. As mentioned in *Section 1.2*, it is also becoming a useful method for demonstrating conformity to the EMC standards, instead of measurements, as stated by the new EMC European Directive [7].

A digital system is usually very complex and consists of several components that need to be simulated to predict *Signal Integrity* (SI) and electromagnetic interference (EMI). An example is shown in Figure 1.22, where a multilayer PCB with its backplane is considered. Some components, such as bypass capacitors, sockets, package chips, vias, and connectors, can be modeled by lumped elements, such as resistances, inductances, and capacitances, as their maximum dimension is usually less than the minimum wavelength of interest. Other components, such as traces, cables attached to a PCB, and power and ground planes, have to be simulated by distributed models to take into account delays and points of resonance.

The available commercial tools that allow simulation can be classified depending on the models as:

- tools for mathematical model implementation;
- SPICE-like circuit simulators;
- full-wave numerical tools;
- professional simulators based on mixed formulations.

1.4.1 Mathematical Tools

Commercial mathematical tools such as *MathCad* and *MatLab* may be useful in computing reflection, crosstalk between parallel coupled lines, and radiated emission when the interconnect to be simulated is a simple point-to-point structure that consists of a driver modeled by

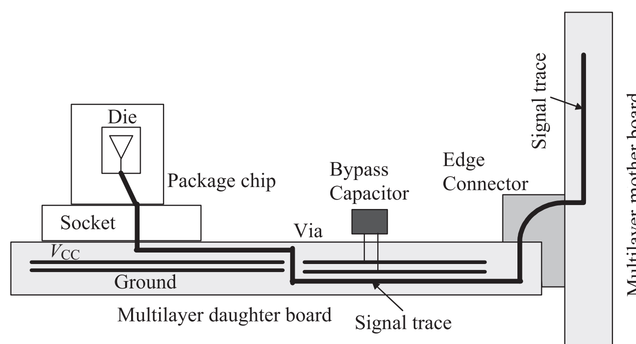

Figure 1.22 Example of parts of a digital system with components needing modeling

Table 1.6 Performances of mathematical codes

Advantages	Disadvantages
• Complex mathematical expressions for interference sources and propagation mechanisms. • Multiconductor lines analyzed as transmission lines with losses. • Fast time-domain analysis. • Matrix computation.	• Canonical structures that consist of a source, line, and load. • Simple sources and loads. • Linear load.

an equivalent Thévenin circuit and receivers represented by simple *RLC* nets. The line can be modeled by using the closed-form TL expression to compute currents and voltages along the line (see *Chapter 5*). For a frequency-domain (i.e. AC) computation as required in radiated emission problems, losses produced by skin, proximity, and dielectric effects can also be accounted for (see *Section 7.1*). Numerous examples concerning the computation of the radiated field at a certain distance from the source once the current distribution has been calculated will be provided in *Chapter 9*. When the simulation of a lossy line must be performed in the time domain, the convolution integrals based on known line scattering parameters can be numerically performed by exploiting the mathematical functions present in the code library, as will be shown in *Section 7.2*.

A powerful characteristic of these codes is the simplicity of managing matrix computation. An example of calculation of return current density in a 2D microstrip and stripline structures is provided in *Section 10.2*. Another important feature offered by matrix computation is that, applying node network theory, more topological complex circuits than point-to-point structure can be analyzed (see *Appendix E*). Some of the main advantages and disadvantages of analytical models are summarized in Table 1.6.

1.4.2 Spice-Like Circuit Simulators

For 2D problems, the best way to perform simulations in DC, AC, and the time domain is to use any circuit simulator based on SPICE. SPICE is an acronym for *Simulation Program with Integrated-Circuit Emphasis*. The original SPICE tool was developed to analyze complex electric circuits, in particular integrated circuits at diode and transistor level. It was developed in the early 1970s at the University of California at Berkeley, which is not the owner. The most widely available free-of-charge version is PSPICE SV, version 9.1, and MICROCAP Evaluation V.9 for Windows. To make the code more user friendly and to improve the performance, numerous software houses have developed and marketed SPICE-like circuit codes. Popular medium-cost commercial codes are PSPICE (*Cadence Design System*) and MicroCap (*Spectrum Software*). A more powerful and high-cost professional code is HSPICE (*Synopsys*). The most important feature of these commercial codes is the powerful component library of diodes, transistors, and *Integrated Circuits* (ICs). This library allows simulation of digital devices at transistor level, as often required when interference produced by the switching of the devices must be investigated (see the examples reported in *Chapter 8*). In particular, in *Section 8.2.3* and *Appendix C* it is shown that a multilayer PCB with ICs populated by decoupling capacitors can be simulated in the time domain to compute the noises between power

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Table 1.7 Performances of SPICE-like circuit simulators

Advantages	Disadvantages
• It is based on the description of the structure by circuit elements.	
• Complex topology easily simulated.	• 2D structures.
• Complex sources and loads described at transistor level.	• Limited use of mathematical expressions.
• Time-domain analysis with non-linear loads.	• No user matrix computation.
• Short computational time.	

and ground planes modeled as a grid of electrically short transmission lines for several situations of decoupling capacitors in terms of values and allocations. The circuit model considered also makes it possible to account for resonance effects of the PCB when excited at particular frequencies. Some of the main performances of the SPICE-like circuit models are reported in Table 1.7.

Unfortunately, the model library of low-cost SPICE codes does not include coupled lines or time-domain analysis of lines with frequency-dependent losses. The models available in the library are the lossless transmission-line model and the lossy-line model with DC resistance. Therefore, users are requested to implement their own models to perform signal integrity simulation for general cases with lossy and coupled interconnects. One of the main tasks of this book is to describe these types of circuit model. In *Chapter 6*, crosstalk models based on lumped and distributed line parameters for two and *n* coupled lines are outlined. In *Chapter 7*, new lossy-line models for analysis directly in the time domain with non-linear loads are presented.

SPICE is also useful for radiated emission problems. For example, in *Section 9.7* it is shown how to model unshielded and shielded cables driven by a differential digital device in order to calculate radiated fields for EMC compliance. In *Chapter 10* it is shown how to use SPICE to compute grounding noise produced by return signal currents for several structures of PCBs and connectors, applying the concept of partial inductance introduced and defined in *Section 3.2*.

The need for suitable modeling of digital devices with their non-linearity for an accurate and fast prediction of signal integrity is also discussed. The behavior models that are presented in *Chapter 2* and verified experimentally in *Chapter 6* are the basis of the IBIS models, a standard for the digital behavior device modeling described in *Section 2.4*. The SPICE-based commercial software used in this book is MicroCap [12], and all the models proposed are validated experimentally.

1.4.3 Full-Wave Numerical Tools

For 3D problems, the simulations should be performed by numerical codes based on the solutions of the Maxwell equations. For this reason, these numerical codes are also called *full-wave* tools. The main advantage offered by this type of programs is the possibility to simulate 3D objects considering their metallic and dielectric parts. The main disadvantage is that only simple sources (i.e. voltage and current sources) and simple loads composed of a simple

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RLC net are allowed. To overcome this limitation, some software houses are working for an integration of their 3D code with SPICE. There are a variety of *full-wave* electromagnetic modeling techniques. However, six techniques are typically used for EMI/EMC problems: the *Finite-Difference Time Domain* (FDTD) method, the *Finite Integration Technique* (FIT), the *Method of Moments* (MOM), the *Finite Element Method* (FEM), the *Partial Element Equivalent Circuit* (PEEC), and the *Transmission-Line Matrix* (TLM) [13, 14].

FDTD and FIT are volume-based solutions of time-domain Maxwell equations in differential and integral forms respectively. The entire volume, which consists of the object to be modeled and the surrounding, is represented by square and/or rectangular grids, the cell dimension of which is small compared with the shortest wavelength of interest. Commercial codes usually determine the grid automatically once the maximum frequency of interest is set. The broadband frequency response of the model is determined by performing a Fourier transform of the time-domain results at the specified monitor points. The boundary conditions of the volume-based solution (the edges of the grid) must be specially controlled to avoid reflection of the radiated field. The technique that allows this is called the *Absorbing Boundary Condition* (ABC). It usually provides an effective reflection of less than −60 dB. FDTD and FIT are not well suited for modelling wires or thin structures, as the number of grid cells increases dramatically.

MOM is a surface current technique. The metal objects to be modeled are converted into a series of plates and wires, or all wires electrically short. A set of linear equations is created to find the RF currents on each wire segment and surface patch. Once these currents are known, the *E*- and *H*-fields at any point in space can be determined by considering the radiation from each segment/patch and performing the vector summation. This makes the technique particularly suitable in solving problems with a long thin structure, such as cables attached to a PCB. The MOM is a frequency-domain solution technique, and therefore the simulation must be run for each frequency. As a digital signal with very fast edge times has a large spectrum, numerous frequencies must be computed. This is the main disadvantage of this technique, together with the fact that the dielectric substrate of a PCB is difficult to model. The first developed code based on MOM was the *Numerical Electromagnetic Code* (NEC) written in FORTRAN and available free of charge. Codes developed by software houses based on NEC and improved in graphic representation and computation techniques can be purchased [15].

FEM is another volume-based solution technique where the space is split into small elements usually having a triangular or tetrahedral shape. The field in each element is approximated by low-order polynomials with unknown coefficients. The Galerkin method is used to determine the coefficients. Once these coefficients are computed, the fields are known within each volume element. The computation is performed in the frequency domain, and results in the time domain are obtained by *Fast Fourier Transform* (FFT).

TLM and PEEC techniques are based on a representation of the volume (TLM) and surface (PEEC) elements used to decompose the computational domain by electrically short transmission lines and lumped-circuit elements, respectively, interfering with all the others.

Some of the main performances of the numerical models are summarized in Table 1.8.

The full-wave solution of several SI and RE problems by the software tool MWS based on FIT [16] and by NEC [15] will be presented in the following chapters.

MWS is used in *Section 6.5* for the analysis of SI. The crosstalk between two couple traces in a PCB is investigated considering a finite ground plane as the return for signal currents

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Table 1.8 Performances of numerical codes

Advantages	Disadvantages
• FDTD, FIT, FEM and TLM are based on the differential form of the Maxwell equations and consider a volume of calculation.	• Simple sources and loads.
• MOM and PEEC methods are based on the integral formulation of the Maxwell equations and consider a surface of calculation.	• Structure with shielded cables cannot be simulated straightforwardly.
• 3D structures with dielectric material and calculation of resonance points.	• Coupled field-to-circuit simulation for shielded cable.
• Scattering parameters.	• Time-consuming.
• Radiation pattern.	• High cost of the code in terms of computer time and memory storage.

with and without cuts. The results are compared with those obtained by using transmission-line theory, which assumes an infinite continuous ground plane.

One of the most important features of the *full-wave* code is the possibility of computing the scattering *S*-parameters in matrix form, which can be used to extract equivalent circuits for SPICE simulations. *Section 7.2* shows an example of *S*-parameter computation for an electrically short segment of twisted-pair cable by MWS. This type of structure is particularly interesting because the losses due to the proximity effect cannot be computed by closed-form expressions. Another important feature of numerical software tools is the possibility of computing the resonance frequencies in cavity structures such as a multilayer PCB populated by decoupling capacitors. An example of this application is provided in *Appendix C*.

Some examples of RE problems will be presented in *Chapter 9*. In particular, two examples of using numerical codes for radiated emission problems are provided. The first example concerns a cable that links two shielded boxes. It highlights the importance of considering both antenna polarizations regardless of whether the radiating cable is in the horizontal position (see *Section 9.7*). The second example concerns how to model a simple PCB, a wire above a finite ground plane, with an attached cable in order to compute radiation patterns (see *Section 9.9*). Comparisons between results at different frequencies obtained by NEC and MWS models are given as reciprocity validation.

The great advantage of a numerical code is the feature that makes it possible to compute radiated fields for more complex structures such as a PCB with cuts in the ground plane, equipped with EMI filters and inserted in a shielded box with an attached cable outgoing from an aperture. An example of this application is described in *Section 10.3*, where the numerical results for the basic structure of PCB, a wire above a ground plane with a long wire attached to the ground plane, are compared with those obtained by closed-form expressions implemented in a mathematical code.

When using numerical codes to compute *S*-parameters to extract equivalent circuits of electrically short discontinuities in a PCB, such as connectors or vias, it is very important to consider the small inductance associated with a discrete port used for excitation, which can introduce significant errors in performing the simulations. This aspect is investigated in detail in *Section 11.2*, comparing actual and ideal results of *S*-parameters computed in both the frequency and the time domain.

An important aspect of a numerical model is its validation by measurements. However, in going through this procedure, it is fundamental that the model reproduces exactly the set-up used for the test, and all metallic parts of the radiating object must be accounted for. Another important point to consider is that the measurements are affected by uncertainties. This is demonstrated in *Section 11.3*, where the radiated fields of a shielded rack with an outgoing cable are computed by NEC and MWS, and the results are compared with the measurements carried out in two different semi-anechoic shielded rooms used for EMC compliance. The last examples of using numerical codes for signal integrity are given in *Chapter 12*, where design rules for routing single-ended and differential traces in PCB are investigated.

1.4.4 Professional Simulators

At the end of this section, it is important to mention professional simulation tools where the integration of mathematical and numerical tools with a circuit simulator is realized in order to allow a designer to perform automatic simulations of PCBs from an industrial point of view.

The information provided in this book can be used as the background for a better understanding of the performance offered by these professional simulators which, for solving signal integrity and EMC problems, enable a partial or full simulation of a PCB, starting from its layout. These tools contain: 2D field solvers for extracting *RLGC* matrices of single/coupled transmission lines; a single/coupled lossy transmission line simulator; a 3D field solver for wirebonds, vias, and metal planes; and behavior modeling of drivers and receivers such as IBIS. They are also called upon to take physical layout files as input data and to post-process simulation results in the time domain (timing and waveform measurement) and the frequency domain (impedance parameter and *S*-parameters). For more information, the reader should visit the website of software houses such as Ansoft, CST, Applied Simulation Technology, Cadence, INCASES, Mentor Graphics, Sigrity, Quantic EMC, etc.

References

[1] Davidson, E., 'Electrical Design of a High Speed Computer Package', *IBM Journal of Research and Development*, **26**(3), May 1982, 349–361.
[2] Blood, W., '*MECL System Design Handbook*', 4th edition, Motorola Semiconductor Products, Inc., Phoenix, AZ, 1983.
[3] GR-1089-CORE, '*Electromagnetic Compatibility and Electrical Safety – Generic Criteria for Network Telecommunications Equipment*', Telcordia Technologies, Morristown, NJ, October 2002.
[4] Paul, C., '*Introduction to Electromagnetic Compatibility*', John Wiley & Sons, Inc., Hoboken, NJ, 2006.
[5] Code of Federal Regulations, Title 47 (47CFR), Part 15, Subpart B, '*Unintentional Radiators*'. Available online: www.hottconsultants.com, www.gpoaccess.gov/cfr/index.html, www.wireless.fcc.gov/rules.html.
[6] International Electrotechnical Commission, CISPR 22, '*Information Technology Equipment – Radio Disturbance Characteristics – Limits and Methods of Measurement*', 4th edition, 2003–2004. Available online: www.iec.ch.
[7] 2004/108/EC, European EMC Directive, 31-12-2004. Available online: http://europa.eu.int/comm/enterprise/electr_equipment/emc/.
[8] EN 55022:1988 (CISPR 22:1997) delayed, 1995 (CISPR 22:1993), '*Information Technology Equipment – Radio Disturbance Characteristics – Limits and Methods of Measurement*'. Available online: http://europa.eu.int/comm/enterprise/newapproach/standardization/harmstds/reflist/emc/ and http://www.cenelec.org.
[9] Young, B., '*Digital Signal Integrity: Modeling and Simulation with Interconnects and Packages*', Prentice Hall PTR, Upper Saddle River, NJ, 2001.

[10] Hall, S., Hall, G., and McCall, J., *'High-Speed Digital System Design – A Handbook of Interconnect Theory and Design Practice*', John Wiley & Sons, Inc., New York, NY, 2000.
[11] True, K.M., *'Long Transmission Lines and Data Signal Quality*', AN 808, National Semiconductor, March 1992. Available online: www.national.com.
[12] www.spectrum-software.com.
[13] Sadiku, M., *'Numerical Techniques in Electromagnetics*', CRC Press, Boca Raton, FL, 1992.
[14] Archambeault, B., Brench, C., and Ramahi, O., *'EMI/EMC Computational Modeling Handbook*', 2nd edition, Kluwer Academic Publishers, Norwell, MA, 2001.
[15] www.nittany-scientific.com.
[16] www.cst.com.