1 Passive Elements and Circuit Theory

The two-port equivalent circuits are widely used in radio frequency (RF) and microwave circuit design to describe the electrical behavior of both active devices and passive networks [1–4]. The two-port network impedance Z-parameters, admittance Y-parameters, or hybrid H-parameters are very important to characterize the nonlinear properties of the active devices, bipolar or field-effect transistors. The transmission $ABCD$-parameters of a two-port network are very convenient for designing the distributed circuits like transmission lines or cascaded elements. The scattering S-parameters are useful to characterize linear circuits, and are required to simplify the measurement procedure. Transmission lines are widely used in matching circuits in power amplifiers, in resonant circuits in the oscillators, filters, directional couplers, power combiners, and dividers. The design formulas and curves are presented for several types of transmission lines including stripline, microstrip line, slotline, and coplanar waveguide. Monolithic implementation of lumped inductors and capacitors is usually required at microwave frequencies and for portable devices. Knowledge of noise phenomena, such as the noise figure, additive white noise, low-frequency fluctuations, or flicker noise in active or passive elements, is very important for the oscillator modeling in particular and entire transmitter design in general.

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1.1 IMMITTANCE TWO-PORT NETWORK PARAMETERS

The basic diagram of a two-port nonautonomous transmission system can be represented by the equivalent circuit shown in Figure 1.1, where V_S is the independent voltage source, Z_S is the source impedance, LN is the linear time-invariant two-port network without independent source, and Z_L is the load impedance. The two independent phasor currents I_1 and I_2 (flowing across input and output terminals) and phasor voltages V_1 and V_2 characterize such a two-port network. For autonomous oscillator systems, in order to provide an appropriate analysis in the frequency domain of the two-port network in the negative one-port representation, it is sufficient to set the source impedance to infinity. For a power amplifier or oscillator design, the elements of the matching or resonant circuits, which are assumed to be linear or appropriately linearized, can be found among the LN-network elements, or additional two-port linear networks can be used to describe their frequency domain behavior.

For a two-port network, the following equations can be considered to be imposed boundary conditions:

$$V_1 + Z_S I_1 = V_S \tag{1.1}$$

$$V_2 + Z_L I_2 = V_L. \tag{1.2}$$

Suppose that it is possible to obtain a unique solution for the linear time-invariant circuit shown in Figure 1.1. Then the two linearly independent equations, which describe the general two-port network

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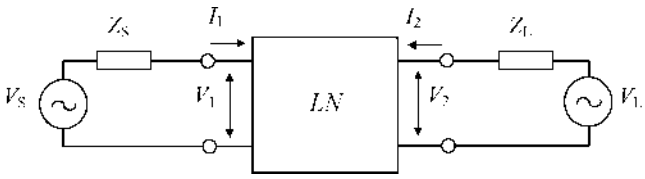

FIGURE 1.1 Basic diagram of two-port nonautonomous transmission system.

in terms of circuit variables V_1, V_2, I_1, and I_2, can be expressed in a matrix form as

$$[M][V] + [N][I] = 0 \tag{1.3}$$

or

$$\left.\begin{aligned} m_{11}V_1 + m_{12}V_2 + n_{11}I_1 + n_{12}I_2 = 0 \\ m_{21}V_1 + m_{22}V_2 + n_{21}I_1 + n_{22}I_2 = 0 \end{aligned}\right\}. \tag{1.4}$$

The complex 2×2 matrices $[M]$ and $[N]$ in Eq. (1.3) are independent of the source and load impedances Z_S and Z_L and voltages V_S and V_L, respectively, and they depend only on the circuit elements inside the *LN* network.

If matrix $[M]$ in Eq. (1.3) is nonsingular when $|M| \neq 0$, then this matrix equation can be rewritten in terms of $[I]$ as

$$[V] = -[M]^{-1}[N][I] = [Z][I] \tag{1.5}$$

where $[Z]$ is the open-circuit impedance two-port network matrix. In a scalar form, matrix Eq. (1.5) is given by

$$V_1 = Z_{11}I_1 + Z_{12}I_2 \tag{1.6}$$

$$V_2 = Z_{21}I_1 + Z_{22}I_2 \tag{1.7}$$

where Z_{11} and Z_{22} are the open-circuit driving-point impedances, and Z_{12} and Z_{21} are the open-circuit transfer impedances of the two-port network. The voltage components V_1 and V_2 due to the input current I_1 can be found by setting $I_2 = 0$ in Eqs. (1.6) and (1.7), resulting in an open-output terminal. Similarly, the same voltage components V_1 and V_2 are determined by setting $I_1 = 0$ when the input terminal becomes open-circuited. The resulting driving-point impedances can be written as

$$Z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} \qquad Z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0} \tag{1.8}$$

whereas the two transfer impedances are

$$Z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0} \qquad Z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0}. \tag{1.9}$$

Dual analysis can be used to derive the short-circuit admittance matrix when the current components I_1 and I_2 are considered as outputs caused by V_1 and V_2. If matrix $[N]$ in Eq. (1.3) is nonsingular

when $|N| \neq 0$, this matrix equation can be rewritten in terms of $[V]$ as

$$[I] = -[N]^{-1}[M][V] = [Y][V] \tag{1.10}$$

where $[Y]$ is the short-circuit admittance two-port network matrix. In a scalar form, matrix Eq. (1.10) is written as

$$I_1 = Y_{11}V_1 + Y_{12}V_2 \tag{1.11}$$

$$I_2 = Y_{21}V_1 + Y_{22}V_2 \tag{1.12}$$

where Y_{11} and Y_{22} are the short-circuit driving-point admittances, and Y_{12} and Y_{21} are the short-circuit transfer admittances of the two-port network. In this case, the current components I_1 and I_2 due to the input voltage source V_1 are determined by setting $V_2 = 0$ in Eqs. (1.11) and (1.12), thus creating a short output terminal. Similarly, the same current components I_1 and I_2 are determined by setting $V_1 = 0$ when input terminal becomes short-circuited. As a result, the two driving-point admittances are

$$Y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2=0} \qquad Y_{22} = \left.\frac{I_2}{V_2}\right|_{V_1=0} \tag{1.13}$$

whereas the two transfer admittances are

$$Y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2=0} \qquad Y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1=0}. \tag{1.14}$$

In some cases, an equivalent two-port network representation can be redefined in order to express the voltage source V_1 and output current I_2 in terms of the input current I_1 and output voltage V_2. If the submatrix

$$\begin{bmatrix} m_{11} & n_{12} \\ m_{21} & n_{22} \end{bmatrix}$$

given in Eq. (1.4) is nonsingular, then

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = -\begin{bmatrix} m_{11} & n_{12} \\ m_{21} & n_{22} \end{bmatrix}^{-1} \begin{bmatrix} n_{11} & m_{12} \\ n_{21} & m_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = [H] \begin{bmatrix} I_1 \\ V_2 \end{bmatrix} \tag{1.15}$$

where $[H]$ is the hybrid two-port network matrix. In a scalar form, it is best to represent matrix Eq. (1.15) as

$$V_1 = h_{11}I_1 + h_{12}V_2 \tag{1.16}$$

$$I_2 = h_{21}I_1 + h_{22}V_2 \tag{1.17}$$

where h_{11}, h_{12}, h_{21}, and h_{22} are the hybrid H-parameters. The voltage source V_1 and current component I_2 are determined by setting $V_2 = 0$ for the short output terminal in Eqs. (1.16) and (1.17) as

$$h_{11} = \left.\frac{V_1}{I_1}\right|_{V_2=0} \qquad h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0} \tag{1.18}$$

where h_{11} is the driving-point input impedance and h_{21} is the forward current transfer function. Similarly, the input voltage source V_1 and output current I_2 are determined by setting $I_1 = 0$ when

input terminal becomes open-circuited as

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0} \qquad h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0} \tag{1.19}$$

where h_{12} is the reverse voltage transfer function and h_{22} is the driving-point output admittance.

The transmission parameters, often used for passive device analysis, are determined for the independent input voltage source V_1 and input current I_1 in terms of the output voltage V_2 and output current I_2. In this case, if the submatrix

$$\begin{bmatrix} m_{11} & n_{11} \\ m_{21} & n_{21} \end{bmatrix}$$

given in Eq. (1.4) is nonsingular, we obtain

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = -\begin{bmatrix} m_{11} & n_{11} \\ m_{21} & n_{21} \end{bmatrix}^{-1} \begin{bmatrix} m_{12} & n_{12} \\ m_{22} & n_{22} \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} = [ABCD] \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{1.20}$$

where $[ABCD]$ is the forward transmission two-port network matrix. In a scalar form, we can write

$$V_1 = AV_2 - BI_2 \tag{1.21}$$

$$I_1 = CV_2 - DI_2 \tag{1.22}$$

where A, B, C, and D are the transmission parameters. The voltage source V_1 and current component I_1 are determined by setting $I_2 = 0$ for the open output terminal in Eqs. (1.21) and (1.22) as

$$A = \left.\frac{V_1}{V_2}\right|_{I_2=0} \qquad C = \left.\frac{I_1}{V_2}\right|_{I_2=0} \tag{1.23}$$

where A is the reverse voltage transfer function and C is the reverse transfer admittance. Similarly, the input independent variables V_1 and I_1 are determined by setting $V_2 = 0$ when the output terminal is short-circuited as

$$B = \left.\frac{V_1}{I_2}\right|_{V_2=0} \qquad D = \left.\frac{I_1}{I_2}\right|_{V_2=0} \tag{1.24}$$

where B is the reverse transfer impedance and D is the reverse current transfer function. The reason a minus sign is associated with I_2 in Eqs. (1.20) to (1.22) is that historically, for transmission networks, the input signal is considered as flowing to the input port whereas the output current flowing to the load. The direction of the current $-I_2$ entering the load is shown in Figure 1.2.

The parameters describing the same two-port network through different two-port matrices (impedance, admittance, hybrid, or transmission) can be cross-converted, and the elements of each

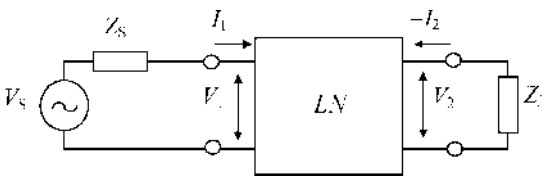

FIGURE 1.2 Basic diagram of loaded two-port transmission system.

TABLE 1.1 Relationships Between *Z*-, *Y*-, *H*- and *ABCD*-Parameters.

	$[Z]$	$[Y]$	$[H]$	$[ABCD]$
$[Z]$	$\begin{matrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{matrix}$	$\begin{matrix} \frac{Y_{22}}{\Delta Y} & -\frac{Y_{12}}{\Delta Y} \\ -\frac{Y_{21}}{\Delta Y} & \frac{Y_{11}}{\Delta Y} \end{matrix}$	$\begin{matrix} \frac{\Delta H}{h_{22}} & \frac{h_{12}}{h_{22}} \\ -\frac{h_{21}}{h_{22}} & \frac{1}{h_{22}} \end{matrix}$	$\begin{matrix} \frac{A}{C} & \frac{AD-BC}{C} \\ \frac{1}{C} & \frac{D}{C} \end{matrix}$
$[Y]$	$\begin{matrix} \frac{Z_{22}}{\Delta Z} & -\frac{Z_{12}}{\Delta Z} \\ -\frac{Z_{21}}{\Delta Z} & \frac{Z_{11}}{\Delta Z} \end{matrix}$	$\begin{matrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{matrix}$	$\begin{matrix} \frac{1}{h_{11}} & -\frac{h_{12}}{h_{11}} \\ \frac{h_{21}}{h_{11}} & \frac{\Delta H}{h_{11}} \end{matrix}$	$\begin{matrix} \frac{D}{B} & -\frac{AD-BC}{B} \\ -\frac{1}{B} & \frac{A}{B} \end{matrix}$
$[H]$	$\begin{matrix} \frac{\Delta Z}{Z_{22}} & \frac{Z_{12}}{Z_{22}} \\ -\frac{Z_{21}}{Z_{22}} & \frac{1}{Z_{22}} \end{matrix}$	$\begin{matrix} \frac{1}{Y_{11}} & -\frac{Y_{12}}{Y_{11}} \\ \frac{Y_{21}}{Y_{11}} & \frac{\Delta Y}{Y_{11}} \end{matrix}$	$\begin{matrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{matrix}$	$\begin{matrix} \frac{B}{D} & \frac{AD-BC}{D} \\ -\frac{1}{D} & \frac{C}{D} \end{matrix}$
$[ABCD]$	$\begin{matrix} \frac{Z_{11}}{Z_{21}} & \frac{\Delta Z}{Z_{21}} \\ \frac{1}{Z_{21}} & \frac{Z_{22}}{Z_{21}} \end{matrix}$	$\begin{matrix} -\frac{Y_{22}}{Y_{21}} & -\frac{1}{Y_{21}} \\ -\frac{\Delta Y}{Y_{21}} & -\frac{Y_{11}}{Y_{21}} \end{matrix}$	$\begin{matrix} -\frac{\Delta H}{h_{21}} & -\frac{h_{11}}{h_{21}} \\ -\frac{h_{22}}{h_{21}} & -\frac{1}{h_{21}} \end{matrix}$	$\begin{matrix} A & B \\ C & D \end{matrix}$

matrix can be expressed by the elements of other matrices. For example, Eqs. (1.11) and (1.12) for the Y-parameters can be easily solved for the independent input voltage source V_1 and input current I_1 as

$$V_1 = -\frac{Y_{22}}{Y_{21}}V_2 + \frac{1}{Y_{21}}I_2 \tag{1.25}$$

$$I_1 = -\frac{Y_{11}Y_{22} - Y_{12}Y_{21}}{Y_{21}}V_2 + \frac{Y_{11}}{Y_{21}}I_2. \tag{1.26}$$

By comparing the equivalent Eqs. (1.21) and (1.22) and Eqs. (1.25) and (1.26), the direct relationships between the elements of the transmission *ABCD*-matrix and admittance Y-matrix are written as

$$A = -\frac{Y_{22}}{Y_{21}} \quad B = -\frac{1}{Y_{21}} \tag{1.27}$$

$$C = -\frac{\Delta Y}{Y_{21}} \quad D = -\frac{Y_{11}}{Y_{21}} \tag{1.28}$$

where $\Delta Y = Y_{11}Y_{22} - Y_{12}Y_{21}$.

A summary of the relationships between the impedance Z-parameters, admittance Y-parameters, hybrid H-parameters, and transmission *ABCD*-parameters is shown in Table 1.1, where $\Delta Z = Z_{11}Z_{22} - Z_{12}Z_{21}$ and $\Delta H = h_{11}h_{22} - h_{12}h_{21}$.

1.2 SCATTERING PARAMETERS

The concept of incident and reflected voltage and current parameters can be illustrated by the one-port network shown in Figure 1.3, where the network impedance Z is connected to the signal source V_S

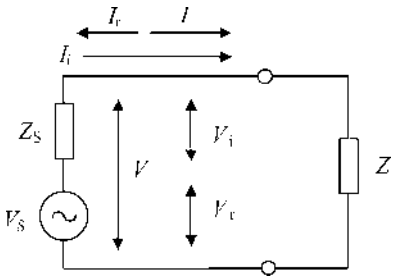

FIGURE 1.3 Incident and reflected voltages and currents.

with the internal impedance Z_S. In a common case, the terminal current I and voltage V consist of incident and reflected components (assume their root mean square [rms] values). When the load impedance Z is equal to the conjugate of source impedance expressed as $Z = Z_S^*$, the terminal current becomes the incident current. It is calculated from

$$I_i = \frac{V_S}{Z_S^* + Z_S} = \frac{V_S}{2\mathrm{Re}Z_S}. \tag{1.29}$$

The terminal voltage, defined as the incident voltage, can be determined from

$$V_i = \frac{Z_S^* V_S}{Z_S^* + Z_S} = \frac{Z_S^* V_S}{2\mathrm{Re}Z_S}. \tag{1.30}$$

Consequently, the incident power, which is equal to the maximum available power from the source, can be obtained by

$$P_i = \mathrm{Re}\left(V_i I_i^*\right) = \frac{|V_S|^2}{4\mathrm{Re}Z_S}. \tag{1.31}$$

The incident power can be presented in a normalized form using Eq. (1.30) as

$$P_i = \frac{|V_i|^2 \,\mathrm{Re}Z_S}{\left|Z_S^*\right|^2}. \tag{1.32}$$

This allows the normalized incident voltage wave a to be defined as the square root of the incident power P_i by

$$a = \sqrt{P_i} = \frac{V_i\sqrt{\mathrm{Re}Z_S}}{Z_S^*}. \tag{1.33}$$

Similarly, the normalized reflected voltage wave b, defined as the square root of the reflected power P_r, can be written as

$$b = \sqrt{P_r} = \frac{V_r\sqrt{\mathrm{Re}Z_S}}{Z_S}. \tag{1.34}$$

The incident power can be expressed by the incident current I_i and the reflected power can be expressed by the reflected current I_r, respectively, as

$$P_i = |I_i|^2 \operatorname{Re} Z_S \tag{1.35}$$

$$P_r = |I_r|^2 \operatorname{Re} Z_S. \tag{1.36}$$

As a result, the normalized incident voltage wave a and reflected voltage wave b can be given by

$$a = \sqrt{P_i} = I_i \sqrt{\operatorname{Re} Z_S} \tag{1.37}$$

$$b = \sqrt{P_r} = I_r \sqrt{\operatorname{Re} Z_S}. \tag{1.38}$$

The parameters a and b can also be called the *normalized incident* and *reflected current waves*, or simply *normalized incident* and *reflected waves*, respectively, since the normalized current waves and the normalized voltage waves represent the same parameters.

The voltage V and current I, related to the normalized incident and reflected waves a and b, can be written as

$$V = V_i + V_r = \frac{Z_S^*}{\sqrt{\operatorname{Re} Z_S}} a + \frac{Z_S}{\sqrt{\operatorname{Re} Z_S}} b \tag{1.39}$$

$$I = I_i - I_r = \frac{1}{\sqrt{\operatorname{Re} Z_S}} a - \frac{1}{1\sqrt{\operatorname{Re} Z_S}} b \tag{1.40}$$

where

$$a = \frac{V + Z_S I}{2\sqrt{\operatorname{Re} Z_S}} \quad b = \frac{V - Z_S^* I}{2\sqrt{\operatorname{Re} Z_S}}. \tag{1.41}$$

The source impedance Z_S is often purely real and, therefore, is used as the normalized impedance. In microwave design technique, the characteristic impedance of the passive two-port networks, including transmission lines and connectors, is considered as real and equal to 50 Ω. This is very important for measuring S-parameters when all transmission lines, source, and load should have the same real impedance. For $Z_S = Z_S^* = Z_0$, where Z_0 is the characteristic impedance, the ratio of the normalized reflected wave and the normalized incident wave for a one-port network is called the *reflection coefficient* Γ, defined as

$$\Gamma = \frac{b}{a} = \frac{V - Z_S^* I}{V + Z_S I} = \frac{V - Z_S I}{V + Z_S I} = \frac{Z - Z_S}{Z + Z_S} \tag{1.42}$$

where $Z = V/I$.

For a two-port network shown in Figure 1.4, the normalized reflected waves b_1 and b_2 can also be represented by the normalized incident waves a_1 and a_2, respectively, as

$$b_1 = S_{11} a_1 + S_{12} a_2 \tag{1.43}$$

$$b_2 = S_{21} a_1 + S_{22} a_2 \tag{1.44}$$

or, in a matrix form,

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{11} \\ S_{21} & S_{21} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{1.45}$$

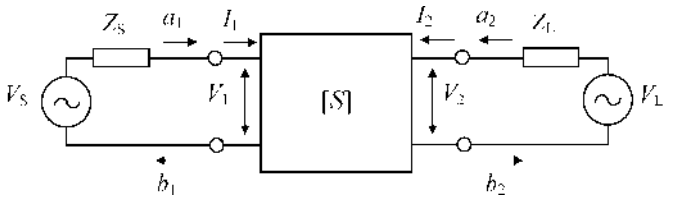

FIGURE 1.4 Basic diagram of *S*-parameter two-port network.

where the incident waves a_1 and a_2 and the reflected waves b_1 and b_2, for complex source and load impedances Z_S and Z_L, are given by

$$a_1 = \frac{V_1 + Z_S I_1}{2\sqrt{\text{Re}Z_S}} \quad a_2 = \frac{V_2 + Z_L I_2}{2\sqrt{\text{Re}Z_L}} \tag{1.46}$$

$$b_1 = \frac{V_1 - Z_S^* I_1}{2\sqrt{\text{Re}Z_S}} \quad b_2 = \frac{V_2 - Z_L^* I_2}{2\sqrt{\text{Re}Z_L}} \tag{1.47}$$

where S_{11}, S_{12}, S_{21}, and S_{22} are the *S*-parameters of the two-port network.

From Eq. (1.45) it follows that if $a_2 = 0$, then

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \quad S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \tag{1.48}$$

where S_{11} is the reflection coefficient and S_{21} is the transmission coefficient for ideal matching conditions at the output terminal when there is no incident power reflected from the load. Similarly,

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \quad S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{1.49}$$

where S_{12} is the transmission coefficient and S_{22} is the reflection coefficient for ideal matching conditions at the input terminal.

To convert *S*-parameters to the admittance *Y*-parameters, it is convenient to represent Eqs. (1.46) and (1.47) as

$$I_1 = (a_1 - b_1)\frac{1}{\sqrt{Z_0}} \quad I_2 = (a_2 - b_2)\frac{1}{\sqrt{Z_0}} \tag{1.50}$$

$$V_1 = (a_1 + b_1)\sqrt{Z_0} \quad V_1 = (a_2 + b_2)\sqrt{Z_0} \tag{1.51}$$

where it is assumed that the source and load impedances are real and equal to $Z_S = Z_L = Z_0$.

Substituting Eqs. (1.50) and (1.51) to Eqs. (1.11) and (1.12) results in

$$\frac{a_1 - b_1}{\sqrt{Z_0}} = Y_{11}(a_1 + b_1)\sqrt{Z_0} + Y_{12}(a_2 + b_2)\sqrt{Z_0} \tag{1.52}$$

$$\frac{a_2 - b_2}{\sqrt{Z_0}} = Y_{21}(a_1 + b_1)\sqrt{Z_0} + Y_{22}(a_2 + b_2)\sqrt{Z_0} \tag{1.53}$$

which can then be respectively converted to

$$-b_1(1+Y_{11}Z_0)-b_2Y_{12}Z_0=-a_1(1-Y_{11}Z_0)+a_2Y_{12}Z_0 \tag{1.54}$$

$$-b_1Y_{21}Z_0-b_2(1+Y_{22}Z_0)=a_1Y_{21}Z_0-a_2(1-Y_{22}Z_0)\,. \tag{1.55}$$

Eqs. (1.54) and (1.55) can be easily solved for the reflected waves b_1 and b_2 as

$$b_1\left[(1+Y_{11}Z_0)(1+Y_{22}Z_0)-Y_{12}Y_{21}Z_0^2\right]=a_1\left[(1-Y_{11}Z_0)(1+Y_{22}Z_0)+Y_{12}Y_{21}Z_0^2\right]-2a_2Y_{12}Z_0 \tag{1.56}$$

$$b_2\left[(1+Y_{11}Z_0)(1+Y_{22}Z_0)-Y_{12}Y_{21}Z_0^2\right]=-2a_1Y_{21}Z_0+a_2\left[(1+Y_{11}Z_0)(1-Y_{22}Z_0)+Y_{12}Y_{21}Z_0^2\right] \tag{1.57}$$

Comparing equivalent Eqs. (1.43) and (1.44) and Eqs. (1.56) and (1.57) gives the following relationships between the scattering S-parameters and admittance Y-parameters:

$$S_{11}=\frac{(1-Y_{11}Z_0)(1+Y_{22}Z_0)+Y_{12}Y_{21}Z_0^2}{(1+Y_{11}Z_0)(1+Y_{22}Z_0)-Y_{12}Y_{21}Z_0^2} \tag{1.58}$$

$$S_{12}=\frac{-2Y_{12}Z_0}{(1+Y_{11}Z_0)(1+Y_{22}Z_0)-Y_{12}Y_{21}Z_0^2} \tag{1.59}$$

$$S_{21}=\frac{-2Y_{21}Z_0}{(1+Y_{11}Z_0)(1+Y_{22}Z_0)-Y_{12}Y_{21}Z_0^2} \tag{1.60}$$

$$S_{22}=\frac{(1+Y_{11}Z_0)(1-Y_{22}Z_0)+Y_{12}Y_{21}Z_0^2}{(1+Y_{11}Z_0)(1+Y_{22}Z_0)-Y_{12}Y_{21}Z_0^2}. \tag{1.61}$$

Similarly, the relationships of S-parameters with Z-, H-, and $ABCD$-parameters can be obtained for the simplified case when the source impedance Z_S and the load impedance Z_L are equal to the characteristic impedance Z_0 [5].

1.3 INTERCONNECTIONS OF TWO-PORT NETWORKS

When analyzing the behavior of a particular electrical circuit in terms of the two-port network parameters, it is often necessary to define the parameters of a combination of the two or more internal two-port networks. For example, the general feedback amplifier circuit consists of an active two-port network representing the amplifier stage, which is connected in parallel with a passive feedback two-port network. In general, the two-port networks can be interconnected using parallel, series, series–parallel, or cascade connections.

To characterize the resulting two-port networks, it is necessary to take into account which currents and voltages are common for individual two-port networks. The most convenient set of parameters is one for which the common currents and voltages represent a simple linear combination of the independent variables. For the interconnection shown in Figure 1.5(a), the two-port networks Z_a and Z_b are connected in series for both the input and output terminals. Therefore, the currents flowing through these terminals are equal when

$$I_1=I_{1a}=I_{1b}\quad I_2=I_{2a}=I_{2b} \tag{1.62}$$

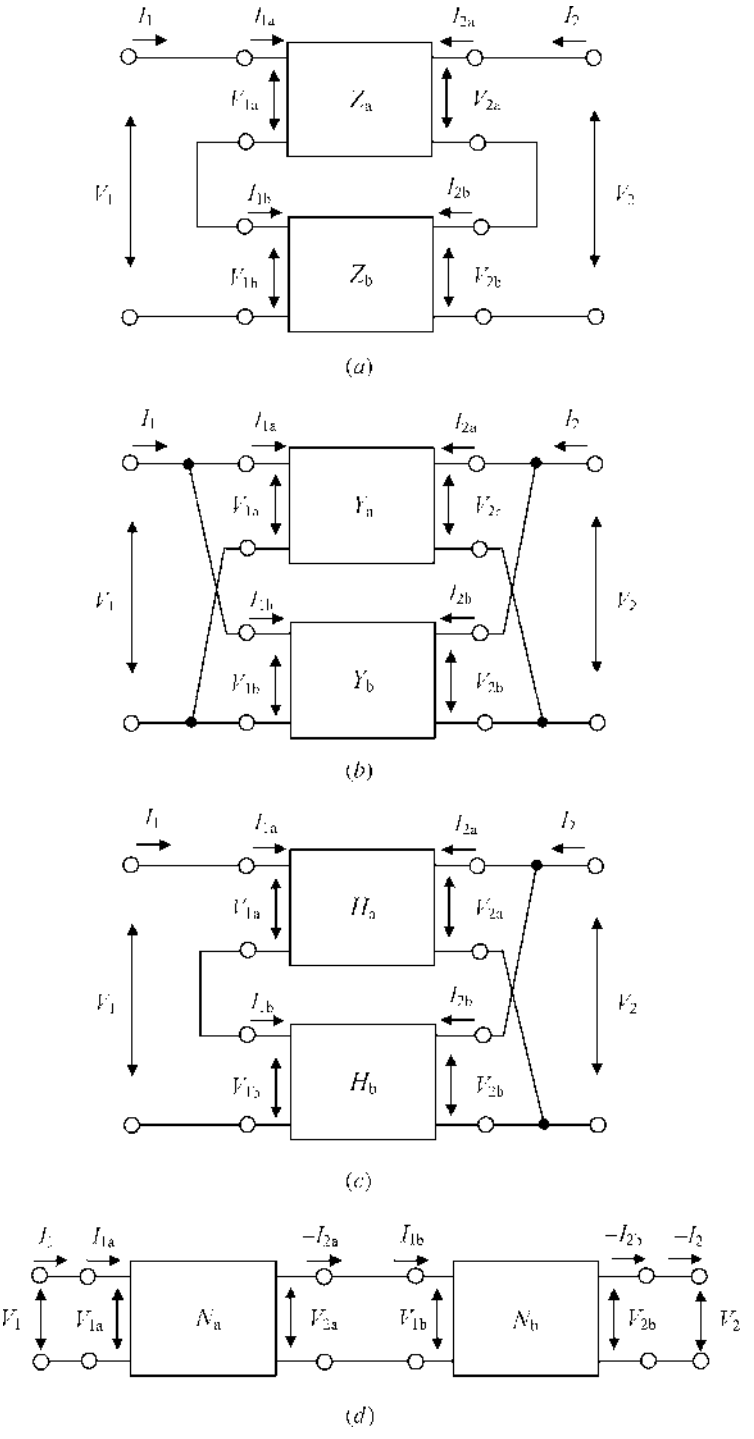

FIGURE 1.5 Different interconnections of two-port networks.

or, in a matrix form,

$$[I] = [I_a] = [I_b]\,. \tag{1.63}$$

The terminal voltages of the resulting two-port network represent the corresponding sums of the terminal voltages of the individual two-port networks when

$$V_1 = V_{1a} + V_{1b} \quad V_2 = V_{2a} + V_{2b} \tag{1.64}$$

or, in a matrix form,

$$[V] = [V_a] + [V_b]\,. \tag{1.65}$$

The currents are common components, both for the resulting and individual two-port networks. Consequently, to describe the properties of such a circuit, it is most convenient to use the impedance matrices. For each two-port network Z_a and Z_b, we can write using Eq. (1.62), respectively,

$$[V_a] = [Z_a]\,[I_a] = [Z_a]\,[I] \tag{1.66}$$

$$[V_b] = [Z_b]\,[I_b] = [Z_b]\,[I]\,. \tag{1.67}$$

Adding both sides of Eqs. (1.66) and (1.67) yields

$$[V] = [Z]\,[I] \tag{1.68}$$

where

$$[Z] = [Z_a] + [Z_b] = \begin{bmatrix} Z_{11a} + Z_{11b} & Z_{12a} + Z_{12b} \\ Z_{21a} + Z_{21b} & Z_{22a} + Z_{22b} \end{bmatrix}. \tag{1.69}$$

The circuit shown in Figure 1.5(*b*) is composed of the two-port networks Y_a and Y_b connected in parallel, where the common components for both resulting and individual two-port networks are input and output voltages, respectively,

$$V_1 = V_{1a} = V_{1b} \quad V_2 = V_{2a} = V_{2b} \tag{1.70}$$

or, in a matrix form,

$$[V] = [V_a] = [V_b]\,. \tag{1.71}$$

Consequently, to describe the circuit properties in this case, it is convenient to use the admittance matrices that give the resulting matrix equation in the form

$$[I] = [Y]\,[V] \tag{1.72}$$

where

$$[Y] = [Y_a] + [Y_b] = \begin{bmatrix} Y_{11a} + Y_{11b} & Y_{12a} + Y_{12b} \\ Y_{21a} + Y_{21b} & Y_{22a} + Y_{22b} \end{bmatrix}. \tag{1.73}$$

The series connection of the input terminals and parallel connection of the output terminals are characterized by the circuit in Figure 1.5(*c*), which shows a series–parallel connection of two-port

networks. The common components for this circuit are the input currents and the output voltages. As a result, it is most convenient to analyze the circuit properties using hybrid matrices. The resulting two-port hybrid matrix is equal to the sum of the two individual hybrid matrices written as

$$[H] = [H_a] + [H_b] = \begin{bmatrix} h_{11a} + h_{11b} & h_{12a} + h_{12b} \\ h_{21a} + h_{21b} & h_{22a} + h_{22b} \end{bmatrix}. \tag{1.74}$$

Figure 1.5(*d*) shows the cascade connection of the two individual two-port networks. For such an approach using the one-by-one interconnection of the two-port networks, the output voltage and the output current of the first network is equal to the input voltage and the input current of the second one, respectively, when

$$V_1 = V_{1a} \quad I_1 = I_{1a} \tag{1.75}$$

$$V_{2a} = V_1 \quad -I_{2a} = I_{1b} \tag{1.76}$$

$$V_{2b} = V_2 \quad -I_{2b} = -I_2 \tag{1.77}$$

In this case, it is convenient to use a system of *ABCD*-parameters given by Eqs. (1.21) and (1.22). As a result, for the first individual two-port network shown in Figure 1.5(*d*),

$$\begin{bmatrix} V_{1a} \\ I_{1a} \end{bmatrix} = \begin{bmatrix} A_a & B_a \\ C_a & D_a \end{bmatrix} \begin{bmatrix} V_{2a} \\ -I_{2a} \end{bmatrix} \tag{1.78}$$

or, using Eqs. (1.75) and (1.76),

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_a & B_a \\ C_a & D_a \end{bmatrix} \begin{bmatrix} V_{1b} \\ I_{1b} \end{bmatrix}. \tag{1.79}$$

Similarly, for the second individual two-port network,

$$\begin{bmatrix} V_{1b} \\ I_{1b} \end{bmatrix} = \begin{bmatrix} A_b & B_b \\ C_b & D_b \end{bmatrix} \begin{bmatrix} V_{2b} \\ -I_{2b} \end{bmatrix} = \begin{bmatrix} A_b & B_b \\ C_b & D_b \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}. \tag{1.80}$$

Then, substituting matrix Eq. (1.80) to matrix Eq. (1.79) yields

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_a & B_a \\ C_a & D_a \end{bmatrix} \begin{bmatrix} A_b & B_b \\ C_b & D_b \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}. \tag{1.81}$$

Consequently, the transmission matrix of the resulting two-port network obtained by the cascade connection of the two or more individual two-port networks is determined by multiplying the transmission matrices of the individual networks. This important property is widely used in the analysis and design of transmission networks and systems.

1.4 PRACTICAL TWO-PORT NETWORKS

1.4.1 Single-Element Networks

The simplest networks, which include only one element, can be constructed by a series-connected admittance Y, as shown in Figure 1.6(*a*), or by a parallel-connected impedance Z, as shown in Figure 1.6(*b*).

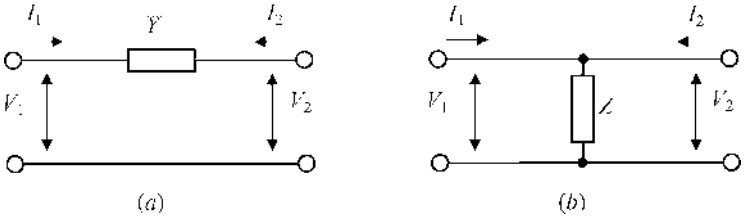

FIGURE 1.6 Single-element networks.

The two-port network consisting of the single series admittance Y can be described in a system of Y-parameters as

$$I_1 = YV_1 - YV_2 \tag{1.82}$$

$$I_2 = -YV_1 + YV_2 \tag{1.83}$$

or, in a matrix form,

$$[Y] = \begin{bmatrix} Y & -Y \\ -Y & Y \end{bmatrix} \tag{1.84}$$

which means that $Y_{11} = Y_{22} = Y$ and $Y_{12} = Y_{21} = -Y$. The resulting matrix is a singular matrix with $|Y| = 0$. Consequently, it is impossible to determine such a two-port network with the series admittance Y-parameters through a system of Z-parameters. However, by using H- and $ABCD$-parameters, it can be described, respectively, by

$$[H] = \begin{bmatrix} 1/Y & 1 \\ -1 & 0 \end{bmatrix} \quad [ABCD] = \begin{bmatrix} 1 & 1/Y \\ 0 & 1 \end{bmatrix}. \tag{1.85}$$

Similarly, for a two-port network with the single parallel impedance Z,

$$[Z] = \begin{bmatrix} Z & Z \\ Z & Z \end{bmatrix} \tag{1.86}$$

which means that $Z_{11} = Z_{12} = Z_{21} = Z_{22} = Z$. The resulting matrix is a singular matrix with $|Z| = 0$. In this case, it is impossible to determine such a two-port network with the parallel impedance Z-parameters through a system of Y-parameters. By using H- and $ABCD$-parameters, this two-port network can be described by

$$[H] = \begin{bmatrix} 0 & 1 \\ -1 & 1/Z \end{bmatrix} \quad [ABCD] = \begin{bmatrix} 1 & 0 \\ 1/Z & 1 \end{bmatrix}. \tag{1.87}$$

1.4.2 π- and T-Type Networks

The basic configurations of a two-port network that usually describe the electrical properties of the active devices can be represented in the form of a π-circuit shown in Figure 1.7(a) and in the form of a T-circuit shown in Figure 1.7(b). Here, the π-circuit includes the current source $g_m V_1$ and the T-circuit includes the voltage source $r_m I_1$.

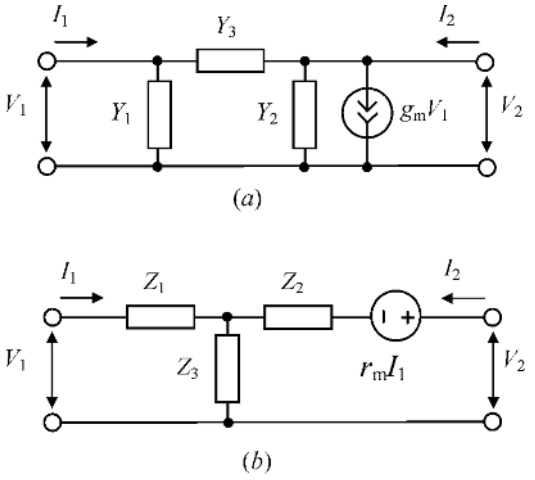

FIGURE 1.7 Basic diagrams of π- and T-networks.

By writing the two loop equations using Kirchhoff's current law or applying Eqs. (1.13) and (1.14) for the π-circuit, we obtain

$$I_1 - (Y_1 + Y_3)\, V_1 + Y_3 V_2 = 0 \tag{1.88}$$

$$I_2 + (g_m - Y_3)\, V_1 + (Y_2 + Y_3)\, V_2 = 0. \tag{1.89}$$

Eqs. (1.88) and (1.89) can be rewritten as matrix Eq. (1.3) with

$$[M] = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \quad \text{and} \quad [N] = \begin{bmatrix} -(Y_1 + Y_3) & Y_3 \\ -g_m + Y_3 & -(Y_2 + Y_3) \end{bmatrix}.$$

Since matrix $[M]$ is nonsingular, such a two-port network can be described by a system of Y-parameters as

$$[Y] = -[M]^{-1}[N] = \begin{bmatrix} Y_1 + Y_3 & -Y_3 \\ g_m - Y_3 & Y_2 + Y_3 \end{bmatrix}. \tag{1.90}$$

Similarly, for a two-port network in the form of a T-circuit using Kirchhoff's voltage law or applying Eqs. (1.8) and (1.9), we obtain

$$[Z] = -[M]^{-1}[N] = \begin{bmatrix} Z_1 + Z_3 & Z_3 \\ r_m + Z_3 & Z_2 + Z_3 \end{bmatrix}. \tag{1.91}$$

If $g_m = 0$ for a π-circuit and $r_m = 0$ for a T-circuit, their corresponding matrices in a system of $ABCD$-parameters can be written as, for π-circuit,

$$[ABCD] = \begin{bmatrix} 1 + \dfrac{Y_2}{Y_3} & \dfrac{1}{Y_3} \\ Y_1 + Y_2 + \dfrac{Y_1 Y_2}{Y_3} & 1 + \dfrac{Y_1}{Y_3} \end{bmatrix} \tag{1.92}$$

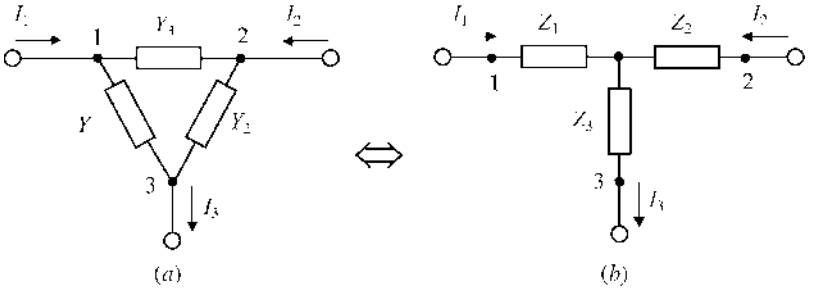

FIGURE 1.8 Equivalence of π- and T-circuits.

for T-circuit,

$$[ABCD] = \begin{bmatrix} 1 + \dfrac{Z_2}{Z_3} & Z_1 + Z_2 + \dfrac{Z_1 Z_2}{Z_3} \\ \dfrac{1}{Z_3} & 1 + \dfrac{Z_1}{Z_3} \end{bmatrix}. \tag{1.93}$$

For the appropriate relationships between impedances of a T-circuit and admittances of a π-circuit, these two circuits become equivalent with respect to the effect on any other two-port network. For a π-circuit shown in Figure 1.8(a), we can write

$$I_1 = Y_1 V_{13} + Y_3 V_{12} = Y_1 V_{13} + Y_3 (V_{13} - V_{23}) = (Y_1 + Y_3) V_{13} - Y_3 V_{23} \tag{1.94}$$

$$I_2 = Y_2 V_{23} - Y_3 V_{12} = Y_2 V_{23} - Y_3 (V_{13} - V_{23}) = -Y_3 V_{13} + (Y_2 + Y_3) V_{23}. \tag{1.95}$$

Solving Eqs. (1.94) and (1.95) for voltages V_{13} and V_{23} yields

$$V_{13} = \frac{Y_2 + Y_3}{Y_1 Y_2 + Y_1 Y_2 + Y_1 Y_2} I_1 + \frac{Y_3}{Y_1 Y_2 + Y_1 Y_2 + Y_1 Y_2} I_2 \tag{1.96}$$

$$V_{23} = \frac{Y_3}{Y_1 Y_2 + Y_1 Y_2 + Y_1 Y_2} I_1 + \frac{Y_1 + Y_3}{Y_1 Y_2 + Y_1 Y_2 + Y_1 Y_2} I_2. \tag{1.97}$$

Similarly, for a T-circuit shown in Figure 1.8(b),

$$V_{13} = Z_1 I_1 + Z_3 I_3 = Z_1 I_1 + Z_3 (I_1 + I_2) = (Z_1 + Z_3) I_1 + Z_3 I_2 \tag{1.98}$$

$$V_{13} = Z_1 I_1 + Z_3 I_3 = Z_1 I_1 + Z_3 (I_1 + I_2) = Z_3 I_1 + (Z_2 + Z_3) I_2 \tag{1.99}$$

and the equations for currents I_1 and I_2 can be obtained by

$$I_1 = \frac{Z_2 + Z_3}{Z_1 Z_2 + Z_1 Z_2 + Z_1 Z_2} V_{13} - \frac{Z_3}{Z_1 Z_2 + Z_1 Z_2 + Z_1 Z_2} V_{23} \tag{1.100}$$

$$I_2 = -\frac{Z_3}{Z_1 Z_2 + Z_1 Z_2 + Z_1 Z_2} V_{13} + \frac{Z_1 + Z_3}{Z_1 Z_2 + Z_1 Z_2 + Z_1 Z_2} V_{23}. \tag{1.101}$$

To establish a T- to π-transformation, it is necessary to equate the coefficients for V_{13} and V_{23} in Eqs. (1.100) and (1.101) to the corresponding coefficients in Eqs. (1.94) and (1.95). Similarly, to establish a π- to T-transformation, it is necessary to equate the coefficients for I_1 and I_2 in Eqs. (1.98)

TABLE 1.2 Relationships Between π- and T-Circuit Parameters.

T- to π-Transformation	π- to T-Transformation
$Y_1 = \dfrac{Z_2}{Z_1Z_2 + Z_2Z_3 + Z_1Z_3}$	$Z_1 = \dfrac{Y_2}{Y_1Y_2 + Y_2Y_3 + Y_1Y_3}$
$Y_2 = \dfrac{Z_1}{Z_1Z_2 + Z_2Z_3 + Z_1Z_3}$	$Z_2 = \dfrac{Y_1}{Y_1Y_2 + Y_2Y_3 + Y_1Y_3}$
$Y_3 = \dfrac{Z_3}{Z_1Z_2 + Z_2Z_3 + Z_1Z_3}$	$Z_3 = \dfrac{Y_3}{Y_1Y_2 + Y_2Y_3 + Y_1Y_3}$

and (1.99) to the corresponding coefficients in Eqs. (1.96) and (1.97). The resulting relationships between admittances for a π-circuit and impedances for a T-circuit are given in Table 1.2.

1.5 THREE-PORT NETWORK WITH COMMON TERMINAL

The concept of a two-port network with two independent sources can generally be extended to any multi-port networks. Figure 1.9 shows the three-port network where all three independent sources are connected to a common point. The three-port network matrix Eq. (1.3) can be described in a scalar form as

$$\left.\begin{aligned} m_{11}V_1 + m_{12}V_2 + m_{13}V_3 + n_{11}I_1 + n_{12}I_2 + n_{13}I_3 = 0 \\ m_{21}V_1 + m_{22}V_2 + m_{23}V_3 + n_{21}I_1 + n_{22}I_2 + n_{23}I_3 = 0 \\ m_{31}V_1 + m_{32}V_2 + m_{33}V_3 + n_{31}I_1 + n_{32}I_2 + n_{33}I_3 = 0 \end{aligned}\right\}. \tag{1.102}$$

If matrix $[N]$ in Eq. (1.102) is nonsingular when $|N| \neq 0$, this system of three equations can be rewritten in admittance matrix representation in terms of the voltage matrix $[V]$, similarly to a two-port network, by

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}. \tag{1.103}$$

The matrix $[Y]$ in Eq. (1.103) is the indefinite admittance matrix of the three-port network and represents a singular matrix with two important properties: the sum of all terminal currents entering the circuit is equal to zero, that is, $I_1 + I_2 + I_3 = 0$; and all terminal currents entering the circuit

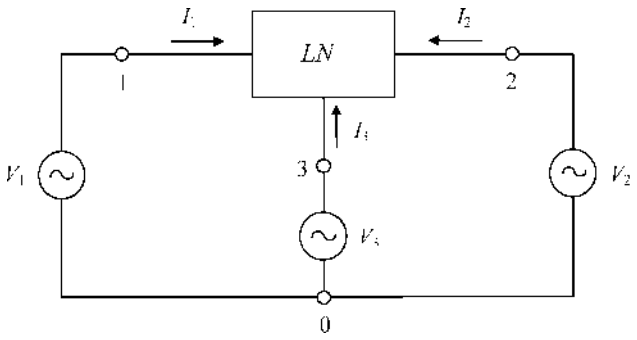

FIGURE 1.9 Basic diagram of three-port network with common terminal.

depend on the voltages between circuit terminals, which makes the sum of all terminal voltages equal to zero, that is, $V_{13} + V_{32} + V_{21} = 0$.

According to the first property, adding the left and right parts of matrix Eq. (1.103) results in

$$(Y_{11} + Y_{21} + Y_{31})\,V_1 + (Y_{12} + Y_{22} + Y_{32})\,V_2 + (Y_{13} + Y_{23} + Y_{33})\,V_3 = 0. \tag{1.104}$$

Since all terminal voltages (V_1, V_2, and V_3) can be set independently from each other, Eq. (1.104) can be satisfied only if any column sum is identically zero,

$$\left.\begin{aligned} Y_{11} + Y_{21} + Y_{31} &= 0 \\ Y_{12} + Y_{22} + Y_{32} &= 0 \\ Y_{13} + Y_{23} + Y_{33} &= 0 \end{aligned}\right\}. \tag{1.105}$$

The neither terminal currents will neither decrease nor increase, with the simultaneous change of all terminal voltages, by the same magnitude. Consequently, if all terminal voltages are equal to a nonzero value when $V_1 = V_2 = V_3 = V_0$, a lack of the terminal currents occurs when $I_1 = I_2 = I_3 = 0$. For example, from the first row of the matrix Eq. (1.103) it follows that $I_1 = Y_{11}V_1 + Y_{12}V_2 + Y_{13}V_3$; then we can write

$$0 = (Y_{11} + Y_{12} + Y_{13})\,V_0 \tag{1.106}$$

which results due to the nonzero value V_0 in

$$Y_{11} + Y_{12} + Y_{13} = 0. \tag{1.107}$$

Applying the same approach to other two rows results in

$$\left.\begin{aligned} Y_{11} + Y_{12} + Y_{13} &= 0 \\ Y_{21} + Y_{22} + Y_{23} &= 0 \\ Y_{31} + Y_{32} + Y_{33} &= 0 \end{aligned}\right\}. \tag{1.108}$$

Consequently, by using Eqs. (1.105) through (1.108), the indefinite admittance Y-matrix of three-port network can be rewritten by

$$[Y] = \begin{bmatrix} Y_{11} & Y_{12} & -(Y_{11} + Y_{12}) \\ Y_{21} & Y_{22} & -(Y_{21} + Y_{22}) \\ -(Y_{11} + Y_{21}) & -(Y_{12} + Y_{22}) & Y_{11} + Y_{12} + Y_{21} + Y_{22} \end{bmatrix}. \tag{1.109}$$

By selecting successively terminal 1, 2, and 3 as the datum terminal, the corresponding three two-port admittance matrices of the initial three-port network can be obtained. In this case, the admittance matrices will correspond to a common emitter configuration shown in Figure 1.10(*a*), a common base configuration shown in Figure 1.10(*b*), and a common collector configuration of the

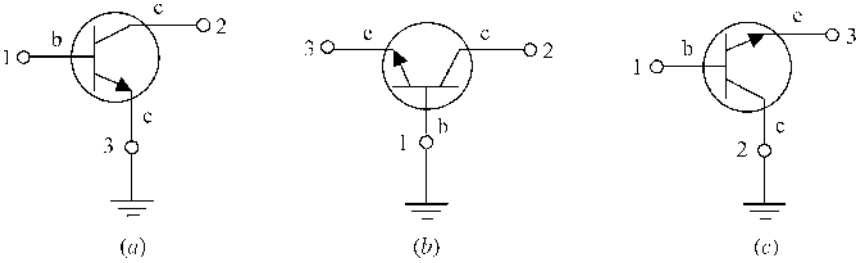

FIGURE 1.10 Bipolar transistors with different common terminals.

TABLE 1.3 *Y*- and *Z*-Parameters of Active Device with Different Common Terminal.

	Y-Parameters	*Z*-Parameters
Common emitter (source)	$\begin{matrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{matrix}$	$\begin{matrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{matrix}$
Common base (gate)	$\begin{matrix} Y_{11}+Y_{12}+Y_{21}+Y_{22} & -(Y_{12}+Y_{22}) \\ -(Y_{21}+Y_{22}) & Y_{22} \end{matrix}$	$\begin{matrix} Z_{11}+Z_{12}+Z_{21}+Z_{22} & -(Z_{12}+Z_{22}) \\ -(Z_{21}+Z_{22}) & Z_{22} \end{matrix}$
Common collector (drain)	$\begin{matrix} Y_{11} & -(Y_{11}+Y_{12}) \\ -(Y_{11}+Y_{21}) & Y_{11}+Y_{12}+Y_{21}+Y_{22} \end{matrix}$	$\begin{matrix} Z_{11} & -(Z_{11}+Z_{12}) \\ -(Z_{11}+Z_{21}) & Z_{11}+Z_{12}+Z_{21}+Z_{22} \end{matrix}$

bipolar transistor shown in Figure 1.10(c), respectively. If the common emitter device is treated as a two-port network characterized by four Y-parameters (Y_{11}, Y_{12}, Y_{21}, and Y_{22}), the two-port matrix of the common collector configuration with grounded collector terminal is simply obtained by deleting the second row and the second column in matrix Eq. (1.109). For the common base configuration with grounded base terminal, the first row and the first column should be deleted because the emitter terminal is considered the input terminal.

A similar approach can be applied to the indefinite three-port impedance network. This allows the Z-parameters of the impedance matrices of the common base and the common collector configurations through known impedance Z-parameters of the common emitter configuration of the transistor to be determined. Parameters of the three-port network that can describe the electrical behavior of the three-port bipolar or field-effect transistor configured with different common terminals are given in Table 1.3.

1.6 LUMPED ELEMENTS

Generally, passive RF and microwave lumped or integrated circuits are designed based on the lumped elements, distributed elements, or combination of both types of elements. Distributed elements represent any sections of the transmission lines of different lengths, types, and characteristic impedances. The basic lumped elements are inductors and capacitors that are small in size in comparison with the transmission-line wavelength λ, and usually their linear dimensions are less than λ/10 or even λ/16. In applications where lumped elements are used, their basic advantages are small physical size and low production cost. However, their main drawbacks are lower quality factor and power-handling capability compared with distributed elements.

1.6.1 Inductors

Inductors are lumped elements that store energy in a magnetic field. Lumped inductors can be realized using several different configurations, such as a short-section of a strip conductor or wire, a single loop, or a spiral. The printed high-impedance microstrip-section inductor is usually used for low inductance values, typically less than 2 nH, and often meandered to reduce the component size. The printed microstrip single-loop inductors are not very popular due to their limited inductance per unit area. The approximate expression for the microstrip short-section inductance in free space is given by

$$L\,(\text{nH}) = 0.2 \times 10^{-3} l \left[\ln\left(\frac{l}{W+t}\right) + 1.193 + \frac{W+t}{3l} \right] K_{\text{g}} \tag{1.110}$$

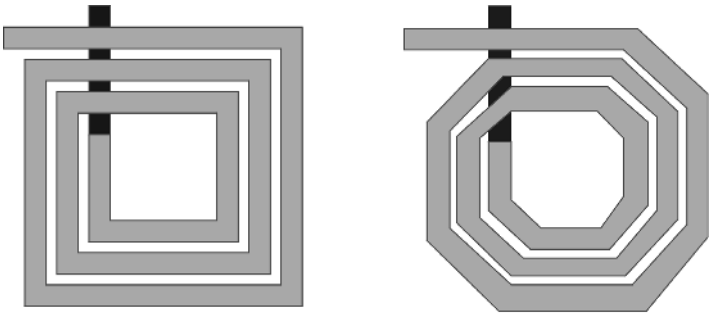

FIGURE 1.11 Spiral inductor layouts.

where the conductor length l, conductor width W, and conductor thickness t are in microns, and the term K_g accounts for the presence of a ground plane, defined as

$$K_g = 0.57 - 0.145 \ln \frac{W}{h}, \quad \text{for } \frac{W}{h} > 0.05 \tag{1.111}$$

where h is the spacing from ground plane [6,7].

Spiral inductors can have a circular configuration, a rectangular (square) configuration shown in Figure 1.11(a), or an octagonal configuration shown in Figure 1.11(b), if the technology allows 45° routing. The circular geometry is superior in electrical performance, whereas the rectangular shapes are easy to lay out and fabricate. Printed inductors are based on using thin-film or thick-film Si or GaAs fabrication processes, and the inner conductor is pulled out to connect with other circuitry through a bondwire, an air bridge, or by using multilevel crossover metal. The general expression for spiral inductor, which is also valid for its planar integration within accuracy of around 3%, is based on Wheeler formula and can be obtained as

$$L\,(\text{nH}) = \frac{K_1 n^2 d_{\text{avg}}}{1 + K_2 \rho} \tag{1.112}$$

where n is the number of turns, $d_{\text{avg}} = (d_{\text{out}} + d_{\text{in}})/2$ is the average diameter, $\rho = (d_{\text{out}} + d_{\text{in}})/(d_{\text{out}} - d_{\text{in}})$ is the fill ratio, d_{out} is the outer diameter in μm, d_{in} is the inner diameter in μm, and the coefficients K_1 and K_2 are layout-dependent as follows: square—$K_1 = 2.34$, $K_2 = 2.75$; hexagonal—$K_1 = 2.33$, $K_2 = 3.82$; octagonal—$K_1 = 2.25$, $K_2 = 3.55$ [8,9].

In contrast to the capacitors, high-quality inductors cannot be readily available in a standard complementary metal-oxide-semiconductor (CMOS) technology. Therefore, it is necessary to use special techniques to improve the inductor electrical performance. By using a standard CMOS technology with only two metal layers and a heavily doped substrate, the spiral inductor will have a large series resistance, compared with three–four metal layer technologies, and the substrate losses become a very important factor due to a relatively low resistivity of silicon. A major source of substrate losses is the capacitive coupling when current is flowing not only through the metal strip, but also through the silicon substrate. Another important source of substrate losses is the inductive coupling when, due to the planar inductor structure, the magnetic field penetrates deeply into the silicon substrate, inducing current loops and related losses. However, the latter effects are particularly important for large-area inductors and can be overcome by using silicon micromachining techniques [10].

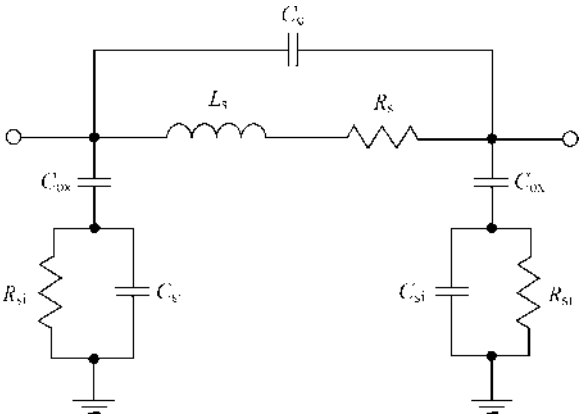

FIGURE 1.12 Equivalent circuit of a square spiral inductor.

The simplified equivalent circuit for the CMOS spiral microstrip inductor is shown in Figure 1.12, where L_s models the self and mutual inductances, R_s is the series coil resistance, C_{ox} is the parasitic oxide capacitance from the metal layer to the substrate, R_{si} is the resistance of the conductive silicon substrate, C_{si} is the silicon substrate parasitic capacitance, and C_c is the parasitic coupling capacitance [11]. The parasitic silicon substrate capacitance C_{si} is sufficiently small, and in most cases it can be neglected. Such a model shows an accurate agreement between simulated and measured data within 10% across a variety of inductor geometries and substrate dopings up to 20 GHz [12]. At frequencies well below the inductor self-resonant frequency ω_{SRF}, the coupling capacitance C_c between metal segments due to fringing fields in both the dielectric and air regions can also be neglected since the relative dielectric constant of the oxide is small enough [13]. In this case, if one side of the inductor is grounded, the self-resonant frequency of the spiral inductor can approximately be calculated from

$$\omega_{SRF} = \frac{1}{\sqrt{L_s C_{ox}}} \sqrt{\frac{L_s - R_s^2 C_{ox}}{L_s - R_{si}^2 C_{ox}}}. \tag{1.113}$$

At frequencies higher than self-resonant frequency ω_{SRF}, the inductor exhibits a capacitive behavior. The self-resonant frequency ω_{SRF} is limited mainly by the parasitic oxide capacitance C_{ox}, which is inversely proportional to the oxide thickness between the metal layer and substrate. The frequency at which the inductor quality factor Q is maximal can be obtained as

$$\omega_Q = \frac{1}{\sqrt{L_s C_{ox}}} \sqrt{\frac{R_s}{2R_{si}}} \left(\sqrt{1 + \frac{4R_{si}}{3R_s}} - 1 \right)^{0.5}. \tag{1.114}$$

The inductor metal conductor series resistance R_s can be easily calculated at low frequencies as the product of the sheet resistance and the number of squares of the metal trace. However, at high frequencies, the skin effect and other magnetic field effects will cause a nonuniform current distribution in the inductor profile. In this case, a simple increase in the diameter of the inductor metal turn does not necessarily reduce correspondingly the inductor series resistance. For example, for the same inductance value, the difference in resistance between the two inductors, when one of which has a two times wider metal strip, is only a factor of 1.35 [14]. Moreover, at very high frequencies, the largest contribution to the series resistance does not come from the longer outer turns, but from the inner turns. This phenomenon is a result of the generation of circular eddy currents in the inner conductors, whose direction is such that they oppose the original change in magnetic field. On the

inner side of the inner turn, coil current and eddy current flow in the same direction, so the current density is larger than average. On the outer side, both currents cancel, and the current density is smaller than average. As a result, the current in the inner turn is pushed to the inside of the conductor.

In hybrid or monolithic applications, bondwires are used to interconnect different components such as lumped elements, planar transmission lines, solid-state devices, and integrated circuits. These bondwires, which are usually made of gold or aluminium, have 0.5- to 1.0-mil diameters, and their lengths are electrically shorter compared with the operating wavelength. To characterize the electrical behavior of the bondwires, simple formulas in terms of their inductances and series resistances can be used. As a first-order approximation, the parasitic capacitance associated with bondwires can be neglected. When $l \gg d$, where l is the bondwire length in μm and d is the bondwire diameter in μm,

$$L\,(\text{nH}) = 0.2 \times 10^{-3} l \left(\ln \frac{4l}{d} + 0.5 \frac{d}{l} - 1 + C \right) \tag{1.115}$$

where $C = 0.25 \tanh(4\delta/d)$ is the frequency-dependent correction factor, which is a function of bondwire diameter and its material's skin depth δ [8,15].

1.6.2 Capacitors

Capacitors are lumped elements that store energy due to an electric field between two electrodes (or plates) when a voltage is applied across them. In this case, charge of equal magnitude but opposite sign accumulates on the opposing capacitor plates. The capacitance depends on the area of the plates, separation, and dielectric material between them. The basic structure of a chip capacitor shown in Figure 1.13(a) consists of two parallel plates, each of area $A = W \times l$ and separated by a dielectric material of thickness d and permittivity $\varepsilon_0\varepsilon_r$, where ε_0 is the free-space permittivity (8.85×10^{-12} farads/m) and ε_r is the relative dielectric constant.

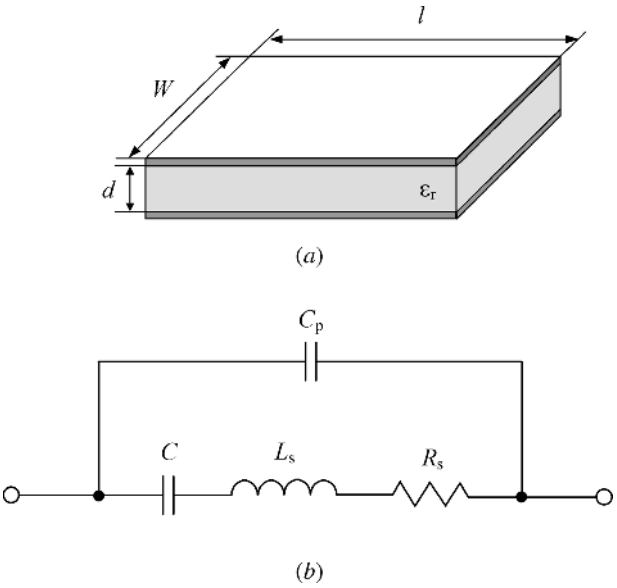

FIGURE 1.13 Parallel capacitor topology and its equivalent circuit.

Chip capacitors are usually used in hybrid integrated circuits when relatively high capacitance values are required. In the parallel-plate configuration, the capacitance is commonly expressed as

$$C\ (\text{pF}) = 8.85 \times 10^{-3} \varepsilon_r \frac{Wl}{d} \tag{1.116}$$

where W, l, and d are dimensions in millimeters. Generally, the low-frequency bypass capacitor values are expressed in microfarads and nanofarads, high-frequency blocking and tuning capacitors are expressed in picofarads, and parasitic or fringing capacitances are written in femtofarads. This basic formula given by Eq. (1.116) can also be applied to capacitors based on a multilayer technique [7]. The lumped-element equivalent circuit of a capacitor is shown in Figure 1.13(*b*), where L_s is the series plate inductance, R_s is the series contact and plate resistance, and C_p is the parasitic parallel capacitance. When $C \gg C_p$, the frequency ω_{SRF}, at which the reactances of series elements C and L_s become equal, is called the *capacitor self-resonant frequency*, and the capacitor impedance is equal to the resistance R_s.

For monolithic applications, where relatively low capacitances (typically less than 0.5 pF) are required, planar series capacitances in the form of microstrip or interdigital configurations can be used. These capacitors are simply formed by gaps in the center conductor of the microstrip lines, and they do not require any dielectric films. The gap capacitor, shown in Figure 1.14(*a*), can be equivalently represented by a series coupling capacitance and two parallel fringing capacitances [16]. The interdigital capacitor is a multifinger periodic structure, as shown in Figure 1.14(*b*), where the capacitance occurs across a narrow gap between thin-film transmission-line conductors [17]. These gaps are essentially very long and folded to use a small amount of area. In this case, it is important to keep the size of the capacitor very small relative to the wavelength, so that it can be treated as a lumped element. A larger total width-to-length ratio results in the desired higher shunt capacitance and lower series inductance. An approximate expression for the total capacitance of interdigital structure, with $s = W$ and length l less than a quarter wavelength, can be given by

$$C\ (\text{pF}) = (\varepsilon_r + 1)\, l\, [(N - 3)\, A_1 + A_2] \tag{1.117}$$

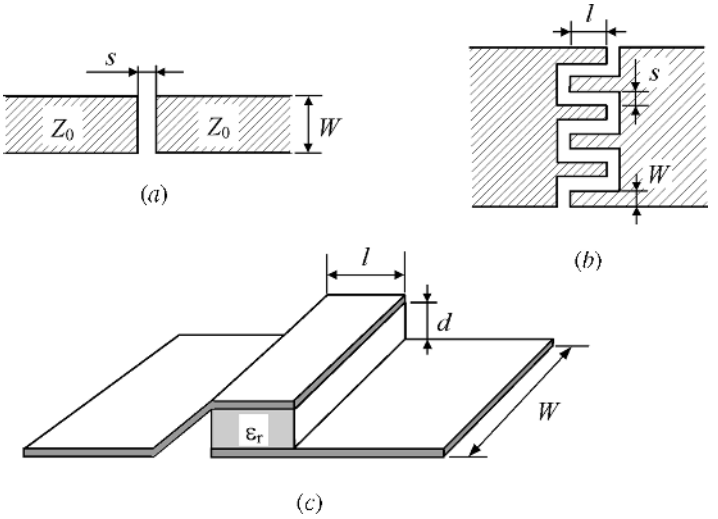

FIGURE 1.14 Different series capacitor topologies.

where N is the number of fingers and

$$A_1\,(\text{pF}/\mu\text{m}) = 4.409\tanh\left[0.55\left(\frac{h}{W}\right)^{0.45}\right]\times 10^{-6} \tag{1.118}$$

$$A_2\,(\text{pF}/\mu\text{m}) = 9.92\tanh\left[0.52\left(\frac{h}{W}\right)^{0.5}\right]\times 10^{-6} \tag{1.119}$$

where h is the spacing from the ground plane.

Series planar capacitors with larger values, which are called the metal-insulator-metal (MIM) capacitors, can be realized by using an additional thin dielectric layer (typically less than 0.5 μm) between two metal plates, as shown in Figure 1.14(*c*) [7]. The bottom plate of the capacitor uses a thin unplated metal, and typically the dielectric material is silicon nitride (Si_3N_4) for integrated circuits on GaAs and SiO_2 for integrated circuits on Si. The top plate uses a thick-plated conductor to reduce the loss in the capacitor. These capacitors are used to achieve higher capacitance values in small areas (10 pF and greater), with typical tolerances from 10% to 15%. The capacitance can be calculated according to Eq. (1.116).

1.7 TRANSMISSION LINE

Transmission lines are widely used in matching circuits in power amplifiers, in resonant and feedback circuits in the oscillators, filters, directional couplers, power combiners, and dividers. When the propagated signal wavelength is compared to its physical dimension, the transmission line can be considered as a two-port network with distributed parameters, where the voltages and currents vary in magnitude and phase over length.

Schematically, a transmission line is often represented as a two-wire line, as shown in Figure 1.15(*a*), where its electrical parameters are distributed along its length. The physical properties of a transmission line are determined by four basic parameters:

1. The series inductance L due to the self-inductive phenomena of two conductors.
2. The shunt capacitance C in view of the close proximity between two conductors.
3. The series resistance R due to the finite conductivity of the conductors.
4. The shunt conductance G that is related to the dielectric losses in the material.

As a result, a transmission line of length Δx represents a lumped-element circuit shown in Figure 1.15(*b*), where ΔL, ΔC, ΔR, and ΔG are the series inductance, the shunt capacitance, the series resistance, and the shunt conductance per unit length, respectively. If all these elements are distributed uniformly along the transmission line, and their values do not depend on the chosen position of Δx, this transmission line is called the *uniform transmission line*. Any finite length of the uniform transmission line can be viewed as a cascade of section length Δx.

To define the distribution of the voltages and currents along the uniform transmission line, it is necessary to write the differential equations using Kirchhoff's voltage law for instantaneous values of the voltages and currents in the line section of length Δx, distant x from its beginning. For the sinusoidal steady-state condition, the telegrapher equations for $V(x)$ and $I(x)$ are given by

$$\frac{d^2V(x)}{dx^2} - \gamma^2 V(x) = 0 \tag{1.120}$$

$$\frac{d^2I(x)}{dx^2} - \gamma^2 I(x) = 0 \tag{1.121}$$

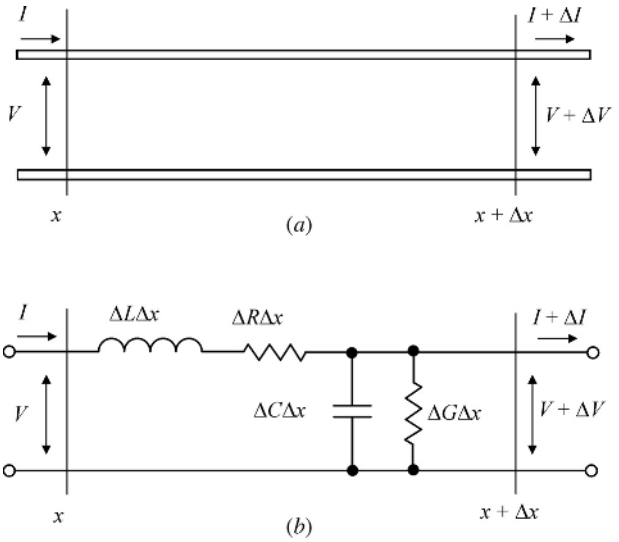

FIGURE 1.15 Transmission line schematics.

where $\gamma = \alpha + j\beta = \sqrt{(\Delta R + j\omega\Delta L)(\Delta G + j\omega\Delta C)}$ is the complex propagation constant (which is a function of frequency), α is the attenuation constant, and β is the phase constant. The general solutions of Eqs. (1.120) and (1.121) for voltage and current of the traveling wave in the transmission line can be written as

$$V(x) = A_1 \exp(-\gamma x) + A_2 \exp(\gamma x) \tag{1.122}$$

$$I(x) = \frac{A_1}{Z_0}\exp(-\gamma x) - \frac{A_2}{Z_0}\exp(\gamma x) \tag{1.123}$$

where $Z_0 = \sqrt{(\Delta R + j\omega\Delta L)/(\Delta G + j\omega\Delta C)}$ is the characteristic impedance of the transmission line, $V_i = A_1\exp(-\gamma x)$ and $V_r = A_2\exp(\gamma x)$ represent the incident voltage and the reflected voltage, respectively, and $I_i = A_1\exp(-\gamma x)/Z_0$ and $I_r = A_2\exp(\gamma x)/Z_0$ are the incident current and the reflected current, respectively. From Eqs. (1.122) and (1.123) it follows that the characteristic impedance of the transmission line Z_0 represents the ratio of the incident (reflected) voltage to the incident (reflected) current at any position on the line as

$$Z_0 = \frac{V_i(x)}{I_i(x)} = \frac{V_r(x)}{I_r(x)}. \tag{1.124}$$

For a lossless transmission line, when $R = G = 0$ and the voltage and current do not change with position, the attenuation constant $\alpha = 0$, the propagation constant $\gamma = j\beta = j\omega\sqrt{\Delta L\Delta C}$, and the phase constant $\beta = \omega\sqrt{\Delta L\Delta C}$. Consequently, the characteristic impedance is reduced to $Z_0 = \sqrt{L/C}$ and represents a real number. The wavelength is defined as $\lambda = 2\pi/\beta = 2\pi/\omega\sqrt{\Delta L\Delta C}$ and the phase velocity as $v_p = \omega/\beta = 1/\sqrt{\Delta L\Delta C}$.

Figure 1.16 represents a transmission line of characteristic impedance Z_0 terminated with a load Z_L. In this case, the constants A_1 and A_2 are determined at the position $x = l$ by

$$V(l) = A_1 \exp(-\gamma l) + A_2 \exp(\gamma l) \tag{1.125}$$

$$I(l) = \frac{A_1}{Z_0}\exp(-\gamma l) - \frac{A_2}{Z_0}\exp(\gamma l) \tag{1.126}$$

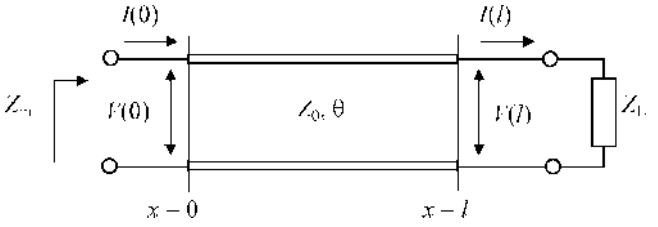

FIGURE 1.16 Loaded transmission line.

and equal to

$$A_1 = \frac{V(l) + Z_0 I(l)}{2} \exp(\gamma l) \tag{1.127}$$

$$A_2 = \frac{V(l) - Z_0 I(l)}{2} \exp(-\gamma l). \tag{1.128}$$

As a result, wave equations for voltage $V(x)$ and current $I(x)$ can be rewritten as

$$V(x) = \frac{V(l) + Z_0 I(l)}{2} \exp[\gamma (l - x)] + \frac{V(l) - Z_0 I(l)}{2} \exp[-\gamma (l - x)] \tag{1.129}$$

$$I(x) = \frac{V(l) + Z_0 I(l)}{2Z_0} \exp[\gamma (l - x)] - \frac{V(l) - Z_0 I(l)}{2Z_0} \exp[-\gamma (l - x)] \tag{1.130}$$

which allows their determination at any position on the transmission line.

The voltage and current amplitudes at $x = 0$ as functions of the voltage and current amplitudes at $x = l$ can be determined from Eqs. (1.129) and (1.130) as

$$V(0) = \frac{V(l) + Z_0 I(l)}{2} \exp(\gamma l) + \frac{V(l) - Z_0 I(l)}{2} \exp(-\gamma l) \tag{1.131}$$

$$I(0) = \frac{V(l) + Z_0 I(l)}{2Z_0} \exp(\gamma l) - \frac{V(l) - Z_0 I(l)}{2Z_0} \exp(-\gamma l). \tag{1.132}$$

By using the ratios $\cosh x = [\exp(x) + \exp(-x)]/2$ and $\sinh x = [\exp(x) - \exp(-x)]/2$, Eqs. (1.131) and (1.132) can be rewritten in the form

$$V(0) = V(l) \cosh(\gamma l) + Z_0 I(l) \sinh(\gamma l) \tag{1.133}$$

$$I(0) = \frac{V(l)}{Z_0} \sinh(\gamma l) + I(l) \cosh(\gamma l) \tag{1.134}$$

which represents the transmission equations of the symmetrical reciprocal two-port network expressed through the *ABCD*-parameters when $AD - BC = 1$ and $A = D$. Consequently, the transmission *ABCD*-matrix of the lossless transmission line with $\alpha = 0$ can be given by

$$[ABCD] = \begin{bmatrix} \cos\theta & jZ_0 \sin\theta \\ \dfrac{j \sin\theta}{Z_0} & \cos\theta \end{bmatrix}. \tag{1.135}$$

Using the formulas to transform *ABCD*-parameters into *S*-parameters yields

$$[S] = \begin{bmatrix} 0 & \exp(-j\theta) \\ \exp(-j\theta) & 0 \end{bmatrix} \tag{1.136}$$

where $\theta = \beta l$ is the electrical length of the transmission line.

In the case of the loaded lossless transmission line, the reflection coefficient Γ is defined as the ratio between the reflected voltage wave and the incident voltage wave, given at x as

$$\Gamma(x) = \frac{V_\mathrm{r}}{V_\mathrm{i}} = \frac{A_2}{A_1}\exp(2j\beta x)\,. \tag{1.137}$$

By taking into account Eqs. (1.127) and (1.128), the reflection coefficient for $x = l$ can be defined as

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} \tag{1.138}$$

where Γ represents the load reflection coefficient and $Z = Z_\mathrm{L} = V(l)/I(l)$. If the load is mismatched, only part of the available power from the source is delivered to the load. This power loss is called the *return loss* (*RL*), and is calculated in decibels as

$$RL = -20\log_{10}|\Gamma|\,. \tag{1.139}$$

For a matched load when $\Gamma = 0$, a return loss is of ∞ dB. A total reflection with $\Gamma = 1$ means a return loss of 0 dB when all incident power is reflected.

According to the general solution for voltage at a position x in the transmission line,

$$V(x) = V_\mathrm{i}(x) + V_\mathrm{r}(x) = V_\mathrm{i}\,[1 + \Gamma(x)]\,. \tag{1.140}$$

Hence, the maximum amplitude (when the incident and reflected waves are in phase) is

$$V_\mathrm{max}(x) = |V_\mathrm{i}|\,[1 + |\Gamma(x)|] \tag{1.141}$$

and the minimum amplitude (when these two waves are out of phase) is

$$V_\mathrm{min}(x) = |V_\mathrm{i}|\,[1 - |\Gamma(x)|]\,. \tag{1.142}$$

The ratio of V_max to V_min, which is a function of the reflection coefficient Γ, represents the *voltage standing wave ratio* (*VSWR*). The *VSWR* is a measure of mismatch and can be written as

$$VSWR = \frac{V_\mathrm{max}}{V_\mathrm{min}} = \frac{1 + |\Gamma|}{1 - |\Gamma|} \tag{1.143}$$

which can change from 1 to ∞ (where $VSWR = 1$ implies a matched load). For a load impedance with zero imaginary part when $Z_\mathrm{L} = R_\mathrm{L}$, the *VSWR* can be calculated using $VSWR = R_\mathrm{L}/Z_0$ when $R_\mathrm{L} \geq Z_0$ and $VSWR = Z_0/R_\mathrm{L}$ when $Z_0 \geq R_\mathrm{L}$.

From Eqs. (1.133) and (1.134) it follows that the input impedance of the loaded lossless transmission line can be obtained as

$$Z_\mathrm{in} = \frac{V(0)}{I(0)} = Z_0\frac{Z_\mathrm{L} + jZ_0\tan(\theta)}{Z_0 + jZ_\mathrm{L}\tan(\theta)} \tag{1.144}$$

which gives an important dependence between the input impedance, the transmission-line parameters (electrical length and characteristic impedance), and the arbitrary load impedance.

1.8 TYPES OF TRANSMISSION LINES

Several types of transmission lines are available when designing RF and microwave active and passive circuits. Coaxial lines have very high bandwidth and high power-handling capability, and are widely used for impedance transformers and power combiners. Planar transmission lines as an evolution of the coaxial and parallel-wire lines are compact and readily adaptable to hybrid and monolithic integrated circuit fabrication technologies at RF and microwave frequencies [18]. If coaxial line is deformed in such a manner that both the center and outer conductors are square or rectangular in cross-section, and then if side walls of the rectangular coaxial system are extended to infinity, the resultant flat-strip transmission system would have a form factor that is adaptable to the printed-circuit technique. Similarly, if the parallel-wire line is replaced by its equivalent of a single wire and its image in a conducting ground plane, and if this single wire is, in turn, progressively distorted into a flat strip, the resulting transmission system is again a planar structure. There is an important aspect that differ flat-strip transmission lines from coaxial lines. In a coaxial line, an impedance discontinuity acts as a shunt capacitance, while a discontinuity in a flat strip has a series inductance in its equivalent circuit. Holes and gaps in center conductor strips also represent discontinuities that can be utilized in many applications to microwave circuitry.

1.8.1 Coaxial Line

A main type of wave propagated along a coaxial line shown in Figure 1.17 is the *transverse electromagnetic* (TEM) wave. When the transverse fields of a TEM wave are the same as the static fields that can exist between the conductors, the electromagnetic properties of a coaxial line can be characterized by the following parameters [19]: the shunt capacitance per unit length

$$C = 2\pi\varepsilon_0\varepsilon_r/\ln\left(\frac{b}{a}\right) \tag{1.145}$$

where a is the radius of inner conductor and b is the inner radius of outer conductor; the series inductance per unit length

$$L = \frac{\mu_0\mu_r}{2\pi}\ln\left(\frac{b}{a}\right) \tag{1.146}$$

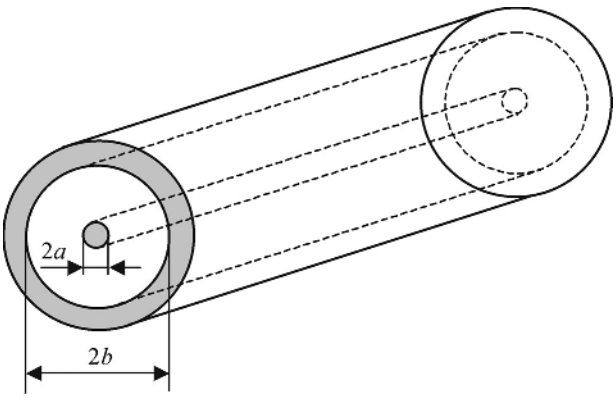

FIGURE 1.17 Coaxial line structure.

where $\mu_0 = 4\pi \times 10^{-7}$ H/m is the permeability of free space and μ_r is the relative magnetic constant or substrate permeability; the series resistance per unit length

$$R = \frac{R_s}{2\pi}\left(\frac{1}{b} + \frac{1}{a}\right) \tag{1.147}$$

where $R_s = \rho/\Delta(f) = \sqrt{\pi\mu_0\rho f}$ is the surface resistivity, ρ is the metallization electrical resistivity, $\Delta(f)$ is the penetration depth, and f is the frequency; the shunt conductance per unit length

$$G = 2\pi\sigma/\ln\left(\frac{b}{a}\right) = 2\pi\omega\varepsilon_o\varepsilon_r \tan\delta/\ln\left(\frac{b}{a}\right) \tag{1.148}$$

where σ is the dielectric conductivity and $\tan\delta$ is the dielectric loss tangent; the characteristic impedance

$$Z_0 = \frac{\eta}{2\pi}\ln\left(\frac{b}{a}\right) \tag{1.149}$$

where $\eta = \sqrt{\mu/\varepsilon}$ is the wave impedance of the lossless coaxial line identical to the intrinsic impedance of the medium.

The conductor loss factor (in Np/m) can be written as

$$\alpha_c = \frac{R}{2Z_0} \tag{1.150}$$

whereas the dielectric loss factor (in Np/m) can be written as

$$\alpha_d = \frac{GZ_0}{2} = \frac{\sigma\eta}{2} = \pi\sqrt{\varepsilon_r}\frac{\tan\delta}{\lambda} \tag{1.151}$$

where λ is the free-space wavelength.

1.8.2 Stripline

The geometry of a commonly used stripline is shown in Figure 1.18. The strip conductor of width W is placed between two flat dielectric substrates with the same dielectric constant. The outer surfaces of these substrates are metallized and serve as a ground conductor. In practice, the strip conductor is etched on one of the dielectric substrates by photolithography process. Since the stripline has two conductors and a homogeneous dielectric, it can support a pure TEM propagation mode, which is the usual mode of operation. The advantages of striplines are good electromagnetic shielding and low attenuation losses, which make them suitable for high-Q and low-interference applications. However, striplines require strong symmetry that makes their tuning complicated due to difficult access to center conductor. As a result, the stripline structure is not convenient for incorporating chip elements and associated bias circuitry.

The exact expression for the characteristic impedance of a lossless stripline of zero thickness is given by

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_r}}\frac{K(k)}{K(k')} \tag{1.152}$$

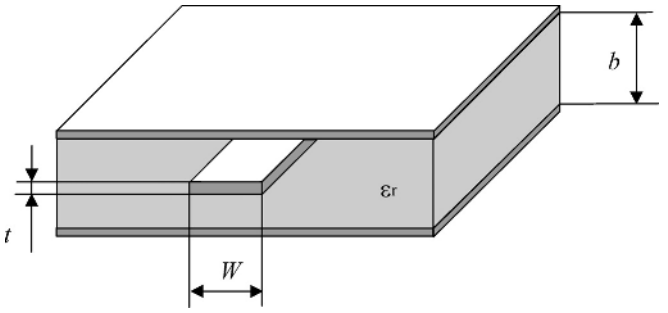

FIGURE 1.18 Stripline structure.

where

$$K(k) = \int_0^{\pi/2} \frac{d\varphi}{\sqrt{1 - k^2 \sin^2 \varphi}} \tag{1.153}$$

is the complete elliptic integral of the first kind, $k = \operatorname{sech}(\pi W/2b)$, and $k' = \sqrt{1 - k^2}$ [20,21].

An expression for the ratio $K(k)/K(k')$ can be simplified to

$$\frac{K(k)}{K(k')} = \begin{cases} \pi / \ln\left(2\dfrac{1 + \sqrt{k'}}{1 - \sqrt{k'}}\right) & \text{for } 0 \le k \le \dfrac{1}{\sqrt{2}} \\ \dfrac{1}{\pi} \ln\left(2\dfrac{1 + \sqrt{k}}{1 - \sqrt{k}}\right) & \text{for } \dfrac{1}{\sqrt{2}} \le k \le 1 \end{cases} \tag{1.154}$$

which provides the relative error lower than 3×10^{-6} [22].

In practice, it makes sense to use a sufficiently simple formula without complicated special functions [23]. In this case, the formula for Z_0 can be written within 1% of the exact results as

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_r}} \frac{b}{W_e + 0.441b} \tag{1.155}$$

where W_e is the effective width of the center conductor defined by

$$\frac{W_e}{b} = \frac{W}{b} - \begin{cases} 0 & \text{for } \dfrac{W}{b} > 0.35b \\ \left(0.35 - \dfrac{W}{b}\right)^2 & \text{for } \dfrac{W}{b} < 0.35b \end{cases}. \tag{1.156}$$

For a stripline with a TEM propagation mode, the dielectric loss factor α_d is the same as for coaxial line, which is determined by Eq. (1.151). An approximation result for the conductor loss factor α_c (in Np/m) can be obtained by

$$\alpha_c = \begin{cases} A\dfrac{2.7 \times 10^{-3} R_s \varepsilon_r Z_0}{30\pi (b - t)} & \text{for } Z_0\sqrt{\varepsilon_r} < 120 \\ B\dfrac{0.16 R_s}{Z_0 b \pi} & \text{for } Z_0\sqrt{\varepsilon_r} > 120 \end{cases} \tag{1.157}$$

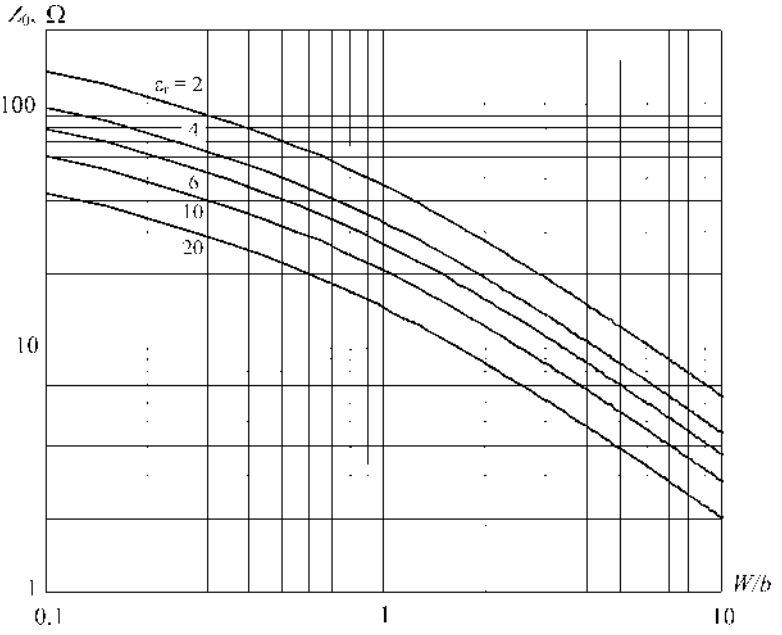

FIGURE 1.19 Stripline characteristic impedance versus W/b.

with

$$A = 1 + \frac{2W}{b-t} + \frac{1}{\pi}\frac{b+t}{b-t}\ln\frac{2b-t}{t} \tag{1.158}$$

$$B = 1 + \frac{b}{0.5W + 0.7t}\left(0.5 + \frac{0.414t}{W} + \frac{1}{2\pi}\ln\frac{4\pi W}{t}\right) \tag{1.159}$$

where t is the thickness of the strip [4].

Figure 1.19 shows the characteristic impedance Z_0 of a stripline as a function of the normalized strip width W/b for various ε_r according to Eqs. (1.155) and (1.156). Typical values of the main electrical and thermal properties of some substrate materials are listed in Table 1.4.

TABLE 1.4 Electrical and Thermal Properties of Substrate Materials.

Typical Substrate	Dielectric Constant, ε_r @ 10 GHz	Loss Tangent, $\tan\delta$ @ 10 GHz	Coefficient of Thermal Expansion (ppm/°C)
Alumina 99.5%	9.8	0.0003	6.7
Aluminum nitride	8.7	0.001	4.5
Barium tetratitanade	37	0.0002	8.3
Beryllia 99.5%	6.6	0.0003	7.5
Epoxy glass FR-4	4.7	0.01	3.0
Fused quartz	3.78	0.0001	0.5
Gallium arsenide	13.1	0.0006	6.5
Silicon	11.7	0.004	4.2
Teflon	2.5	0.0008	15

1.8.3 Microstrip Line

In a microstrip line, the grounded metallization surface covers only one side of dielectric substrate, as shown in Figure 1.20. Such a configuration is equivalent to a pair-wire system for the image of the conductor in the ground plane which produces the required symmetry [24]. In this case, the electric and magnetic field lines are located in both the dielectric region between the strip conductor and the ground plane and in the air region above the substrate. As a result, the electromagnetic wave propagated along a microstrip line is not a pure TEM, since the phase velocities in these two regions are not the same. However, in a quasistatic approximation, which gives sufficiently accurate results as long as the height of the dielectric substrate is very small compared with the wavelength, it is possible to obtain the explicit analytical expressions for the electrical characteristics. Since microstrip line is an open structure, it has a major fabrication advantage over the stripline due to simplicity of practical realization, interconnection, and adjustments.

The exact expression for the characteristic impedance of a lossless microstrip line with finite strip thickness is given by [25,26]

$$Z_0 = \begin{cases} \dfrac{60}{\sqrt{\varepsilon_{re}}} \ln\left(\dfrac{8h}{W_e} + \dfrac{W_e}{4h}\right) & \text{for } \dfrac{W}{h} \le 1 \\ \dfrac{120\pi}{\sqrt{\varepsilon_{re}}} \left[\dfrac{W_e}{h} + 1.393 + 0.667 \ln\left(\dfrac{W_e}{h} + 1.444\right)\right]^{-1} & \text{for } \dfrac{W}{h} \ge 1 \end{cases} \tag{1.160}$$

where

$$\frac{W_e}{h} = \frac{W}{h} + \frac{\Delta W}{h} \tag{1.161}$$

$$\frac{\Delta W}{h} = \begin{cases} \dfrac{1.25}{\pi} \dfrac{t}{h} \left(1 + \ln \dfrac{4\pi W}{t}\right) & \text{for } \dfrac{W}{h} \le 1/2\pi \\ \dfrac{1.25}{\pi} \dfrac{t}{h} \left(1 + \ln \dfrac{2h}{t}\right) & \text{for } \dfrac{W}{h} \ge 1/2\pi \end{cases} \tag{1.162}$$

$$\varepsilon_{re} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12h/W}} - \frac{\varepsilon_r - 1}{4.6} \frac{t}{h} \sqrt{\frac{h}{W}}. \tag{1.163}$$

Figure 1.21 shows the characteristic impedance Z_0 of a microstrip line with zero strip thickness as a function of the normalized strip width W/h for various ε_r according to Eqs. (1.160) to (1.163).

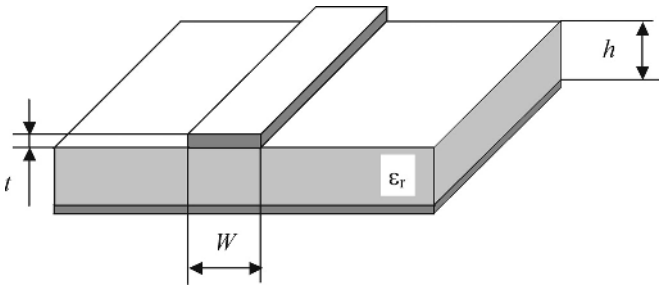

FIGURE 1.20 Microstrip line structure.

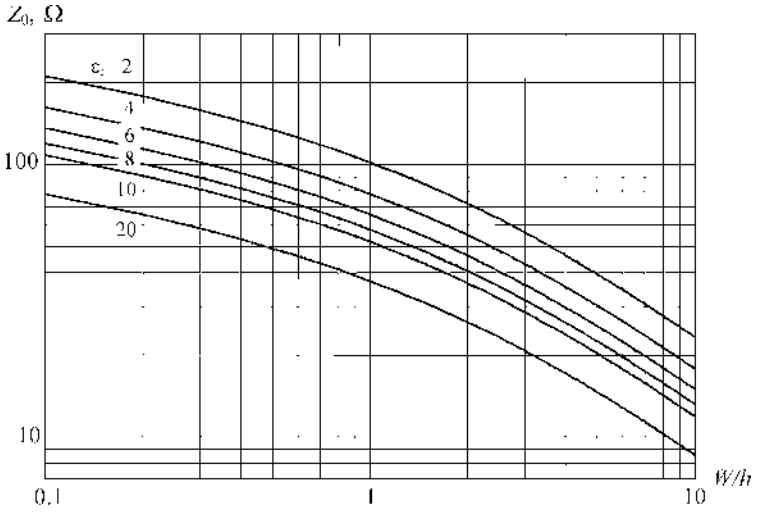

FIGURE 1.21 Microstrip characteristic impedance versus W/h.

In practice, it is possible to use a sufficiently simple formula to estimate the characteristic impedance Z_0 of a microstrip line with zero strip thickness written as [27]

$$Z_0 = \frac{120\pi}{\sqrt{\varepsilon_r}} \frac{h}{W} \frac{1}{1 + 1.735\varepsilon_r^{-0.0724}(W/h)^{-0.836}}. \tag{1.164}$$

For a microstrip line in a quasi-TEM approximation, the conductor loss factor α_c (in Np/m) as a function of the microstrip-line geometry can be obtained by

$$\alpha_c = \begin{cases} 1.38A \dfrac{R_s}{hZ_0} \dfrac{32 - (W_e/h)^2}{32 + (W_e/h)^2} & \text{for } \dfrac{W}{h} \le 1 \\ 6.1 \cdot 10^{-5} A \dfrac{R_s Z_0 \varepsilon_{re}}{h} \left(\dfrac{W_e}{h} + \dfrac{0.667\, W_e/h}{1.444 + W_e/h} \right) & \text{for } \dfrac{W}{h} \ge 1 \end{cases} \tag{1.165}$$

with

$$A = 1 + \frac{h}{W_e} \left(1 + \frac{1}{\pi} \ln \frac{2B}{t} \right) \tag{1.166}$$

$$B = \begin{cases} 2\pi W & \text{for } \dfrac{W}{h} \le 1/2\pi \\ h & \text{for } \dfrac{W}{h} \ge 1/2\pi \end{cases} \tag{1.167}$$

where W_e/h is given by Eqs. (1.161) and (1.162) [28].

The dielectric loss factor α_d (in Np/m) can be calculated by

$$\alpha_d = 27.3 \frac{\varepsilon_r}{\varepsilon_r - 1} \frac{\varepsilon_{re} - 1}{\sqrt{\varepsilon_{re}}} \frac{\tan\delta}{\lambda}. \tag{1.168}$$

Conductor loss is a result of several factors related to the metallic material composing the ground plane and walls, among which are conductivity, skin effect, and surface ruggedness. For most microstrip lines (except some kinds of semiconductor substrate such as silicon), the conductor loss is

TABLE 1.5 Electrical Resistivity of Conductor Materials.

Material	Symbol	Electrical Resistivity (μΩ cm)	Material	Symbol	Electrical Resistivity (μΩ cm)
Aluminum	Al	2.65	Palladium	Pd	10.69
Copper	Cu	1.67	Platinum	Pt	10.62
Gold	Au	2.44	Silver	Ag	1.59
Indium	In	15.52	Tantalum	Ta	15.52
Iron	Fe	9.66	Tin	Sn	11.55
Lead	Pb	21.0	Titanium	Ti	55.0
Molybdenum	Mo	5.69	Tungsten	W	5.6
Nickel	Ni	8.71	Zinc	Zn	5.68

much more significant than the dielectric loss. The conductor losses increase with increasing characteristic impedance due to greater resistance of narrow strips. The electrical resistivity of some conductor materials is given in Table 1.5.

1.8.4 Slotline

Slotlines are usually used when it is necessary to realize a high value of the characteristic impedance Z_0 [29,30]. A slotline is dual to a microstrip line and represents a narrow slot between two conductive surfaces, one of which is grounded. Changing the width of the slot can easily change the characteristic impedance of the slotline. The transverse electric H-mode wave propagates along the slotline. Three basic types of slotlines are unilateral, antipodal, and bilateral. The geometry of a unilateral slotline is shown in Figure 1.22, with a narrow gap in the conductive coating on one side of the dielectric substrate and being bare on the other side of substrate. Slotline can be used either alone or with microstrip line on the opposite side of substrate.

It is difficult to provide exact analytical expressions to calculate the slotline parameters. However, an equation for Z_0 can be obtained for a quasi-TEM approximation with zero conductor thickness and infinite width of the entire slotline system as

for $0.02 \leq W/h \leq 0.2$

$$Z_0 = 72.62 - 15.283\ln\varepsilon_r + 50\left(1 - 0.02\frac{h}{W}\right)\left(\frac{W}{h} - 0.1\right) + (19.23 - 3.693\ln\varepsilon_r)\ln\left(10^2\frac{W}{h}\right) - \left(11.4 - 2.636\ln\varepsilon_r - 10^2\frac{h}{\lambda}\right)^2 \times \left[0.139\ln\varepsilon_r - 0.11 + \frac{W}{h}(0.465\ln\varepsilon_r + 1.44)\right] \quad (1.169)$$

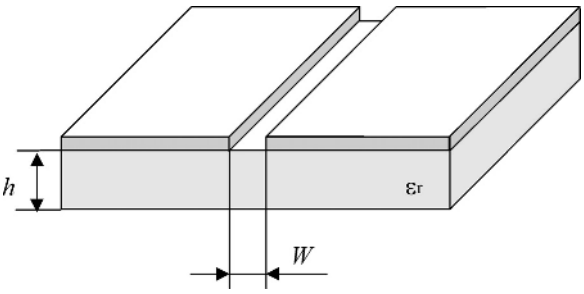

FIGURE 1.22 Slotline structure.

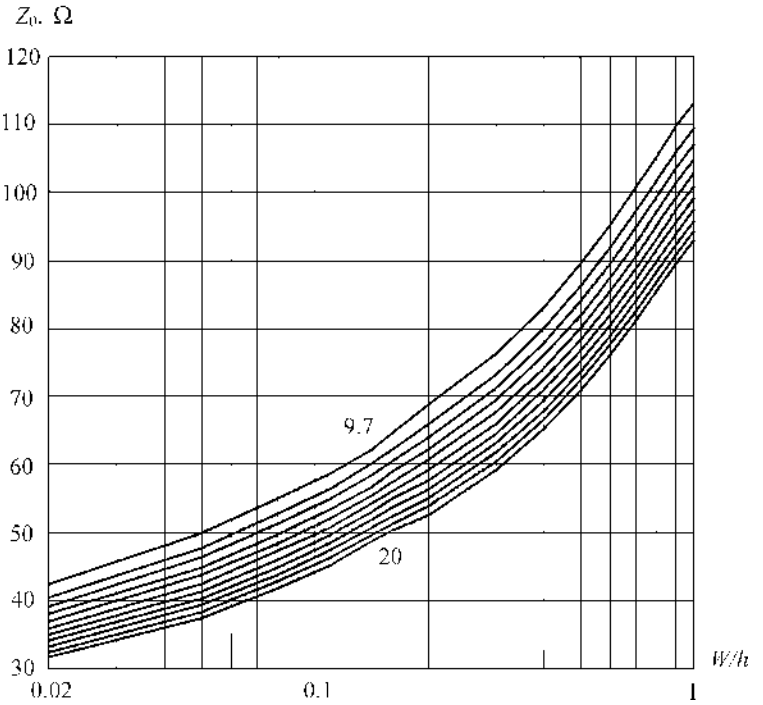

FIGURE 1.23 Slotline characteristic impedance versus W/h.

for $0.2 \leq W/h \leq 1.0$

$$Z_0 = 113.19 - 23.257\ln\varepsilon_r + 1.25\frac{W}{h}(114.59 - 22.531\ln\varepsilon_r) + 20\left(1 - \frac{W}{h}\right)\left(\frac{W}{h} - 0.2\right)$$
$$- \left[0.15 + 0.1\ln\varepsilon_r + \frac{W}{h}(0.899\ln\varepsilon_r - 0.79)\right]$$
$$\times \left[10.25 - 2.171\ln\varepsilon_r + \frac{W}{h}(2.1 - 0.617\ln\varepsilon_r) - 10^2\frac{h}{\lambda}\right]^2 \tag{1.170}$$

where $0.01 \leq h/\lambda \leq 0.25/\sqrt{\varepsilon_r - 1}$ and λ is the free-space wavelength [31].

Figure 1.23 shows the characteristic impedance Z_0 of a slotline within the error of 2% as a function of the normalized slot width W/h for $h/\lambda = 0.02$ and various $\varepsilon_r = 9.7, 11, 12, \ldots, 20$ calculated by Eqs. (1.169) and (1.170).

1.8.5 Coplanar Waveguide

A coplanar waveguide (CPW) is similar in structure to a slotline, the only difference being a third conductor centered in the slot region. The center strip conductor and two outer grounded conductors lie in the same plane on substrate surface, as shown in Figure 1.24 [32,33]. A coplanar configuration has some advantages such as low dispersion, ease of attaching shunt and series circuit components, no need for via holes, or simple realization of short-circuited ends, which makes a coplanar waveguide suitable for hybrid and monolithic integrated circuits. In contrast to the microstrip and stripline, the coplanar waveguide has shielding between adjacent lines that creates a better isolation between them. However, like microstrip and stripline, the coplanar waveguide can be also described by a quasi-TEM

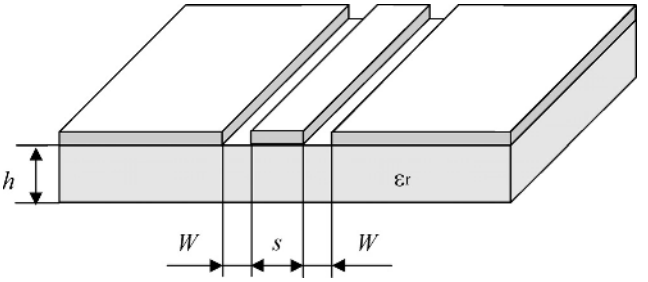

FIGURE 1.24 Coplanar waveguide structure.

approximation for both numerical and analytical calculations. Because of the high dielectric constant of the substrate, most of the RF energy is stored in the dielectric and the loading effect of the grounded cover is negligible if it is more than two slot widths away from the surface. Similarly, the thickness of the dielectric substrate with higher relative dielectric constants is not so critical, and practically it should be one or two times the width W of the slots.

The approximate expression of the characteristic impedance Z_0 for zero metal thickness which is satisfactory accurate in a wide range of substrate thicknesses can be written as

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{re}}} \frac{K(k')}{K(k)} \tag{1.171}$$

where

$$\varepsilon_{re} = 1 + \frac{\varepsilon_r - 1}{2} \frac{K(k')}{K(k)} \frac{K(k_1)}{K\left(k_1'\right)} \tag{1.172}$$

$k = s/(s + 2W)$, $k_1 = (\sinh \pi s/4h)/(\sinh \pi (s + 2W)/4h)$, $k' = \sqrt{1 - k^2}$, $k_1' = \sqrt{1 - k_1^2}$, and K is the complete elliptic integral of the first kind [34]. The values of ratios $K(k)/K(k')$ and $K(k_1)/K(k_1')$ can be defined from Eq. (1.154). Figure 1.25 shows the characteristic impedance Z_0 of a coplanar waveguide as a function of the parameter $s/(s + 2W)$ for various ε_r according to Eqs. (1.171) and (1.172).

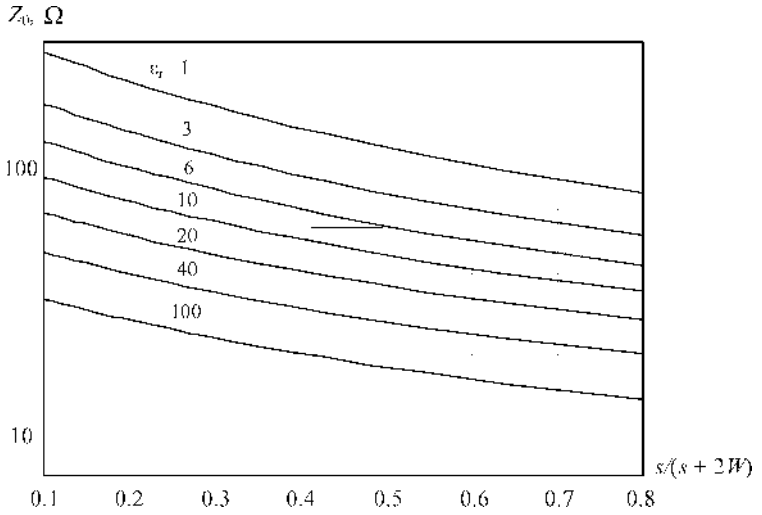

FIGURE 1.25 Coplanar waveguide characteristic impedance versus $s/(s + 2W)$.

1.9 NOISE

The electrical performance of RF and microwave transmitters of different applications can be affected by many factors, with the effect of noise as one of the most fundamental. In this case, it is necessary to keep the ratio of average (or peak) signal power to average noise power so large that the noise in a transmitter path has no harmful effects on overall system performance. Several basic approaches can provide this where it is possible, such as powerful transmitters and high-gain antennas to develop large signals at the receiver input, stabilized oscillators with minimum phase noise, power amplifier and mixer circuits so that they introduce a minimum amount of additional noise when processing signals, and modulation and coding schemes that facilitate the separation of signal and noise.

1.9.1 Noise Sources

There are several primary noise sources in the electrical circuit. *Thermal* or *white noise* is created by random motion of charge carriers due to thermal excitation, being always found in any conducting medium whose temperature is above absolute zero whatever the nature of the conduction process or the nature of the mobile charge carriers [35]. This random motion of carriers creates a fluctuating voltage on the terminals of each resistive element which increases with temperature. However, if the average value of such a voltage is zero, then the noise power on its terminal is not zero being proportional to the resistance of the conductor and to its absolute temperature. The resistor as a thermal noise source can be represented by either of the noise sources shown in Figure 1.26. The noise voltage source and noise current source can be respectively described by Nyquist equations through their mean-square noise voltage and noise current values as

$$\overline{e_{\mathrm{n}}^2} = 4kTR\Delta f \tag{1.173}$$

$$\overline{i_{\mathrm{n}}^2} = \frac{4kT\Delta f}{R} \tag{1.174}$$

where $k = 1.38 \times 10^{-23}$ J/K is the Boltzmann constant, T is the absolute temperature, and $kT = 4 \times 10^{-21}$ W/Hz $= -174$ dBm/Hz at ambient temperature $T = 290$ K. The thermal noise is proportional to the frequency bandwidth Δf, and it can be represented by the voltage source in series with resistor R, or by the current source in parallel to the resistor R. The maximum noise power can be delivered to the load when $R = R_{\mathrm{L}}$, where R_{L} is the load resistance, being equal to $kT\Delta f$. Hence, the noise power density when the noise power is normalized by Δf is independent of frequency and is considered as white noise. The root-mean-square noise voltage and current are proportional to the square root of the frequency bandwidth Δf.

Shot noise is associated with the carrier injection through the device *p-n* junction, being generated by the movement of individual electrons within the current flow. In each forward biased junction,

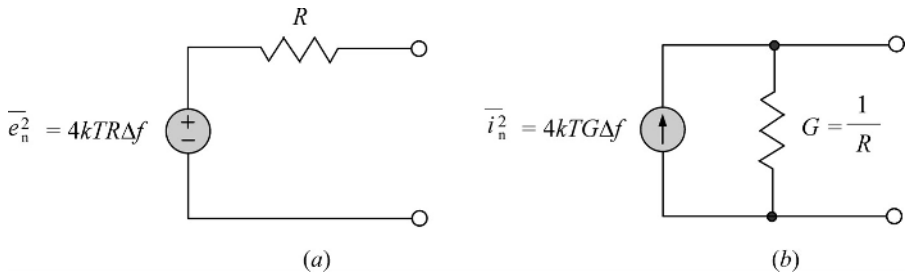

FIGURE 1.26 Equivalent circuits to represent thermal noise sources.

there is a potential barrier that can be overcome by the carriers with higher thermal energy. Such a process is random and mean-square noise current can be given by

$$\overline{i_n^2} = 2qI\Delta f \tag{1.175}$$

where q is the electron charge and I is the direct current flowing through the p-n junction. The shot noise depends on the thermal energy of the carriers near the potential barrier and its power density is independent of frequency. It has essentially a flat spectral distribution and can be treated as the thermal or white type of noise with current source $\overline{i_n^2}$ connected in parallel to the small-signal junction resistance. In a voltage noise representation, when the noise voltage source is connected in series with such a resistor, it can be written as

$$\overline{e_n^2} = 2kTr\Delta f \tag{1.176}$$

where $r = kT/qI$ is the junction resistance.

Circuits containing more than one resistor can be analyzed by reducing their number to the only one (Thevenin) equivalent resistance to obtain the mean-square noise voltage in the form of Eq. (1.173) [36]. As an example, the noise equivalent of a circuit shown in Figure 1.27(a), where a signal source V_S is driving a hypothetical noise-free load resistor R_{in} (which can be considered an input of the power amplifier) through three noise resistors R_1, R_2, and R_3, is a noise voltage source $\overline{e_n^2} = 2kTR_T\Delta f$ connected in series with an ideal (noise-free) resistor equal to the Thevenin resistance R_T, as shown in Figure 1.27(b).

Consider now a simple parallel RC circuit shown in Figure 1.28(a), where the thermal noise due to the parallel resistor is represented by a parallel noise current source i_n. Nyquist has determined the thermal noise output of a two-port network containing both resistive and reactive elements, as shown in Figure 1.28(b). In this case, the mean-square thermal noise voltage is given by

$$\overline{e_n^2} = 4kT\int_{\Delta f} R(f)\,df \tag{1.177}$$

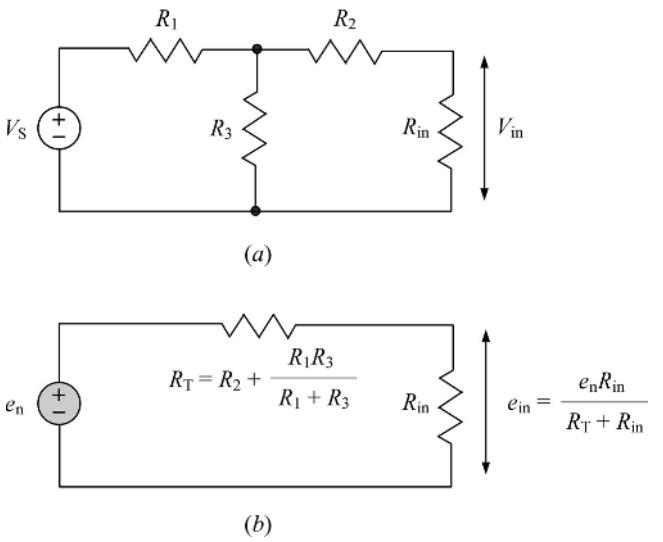

FIGURE 1.27 Circuit with three resistors and its equivalent with noise voltage source.

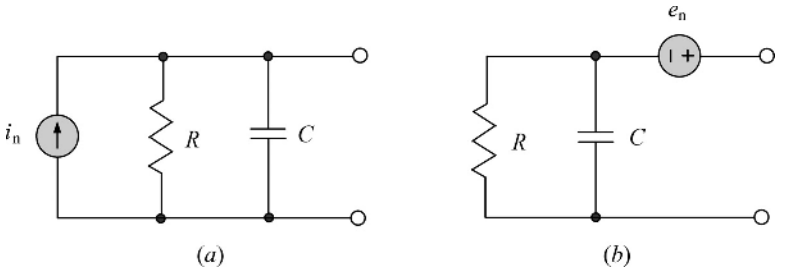

FIGURE 1.28 Noise characterization of two-port *RC* network.

where integration is performed over the frequency bandwidth of interest Δf and

$$R(f) = \frac{R}{1 + (2\pi f C R)^2} \tag{1.178}$$

is the real part of the output circuit impedance at frequency f.

Hence, the parallel current noise source can be equivalently transformed to the series noise voltage source by integration over infinite frequency bandwidth with the total mean-square noise voltage given by

$$\overline{e_n^2} = \frac{4kT}{2\pi} \int_0^\infty \frac{R d\omega}{1 + (\omega C R)^2} = \frac{2kTR}{\pi} \int_0^\infty \frac{d\omega}{1 + (\omega C R)^2} = \frac{kT}{C} \tag{1.179}$$

where the resistance R has no effect on the noise voltage which depends on the value of the capacitance C and temperature T only [36,37].

1.9.2 Noise Figure

It is well-known that any linear noisy two-port network can be represented as a noise-free two-port part with noise sources at the input and the output connected in different way [38,39]. For example, the noisy linear two-port network with internal noise sources shown in Figure 1.29(*a*) can be redrawn, either in the impedance form with external series voltage noise sources shown in Figure 1.29(*b*) or in the admittance form with external parallel current noise sources shown in Figure 1.29(*c*).

However, to fully describe the noise properties of the two-port network at fixed frequency, sometimes it is convenient to represent it through the noise-free two-port part and the noise sources equivalently located at the input. Such a circuit is equivalent to the configurations with noise sources located at the input and the output [40]. In this case, it is enough to use four parameters: the noise spectral densities of both noise sources and the real and imaginary parts of its correlation spectral density. These four parameters can be defined by measurements at the two-port network terminals. The two-port network current and voltage amplitudes are related to each other through a system of two linear algebraic equations. By taking into account the noise sources at the input and the output, these equations in the impedance and admittance forms can be respectively written as

$$V_1 = Z_{11} I_1 + Z_{12} I_2 - V_{n1} \tag{1.180}$$

$$V_2 = Z_{21} I_1 + Z_{22} I_2 - V_{n2} \tag{1.181}$$

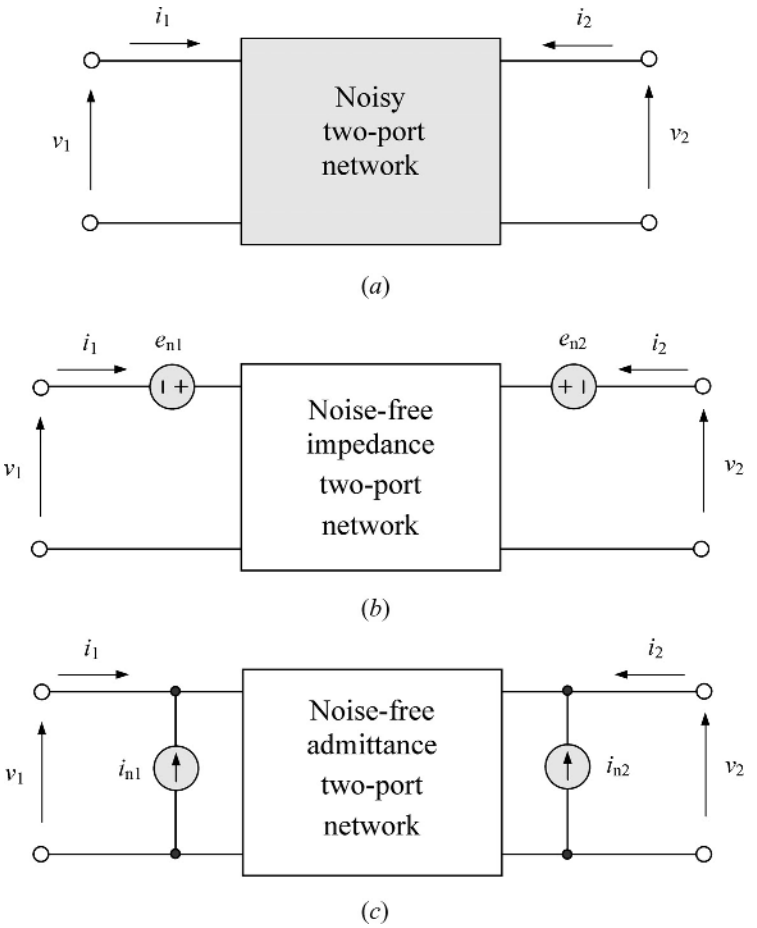

FIGURE 1.29 Linear two-port network with noise sources.

and

$$I_1 = Y_{11}V_1 + Y_{12}V_2 - I_{n1} \tag{1.182}$$

$$I_2 = Y_{21}V_1 + Y_{22}V_2 - I_{n2} \tag{1.183}$$

where the voltage and current noise amplitudes represent the Fourier transforms of noise fluctuations.

The equivalent two-port network with voltage and current noise sources located at its input is shown in Figure 1.30(a), where $[Y]$ is the two-port network admittance matrix and ratios between current and voltage amplitudes can be written as

$$I_1 = Y_{11}(V_1 + V_{ni}) + Y_{12}V_2 - I_{ni} \tag{1.184}$$

$$I_2 = Y_{21}(V_1 + V_{ni}) + Y_{22}V_2. \tag{1.185}$$

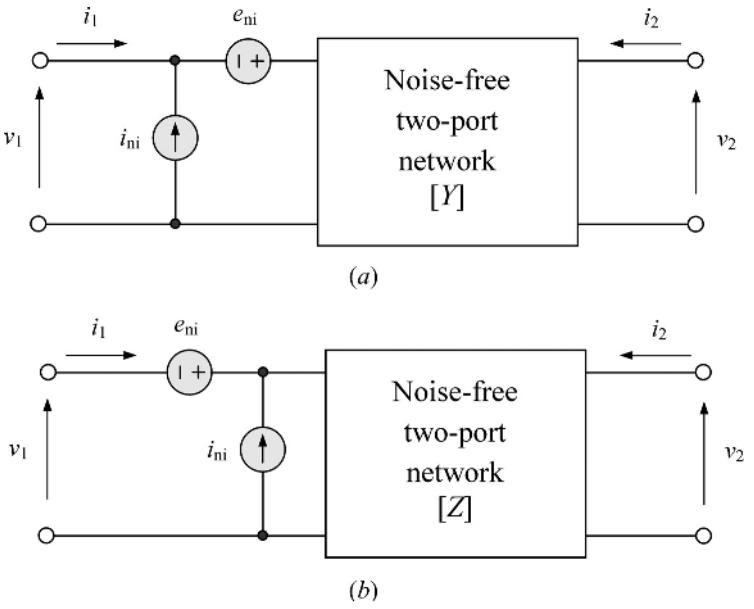

FIGURE 1.30 Linear two-port network with noise sources at input.

From comparison of Eqs. (1.182) and (1.183) with Eqs. (1.184) and (1.185) it follows that

$$V_{ni} = -\frac{I_{n2}}{Y_{21}} \tag{1.186}$$

$$I_{ni} = I_{n1} - \frac{Y_{11}}{Y_{21}} I_{n2} \tag{1.187}$$

representing the relationships between the current noise sources at the input and the output corresponding to the circuit shown in Figure 1.29(c) and the voltage and current noise sources at the input only corresponding to the circuit shown in Figure 1.30(a). In this case, Eqs. (1.186) and (1.187) are valid only if $Y_{21} \neq 0$ that always takes place in practice. Similar equations can be written for the circuit with the series noise voltage source followed by a parallel noise current source shown in Figure 1.30(b) in terms of impedance Z-parameters to represent the relationships between the voltage noise sources at the input and the output corresponding to the circuit shown in Figure 1.29(b). The use of voltage and current noise sources at the input enables the combination of all internal two-port network noise sources.

To evaluate the quality of a two-port network, it is important to know the amount of noise added to a signal passing through it. Usually, this can be done by introducing an important parameter such as a *noise figure* or *noise factor*. The noise figure of the two-port network is intended as an indication of its noisiness. The lower the noise figure, the less is the noise contributed by the two-port network. The noise figure is defined as

$$F = \frac{S_{in}/N_{in}}{S_{out}/N_{out}} \tag{1.188}$$

where S_{in}/N_{in} is the signal-to-noise ratio available at the input and S_{out}/N_{out} is the signal-to-noise ratio available at the output.

For a two-port network characterizing by the available power gain G_A, the noise figure can be rewritten as

$$F = \frac{S_{in}/N_{in}}{G_A S_{in}/G_A(N_{in} + N_{add})} = 1 + \frac{N_{add}}{N_{in}} \tag{1.189}$$

where N_{add} is the additional noise power added by the two-port network referred to the input. From Eq. (1.189) it follows that the noise figure depends on the source impedance Z_S shown in Figure 1.31(a), but not on the circuit connected to the output of the two-port network.

Hence, if the two-port network is driven from the source with impedance $Z_S = R_S + jX_S$, the noise figure F of this two-port network in terms of the model shown in Figure 1.31(b) with input voltage and current noise sources and noise-free two-port network can be obtained by

$$F = 1 + \frac{\overline{|e_n + Z_S i_n|^2}}{4kT R_S \Delta f} = 1 + \frac{R_n + |Z_S|^2 G_n + 2\sqrt{R_n G_n}\,\mathrm{Re}(C Z_S)}{R_S} \tag{1.190}$$

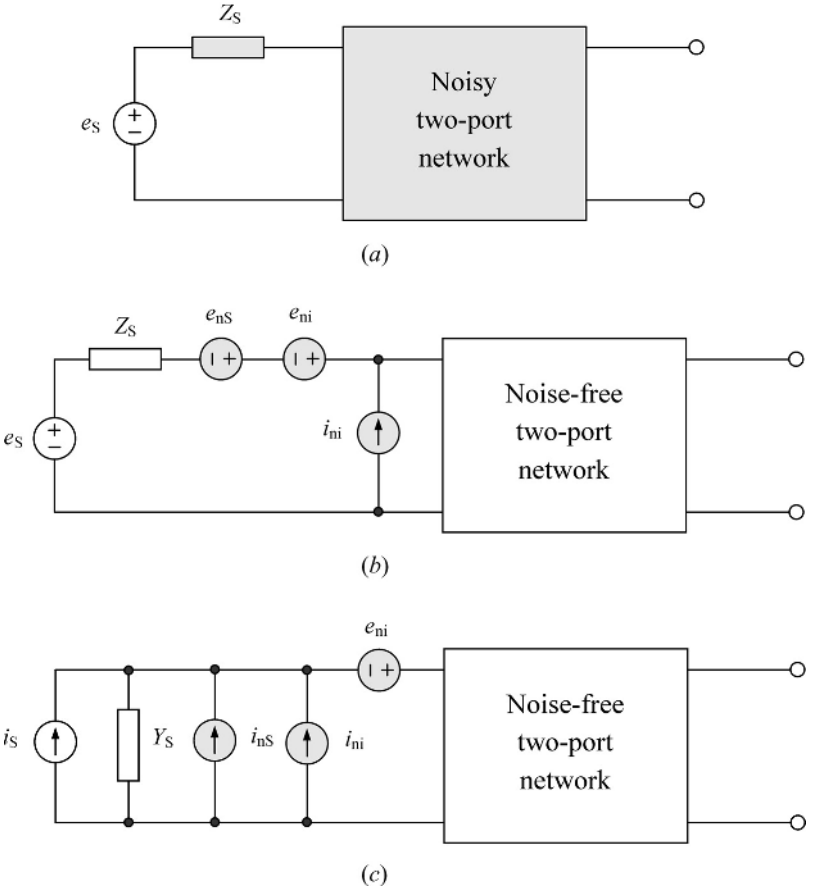

FIGURE 1.31 Linear two-port networks to calculate noise figure.

where

$$R_{\mathrm{n}} = \frac{\overline{e_{\mathrm{ni}}^2}}{4kT\,\Delta f} \tag{1.191}$$

is the equivalent input-referred noise resistance corresponding to the noise voltage source,

$$G_{\mathrm{n}} = \frac{\overline{i_{\mathrm{ni}}^2}}{4kT\,\Delta f} \tag{1.192}$$

is the equivalent input-referred noise conductance corresponding to the noise current source, and

$$C = \frac{\overline{i_{\mathrm{ni}} e_{\mathrm{ni}}^*}}{\sqrt{\overline{i_{\mathrm{ni}}^2}\,\overline{e_{\mathrm{ni}}^2}}} \tag{1.193}$$

is the correlation coefficient representing a complex number less than or equal to unity in magnitude [39]. Here, G_{n} and R_{n} generally do not represent the particular circuit immitances but depend on the bias level resulting in a dependence of the noise figure on the operating bias point of the active device.

As the source impedance Z_{S} is varied over all values with positive R_{S}, the noise figure F has a minimum value of

$$F_{\min} = 1 + 2\sqrt{R_{\mathrm{n}} G_{\mathrm{n}}}\left[\sqrt{1 - (\mathrm{Im}C)^2} + \mathrm{Re}C\right] \tag{1.194}$$

which occurs for the optimum source impedance $Z_{\mathrm{Sopt}} = R_{\mathrm{Sopt}} + jX_{\mathrm{Sopt}}$ given by

$$\left|Z_{\mathrm{Sopt}}\right|^2 = \frac{R_{\mathrm{n}}}{G_{\mathrm{n}}} \tag{1.195}$$

$$X_{\mathrm{Sopt}} = \sqrt{\frac{R_{\mathrm{n}}}{G_{\mathrm{n}}}}\mathrm{Im}C. \tag{1.196}$$

As a result, the noise figure F for the input impedance Z_{S} which is not optimum can be expressed in terms of $F_{\min}$ as

$$F = F_{\min} + \left|Z_{\mathrm{S}} - Z_{\mathrm{Sopt}}\right|^2 \frac{G_{\mathrm{n}}}{R_{\mathrm{S}}} = F_{\min} + \left[\left(R_{\mathrm{S}} - R_{\mathrm{Sopt}}\right)^2 + \left(X_{\mathrm{S}} - X_{\mathrm{Sopt}}\right)^2\right]\frac{G_{\mathrm{n}}}{R_{\mathrm{S}}}. \tag{1.197}$$

Similarly, the noise figure F can be equivalently expressed using a model shown in Figure 1.31(c) with source admittance $Y_{\mathrm{S}} = G_{\mathrm{S}} + jB_{\mathrm{S}}$ as

$$F = F_{\min} + \left|Y_{\mathrm{S}} - Y_{\mathrm{Sopt}}\right|^2 \frac{R_{\mathrm{n}}}{G_{\mathrm{S}}} = F_{\min} + \left[\left(G_S - G_{\mathrm{Sopt}}\right)^2 + \left(B_S - B_{\mathrm{Sopt}}\right)^2\right]\frac{R_{\mathrm{n}}}{G_{\mathrm{S}}} \tag{1.198}$$

where $F_{\min}$ is the minimum noise figure of the two-port network which can be realized with respect to the source admittance Y_{S}, $Y_{\mathrm{Sopt}} = G_{\mathrm{Sopt}} + jB_{\mathrm{Sopt}}$ is the optimal source admittance, and R_{n} is the equivalent noise resistance which measures how rapidly the noise figure degrades when the source admittance Y_{S} deviates from its optimum value Y_{Sopt} [41]. Since the admittance Y_{S} is generally complex, then its real and imaginary parts can be controlled independently. To obtain the minimum value of the noise figure, the two matching conditions of $G_{\mathrm{S}} = G_{\mathrm{Sopt}}$ and $B_{\mathrm{S}} = B_{\mathrm{Sopt}}$ must be satisfied.

The physical interpretation of the noise sources which are assumed to be stationary random processes is given by their self- and cross-power spectral densities which are defined as the Fourier

transform of their auto- and cross-correlation function. These spectral densities in two-port matrix form leads to the so-called correlation matrices with their admittance, impedance, or chain representations [42]. The correlation matrix C belonging to the noise sources s_{n1} and s_{n2} can be written as

$$C = \frac{1}{\Delta f}\begin{bmatrix} \overline{s_{n1}s_{n1}^*} & \overline{s_{n1}s_{n2}^*} \\ \overline{s_{n2}s_{n1}^*} & \overline{s_{n2}s_{n2}^*} \end{bmatrix} \tag{1.199}$$

where the asterisk denotes the complex conjugate. For example, the admittance correlation matrix for the circuit shown in Figure 1.29 (c) with two parallel current noise sources is obtained as

$$C_Y = \frac{1}{\Delta f}\begin{bmatrix} \overline{i_{n1}i_{n1}^*} & \overline{i_{n1}i_{n2}^*} \\ \overline{i_{n2}i_{n1}^*} & \overline{i_{n2}i_{n2}^*} \end{bmatrix}. \tag{1.200}$$

Determination of the noise correlation matrix is based on the following procedure:

- Each element in the diagonal matrix is equal to the sum of the noise current of each element connected to the corresponding node: the first diagonal element is the sum of noise currents connected to the node 1, while the second diagonal element is the sum of noise currents connected to node 2.
- The off-diagonal elements are the negative noise current of the element connected to the pair of the corresponding node; therefore, a noise current source between nodes 1 and 2 goes into the matrix at locations (1, 2) and (2, 1).
- If a noise current source is grounded, it will only contribute to one entry in the noise correlation matrix—at the appropriate location on the diagonal; if it is not grounded, it will contribute to four entries in the matrix—two diagonal entries corresponding to the two nodes and two off-diagonal entries.

By applying these rules for the circuit with two current noise sources shown in Figure 1.32, the admittance noise correlation matrix C_Y can be defined as

$$C_Y = \frac{1}{\Delta f}\begin{bmatrix} \overline{i_{n1}^2} & -\overline{i_{n1}^2} \\ -\overline{i_{n1}^2} & \overline{i_{n1}^2} + \overline{i_{n2}^2} \end{bmatrix}. \tag{1.201}$$

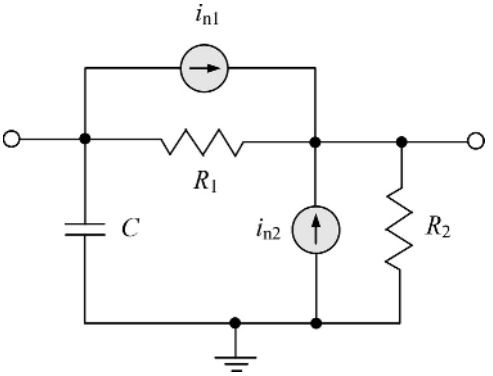

FIGURE 1.32 Circuit with two noise current sources.

To form the impedance noise correlation matrix with voltage noise sources, we can write

$$C_{\mathrm{Z}} = \frac{1}{\Delta f}\begin{bmatrix} \overline{e_{\mathrm{n1}} e_{\mathrm{n1}}^*} & \overline{e_{\mathrm{n1}} e_{\mathrm{n2}}^*} \\ e_{\mathrm{n2}} e_{\mathrm{n1}}^* & e_{\mathrm{n2}} e_{\mathrm{n2}}^* \end{bmatrix} = [Z]\,[C_{\mathrm{Y}}]\,[Z]^{\mathrm{T}} \tag{1.202}$$

where $[Z]$ is the impedance Z-matrix of the two-port network and T denotes the Hermitian or transposed conjugation.

In the case where the correlation matrix cannot be theoretically derived, the measurements can be used for its determination. Such measurements are usually done by defining the equivalent noise resistance R_{n}, the optimal source admittance Y_{Sopt}, and the minimum noise figure F_{min}. As a result, the chain representation of the noise correlation matrix is obtained as

$$C_{\mathrm{A}} = 4kT\begin{bmatrix} R_{\mathrm{n}} & \dfrac{F_{\mathrm{min}}-1}{2} - R_{\mathrm{n}} Y_{\mathrm{Sopt}} \\ \dfrac{F_{\mathrm{min}}-1}{2} - R_{\mathrm{n}} Y_{\mathrm{Sopt}}^* & R_{\mathrm{n}} \left|Y_{\mathrm{Sopt}}\right|^2 \end{bmatrix} \tag{1.203}$$

where T is the absolute temperature [42]. If the correlation matrix has been determined, the noise parameters can be calculated analytically from

$$R_{\mathrm{n}} = \frac{C_{11}^{\mathrm{A}}}{4kT} \tag{1.204}$$

$$Y_{\mathrm{Sopt}} = \sqrt{\frac{C_{22}^{\mathrm{A}}}{C_{11}^{\mathrm{A}}} - \mathrm{Im}^2\left(\frac{C_{12}^{\mathrm{A}}}{C_{11}^{\mathrm{A}}}\right)} - j\mathrm{Im}\left(\frac{C_{12}^{\mathrm{A}}}{C_{11}^{\mathrm{A}}}\right) \tag{1.205}$$

$$F_{\mathrm{min}} = 1 + \frac{C_{12}^{\mathrm{A}} + C_{11}^{\mathrm{A}} Y_{\mathrm{Sopt}}}{2kT}. \tag{1.206}$$

where C_{11}^{A}, C_{12}^{A}, C_{21}^{A}, and C_{22}^{A} are the elements of the chain correlation matrix C_{A}.

In a multistage transmitter system, the input signal travels through a cascade of many different components, each of which may degrade the signal-to-noise ratio to some degree. For a cascade of two stages having available gains G_{A1} and G_{A2} and noise figures F_1 and F_2, using Eq. (1.189) results in the output-to-input noise power ratio $N_{\mathrm{out}}/N_{\mathrm{in}}$ written as

$$\frac{N_{\mathrm{out}}}{N_{\mathrm{in}}} = G_{\mathrm{A2}}\left[G_{\mathrm{A1}}\left(1 + \frac{N_{\mathrm{add1}}}{N_{\mathrm{in}}}\right) + \frac{N_{\mathrm{add2}}}{N_{\mathrm{in}}}\right] = G_{\mathrm{A1}} G_{\mathrm{A2}}\left(F_1 + \frac{F_2 - 1}{G_{\mathrm{A1}}}\right) \tag{1.207}$$

where N_{add1} and N_{add2} are the additional noise powers added by the first and second stages, respectively. Consequently, an overall noise figure $F_{1,2}$ for a two-stage system based on Eq. (1.188) can be given by

$$F_{1,2} = F_1 + \frac{1}{G_{\mathrm{A1}}}(F_2 - 1). \tag{1.208}$$

Eq. (1.208) can be generalized to a multistage transmitter system with n stages as

$$F_{1,\mathrm{n}} = F_1 + \frac{F_2 - 1}{G_{\mathrm{A1}}} + \cdots + \frac{F_{\mathrm{n}} - 1}{G_{\mathrm{A1}} G_{\mathrm{A2}} \ldots G_{\mathrm{A(n-1)}}} \tag{1.209}$$

which means that the noise figure of the first stage has the predominant effect on the overall noise figure, unless G_{A1} is small or F_2 is large [43].

1.9.3 Flicker Noise

The flicker or 1/*f* noise is a low-frequency noise associated with a fluctuation in the conductance with a power spectral density proportional to $f^{-\gamma}$, where $\gamma = 1.0 \pm 0.1$ in a wide frequency range, usually measured from 1 Hz to 10 kHz [44]. Its spectrum cannot be exactly f^{-1} at offset frequencies from $f = 0$ to $f \to \infty$, since neither the integral over the power density nor the Fourier transform would be able to have finite values. Unlike the thermal or shot noise sources, the origin of the 1/*f* noise is not exactly clear and open to debate despite its predictable behavior. Generally, it is a result of both surface and bulk effects in the semiconductor material and is not generated by the current. In series experiments it was shown that there is a type of 1/*f* noise that is a fluctuation in the carrier mobility due to lattice scattering.

Significant contribution to the low-frequency noise is made by the generation-recombination and burst noises [45]. The generation-recombination noise associated with the fluctuations in the number of the carriers rather than their mobility is due to trap centers within the bandgap of a semiconductor. It may have any frequency behavior between f^0 and f^{-2}. If not masked by thermal noise, the low-frequency noise generated from these trap centers becomes f^{-2} at very high frequencies. However, if the lifetime of the carriers in the semiconductor is finite, the noise spectral density reaches a plateau at very low frequencies. Burst noise (random telegraph noise) is a special kind of generation-recombination noise due to a single trap in the active device region. It is often observed in submicron devices or in devices with very poor crystalline quality. In such devices, a trap level with certain energy and at a specific location in the active device region (a single localized trap) traps and detraps the carriers causing an on-off time-dependent signal similar to a telegraph signal [46].

The physical origin of a low-frequency 1/*f* noise for any type of the metal-oxide-semiconductor field-effect transistor (MOSFET) devices including CMOS transistors is based on two dominant processes: random fluctuation of the carriers in the channel due to fluctuations in the surface potential caused by trapping and releasing of the carriers by traps located near the Si–SiO_2 interface, and mobility fluctuations due to carrier interactions with lattice fluctuations [47]. However, for a CMOS transistor depending on its type, one effect can prevail over the other. For example, flicker noise in *n*-channel devices is mostly attributed to carrier number fluctuations, while flicker noise in *p*-channel devices is often attributed to mobility fluctuations. It was observed that pMOS transistors have significantly lower 1/*f* noise than nMOS transistors of the same size and fabricated with the same CMOS process (by one order of magnitude or more). This is because, when an n^+-polysilicon gate layer is used for both the nMOS and pMOS devices, nMOS transistors have a surface channel while pMOS transistors have a buried channel [48].

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