Chapter 1

Introduction to Power Inverters

Dc-ac power converters are part of the general power electronic converters family and are designed and operated to convert electric energy from one stage voltage, current, and/or frequency to another. Dc-ac converters, as with other power electronic converters, are composed of groups of semiconductor switching elements and are operated in a particular sequential manner to produce outputs with predefined specifications (voltage, current, and/or frequency). In general, power electronic converters operate by switching their elements in either full ON or full OFF modes in a sequential periodic manner to meet sets of predefined conditions on the output stage. The dc-ac converter is usually called the inverter. Hence, the term *dc-ac converter* will be replaced by simply *the inverter* in this book.

Inverters have gained ever-increasing popularity in a wide range of industrial applications, including ac motor drives, control systems, power supplies, uninterruptible power supply (UPS) systems, power quality, power systems, and renewable energy utilization. The majority of these applications utilize sets of conditions to ensure acceptable levels of power quality. Such sets of conditions for power quality have become standards for allowable levels of harmonic generation and distortion in inverter outputs. As a consequence, inverter performance been pushed toward modes of operation that has meet the standards imposed for output quality.

1.1 FUNDAMENTAL INVERTER TOPOLOGIES

Inverters are composed of groups of semiconductor switching elements such as the insulated gate bipolar transistor (IGBT), metal-oxide-semiconductor field–effect transistor (MOSFET), and bipolar junction transistor (BJT). These switching elements can be represented by a resistance R_C such that:

$$OFF \Rightarrow R_C \rightarrow \infty \tag{1.1}$$

$$ON \Rightarrow R_C \rightarrow 0 \tag{1.2}$$

An Introduction to Wavelet Modulated Inverters, by S.A. Saleh and M. Azizur Rahman

The connection of switching elements for constructing inverters must meet the rules of basic circuit theory, in particular, transient operating conditions. Such conditions impose the following two basic constraints on the operation of switching elements in inverters:

1. A switching element is not to be connected in series with a current source (an inductive element). This is required to ensure a finite voltage across the switching element during status change (i.e., ON to OFF or OFF to ON). Generally, any combination of ON and OFF switching elements should never open-circuit an inductor.
2. A switching element is not to be connected in parallel with a voltage source (a capacitive element). This ensures a finite current through the switching element during status change. The general rule, therefore, is that any combination of ON and OFF switching elements should never short-circuit a capacitor.

Inverters can be voltage-source (VS) inverters (e.g. a dc voltage is used on the input side), or current-source (CS) inverters (e.g. a dc current is used on the input side). In general, inverters are categorized into two main types:

1. Single-phase (1ϕ) inverters
2. Three-phase (3ϕ) inverters

1.1.1 Single-Phase (1ϕ) Inverters

There are two common topologies for single-phase (1ϕ) inverters known as the half-bridge or the center-tapped and the full-bridge or the *H*-bridge topologies. The first topology of 1ϕ inverters is the half-bridge or the center-tapped inverters. Figure 1.1 shows a schematic diagram for the half-bridge 1ϕ inverter along with the switching and output voltage waveforms. The basic operation of the half-bridge inverter can be represented by defining sets of switching functions so that:

$$OFF \Rightarrow 0 \tag{1.3}$$

$$ON \Rightarrow 1 \tag{1.4}$$

These sets of switching functions are capable of defining the output of the inverter as a function of the switching actions. The output voltage waveform shown in Figure 1.1 can be described by the following equation as:

$$v_0(t) = \frac{V_{DC}}{2}(Q_1(t) - Q_2(t)) \tag{1.5}$$

where $Q_1(t)$ and $Q_2(t)$ are switching actions of the switching elements Q_1 and Q_2, respectively. Because Q_1 and Q_2 cannot be ON at the same time, as well as for continuous output current, the relation between $Q_1(t)$ and $Q_2(t)$ can be stated as:

$$Q_1(t) + Q_2(t) = 1 \tag{1.6}$$

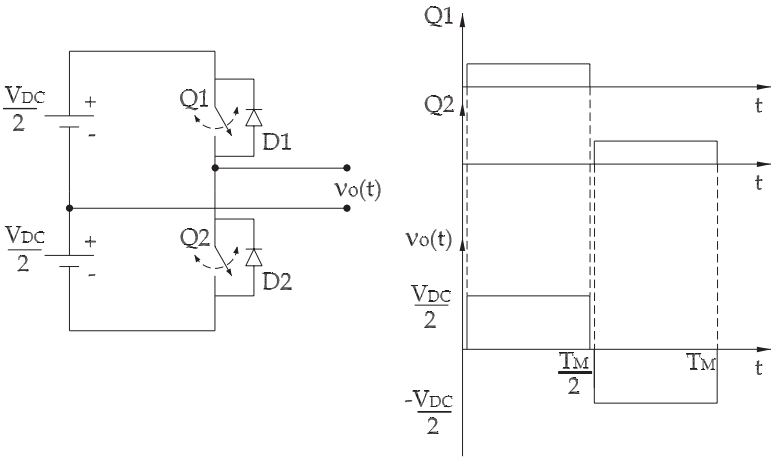

Figure 1.1 Schematic diagram of the half-bridge 1ϕ inverter along with switching and output waveforms.

This provides the output voltage as a function of the switching actions as:

$$v_0(t) = \frac{V_{DC}}{2}(2Q_1(t) - 1) \tag{1.7}$$

The output voltage of the half-bridge inverter $v_o(t)$ has a root mean square (RMS) value given as:

$$(v_0)_{RMS} = \left(\frac{2}{T_M}\int_0^{\frac{T_M}{2}} \frac{V_{DC}^2}{4} dt\right)^{\frac{1}{2}} = \frac{V_{DC}}{2} \tag{1.8}$$

The second topology of 1ϕ inverters is the full-bridge or the *H*-bridge that has two single-phase legs of the same type. This inverter topology is preferred in high power applications due to the fact that the output voltage is twice that of the half-bridge inverter. Also, the current flowing in each switch is half the current that flows in each switch of the half-bridge inverter. Figure 1.2 shows a schematic diagram for the full-bridge or the *H*-bridge inverter along with the switching and the output voltage waveforms. The output voltage waveform shown in Figure 1.2 can be described as:

$$V_A(t) = \frac{V_{DC}}{2}(Q_1(t) - Q_4(t)) \tag{1.9}$$

$$V_B(t) = \frac{V_{DC}}{2}(Q_3(t) - Q_2(t)) \tag{1.10}$$

where $Q_1(t)$, $Q_2(t)$, $Q_3(t)$, and $Q_4(t)$ are switching actions of the switching elements Q_1, Q_2, Q_3, and Q_4, respectively. Since Q_1 and Q_4 or Q_3 and Q_2 cannot be ON at the same time as continuous output current, the relation between $Q_1(t)$, $Q_2(t)$, $Q_3(t)$, and $Q_4(t)$ can be stated as:

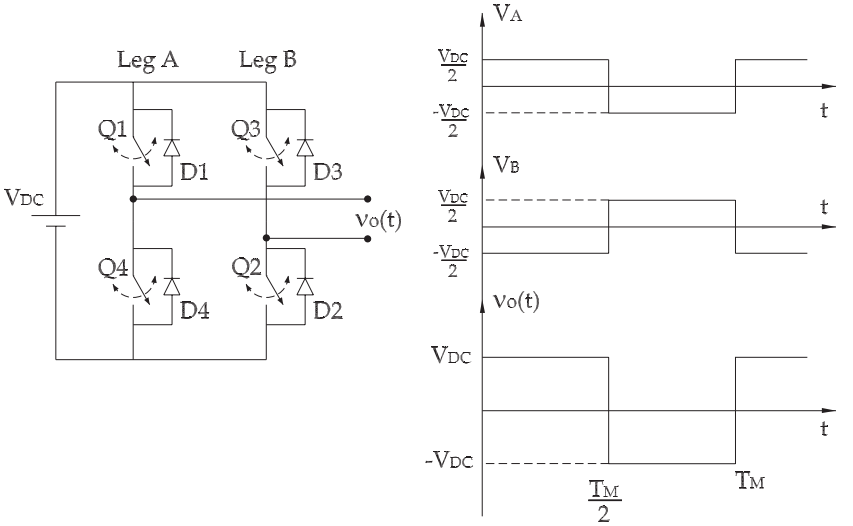

Figure 1.2 Schematic diagram of the full-bridge (*H*-bridge) 1ϕ inverter and the voltage waveforms. The output voltage is $v_o(t) = V_A(t) - V_B(t)$.

$$Q_1(t) + Q_4(t) = 1 \tag{1.11}$$

$$Q_3(t) + Q_2(t) = 1 \tag{1.12}$$

This can provide the output voltages as functions of the switching actions as:

$$V_A(t) = \frac{V_{DC}}{2}(2Q_1(t) - 1) \tag{1.13}$$

$$V_B(t) = \frac{V_{DC}}{2}(2Q_3(t) - 1) \tag{1.14}$$

The output voltage of the full-bridge inverter $v_o(t)$ can be expressed as:

$$v_o(t) = V_{DC}(Q_1(t) - Q_3(t)) \tag{1.15}$$

The output voltage of the full-bridge inverter $v_o(t)$ has an RMS value given as:

$$(v_o)_{RMS} = \left(\frac{2}{T_M}\int_0^{\frac{T_M}{2}} V_{DC}^2 dt\right)^{\frac{1}{2}} = V_{DC} \tag{1.16}$$

1.1.2 Three-Phase (3ϕ) Inverters

Three-phase inverters are used for variable-frequency drive applications and for high power applications such as HVDC power transmission. The conventional three-phase inverter consists of three single-phase legs, each connected to one phase on the output side. The fundamental operation of the three legs is coordinated so that

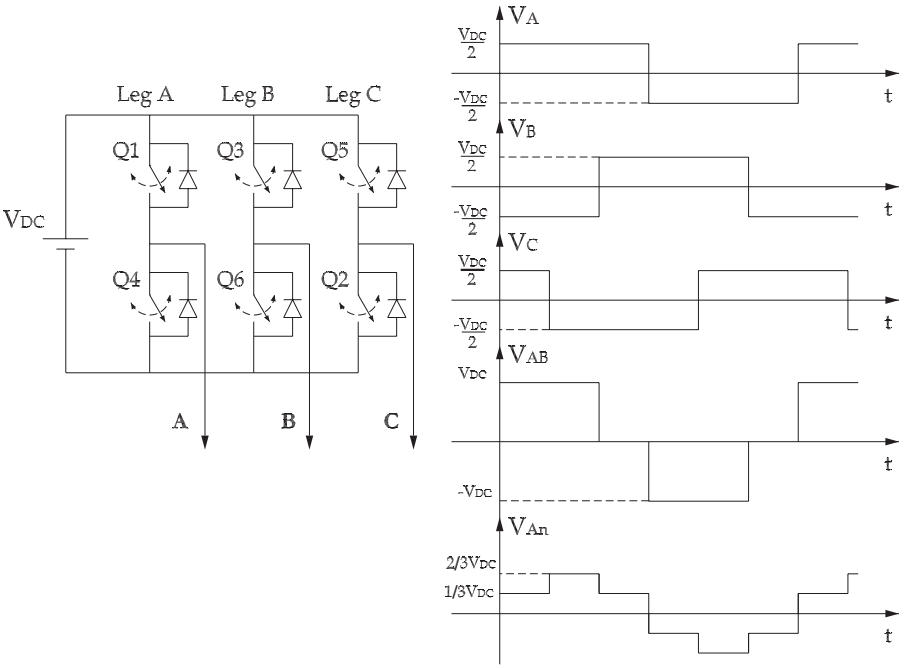

Figure 1.3 Schematic diagrams of the three-phase (3ϕ) inverter and the output voltage waveforms.

one switch operates at each 60-degree point of the fundamental output waveform. This creates a line-to-line output waveform that has six steps. The six-step waveform has a zero-voltage step between the positive and negative sections of the square-wave such that the harmonics that are multiples of three are eliminated. Note that switching elements of 3ϕ inverters can be operated in the 180-degree-conduction and the 120-degree-conduction. Figure 1.3 shows the schematic diagram of the 3ϕ inverter along with the switching and output waveforms for the 180-degree-conduction operation. The output voltage waveforms across each leg shown in Figure 1.3 can be described as:

$$V_A(t) = \frac{V_{DC}}{2}(Q_1(t) - Q_4(t)) \tag{1.17}$$

$$V_B(t) = \frac{V_{DC}}{2}(Q_3(t) - Q_6(t)) \tag{1.18}$$

$$V_C(t) = \frac{V_{DC}}{2}(Q_5(t) - Q_2(t)) \tag{1.19}$$

where $Q_1(t)$, $Q_2(t)$, $Q_3(t)$, $Q_4(t)$, $Q_5(t)$, and $Q_6(t)$ are switching actions of the switching elements Q_1, Q_2, Q_3, Q_4, Q_5, and Q_6, respectively. Since Q_1 and Q_4, Q_3, and Q_6, and

Q_5 and Q_2 cannot be ON at the same time as continuous output current, the following relations can be stated:

$$Q_1(t)+Q_4(t)=1 \tag{1.20}$$

$$Q_3(t)+Q_6(t)=1 \tag{1.21}$$

$$Q_5(t)+Q_2(t)=1 \tag{1.22}$$

This can provide the leg voltages as functions of the switching actions as:

$$V_A(t)=\frac{V_{DC}}{2}(2Q_1(t)-1) \tag{1.23}$$

$$V_B(t)=\frac{V_{DC}}{2}(2Q_3(t)-1) \tag{1.24}$$

$$V_C(t)=\frac{V_{DC}}{2}(2Q_5(t)-1) \tag{1.25}$$

The output line-to-line voltages of the 3ϕ inverter can be expressed as:

$$v_{AB}(t)=V_A(t)-V_B(t)=V_{DC}(Q_1(t)-Q_3(t)) \tag{1.26}$$

$$v_{BC}(t)=V_B(t)-V_C(t)=V_{DC}(Q_3(t)-Q_5(t)) \tag{1.27}$$

$$v_{CA}(t)=V_C(t)-V_A(t)=V_{DC}(Q_5(t)-Q_1(t)) \tag{1.28}$$

The inverter topologies are very popular for widespread applications in different industrial sectors. The demand for utilizing inverters in industrial applications with high power has pushed toward developing new inverter topologies with high power ratings. Such topologies are characterized by power levels, output quality, switching elements, and diversity of topological designs and structures. These inverter topologies have created a new family of inverters called multi-level inverters.

1.2 MULTILEVEL INVERTER TOPOLOGIES

The conventional inverter topologies operation is based on switching each leg to positive, zero, and negative voltage levels (the same applies for current source inverters (CSI)). Such inverter topology can be limited to the current as well as voltage ratings of the switching elements used for high power applications. One of the latest approaches to overcome such inverter limitations is through increasing the number of voltage levels (or current levels in CSI) on the output side of the inverter. This has lead to the concept of multi-level inverters. It is worth mentioning that the concept of multilevel inverters is applicable for both 1ϕ and 3ϕ inverters, however, the majority of multilevel inverters are designed as 3ϕ ones.

1.2.1 Neutral-Point Clamped Multilevel Inverter

The first multilevel inverter was the 3ϕ neutral-point clamped (NPC) inverter that has a zero-voltage center point, which can be switched to output phases. The switching of the zero-voltage points to the output phases made it possible to switch each inverter leg to three levels of voltage. Figure 1.4 shows a schematic diagram of a 3ϕ three-level VS NPC inverter. One of the advantages of the NPC multilevel inverters is that they have twice the number of the switching elements as the six-pulse 3ϕ inverters, where each switching element blocks only half the dc bus voltage. Also, the increase in the number of switching elements guarantees a reduced switch utilization.

The purpose of producing different levels of voltage is to sequentially activate only two switching elements in each leg. For the three-level NPC inverter shown in Figure 1.4, the output voltages can be expressed as functions of the switching actions:

$$v_{AB}(t) = V_A(t) - V_B(t) = V_{DC}(Q_{a1}(t) - Q_{a3}(t) - Q_{b1}(t) + Q_{b3}(t)) \tag{1.29}$$

$$v_{BC}(t) = V_B(t) - V_C(t) = V_{DC}(Q_{b1}(t) - Q_{b3}(t) - Q_{c1}(t) + Q_{c3}(t)) \tag{1.30}$$

$$v_{CA}(t) = V_C(t) - V_A(t) = V_{DC}(Q_{c1}(t) - Q_{c3}(t) - Q_{a1}(t) + Q_{a3}(t)) \tag{1.31}$$

The aforementioned equations for the output line-to-line voltages indicate that each one of the three voltages can have $\pm 2V_{DC}$, $\pm V_{DC}$, or zero. Figure 1.5 shows the output voltage waveforms for the leg A voltage, line-to-line voltage, and line-to-neutral voltage.

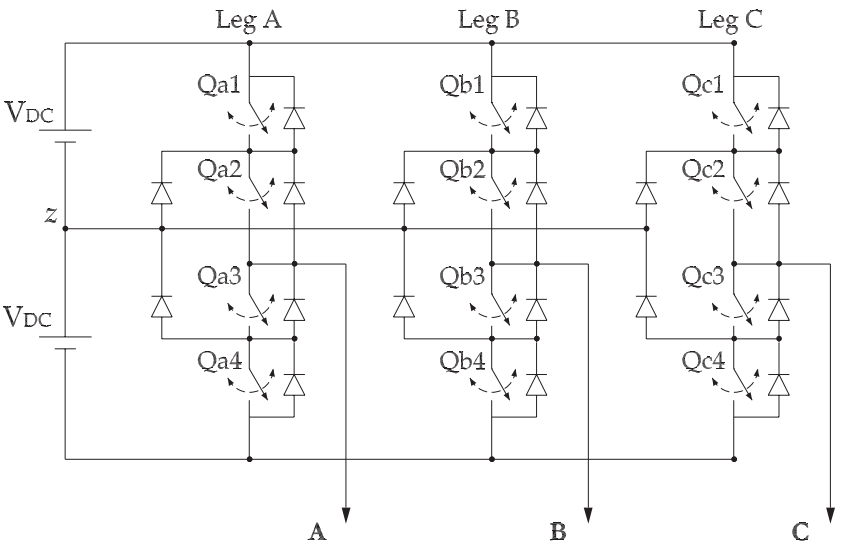

Figure 1.4 Schematic diagram of a 3ϕ three-level voltage source (VS) neutral-point clamped (NPC) inverter.

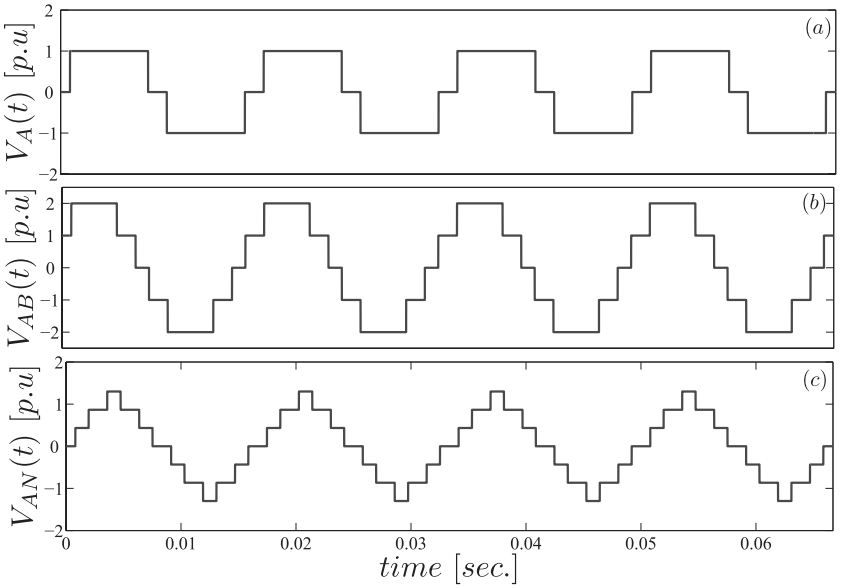

Figure 1.5 The three-level NPC inverter output voltages: (a) the NPC inverter per-unit leg A output voltage V_A, (b) the NPC inverter per-unit line-to-line output voltage V_{AB}, and (c) the NPC inverter per-unit line-to-neutral output voltage V_{AN}. The voltage base value is the dc voltage V_{DC}.

1.2.2 Diode-Clamped Multilevel Inverter

Diode-clamped multilevel (DCM) inverters extend the concept of several levels of the output voltage achieved using the NPC inverters. These inverters use diodes to limit the voltage stress across the switching elements so that different levels of voltage can be produced on the inverter output. The basic structure of the DCM inverter utilizes switching elements connected in series with their respective main diodes. All are connected in parallel with the clamping diodes. In each leg of the inverter, the forward voltage across each switching element is clamped by the connection of diodes between switching elements and the nodes. Figure 1.6 shows a schematic diagram of a 3ϕ four-level VS DCM inverter.

Note that each active switching element blocks one level of the dc bus voltage. However, the clamping diodes may block a voltage higher than the one blocked by the switching element, indicating that their ratings for reverse voltage blocking need to be set adequately.

1.2.3 Capacitor-Clamped Multilevel Inverter

The capacitor-clamped multilevel (CCM) inverter offers the same advantages as both NPC and DCM inverters in the ability to produce output voltages with different levels. However, the CCM inverter offers additional operational advantages that

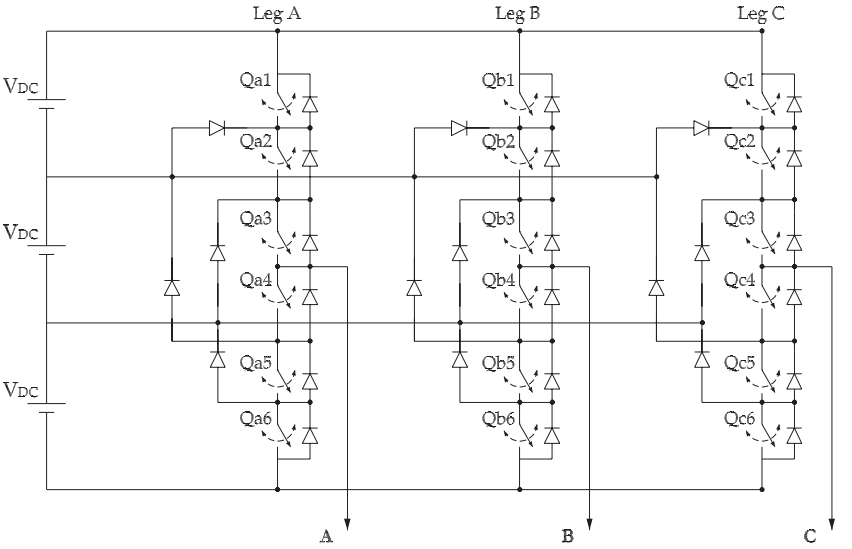

Figure 1.6 Schematic diagram of a 3ϕ four-level voltage source (VS) diode-clamped multilevel (DCM) inverter.

include lower cost and higher efficiency due to the fact that fewer diodes are used. The operation of this inverter topology can be simply described as follows: the capacitors in each leg are charged to different voltage levels. Figure 1.7 shows a schematic diagram of a 3ϕ four-level VS CCM inverter.

A combination of ON switching elements allows different voltages from different capacitors to synthesize the output voltage. The voltage waveforms shown in Figure 1.5 can be obtained using a three-level VS capacitor-clamped multilevel inverter.

1.2.4 Cascaded *H*-Bridge Multilevel Inverter

The cascaded single-phase *H*-bridge multilevel inverter uses different single-phase *H*-bridge ones, each with an independent dc voltage source. The different legs of a cascaded *H*-bridge multilevel inverter can have different levels of voltage that are switched by the individual 1ϕ *H*-bridge inverters, where three levels of voltage (V_{DC}, 0, and $-V_{DC}$) can be obtained. The ac outputs of the 1ϕ *H*-bridge inverters in each leg are connected in series such that the synthesized voltage waveform is the sum of the *H*-bridge inverters' outputs. Figure 1.8 shows a schematic diagram of a 3ϕ five-level VS cascaded single-phase *H*-bridge multilevel inverter.

The general rule for the number of levels in the output phase-to-neutral voltage VS cascaded single-phase *H*-bridge multilevel inverter is stated as:

$$m = 2s + 1 \tag{1.32}$$

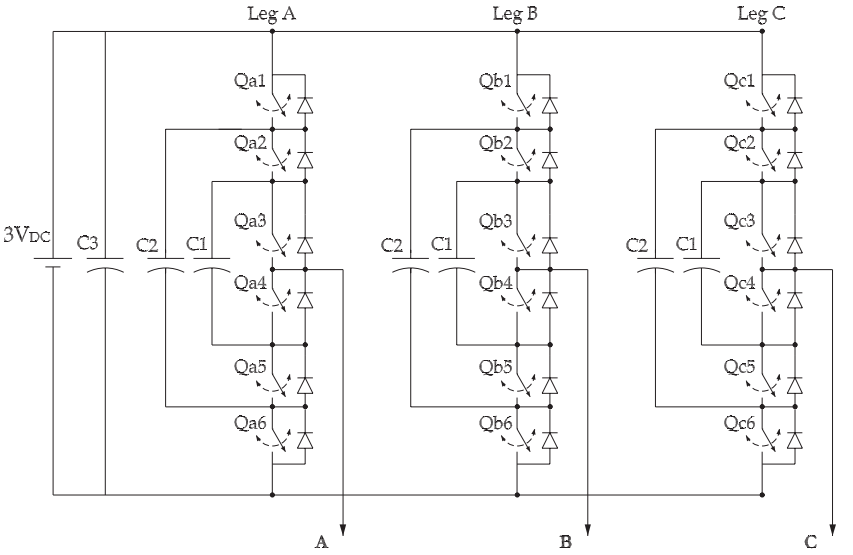

Figure 1.7 Schematic diagram of a 3ϕ four-level voltage source (VS) capacitor-clamped multilevel (CCM) inverter.

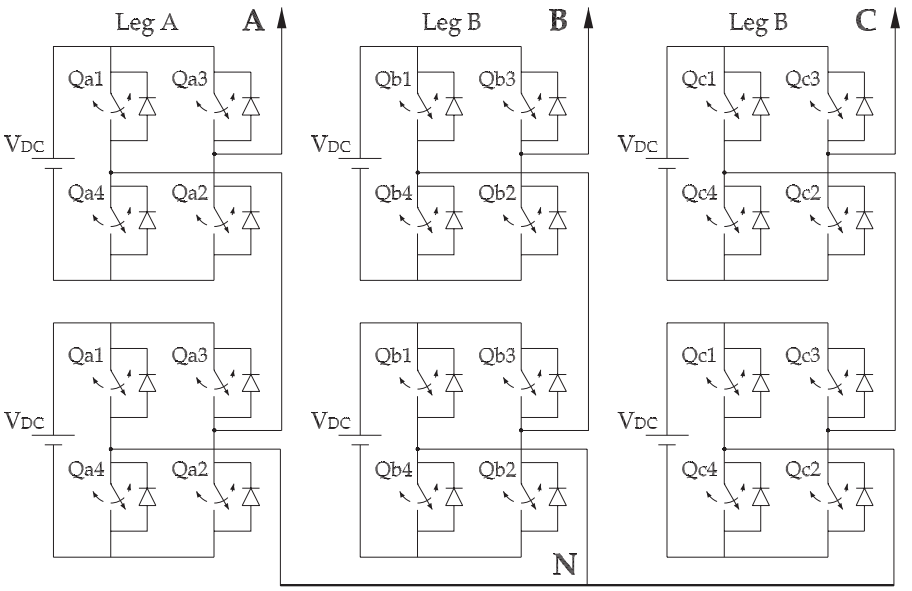

Figure 1.8 Schematic diagram of a 3ϕ four-level voltage source (VS) cascaded single-phase *H*-bridge multilevel inverter.

where m is the number of voltage levels and s is the number of dc voltage supplies. The main advantages of the cascaded single-phase H-bridge multilevel inverter are its ability to offer improved regulation of the dc bus voltage and its structure, which is modular to simplify control as well as maintenance.

There are other topologies for multilevel inverters that are mostly based on hybrid combinations of the aforementioned multilevel inverters. Furthermore, these hybrid multilevel inverters are designed and operated to meet specific conditions required by certain applications. Among these hybrid multilevel inverters are the generalized multilevel topology, the mixed-level hybrid multilevel topology, soft-switched multilevel topology, and the back-to-back diode-clamped multilevel topology.

1.3 FUNDAMENTAL INVERTER SWITCHING

The principle of inverter operation is thoroughly discussed in the literature. Inverter operation coordinates the states of all switching elements and ensures their compliance with fundamental conditions for switching circuits. These conditions are required to avoid creating short circuits across the dc supply and to provide each switching element with the required time for changing its status from ON to OFF or OFF to ON. Adherence to these conditions by certain sequential switching method produces ac outputs. However, outputs of these inverters contain different frequency components in addition to the desired fundamental frequency component. Such frequency components can create undesired features in the ac outputs as well as various levels of operational imperfections.

Concerns about inverter output quality, which reflects the amount of output energy distributed in the harmonic frequencies, have been a challenging issue since the first application of inverters as power conditioners. subsequently, operating inverters employing various switching strategies to reduce the output harmonic generation and distortion have been a topic for intensive research. The main objectives of such research are to develop and test switching techniques capable of operating inverters to produce outputs with high quality over wide ranges of loading conditions. These objectives can be interpreted as concentrating as much energy of the inverter output as possible in the desired frequency component. Two fundamental strategies have been developed to operate both 1ϕ and 3ϕ inverters that are the square-wave and multi-switching strategies. Figure 1.9 shows waveforms for an inverter output operated using both the square-wave and multiswitching strategies. The spectra of the inverter outputs of Figure 1.9 are shown in Figure 1.10. The multiswitching strategy has been found effective in reducing the output harmonic content and, as a result, is capable of improving the quality of inverter outputs. The multiswitching strategy is based on activating a group of switching elements ON and OFF with a rate higher than the desired output frequency. The switching technique of changing the status of a switching element from ON to OFF or OFF to ON is known as the modulation technique. There are several modulation techniques that

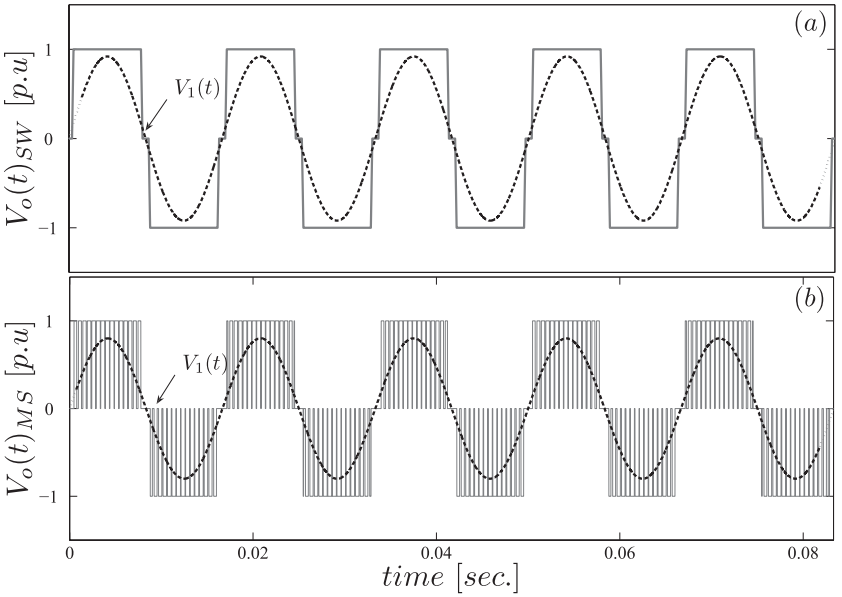

Figure 1.9 Strategies for inverter operation: (a) the inverter per-unit output obtained using the square-wave (SW) strategy and (b) the inverter per-unit output obtained using the multiswitching (MS) strategy. $V_1(t)$ the time function of the fundamental component of $V_o(t)$.

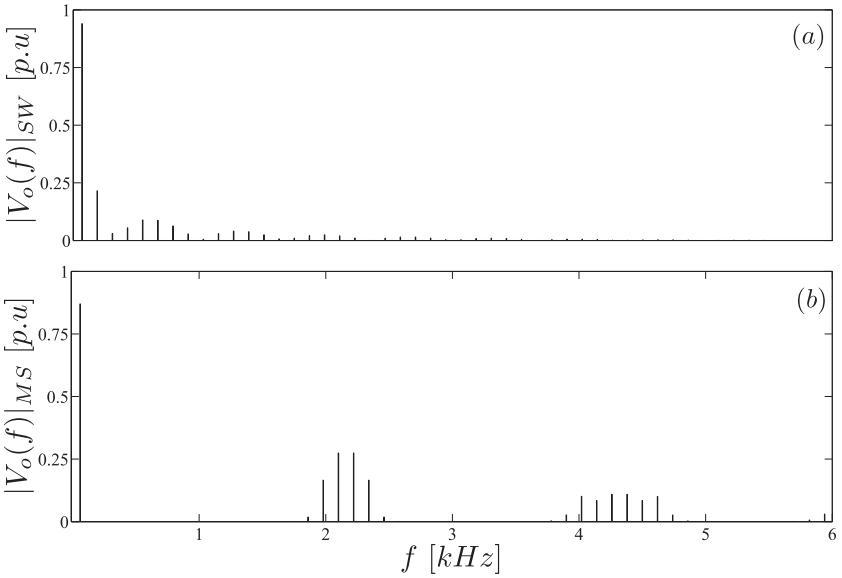

Figure 1.10 Strategies for inverter operation: (a) the per-unit magnitude spectrum of the inverter output obtained using the square-wave (SW) strategy and (b) the per-unit magnitude spectrum of the inverter output obtained using the multiswitching (MS) strategy.

have been developed and tested for operating inverters to achieve the aforementioned objectives by meeting the following conditions:

- wide linear modulation range
- minimum switching loss and improved overall inverter efficiency
- high output quality evaluated through the total harmonic distortion (THD) factors of inverter outputs
- high magnitude of the output fundamental frequency component
- simple implementation for practical applications
- low computation time

Various approaches have been used to develop new modulation techniques that can improve the performance of both 1ϕ and 3ϕ inverters. These approaches have provided continuous advancements in both solid-state technology and digital systems. One of the remarkable new technologies in operating inverters is the ability to realize high switching frequencies in stable and reliable manners. Also, with these advancements and the developments in micro-processor technology, modulation techniques that require complex computations have become implementable for both testing and operation levels. Application of inverters in high power applications has made switching losses, switching capabilities, and inverter efficiency critical issues that must be taken into account in performance evaluation. The fundamental approaches to inverter modulation are as follows:

- Carrier-based pulse-width modulation (PWM) generates switching pulses by comparing a high-frequency carrier signal with a low-frequency sinusoidal modulating signal. The PWM inverters offers linear modulation, improved quality relative to the single-pulse (square-wave) switching strategy, and were the first implementation of multiswitched inverters. The carrier-based PWM technique and its subsequent improvements are very popular in a wide range of applications. As the research to improve inverter performance continued, the non-sinusoidal carrier-based PWM technique was introduced. This technique was developed to extend the linear modulation range and to improve the magnitude of the output fundamental frequency component (the desired frequency component). The nonsinusoidal PWM was further improved and defined as space-vector modulation (SVM), which is only used for 3ϕ inverters. It is worth mentioning that PWM inverters are very popular and are used extensively in various industrial applications.
- Selected harmonic elimination (SHE) calculates the switching angles to determine the locations and widths of the switching pulses. SHE inverters offer the possibility of eliminating certain frequency components (harmonics) present in the inverter output.
- Random PWM (RPWM) concentrates energy in the inverter output in a narrow frequency band by randomizing the frequency of the carrier-signal. RPWM inverters provided further improvements on the inverter performance

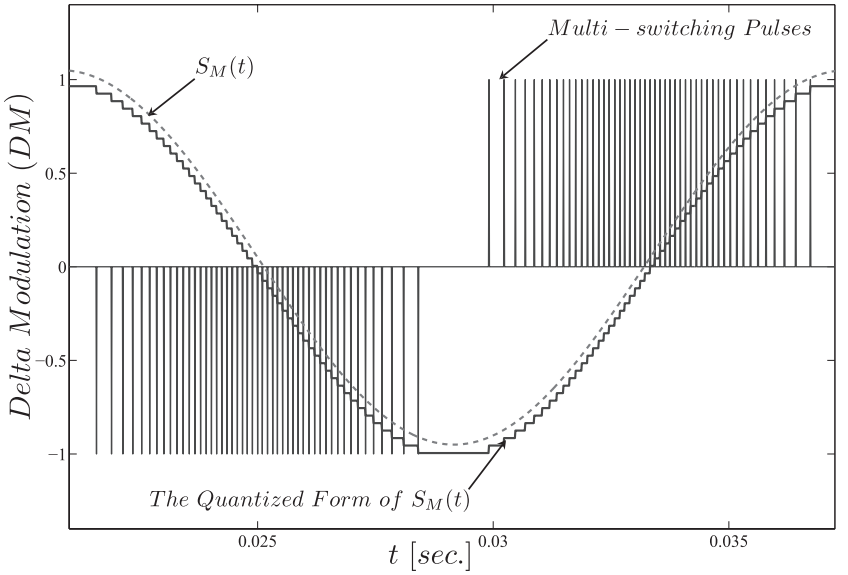

Figure 1.11 Quantization of the reference-modulating signal and the generated pulses as segment heights change.

through the effective reduction of the energy distributed in the harmonic frequency bands, while concentrating most of the energy of the inverter output in the desired frequency component.

- The delta modulation (DM) technique approximates the reference-modulating signal by sinusoid piece-wise linear segments. Each segment is compared to the reference-modulating signal to determine the increase or decrease in its relative amplitude. Only the change in amplitude is considered for changing the state of the modulated signal. In the DM technique, pulse widths are not modulated but rather have constant widths. The correct terminology for such a modulation technique is pulse density modulation (PDM) or pulse frequency modulation (PFM). The DM technique is the simplest method for quantizing analog signals into digital sequences of data with significant accuracy. This accuracy can be achieved by using switching frequencies much higher than the frequency of the reference-modulating signal. Figure 1.11 shows simple DM multi-switching signals generated by quantizing a sinusoidal reference-modulating with a sampling interval of 0.00001 second, while the quantizer period is around 0.0375 second.

Other approaches are reported in the literature that have been used to develop inverter switching techniques, among which are the direct pulse-width modulation technique (DPWM), the optimal PWM, and others.

1.4 HARMONIC DISTORTION

Harmonics are defined as high-frequency components of currents or voltages in electric systems. These frequency components are integer multiples of the fundamental frequency. Harmonic contents of any power supply can create different problems, including power losses, mechanical resonances due to magnetic fields generated by such frequency components, overheating of motors, and high currents in neutral paths. The magnitudes of harmonic contents can cause harmonic distortion, which reflects the amount of energy distributed in the harmonic frequencies relative to that contained in the fundamental frequency component. The introduction of various algorithms and procedures to realize different inverter modulation techniques has created a significant demand for performance comparison. Furthermore, with each new modulation technique, a simple performance criterion is required to highlight the advantages of such a new technique as well as to demonstrate the capabilities of overcoming difficulties faced by other techniques.

The inverter output $v_o(t)$ is an aperiodic function that has a finite period T_m. The function $v_o(t)$ has a root mean square (RMS) that is given as:

$$(V_o)_{rms} = \left(\frac{1}{T_m} \int_0^{T_m} \upsilon_o^2(t)\, dt \right)^{\frac{1}{2}} \tag{1.33}$$

Also, the periodic nature of $v_o(t)$ allows its representation using the Fourier series:

$$v_o(t) = \frac{a_0}{2} \sum_{n=1}^{\infty} a_n \cos(2n\pi f_m t) + b_n \sin(2n\pi f_m t) \tag{1.34}$$

where $f_m = \dfrac{1}{T_m}$ is the frequency of the inverter output $v_o(t)$. The Fourier series coefficients $\{a_n\}$ and $\{b_n\}$ are given by:

$$a_n = \frac{1}{T_m} \int_0^{T_m} \upsilon_o(t) \cos(2n\pi f_m t)\, dt \quad n = 0, 1, 2 \ldots \infty \; and \quad 0 < t < T_m \tag{1.35}$$

$$b_n = \frac{1}{T_m} \int_0^{T_m} \upsilon_o(t) \sin(2n\pi f_m t)\, dt \quad n = 1, 2, 3 \ldots \infty \; and \quad 0 < t < T_m \tag{1.36}$$

The inverter output $v_o(t)$ is an odd function, which sets the coefficient as $\{an\} = 0$. Moreover, due to the quarter-cycle symmetry of $v_o(t)$, all the even frequency components will have $\{b_n\}_{n=2,4,6\ldots}$ evaluated with 0. These two features of the inverter output $v_o(t)$ simplify the Fourier series as:

$$v_o(t) = \sum_{n=1,3,5\ldots}^{\infty} b_n \sin(2n\pi f_m t) \tag{1.37}$$

Substituting Fourier series expansion into equation (1.33) yields:

$$(V_o)_{rms} = \left(\frac{1}{T_m} \int_0^{T_m} \sum_{n=1,3,5\ldots}^{\infty} b_n^2 \sin^2(2n\pi f_m t)\, dt \right)^{\frac{1}{2}} \tag{1.38}$$

$$(V_o)_{rms} = \left(\frac{1}{T_m} \int_0^{T_m} \sum_{n=1,3,5...}^{\infty} \frac{b_n^2}{2} (1 - \cos(4n\pi f_m t)) dt \right)^{\frac{1}{2}} \tag{1.39}$$

The integration of the double-frequency terms is evaluated with 0 over the interval T_m. This simplifies the inverter output RMS value to:

$$(V_o)_{rms} = \left(\sum_{n=1,3,5...}^{\infty} \frac{b_n^2}{2} \right)^{\frac{1}{2}} = \left(\sum_{n=1,3,5...}^{\infty} (b_n^2)_{rms} \right)^{\frac{1}{2}} \tag{1.40}$$

As in most inverter applications, the fundamental frequency component ($n = 1$) is considered, a factor that reflects the distortion caused by other frequency components with respect to the fundamental frequency component. This factor is defined as the total harmonic distortion (THD) factor, which has the following mathematical expression:

$$THD = \frac{\sqrt{\sum_{n=3,5,...}^{\infty} V_n^2}}{V_1} \tag{1.41}$$

where $V_n = b_n$, $n = 3, 5, \ldots$. With the introduction of advanced multiswitching techniques, the existence of inverter output harmonic components became more complicated for the conventional Fourier series approach. In 1975, Bowes presented a double Fourier integral formula that had originally been developed for communication applications. The double Fourier integral formula approach is based on defining two independent linear time variables function as:

$$x(t) = \omega_c t + \theta_c \tag{1.42}$$

$$y(t) = \omega_m t + \theta_m \tag{1.43}$$

where ω_c is the carrier signal frequency, θ_c is an arbitrary phase shift of the carrier signal, ω_m is the modulating signal frequency, and θ_m is an arbitrary phase shift of the reference-modulating signal. A multivariable function $f(t)$ can be defined as:

$$f(t) = f(x(t), y(t)) \tag{1.44}$$

Using Fourier analysis theory, complex coefficients of Fourier series for the function $f(t)$ can be determined as:

$$C_{mn} = \frac{1}{2\pi^2} \int_{-\pi}^{\pi} \int_{-\pi}^{\pi} f(x(t), y(t)) e^{j(mx+ny)} dx dy \tag{1.45}$$

The complex coefficients C_{mn} can determine the magnitude and the phase of each harmonic component present in the function $f(t)$. This analysis was used as a performance criterion for testing effective switching strategies that resulted in implementing the naturally sampled PWM scheme. In the early 1980s, the same criterion was further expanded by Bowes and Mount to successfully implement and test the regularly sampled PWM inverter using microprocessor technology.

1.5 SUMMARY

This chapter has presented an introduction to the fundamental structures and operation of inverters. Some sections in this introductory chapter have been devoted to a brief presentation of the popular topologies used in inverter applications along with their structure and basis of operation. Furthermore, the two basic inverter switching methods have been discussed, along with their general waveforms. The last part of this chapter has focused on the Fourier analysis methods that are used to model the distortions in inverter outputs.