CHAPTER 1

Introduction

1.1 INTRODUCTION OF ELECTRONIC PACKAGE INTEGRATION

The rapid growth and convergence of digital computers and wireless communication have been driving semiconductor technology to continue its evolution following Moore's law in today's nanometer regime. Future electronic systems require higher bandwidth with lower power consumption to handle the massive amount of data, especially for large memory systems, high-definition displays, and high-performance microprocessors. Electronic packaging is one of the key technologies to realize a wider bus architecture with high bandwidth operating at higher frequencies. Various packages have been developed toward a higher density structure. In particular, a three-dimensional (3D) integration based on through-silicon via (TSV) [1] arrays technology provides a potential solution to reduce the size and to increase the performance of the systems. Furthermore, nano-interconnects to replace the Cu-based interconnects provides a promising solution for long-term application.

There is a great challenge for further increasing of the signal speed in electronic systems due to the serious electromagnetic compatibility (EMC) problem. Figure 1.1 plots the technology trends versus actuals and survey, and Figure 1.2 shows the trends of microprocessors predicted by the International Technology Roadmap for Semiconductors (ITRS) [2, 3]. From these figures one can see that

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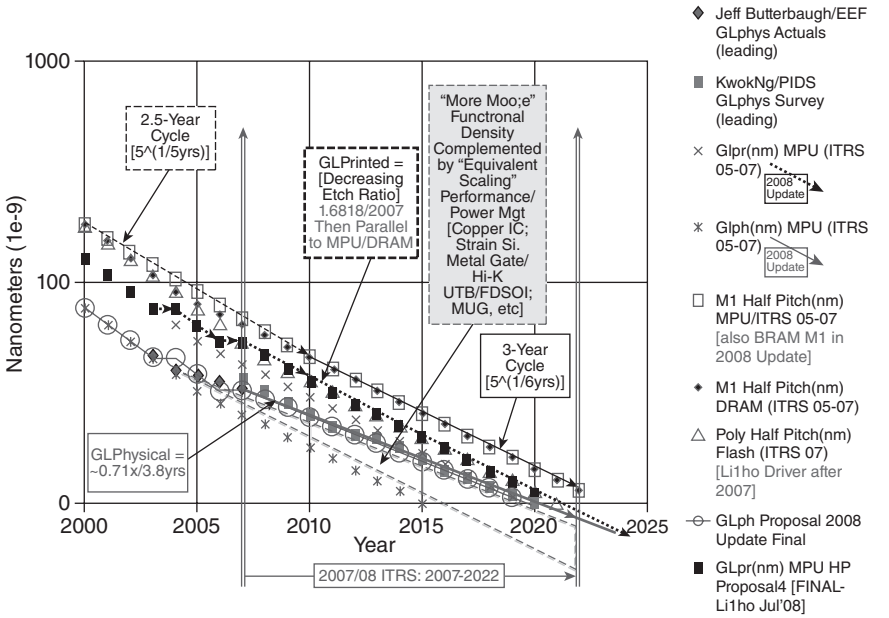

Figure 1.1 2008 ITRS update—technology trends versus actuals and survey [2].

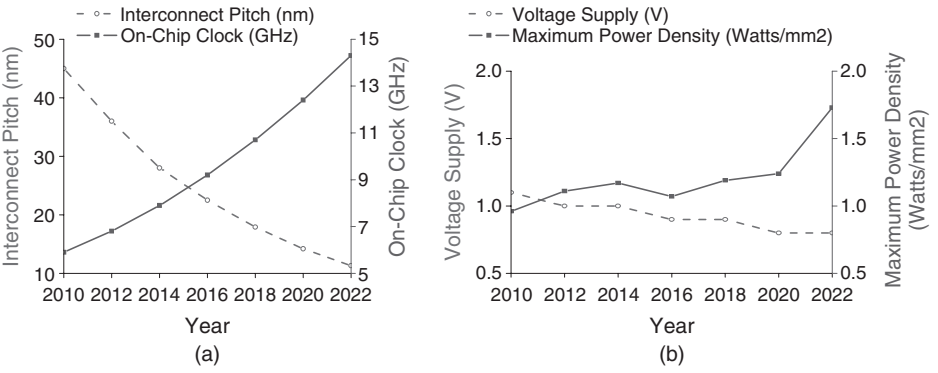

Figure 1.2 The trends of microprocessor predicted by the International Technology Roadmap for Semiconductors (ITRS).

- Interconnect pitch will continue to decrease to 11.3 nanometer, while the on-chip clock frequency will be increased to 14.3 GHz by 2022. Due to the reduction of the feature size and pitch, more and more circuits are integrated into one electronic package, such as the system in package (SIP) and the 3D integration. This results in a complex and high-density environment inside the electronic systems. At the same time, with the ever-increasing clock frequency (also its high-frequency harmonics), the physical size of the small electronic package becomes electrically large, and so the electromagnetic wave propagation inside such a small structure must be considered.
- Until 2011, the voltage supply of the microprocessor is continually reduced with an increased power density. The electromagnetic noise will be pronounced due to the increased power density, which then makes the decreased voltage supply unstable. To design a high-speed and stable electronic system, we need better understand the electromagnetic interactions and the EMC issues inside the electronic package.

The EMC researches related to the high-speed circuit systems have a long history, which can be classified into different levels according to the size of the interested objects, which includes the system level, printed circuit board (PCB) level, electronic package level, and component level. The increasing clock frequency makes the size of tiny structures on the chip be comparable with the wavelength of interest. The fluctuation of electromagnetic wave cannot be ignored any more. Therefore, we must accurately model the electromagnetic wave behavior for all scales of the high-speed circuit systems. In the near future, the nanoscale integrated circuits (ICs) will be characterized by using the *electric and magnetic fields* instead of the conventional *voltage and current*. *EM in micro-E* is becoming a hot topic in both academic community and industrial applications.

The EMC analysis for high-speed electronics includes lots of issues, such as the ground bounce, cross talk, conducted emission, radiated emission, conducted immunity, and radiated immunity. The interaction between on-board capacitance and on-chip capacitance causes an antiresonance which induces a peak in the total power distribution network (PDN) impedance as shown in Figure 1.3. Figure 1.4 shows a typical multilayered advanced electronic package which consists of two

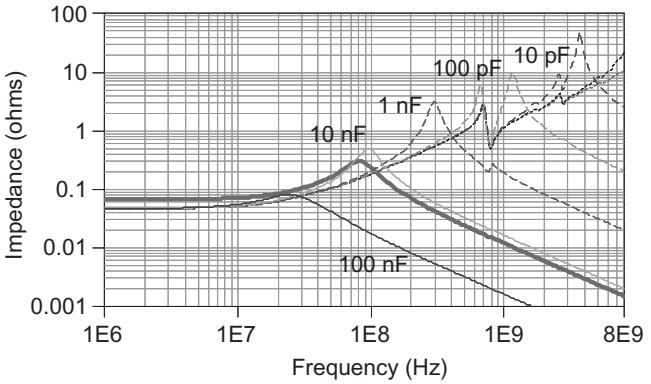

Figure 1.3 Example of antiresonances in total PDN impedances for various on-chip capacitance values [3]. (See color insert.)

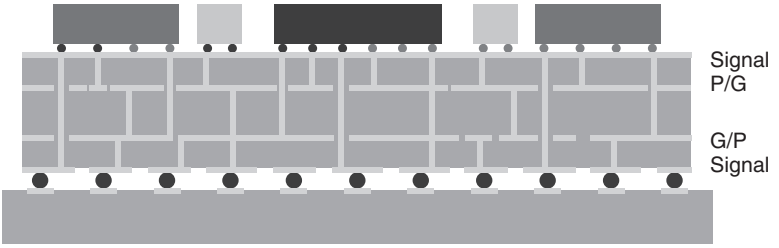

Figure 1.4 A schematic diagram of a multilayered electronic package [37].

main electrically functional systems: the PDN and the signal distribution network (SDN). The passive structures are composed of three main categories: (1) traces or transmission lines, typically microstrip lines or striplines, (2) vias used as vertical interconnections, and (3) conductor plates serving as power or ground planes. Because of the complexity of an advanced package, it is difficult to model the entire SDN or PDN simultaneously. Yet, we need to consider the impact of the PDN on the SDN in order to characterize the SDN more accurately. Many researchers have proposed various approaches to study the electrical properties of the above passive structures [4–44].

A typical EMC problem residing in this PDN of the electronic package is illustrated in Figure 1.5. In Figure 1.5, the power and ground planes are used to supply DC power for the circuits integrated in the electronic package. The signal traces are often laid out in different

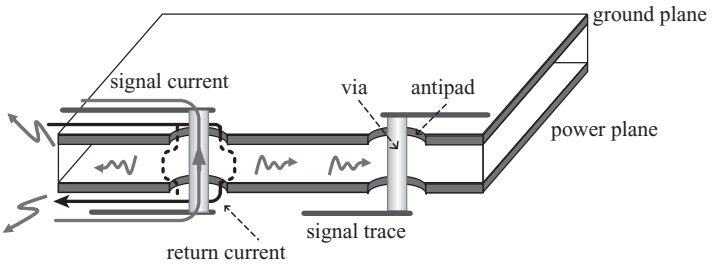

Figure 1.5 Noise coupling inside and emission from the power-ground planes.

layers of power-ground planes. Their return currents flow on the power-ground planes just below them. When the traces pass through different layers, their return currents also exchange from one plane to another plane, as shown in Figure 1.5. Accordingly, a vertical displacement current is induced between different planes for the continuity of the return currents. This displacement current will excite electromagnetic field noise, which then propagates inside the power-ground planes and couples to other signal traces passing through the same layer. At the same time, this noise also leaks to the surrounding area of the electronic package through the periphery and gaps of the power-ground planes. These interferences will be further amplified if the noise's spectrum covers any inherent resonant frequency of the cavity-like power-ground planes.

To achieve first-pass design success, we must employ an advanced modeling and simulation technique to analyze the electrical performance of the 3D electronic packages, PCB, and chips at the system level. However, both industry and academia communities face the great challenges in developing the electrical design and simulation tools due to the multiscale nature of the problem, the strong local and global electromagnetic coupling, and the complexity of 3D integration systems. ITRS has summarized the state of the art of current semiconductor industry development, where the major challenges for simulation and modeling are listed as [2] mixed-signal co-design and simulation environment, rapid turnaround modeling and simulation, electrical (power disturbs, electromagnetic interference (EMI), signal and power integrity associated with higher frequency/current and lower voltage switching), system-level co-design, electronic design automation (EDA) for "native" area array to meet the roadmap projections, and models for

reliability prediction. Therefore, advanced modeling techniques, which stand up to the challenges imposed by the complexity of nanoscale silicon chips and their interconnections including 3D ICs, 3D packaging, and PCB [45–47], are in great demand.

1.2 REVIEW OF MODELING TECHNOLOGIES

Modeling of transmission lines has a long history and is well documented in many textbooks [4]. So in the following, we will mainly review the modeling of vias and power-ground planes for electronic packaging and PCBs. Such modeling methods can be roughly classified into three categories: (1) lumped circuit approaches, (2) full-wave approaches, and (3) hybrid circuit coupled full-wave approaches.

For its simplification and ease of understanding, at the beginning of the research, lumped circuit approaches have been used for the electrical modeling of electronic packages. Such examples are shown in Figures 1.6 and 1.7. Empirical and analytical formulae for via capacitance and inductance can be easily found in many handbooks. Quasi-static numerical methods have also been introduced to calculate the

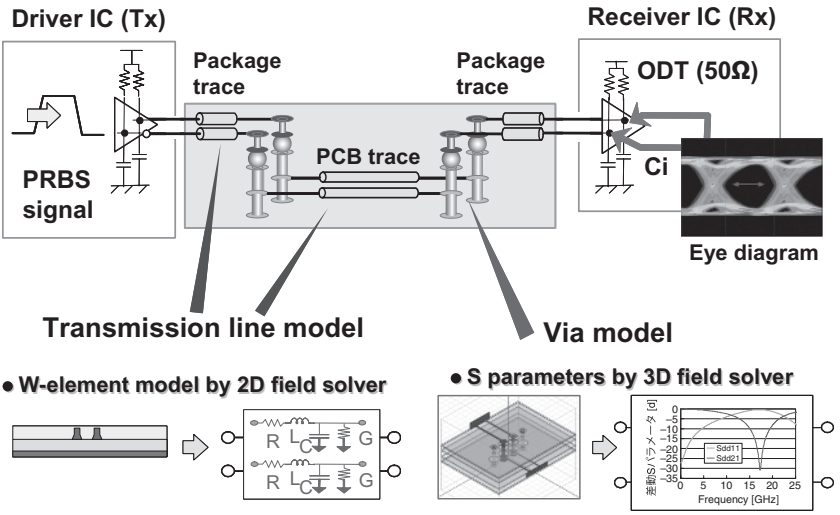

Figure 1.6 A typical transmission line model on a printed circuit board [3]. PRBS: pseudo-random binary sequence. ODT: on die termination.

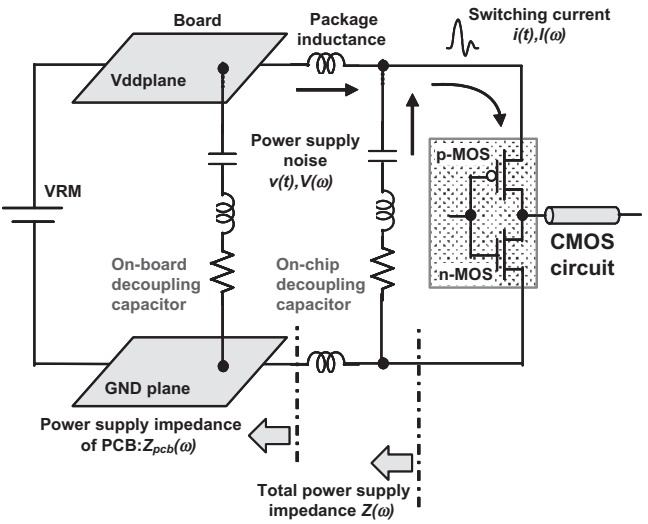

Figure 1.7 Power distribution network [3].

lumped circuit values in T or PI types of via models [5, 6]. These methods allow rapid computation, but often suffer from accuracy problems. The authors in Reference 7 proposed a model of a magnetic-frill array and utilized microwave network theory for analysis of vias in multilayered packages. But it is a single via model which is difficult to be generalized to multiple vias. The equivalent circuits of much complex via array can be extracted by using de-embedding method [8]. Distributed circuit approaches have also been widely used for package modeling, such as the partial element equivalent circuit (PEEC) method [9, 10].

Second, full-wave methods both in the time and frequency domains have been employed to study the packaging problems. The commonly used full-wave commercial simulators include Ansoft HFSS and CST Microwave Studio, which are based on finite element method (FEM) [11, 12] and finite integral technique, respectively. Other full-wave algorithm includes the finite-difference time-domain (FDTD) method [13] and the transmission line matrix method (TLM) [14]. Recently, the integral equation-based full-wave method begins to attract more attention and had been employed. The advantage of the integral equation method is that it can use the suitable Green's function to present

the effect of the complex environment, so that the unknowns are only placed on discontinuities inside the PDN. This can give an efficient simulation. According to the different Green's functions used, the integral equation methods can be classified into (a) two-dimensional (2D) integral equations, including 2D mode method [15] and image method for rectangular power and ground planes, and 2D transverse magnetic (TM) integral equation for arbitrarily shaped power and ground planes [16–18]; (b) 3D integral equations, including 3D cavity mode method for rectangular power and ground planes [19] and parallel plate mode method for arbitrarily shaped power and ground planes [20, 21]. For most real applications the parallel plates have regular shapes, such as rectangles, circles, or triangles, a closed form of the Green's functions can be formulated which results in an impedance formula in terms of the summation of infinite number of resonant modes [22–24]. This 2D integral equation method is sometimes called the cavity resonator method. Segmentation techniques may be applied to extend the cavity resonator method for parallel plates with irregular shapes.

These full-wave methods are versatile and able to solve a wide range of problems, but at the expense of large memory usage and long CPU time, especially for those 3D full-wave methods. Although the overall size of the electronic packages is small enough to apply these full-wave methods, the high aspect ratio of the power and ground planes and the tiny structures, such as the signal traces and narrow slots, result in a huge number of meshing. This makes these full-wave methods very expensive in terms of computing time and memory requirement.

Third, to avoid the computational cost of these full-wave methods and the geometrical limitations of the analytical methods, a more efficient approach is to combine both methods together, so that we can benefit from both analytic and numerical techniques. The coupled circuit-field approaches are also widely used to model the electronic packages in order to leverage the advantages of both circuit and full-wave approaches. An important approach under this category is rooted in the theory of modal decomposition and the salient features of electronic packages. The transmission lines and power-ground planes in an electronic package convey different modes, that is, transmission line modes and parallel plate modes. Modal decomposition can be used to decouple these two modes, which are then solved independently. These two modes are finally recombined to reflect the original problem. The

coupling between the transmission line mode and the parallel-plate mode often occurs due to the vias. The current flowing in the via excites the parallel-plate mode field, while the transmission line experiences the loading effect of the power-ground plane in the presence of the via.

The complete modal decomposition and recombination approach has been demonstrated by several researchers. Current or voltage controlled sources are used to link these two modes. A general modal recombination approach was presented in Reference 26 for coupled striplines and nonideal power-ground planes, while the parallel-plate mode associated with the power-ground planes has been studied by many researchers. 2D full-wave methods have been extensively employed in the literature to model the power-ground planes. The 2D integral equation method is also called the contour integral method and has been used in Reference 16 to study general parallel-plate structures with arbitrary shapes. Another 2D approach, called the 2D FDTD, has also been used to model parallel plates [27]. Discretization of the metal plates by the finite-difference method was interpreted as a 2D distributed *LC* circuit, and a rigorous derivation is given in Reference [27]. The 2D distributed *RLCG* (resistance, inductance, capacitance, and conductance) circuit network, which is widely used in the literature to represent the power and ground planes, can be considered as an extension of the *LC* network derived from the finite-difference method. Instead of using Simulation Program with Integrated Circuit Emphasis (SPICE)-like solvers to simulate the large equivalent circuit network of power-ground planes, the latency insertion method is proposed in Reference 28 to perform fast transient simulation of large *RLC* networks. Moreover, a transmission matrix method reported in Reference 29 divides the 2D distributed *RLCG* circuit network into many interdependent blocks, and each block is formulated as a transmission (*ABCD*) matrix. Cascading those transmission matrices produces a fast way to obtain the desired impedance of the power-ground plane. A multilayered finite-difference method (MFDM) was recently proposed in Reference 26. The 2D finite element method (2D FEM) is also used to simulate power-ground planes [30] and had been integrated into the commercial software Ansoft SIWave. In addition, the radial transmission line theory has been applied to derive an admittance matrix to account for the effect of the parallel plates [31]. However, image theory [32] is needed to model the reflection from the edges of finite-sized substrates. Image theory is elegant for modeling the boundary with a

regular shape but is cumbersome for modeling arbitrary shapes of the edges of PCBs or packages. In the model decomposition and recombination approach, a single via can be represented by a PI type of equivalent circuit. The capacitance and inductance in the PI circuit are usually computed by analytical formulae or quasi-static solvers. Recently, an elegant analytical formula was derived for the via barrel-plate capacitance [6].

1.3 ORGANIZATION OF THE BOOK

This book is organized in six chapters. Chapter 1 provides an overview of the state-of-art of electrical modeling and simulation techniques for electrical packaging systems. Chapter 2 focuses on the macromodeling technique widely used in the electrical and electromagnetic modeling and simulation of complex interconnects in 3D integrated systems. Macromodels are generated by employing the vector fitting (VF) method to perform rational-function approximation of scattering or admittance network parameters of high-speed complex interconnects and passive circuits. Subsequently, the macromodel can be synthesized as an equivalent circuit, which is compatible with the SPICE circuit simulator and can be combined with other external linear or nonlinear circuits to perform signal and power integrity analysis or other electrical performance analysis of electronic systems. The stability, causality, and passivity assessment and enforcement of the macromodel are also discussed in detail. Finally, numerical examples of macromodeling are presented and discussed.

In Chapter 3, the semianalytical scattering matrix method (SMM) based on the *N*-body scattering theory is presented for modeling of 3D electronic package and multilayered PCBs with multiple vias. Using the modal expansion of fields in a parallel-plate waveguide, the formula derivation of the SMM is presented in detail. In the conventional SMM, the power-ground planes are assumed to be infinitely large so they cannot capture the resonant behavior of the real-world packages. In particular, the SMM method has been extended to solve the finite domain of power-ground planes in coupling with a novel boundary modeling method proposed by the author's group. This method has demonstrated its unique features which is capable to efficiently handle the complex real-world 3D package integration and PCB structures.

In Chapter 4, 2D and 3D integral equation methods are employed for the analysis of PDN in 3D package integration. The 2D integral equation method provides a comprehensive way for one to quickly extract the equivalent circuits of the PDN, and then substitute them into a SPICE-like simulator to perform the signal and power integrity analysis. The 3D integral equation method provides a more accurate solution for both the emission and susceptibility issues of the PDN. Both of the 2D and 3D integral equation methods are optimized by making a full use of the structural features of the PDN.

Chapter 5 is based on the physical-based algorithm to extract the equivalent circuit of the complex PDN in 3D integrated systems and PCBs. An intrinsic via circuit model is first derived through rigorous electromagnetic analysis for an irregular plate pair with multiple vias in a PCB. The derivation of the intrinsic via circuit model naturally leads to a new impedance definition of plate pair or power-bus, which is expressed in terms of cylindrical waves. The new plate pair impedance has clear physical meaning and makes possible signal/power integrity co-simulations. Numerical and measurement examples have indicated that while the new impedance gives almost the same results to the conventional one in a plate pair with few vias, it can correctly predict the resonant frequency shift in the case of a plate pair with a large amount of vias.

Chapter 6 presents a compact wideband equivalent-circuit model for electrical modeling of TSVs and addresses the metal-oxide-semiconductor (MOS) capacitance effects of TSVs.

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