1 ESD Design Synthesis

1.1 ESD DESIGN SYNTHESIS AND ARCHITECTURE FLOW

In the ESD design synthesis process, there is a flow of steps and procedures to construct a semiconductor chip [1–13]. In many cases, the floorplanning process is a function of the type of semiconductor chip. The following design synthesis procedure is an example of an ESD design flow needed for semiconductor chip implementations:

- **I/O, Domains and Core Floorplan:** Define floorplan of regions of cores, domains, and peripheral I/O circuitry.
- **I/O Floorplan:** Define area and placement for I/O circuitry.
- **ESD Signal Pin Floorplan:** Define ESD area and placement.
- **ESD Power Clamp Network Floorplan:** Define ESD power clamp area and placement for a given domain.
- **ESD Domain-to-Domain Network Floorplan:** Define ESD networks between the different chip domains area and placement for a given domain.
- **ESD Signal Pin Network Definition:** Define ESD network for the I/O circuitry.
- **ESD Power Clamp Network Definition:** Define ESD power clamp network within a power domain.
- **Power Bus Definition and Placement:** Define placement, bus width, and resistance requirements for the power bus.
- **Ground Bus Definition and Placement:** Define placement, bus width, and resistance requirements for the ground bus.
- **I/O to ESD Guard Rings:** Define guard rings between I/O and ESD networks.

ESD: Design and Synthesis, First Edition. Steven H. Voldman.

- **I/O Internal Guard Rings:** Define guard rings within the I/O circuitry.
- **I/O External Guard Rings:** Define guard rings between I/O circuitry and adjacent external circuitry.

1.1.1 Top-Down ESD Design

In the ESD design synthesis, the implementation can be thought of as a "top-down ESD design" process. Figure 1.1 is an example of a "top-down ESD design flow." In the ESD design synthesis process, there is a flow of steps and procedures to construct a semiconductor chip. In my experience, in the planning stages of a semiconductor chip, the circuit team leader addresses the ESD design synthesis from a procedure as shown. With a "top-down ESD design synthesis" the integration, placement, sizing, and requirements are addressed. This process will be independent of whether the semiconductor chip is for digital logic [1–7,11], analog design [14,31–33], power electronics [26–30,35–38], or radio frequency applications [8,39–41].

1.1.2 Bottom-Up ESD Design

In the ESD design synthesis, the implementation can also be addressed as a "bottom-up ESD design" process. Figure 1.2 is an example of a "bottom-up ESD design flow." In a bottom-up ESD design synthesis process, the circuits are defined, and the corresponding ESD networks.

One of the difficulties of ESD and the latchup design synthesis process is that the ESD design synthesis requires some "top-down" procedures, some "bottom-up" thinking, and integration. This will become more apparent throughout this text.

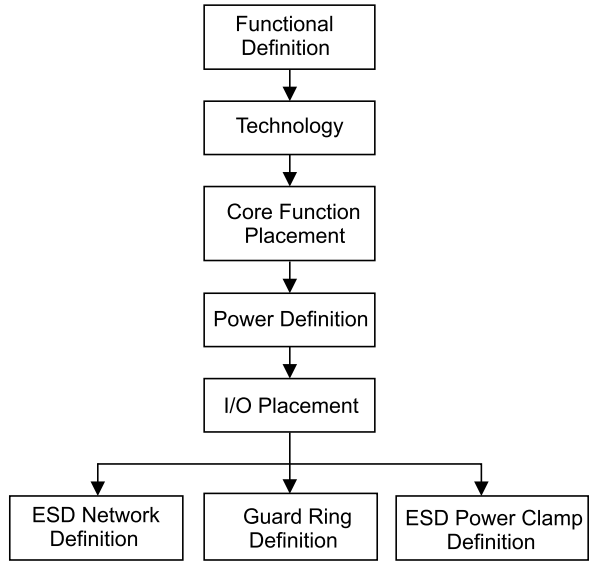

Figure 1.1 Top-down ESD design flow

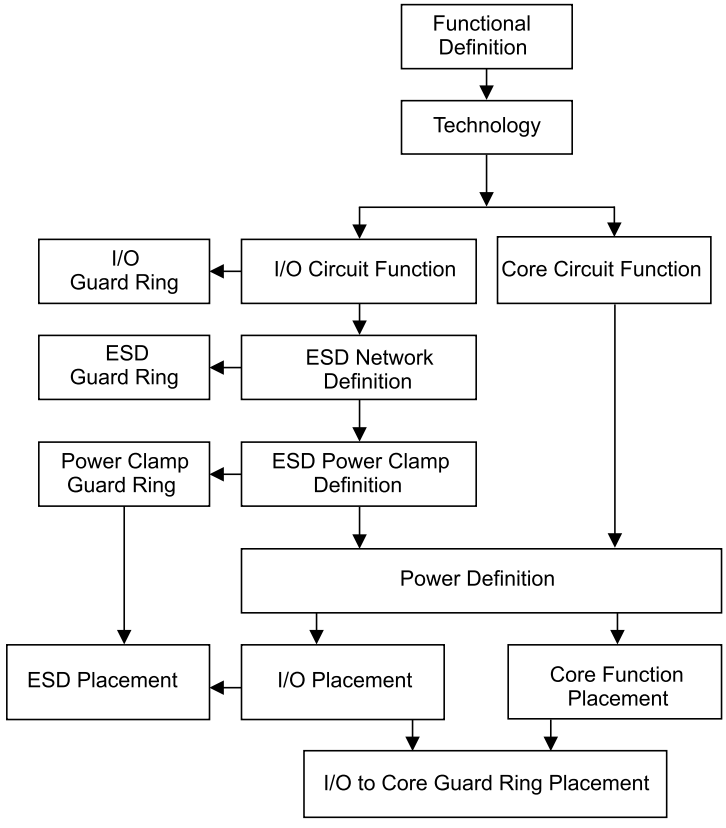

Figure 1.2 Bottom-up ESD design flow

1.1.3 Top-Down ESD Design – Memory Semiconductor Chips

In the ESD design synthesis of a memory chip, the thought process is a "top-down ESD design" process, with the floorplanning driven by the array region. These designs are "array-dominated" designs, with the focus on the array [7]. The I/O region is limited in physical area, and the architecture is driven by the number of output pins, how to integrate it with the packaging, and how to support the I/O and ESD in the least amount of space. Figure 1.3 is an example of a "top-down ESD design flow" for a memory chip.

1.1.4 Top-Down ESD Design – ASIC Design System

In the ESD design synthesis of an applications-specific IC (ASIC) architecture, the procedure for the ESD design integration is significantly different. In the ASIC environment, the chip size, the number of I/O, and its ESD integration is dependent on the chip size. In this "top-down" methodology, the number of I/O, supported bus locations, placement of the I/O cells, integration of the ESD elements, and power are all synthesized in a different flow. Figure 1.4 is an example of a "top-down ESD design flow" for an ASIC methodology.

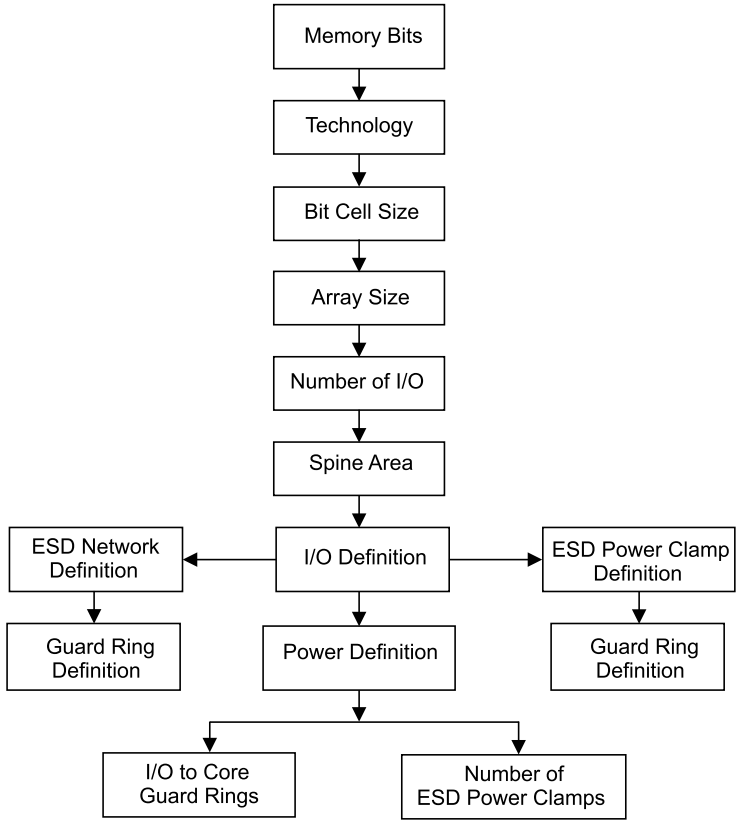

Figure 1.3 Top-down ESD design flow – memory

1.2 ESD DESIGN – THE SIGNAL PATH AND THE ALTERNATE CURRENT PATH

In semiconductor chip design, the role of a semiconductor chip is to receive a signal, process the signal, and transmit the signal.

In ESD design synthesis, the role of the ESD network solution is to establish an alternate current path to avoid damage along the signal path that impacts its function or operation characteristics [7,11]. As a result, simplistically, the ESD network must transmit the ESD current out of the sensitive signal path to an alternative path or current loop. This is achieved by diverting the ESD current to the power grid, or the ground plane. The fundamental requirements along the alternative current path are as follows:

- An alternative current path must exist between any signal pin and any grounded reference (e.g., signal pin, power pin, ground pin).
- An ESD element must divert the ESD current to the power plane or ground plane.

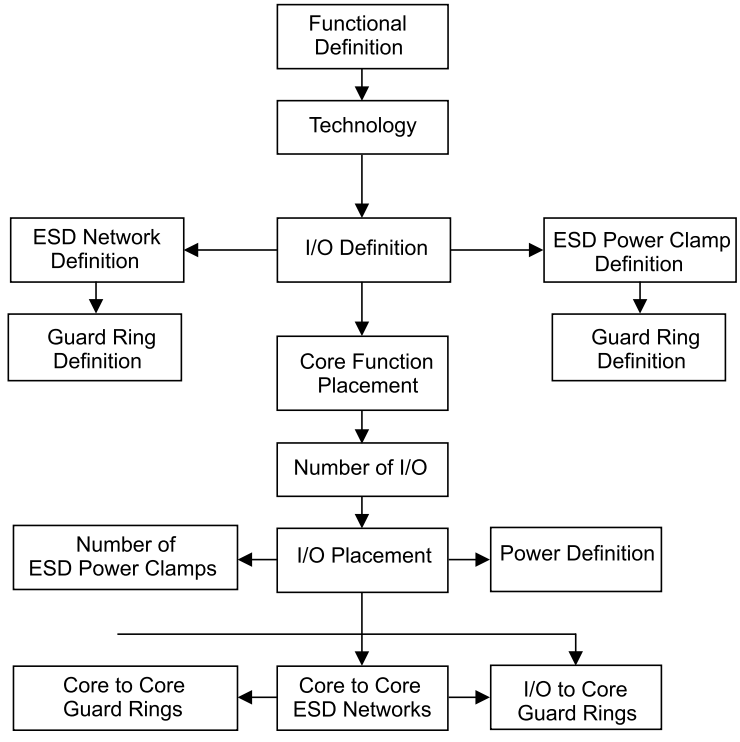

Figure 1.4 Top-down ESD design flow – ASICs

- An ESD element must be able to transmit the ESD current to the power rail or ground rail without damage (to some specification level).
- The power rail and ground rail must be able to source the ESD current without damage (to some specification level).
- The alternative current path must achieve the ESD current discharge to the grounded reference to some specification level prior to damage along the signal path.

To achieve this objective, there are some conditions on the alternative current path:

- ESD networks are required to address both positive and negative polarity events.
- The ESD network must have low turn-on voltage and low resistance prior to destruction of the circuitry along the signal path.
- The power grid and the ground rail resistance must be sufficiently low to avoid IR voltage drops.
- Bi-directional electrical connectivity must exist, providing an alternative current path between all independent rails through ESD networks, or other means (e.g., circuitry, inductors, bond wires, packaging, etc.).

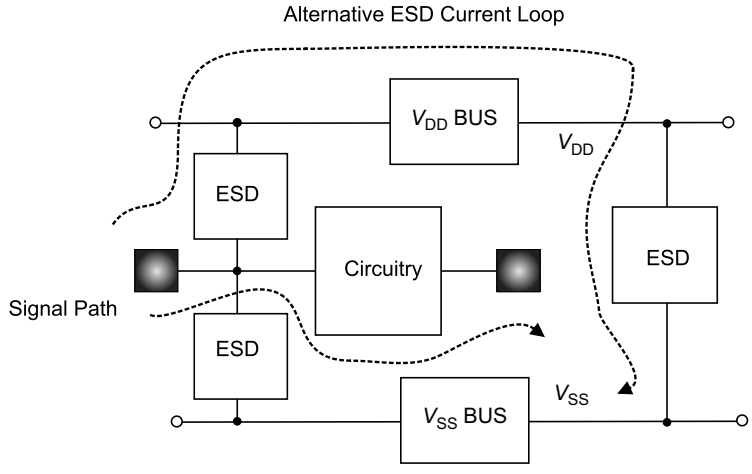

Figure 1.5 The signal path and alternative ESD current path

Figure 1.5 shows an example of a semiconductor high-level schematic of the chip architecture. The figure highlights the signal path and the alternative ESD current path created by the ESD networks.

1.3 ESD ELECTRICAL CIRCUIT AND SCHEMATIC ARCHITECTURE CONCEPTS

In this section, discussion of ESD from a chip architecture, and the electrical schematic viewpoint will be shown. What are the ideal characteristics that we are looking for from an ESD network? What are the ideal characteristics from a frequency domain perspective? How is the chip architecture related to the testing procedure and the events that occur in a real chip?

1.3.1 The Ideal ESD Network and the Current–Voltage DC Design Window

The DC *I–V* characteristics may determine the "on" and "off" characteristics of the ESD network during functional operation, and its ESD effectiveness as an ESD network to protect other circuitry. An ideal ESD network has the following characteristics [7,11]:

- The ESD device, circuit, or network is "off" during the DC functional regime between signal levels between the most negative power supply voltage and the most positive power supply (associated with the signal pin).
- The ESD network has an "infinite resistance" when in the "off" state, which can be expressed as

$$\left.\frac{dI}{dV}\right|_{\text{off}} = \frac{1}{R} = 0$$

The ESD network is "on" during voltage excursions that undershoot below the most negative power supply, or voltage excursions that overshoot the most positive power supply (during ESD testing).

- The ESD network has a "zero resistance" when

$$\left.\frac{dI}{dV}\right|_{\text{on}} = \frac{1}{R} = \infty$$

The ESD network operation extends beyond the "electrical safe-operation area" (electrical SOA) in DC voltage level or DC current level [26–30].

- The ESD network operation does not extend beyond a "thermal safe-operation area" (thermal SOA) in DC voltage level or DC current level [26–30].
- The ESD network operation does not reach the current-to-failure, voltage-to-failure, or power-to-failure prior to the ESD specification level objective [15–30].

ESD networks can consist of *I–V* characteristics of the following form:

- Step function *I–V* characteristics.
- S-type *I–V* characteristics.
- N-type *I–V* characteristics.

Step function *I–V* characteristics have a single "off" state as the structure is biased. At some voltage value, the device is "on." For example, a diode element has a step function *I–V* characteristic and is suitable for ESD protection. In the case of a diode element, the ideality is a function of the on-resistance of the diode element.

1.3.2 The ESD Design Window

In the defining of an ESD network, there is a desired range of operation. The "ESD design window" is the region of desired operation on a current–voltage (*I–V*) plot (Figure 1.6). On the *I–V* plot, there is a region defined for functional operation of the semiconductor chip. The application voltage is designated as from a voltage of $V = 0$ to $V = V_{\text{DD}}$. On the *x*-axis, there is an absolute maximum voltage (also known as ABS MAX). On the *y*-axis, there is an operational current and an absolute current magnitude which the application must remain below without damage. The operational current–voltage range forms a rectangular region on the *I–V* plot. The ESD network must operate between the V_{DD} power supply and the absolute maximum voltage. On the current axis, the ESD network must discharge as high as possible to avoid the failure of the semiconductor component. The ESD current discharge should achieve the ESD specification levels. Hence, there is a region in which the ESD network is to operate without interfering with functional operation, but must discharge enough current prior to destruction of the semiconductor chip. In addition, the current

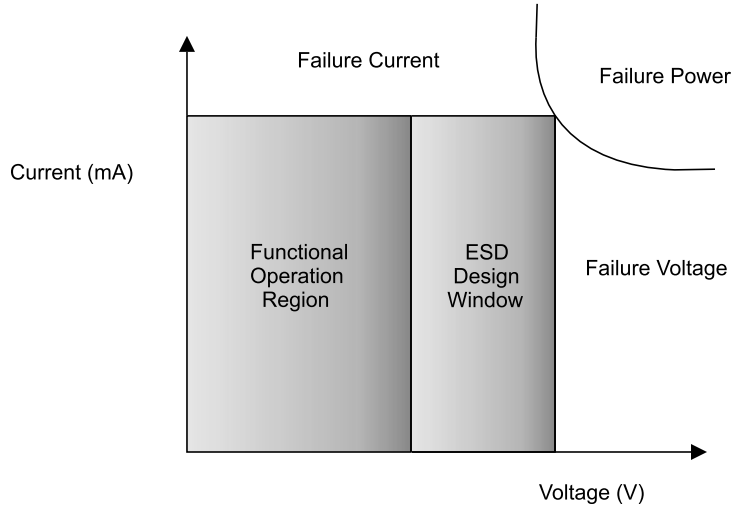

Figure 1.6 ESD design window and SOA

magnitude must exceed the latchup current criteria for voltages lower than the power supply voltage.

Figure 1.7 shows an example of a diode in the ESD design window. Because of the non-ideality of the diode element, there is a region where the DC voltage of the semiconductor devices in the technology are exceeded.

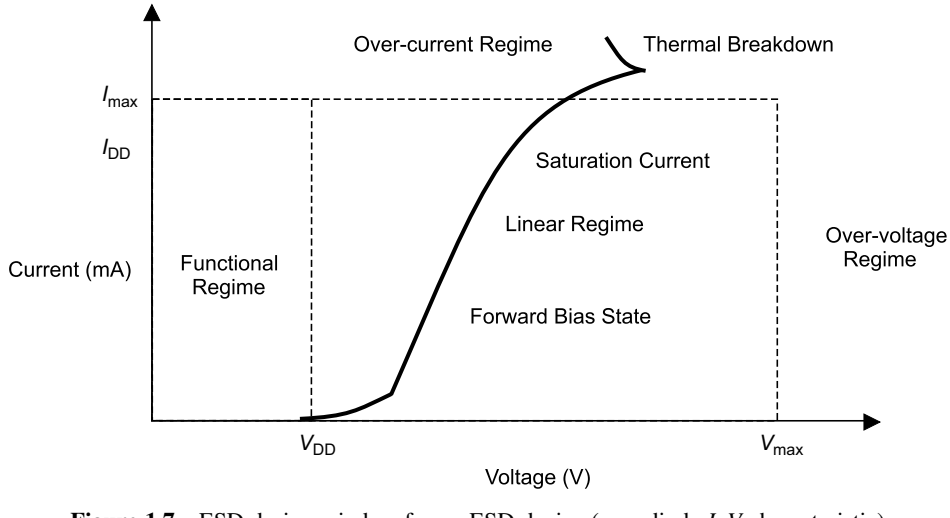

Figure 1.7 ESD design window for an ESD device (e.g., diode *I–V* characteristic)

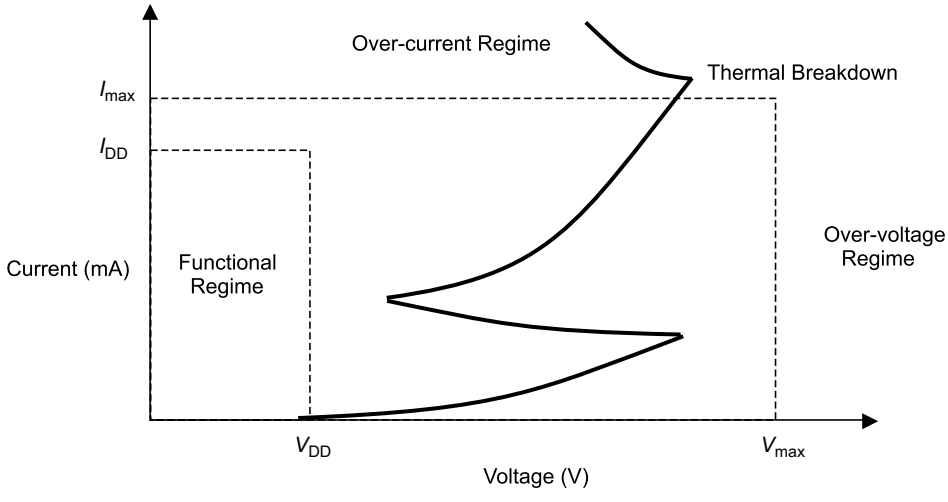

Figure 1.8 ESD design window for an S-type *I–V* characteristic ESD device

S-type characteristics are semiconductor devices or circuits that have two current states for a given voltage state. For example, an n-channel MOSFET or silicon-controlled rectifier (e.g., pnpn device) has an S-type *I–V* characteristic. Figure 1.8 shows an example of an n-channel MOSFET in a MOSFET drain-to-source configuration in an ESD design window. To utilize the MOSFET as an ESD network, the MOSFET snapback must occur within the current–voltage window of the technology limits of its safe operation area (SOA) of the other structures in the technology.

Figure 1.9 shows the ESD design window as a function of the technology generation. As observed, as the power supply voltage is reduced, the ESD design window decreases for successive technology generations.

1.3.3 The Ideal ESD Networks in the Frequency Domain Design Window

From an RF ESD design perspective, the characteristics of an RF ESD design are focused on its RF characteristics at the RF application frequency [8]. Figure 1.10 shows an example of ESD phenomenon frequencies, and RF application frequencies. RF applications are now faster than ESD phenomena for applications that exceed 5 GHz. This opens opportunities for unique RF ESD design implementations [8].

From an RF perspective, the ideal RF ESD network has the following features [8]:

- An ideal RF ESD network would have zero impedance during an ESD pulse.
- An ideal RF ESD network has infinite impedance during RF functional applications.

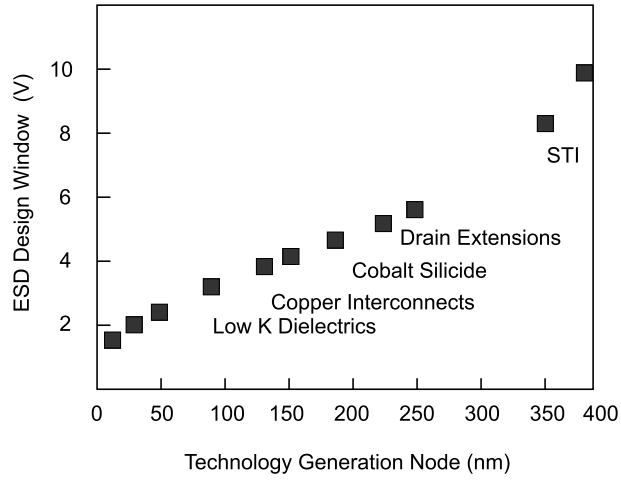

Figure 1.9 ESD design window as a function of technology generation

- An ideal RF ESD network during RF functional operation would not be a function of the current or voltage conditions.
- An ideal RF ESD network during RF functional operation is not temperature dependent.

Hence, from the frequency design window for RF ESD design, it is desirable to have an RF ESD network with zero impedance at low frequencies (e.g., HBM, MM, and CDM phenomenon regime below 5 GHz), and high impedance in the application frequency (e.g., RF application frequency regime).

Figure 1.11 shows the RF ESD frequency design window, and an ideal impedance characteristic imposed on the window. In a frequency regime below the CDM phenomenon, the ideal ESD impedance would be high during DC functional response, with zero impedance during an ESD event. At high frequencies, in the range of the RF application frequency, the impedance would have a high value (Figure 1.12).

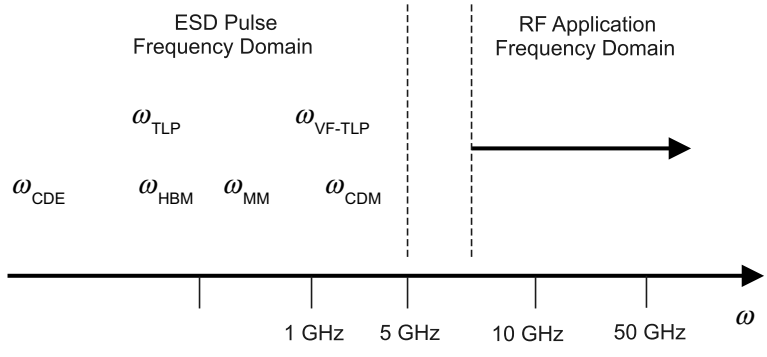

Figure 1.10 RF application frequency and ESD pulse event frequency

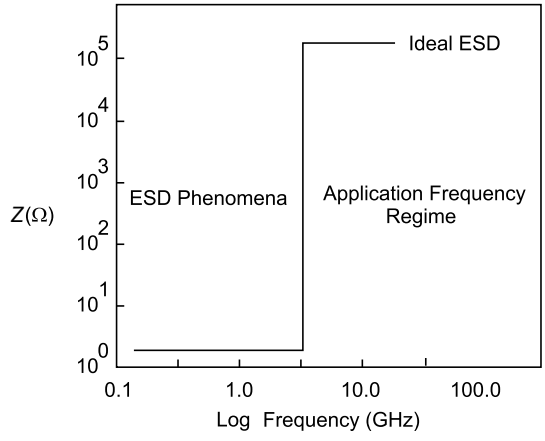

Figure 1.11 RF ESD frequency domain design window and the RF ESD device impedance

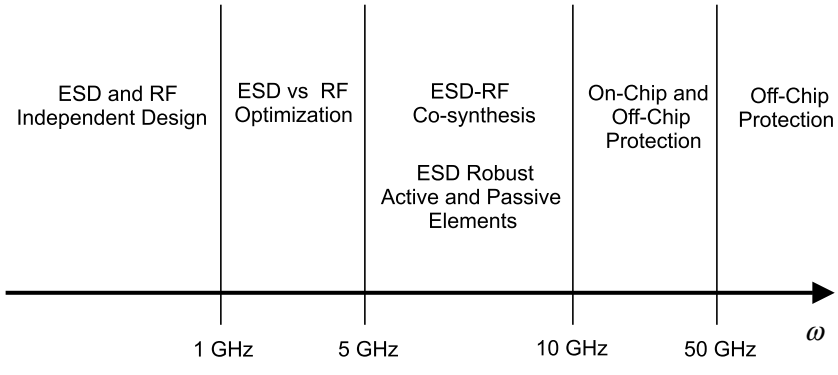

Figure 1.12 Design methodology vs. application frequency

1.4 MAPPING SEMICONDUCTOR CHIPS AND ESD DESIGNS

In semiconductor chip design, products are mapped from technology-to-technology for improved productivity. Designs are mapped from one foundry to another, and from technology generation to technology generation. Designs undergo re-mapping from bipolar to CMOS [6–8,39–41], and CMOS to SOI processes [6–8,11,41–44]. Additionally, there are both generational changes as well as productivity "shrinks." In this process the ESD design synthesis is influenced.

1.4.1 Mapping Across Semiconductor Fabricators

In semiconductor development, it is not uncommon to implement the same semiconductor chip design in multiple semiconductor fabrication facilities in today's business environments. Mapping of a semiconductor chip can occur in the following manner:

- Multiple semiconductor fabricators using the same technology.
- Multiple semiconductor fabricators using different technologies.

In the case of a utilization of multiple semiconductor fabricators, two different manufacturing lines can satisfy the same electrical specifications but in fact have unique features that influence the ESD semiconductor design. Semiconductor variations that influence ESD results can be as follows:

- Incoming wafer specifications for doping concentration.
- Incoming wafer specifications for epitaxy thickness.
- Photolithography tool bias conditions.
- Etch bias conditions.

In many manufacturing processes, the specifications contain only a lower-bound condition for some values. In other cases, although there is a range for a specification, there is variation within the specification window that can influence ESD results.

As an example, incoming wafers may be supplied from different vendors to different manufacturing facilities. Although the wafer specification is equivalent, the wafers may be "centered" differently within the specification window. In a p-/p++ substrate wafer, the epitaxial thickness may vary within the specification, as well as the measurement technique to control epitaxial thickness. In one case, a CMOS semiconductor chip was mapped into three different facilities on a p-/p++ wafer in a single-well semiconductor process. The ESD protection solution was a silicon controlled rectifier (SCR), whose triggering means the n-well-to-substrate breakdown. In the three different facilities, the breakdown voltages were different, leading to a different triggering voltage for the same semiconductor design. As a result, only one facility achieved the HBM ESD objective, whereas the other facilities did not.

To guarantee ESD equivalent results from fabricator-to-fabricator for a given technology, all electrical parameters that influence the ESD networks should be verified, and controlled to equivalent parameters. Secondly, ESD testing should be performed to determine the ESD pin distribution of the semiconductor product; this can be achieved by testing all signal and power pins to failure.

In the case of mapping across semiconductor fabricators of different semiconductor processes, the ESD robustness of all processes is not equivalent. Semiconductor process differences can influence the ESD circuits, and the functional circuits. All process variables can influence the ESD protection levels; which process features influence the product ESD robustness is dependent on the ESD circuit type used, and worst case ESD failure mechanism. To guarantee ESD equivalent results from fabricator-to-fabricator for a different technology, all electrical parameters that influence the ESD networks should be verified. Transmission line pulse (TLP) and human body model (HBM) measurements of the semiconductor device library and the ESD circuit library may be used to verify equivalency. Secondly, ESD testing should be performed to determine the ESD pin distribution of the semiconductor product; this can be achieved by testing all signal and power pins to failure.

Given that the semiconductor fabricators provide a set of ESD benchmark structures to quantify the semiconductor technology, and ESD TLP measurements, design adjustments can be made to the ESD circuit design and functional circuitry to compensate for differences between the semiconductor fabricators.

1.4.2 ESD Design Mapping Across Technology Generations

In semiconductor development, semiconductor chip designs are mapped from one technology generation to another for performance improvements, chip size reduction, and cost.

In the ESD design synthesis of mapping across technology generations, the semiconductor design can undergo different design and architectural conditions. In the re-mapping from one technology generation to another technology generation, the type of mapping can influence the ESD design. Two mapping processes are as follows:

- Lower power supply voltage for both peripheral I/O and core circuitry.
- Maintain the power supply voltage on the peripheral I/O, but reduced core circuitry supply voltage.

In the first case, the reduction of the power supply voltage for the entire semiconductor chip can lead to both circuit topology and technology differences that influence the ESD results. With the lowering of the power supply voltage, given that the first generation contained elements in series, these can be reduced with the re-mapping process. With a reduction of the series elements in the ESD networks, ESD improvement can be obtained.

With the technology scaling, the physical dimensions of the devices are reduced. Dimensional scaling of the technology can influence the ESD results as follows:

- Lower dielectric breakdown voltage.
- Lower MOSFET and bipolar snapback voltage.
- Different current-to-failure.
- Different power-to-failure.
- Different voltage-to-failure.

With the technology scaling, the changes in the ESD robustness can be lower or higher, depending on the decisions of the doping concentration and film thickness. In the case where the ESD robustness is reduced, design modifications can be made to improve the product ESD results. The design modification can be the physical size of the ESD networks, innovation, or novelty.

In the second case, the product must maintain the same external or application voltages in the scaled technology. To obtain the density advantage of the scaled technology, the semiconductor chip design synthesis may take various directions:

- Single power supply supporting both mixed voltage interface circuitry.
- Single power supply, and regulated voltage for core circuitry.
- Multiple power supply pins.

In the case of many product applications, the peripheral circuitry is required to receive or transmit signals to semiconductor chips different from the native voltage of semiconductor

technology. The ESD architecture and design synthesis are highly influenced by these conditions in both digital, analog, and power designs.

1.4.3 Mapping from Bipolar Technology to CMOS Technology

In the mapping of a design from bipolar technology to CMOS technology, the ESD design must be adjusted since the bipolar transistors differ significantly from CMOS MOSFET transistors [6–8,14]. Bipolar transistors operate as vertical bulk devices, whereas MOSFET transistors operate as lateral surface devices. As a result, bipolar transistors provide lower current densities, and are more suitable for power and ESD implementations. Bipolar transistors can also be utilized as forward biased elements, or reverse breakdown devices, providing flexibility in the different types of implementations.

In the bipolar implementations, bipolar transistors are utilized for ESD protection on the signal pins, and the power rails. Bipolar transistors are typically used in collector-to-emitter configuration. Bipolar transistors are also used in diode configuration (e.g., base-collector, or emitter-base). In the mapping of a schematic design from bipolar technology to CMOS technology, bipolar diodes can be mapped directly as CMOS-based p–n diode elements formed out of diffusions and wells [8]. ESD inputs that are grounded base bipolar circuits (e.g., collector connected to input, and emitter connected to ground) can be mapped into grounded gate MOSFETs. ESD power clamps between power rails can be mapped from bipolar collector–emitter configured networks to grounded-gate triggered MOSFET power clamps or RC-triggered MOSFET power clamps.

One of the critical differences is that the size and layout of the implementations are significantly different between the bipolar elements and the CMOS elements (Figure 1.13). Since the bipolar transistors are bulk devices, and MOSFETs are surface devices, the perimeter and width of the MOSFET ESD devices are increased to achieve the same levels of ESD robustness.

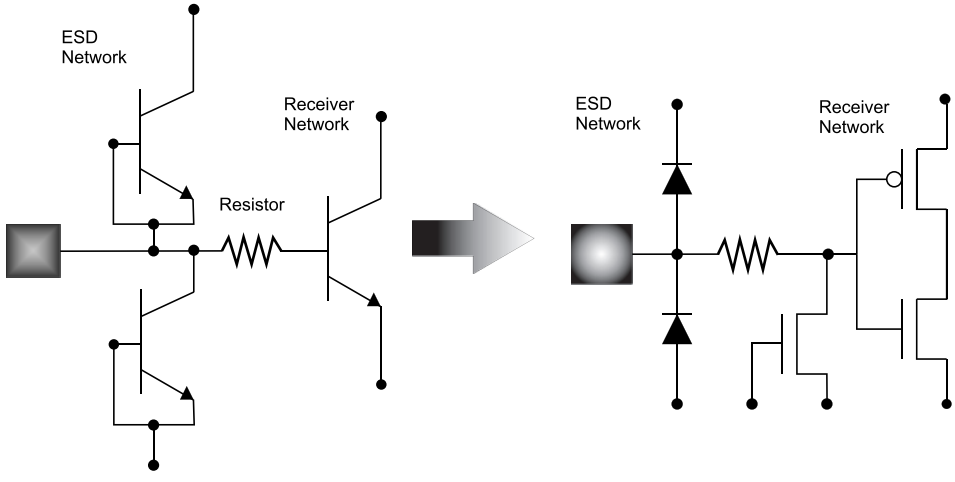

Figure 1.13 Mapping of bipolar to CMOS technology

1.4.4 Mapping from Digital CMOS Technology to Mixed Signal Analog–Digital CMOS Technology

In the mapping of a semiconductor chip from a digital CMOS technology to a digital–analog technology, the ESD design synthesis, architecture, and physical elements may require adjustments [14]. With the introduction of an analog domain, modifications are needed in the architecture of the semiconductor chip. Digital and analog domains are required to be established, as well as ESD protection for each independent power domain. In addition, added ESD protection is needed for signal lines that cross both domains. Digital designs also typically have simple connections, whereas analog networks typically have a higher number of electrical connections to many different sub-functions.

Another key difference is that the floorplanning of the semiconductor chip into separated analog and digital domains influences the placement of the physical elements and the electrical connections. In addition, the analog design layout may consist of different analog design layout considerations of both active and passive elements; these practices will be discussed in later sections of the text.

1.4.5 Mapping from Bulk CMOS Technology to Silicon on Insulator (SOI)

For performance enhancements, CMOS designs can be mapped from bulk CMOS to silicon on insulator (SOI) technology [6,7,11,43,44]. In the mapping from a bulk CMOS technology to an SOI technology, modifications are required in both the functional circuitry and the ESD designs. Mapping of the ESD design will be dependent on the ESD device choice, the thickness of the silicon film, the isolation, the technology features, and technology type. Various forms of SOI technology exist:

- Thin film partially depleted SOI (PD-SOI) MOSFET.
- Thick body partially depleted SOI (PD-SOI) MOSFET.
- Thin body fully depleted SOI (FD-SOI) MOSFET.
- SOI FinFET technology.
- Bipolar CMOS–DMOS SOI.

In partially depleted SOI (PD-SOI) technology, the MOSFET junctions extend to the buried oxide (BOX) region [6,7]. The silicon film on the BOX region is on the scale of the MOSFET junction depth. Isolation is formed, which extends from the device surface to the BOX film. The introduction of the BOX film, and integration with the isolation technology, leads to the elimination of all desired and undesired parasitic elements under the isolation structure. From an ESD perspective, all undesired parasitic elements are eliminated. For I/O and ESD elements, isolating guard rings are no longer required. External latchup and internal latchup is no longer an issue in thin body PD-SOI.

In the re-mapping process from CMOS to PD-SOI, the diode elements and SCRs can not conduct current vertically, or under the isolation region; this leads to modification of the ESD

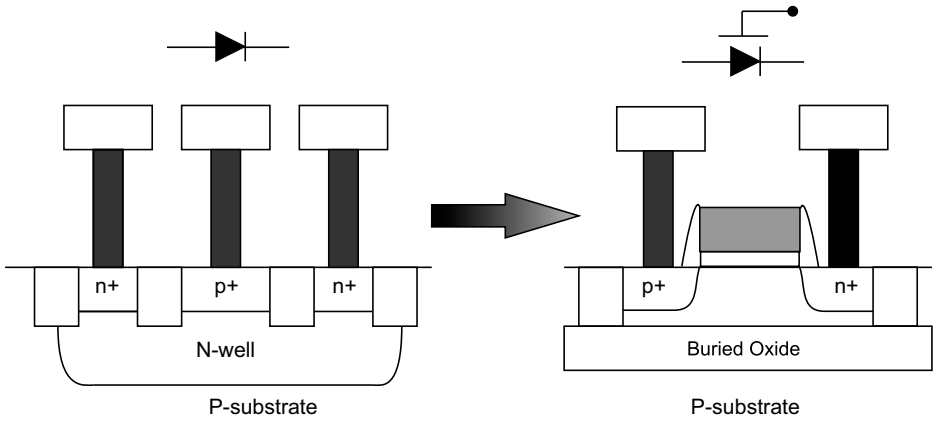

Figure 1.14 Mapping of bulk CMOS to SOI technology

networks to allow a conduction path. Lateral elements will be required for ESD protection due to the elimination of any active device under the isolation structure. As a result, new ESD structures will be required.

For thick body PD-SOI, the buried oxide film extends under the well or buried layer depths and does not fully isolate the p-channel MOSFET and n-channel MOSFET devices. The isolation structure may extend to the buried oxide film, allowing separation of tubs and floating relative to the substrate wafer. As a result, in the re-mapping from CMOS to thick body SOI, ESD networks that utilize surface devices may not require design modification.

For bulk bipolar CMOS–DMOS (BCD) technology, the depth of the BOX region separates the devices from the substrate wafer, and provides isolation of the different device types. The devices that extend to the BOX region will be influenced in the mapping process. The BOX region will influence both the breakdown voltages and the current conduction. As a result, ESD networks will require modifications.

In the mapping from bulk CMOS to FinFET technology, the layout and design of all devices in the technology are modified [11]. ESD networks will also be required to be modified due to the means of current distribution in the FinFET structure (Figure 1.14).

1.4.6 ESD Design – Mapping CMOS to RF CMOS Technology

Today, many designs are being defined from a CMOS base to an RF CMOS base technology [8,11,39–41]. CMOS-based designs are typically developed as a custom layout, including the ESD networks. In the CMOS ESD designs, the designs are not scalable elements and typically do not have scalable models.

Ironically, today many applications are using RF CMOS technology for the usage of the scalable models and AC models. In many application spaces, RF CMOS foundry technologies are being used for the higher-quality models. For analog design, small and large signal models are needed in the linear and the saturation region of the MOSFET devices, as well as in high-quality passive elements with good matching characteristics.

In the mapping of a digital or analog design into an RF CMOS technology, the ability to have better-quality AC models is available. For ESD design, it is also possible to have ESD designs

with scalable elements. ESD designs can be constructed from parameterized cell elements. The primitive ESD design elements can be hierarchically defined, forming hierarchical parameterized cell ESD networks. Such elements can be constructed in a Cadence™ design environment [8]. By using an RF CMOS technology, the design synthesis environment allows for this ESD design strategy.

In the mapping of CMOS to RF CMOS, the circuit topology of the RF networks will introduce passive elements, such as capacitors and inductors [8]. Inductors and capacitors are used for DC isolation, input and output matching, filters, and matching. Inductors and capacitors are preferred resistor elements. As a result, in the re-mapping of circuits to RF CMOS, resistor elements are replaced by both capacitor and inductor elements. In ESD networks, typical CMOS ESD solutions (such as resistor ballasting and series resistor elements) are replaced with inductive and inductive–capacitive techniques.

In addition, in the ESD design synthesis, the RF circuits and ESD networks must be co-synthesized [8]. ESD-RF design co-synthesis is needed to achieve the RF performance objectives and matching characteristics.

1.5 ESD CHIP ARCHITECTURE, AND ESD TEST STANDARDS

The ESD standards are written to test the ESD robustness between possible "events." These events contain two features. The first feature is a given waveform. The second feature is the possible interactions that can occur within a semiconductor chip. The possible interaction is the case that a given pin receives an ESD event, and a second pin is the reference ground. The first feature tests the nature of the pulse, and the second feature is evaluating the current paths. In the ESD standards, different procedures exist in application of the ESD pulse to the pin or package, as well as the "pin combinations."

1.5.1 ESD Chip Architecture and ESD Testing

The pin combinations are evaluating the ESD robustness of the possible paths, which in essence is testing the existence of a suitable ESD current path to discharge the ESD current. As a result, the chip architecture must be constructed to establish current paths, alternate current paths, and "elements" within the path that are suitable to discharge the ESD current. The elements in the path are the devices, circuits, and electrical interconnects within the path.

A key point is that for some of the ESD standards, the semiconductor chip architecture is structured to satisfy the ESD pin combinations of the ESD test standard.

1.6 ESD TESTING

In this section, a brief discussion of ESD testing will be given, with relevance to ESD chip architecture. As stated in the last section, the architecture of the chip is structured to pass the ESD testing procedure. As a supplier, or customer, it is an expectation that a certain number of ESD test standards are performed, and achieve given objectives.

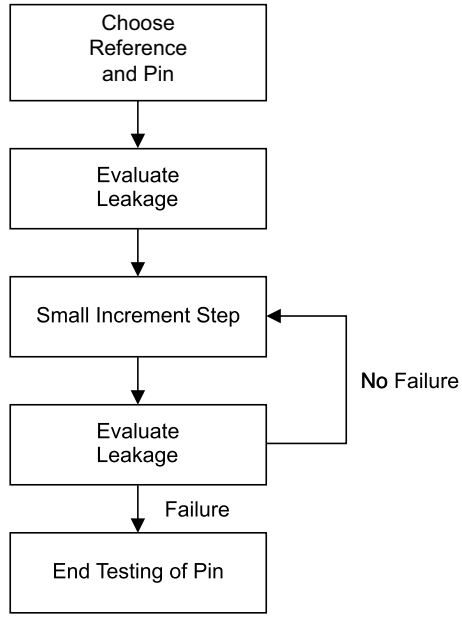

Figure 1.15 ESD test flow

1.6.1 ESD Qualification Testing

Qualification testing to demonstrate ESD robustness is performed by the supplier, or customer. ESD testing is typically completed in the environment that it is shipped from the supplier to the customer. Figure 1.15 is an example of the ESD test flow. The ESD testing can be completed on wafer, bare die, or packaged components. The majority of the ESD testing standards are defined and structured to address the packaged component.

1.6.2 ESD Test Models

ESD specifications contain different waveforms and pin combinations depending on the intent of the ESD event that the procedure is to simulate [47–82]. Component-level ESD test models include the following:

- Human body model (HBM) [47–53].
- Machine model (MM) [54].
- Charged device model (CDM) [55].
- Socketed device model (SDM).
- Human metal model (HMM) [79–82].

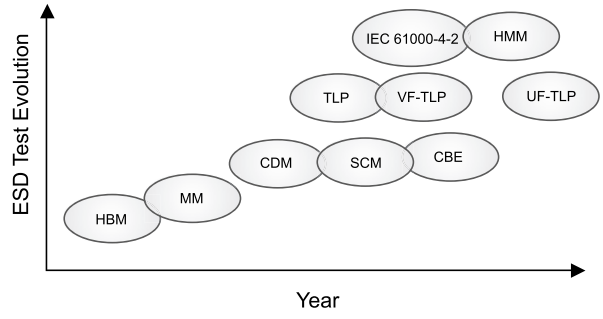

Figure 1.16 ESD testing evolution

ESD system-level tests, presently being performed on chips, sub-systems, and systems, are as follows [56–64,76–82]:

- Charged board event (CBE).
- Cable discharge event (CDE) [56–64].
- IEC 61000-4-2 ESD pulse [76–79].
- Human metal model [79–82].

Figure 1.16 is a chart demonstrating the evolution of testing in the semiconductor industry. The HBM test model was the first developed ESD specification for qualification of semiconductor devices. This was followed by the MM test specification, and CDM test specification. Today, there are additional test specifications at various phases of becoming ESD test standards.

1.6.3 ESD Characterization Testing

ESD characterization tests that are being performed on wafers and on packages include the following [47–54,65–75]:

- Human body model (HBM) [47–53].
- Machine model (MM) [54].
- Transmission line pulse (TLP) [65–68].
- Very fast transmission line pulse (VF-TLP) [69–74].
- Ultra-fast transmission line pulse (UF-TLP) [75].

Wafer-level HBM and MM testing can be performed as a two-pin test.

1.6.4 TLP Testing

ESD characterization tests that are being performed on wafers and on packages include the following [65–75]:

- Transmission line pulse (TLP) [65–68].

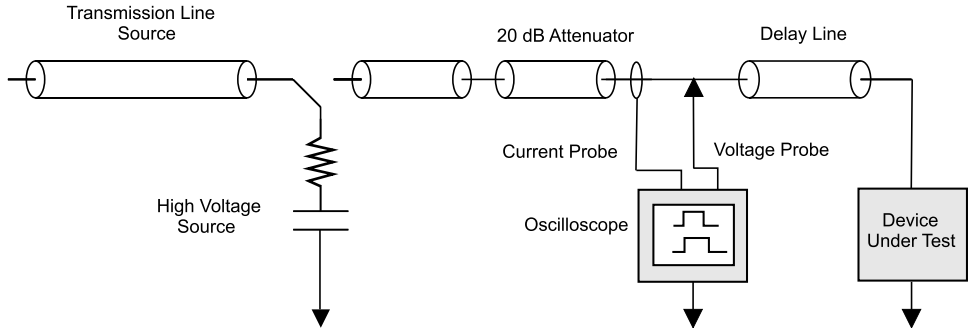

Figure 1.17 TLP test system

- Very fast transmission line pulse (VF-TLP) [69–74].
- Ultra-fast transmission line pulse (UF-TLP) [75].

In Figure 1.17, an example of a TLP system is shown. In a TLP system, a transmission line (TL) cable is charged by a high-voltage source. A switch is closed to apply the stress to the device-under-test (DUT). The TL pulse width is defined by the length of the cable in a given test system. The voltage and current are measured across the device under test as the pulse propagates through the device. There are various configurations of the TLP system. In some TLP systems, the configurations are such as to measure the reflected and transmitted signal through the device. A current and voltage value is determined in the device through averaging of the data in a "measurement window" within the pulse event.

A pulsed *I–V* characteristic can be constructed by increasing the voltage on the cable, and extracting the (*I*,*V*) data points in this successive step stress. Figure 1.18 shows an

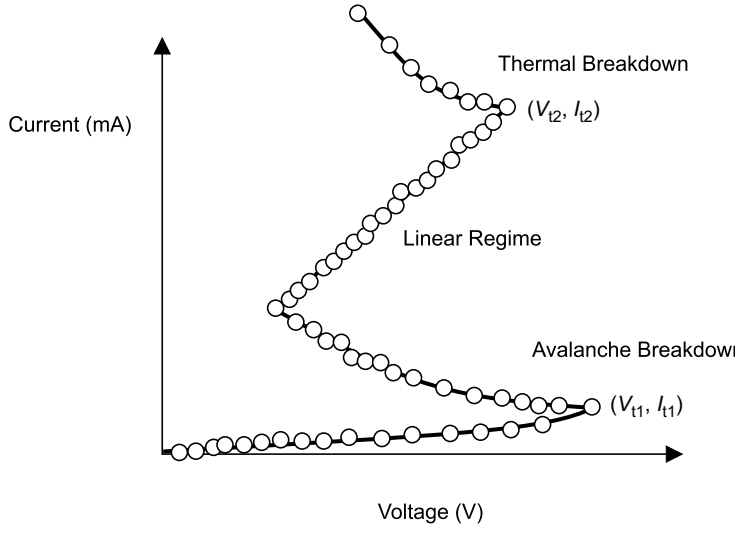

Figure 1.18 TLP pulsed *I–V* characteristic

example of a TLP pulsed *I–V* characteristic. Each point represents a single pulse in the step stress, where the (*I*,*V*) point is an averaged measurement extracted from the measurement window.

1.7 ESD CHIP ARCHITECTURE AND ESD ALTERNATIVE CURRENT PATHS

In the ESD design synthesis of a semiconductor chip, both the electrical characteristics and the physical placement are key to good full-chip ESD design. In the following section, a brief introduction is provided on the chip architecture of the I/O circuits, cores, and ESD elements.

1.7.1 ESD Circuits, I/O, and Cores

In the design synthesis of a semiconductor chip, the physical placement and chip architecture of the I/O circuits, the ESD elements and the core circuitry are key to the planning process, as well as the success of the implementation in achieving ESD robust designs [1–14].

I/O circuitry physical placements are found for a semiconductor chip as follows:

- **Peripheral I/O:** Periphery of the semiconductor chip.
- **Internal I/O Banks:** Large I/O clusters (also referred to as "banks") within the semiconductor chip interior.
- **Small Internal I/O Banks:** Small I/O clusters (e.g., "nibble" architecture) within the semiconductor chip interior.
- **Array I/O:** Individual "array" I/O distributed within the semiconductor core.

In each of these different design implementations, the architectures introduce new challenges to the ESD design synthesis implementation. The placement of the ESD signal pin devices, within domain ESD circuits (e.g., ESD power clamps) and domain-to-domain ESD circuits (e.g., ground-to-ground) are highly influenced by these architectures. In future sections, these will be discussed in great detail.

1.7.2 ESD Signal Pin Circuits

ESD circuits are placed on signal pins to re-direct the ESD current from the signal path to an alternative current path [7]. The ESD signal pin circuitry establishes connectivity to at least one power rail. ESD signal pin networks can be classified as follows:

- Single power rail connectivity.
- Dual power rail connectivity.
- Triple power rail connectivity.

Single power rail signal pin ESD networks are used in NMOS, CMOS, bipolar, DMOS, and BCD technologies. Examples of single power rail signal pin ESD networks are as follows:

- NMOS – thick oxide MOSFET – resistor – thin oxide MOSFET.
- CMOS – grounded gate NMOS (GGNMOS).
- CMOS – SCRs.
- Bipolar – grounded base bipolar in collector–emitter configuration.
- DMOS – grounded gate LDMOS transistor.

The advantage of a single power rail connected ESD signal pin network is that it is typically not connected to the power supply voltage, but connected to a ground power rail. This avoids issues associated with power-up and power-down conditions, power rail sequencing, power loss, and fail-safe conditions. The disadvantage is that during the reference grounding of the power rail V_{DD}, there is no current path established. These structures provide one mode of operation in a forward bias mode, and a second in reverse bias mode.

Dual power rail signal pin ESD networks are used in CMOS, bipolar, DMOS, and BCD technologies. Examples of dual power rail signal pin ESD networks are:

- CMOS – dual diode ESD networks.
- CMOS – series diode ESD networks.
- CMOS – dual silicon controlled rectifiers (DSCRs).
- LDMOS – dual diode configured LDMOS transistors.

The advantage of a dual power rail connected ESD signal pin network is that it is connected to the power supply voltage and ground power rail. Figure 1.19 shows a dual power rail connected ESD network. This establishes two alternative forward bias current paths and electrical connectivity to both power rails for positive or negative ESD pulse events. In these networks, the voltage across the structure is significantly less due to the low turn-on voltage, leading to less power density in the metallurgical junctions.

Triple rail ESD signal pin networks are also used in applications with multiple power or ground connections. An example is as follows:

- CMOS – DRAM triple rail ESD networks.

The advantage of triple rail ESD networks is that they establish direct connectivity to separate power supplies, or separate ground connections. Triple rail ESD networks also save significant space and have low capacitance.

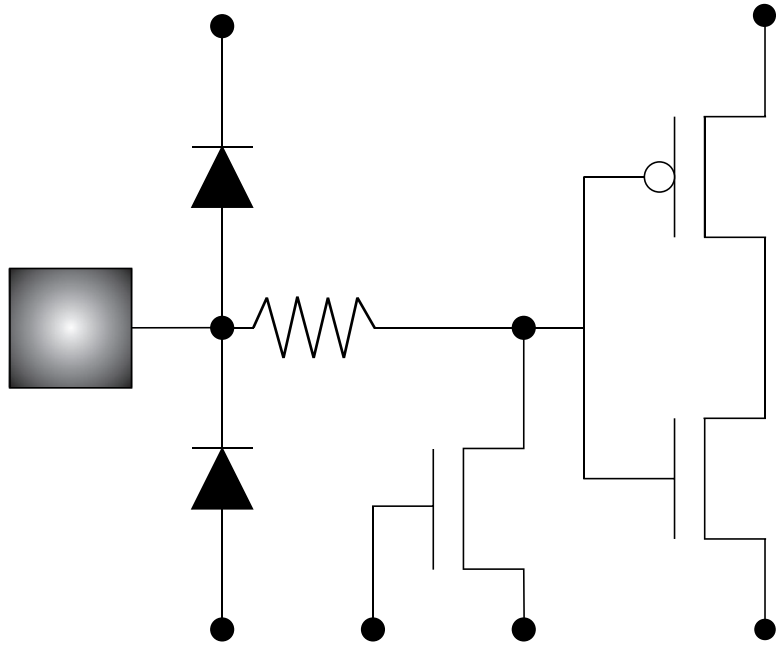

Figure 1.19 ESD input circuit

1.7.3 ESD Power Clamp Networks

In the ESD design synthesis, within a given circuit power domain, ESD networks are placed between the power and ground rails to improve the ESD robustness of the semiconductor chip [1–14].

ESD power clamps serve several purposes in the ESD design methodology:

- **Power Rail ESD Protection:** ESD power clamps provide ESD protection between the power rails (e.g., V_{DD}) and ground rails (e.g., V_{SS}).
- **Over-voltage Protection:** ESD power clamps provide over-voltage and over-current protection to the functional circuits in parallel with the ESD power clamp.
- **Alternative Current Loop:** ESD power clamps provide closure of an alternative current loop between signal pins and its power and ground rails.
- **Bi-directionality:** ESD power clamps establish bi-directional current paths between the power rail and the ground rails.
- **Signal Pin to Signal Pin:** ESD power clamps provide pin-to-pin ESD protection by establishment of a bi-directional current path (in conjunction with the ESD signal pin devices).
- **Low Impedance:** ESD power clamps lower the impedance of the semiconductor chip from the power rail to its associated ground rail in the alternative current loop.

- **Impedance Independence for Chip Capacitance:** ESD power clamps provide independence of the impedance of the semiconductor chip in the ESD protection process.

ESD power clamps can be classified as follows:

- Voltage-initiated forward bias ESD clamps.
- Voltage-initiated reverse bias breakdown ESD clamps.
- Active circuit-initiated ESD power clamps.
- Frequency-triggered ESD power clamps.
- Frequency and voltage-triggered ESD power clamps.

ESD power clamps can serve native-voltage, mixed-voltage, or high-voltage semiconductor chip sectors. ESD power clamps use both passive and active elements. For CMOS technology, ESD power clamps are formed using MOSFETs, diode, resistor, and capacitor elements. For bipolar technology, the ESD power clamps are constructed of bipolar transistors, varactors, and resistor elements. In a BiCMOS technology, both CMOS-based and bipolar-based ESD power clamps can be utilized. In addition, hybrid BiCMOS ESD power clamps can be formed that utilize both bipolar and MOSFET transistor elements in the same ESD power clamp circuit. In a power technology, the ESD power clamps can utilize PDMOS and NDMOS transistor elements. Figure 1.20 shows an example of an ESD power clamp.

1.7.4 ESD Rail-to-Rail Circuits

In the architecture of a semiconductor chip, the power grid is separated into different power domains. Power domains are separated for the following reasons:

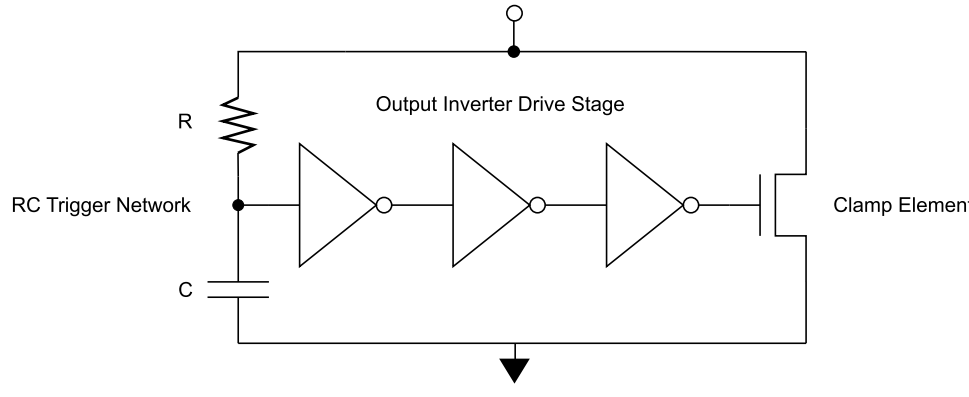

Figure 1.20 ESD power clamp

- Noise isolation between grounds.
- Different power supply voltage requirements.
- Different circuit functions.

ESD failure mechanisms can occur with the separation of ground rails. This can occur in the following applications:

- ESD failure between peripheral I/O circuit ground (e.g., V_{SS}(I/O)) and chip substrate (V_{SUB}).
- ESD failure between peripheral I/O circuit ground and core ground.
- ESD failure between digital ground (e.g., V_{SS}) and analog ground (e.g., AV_{SS}).
- ESD failure between digital ground (e.g., V_{SS}) and radio frequency ground (RFV_{SS}).

ESD networks are needed between the power rails to establish a current path between the power rails. Establishment of a current path between the power rails provides both ESD protection between the two power rails, and ESD protection between a signal pin to power rail.

In the architecture of a semiconductor chip, the voltage of each ground can be of the same potential ($V_{SS} = AV_{SS} = 0$) or different values ($V_{SS} = 0$, and $V_{EE} = -3$ V).

ESD failure mechanisms can occur with the separation of V_{DD} power rails. This can occur in the following applications:

- ESD failure between peripheral I/O circuit (e.g., V_{DD}(I/O)) and chip power (V_{DD}).
- ESD failure between peripheral I/O circuit (e.g., V_{DD}(I/O)) and core (V_{DD}) with a regulator between the two power rails.
- ESD failure between digital power (e.g., V_{DD}) and analog power (e.g., AV_{DD}).
- ESD failure between digital power (e.g., V_{DD}) and radio frequency ground (RFV_{CC}).

ESD networks are needed between the power rails to establish a current path between the power rails. Establishment of a current path between the power rails provides both ESD protection between the two power rails, and ESD protection between a signal pin to power rail.

In the architecture of a semiconductor chip, the voltage of each power can be of the same potential ($V_{DD} = AV_{DD}$) or different values ($V_{CC} = 5$ V, and $V_{DD} = 3.3$ V).

A common rail-to-rail network is the usage of a bi-directional series diode string (Figure 1.21). Bi-directional diode strings can consist of CMOS diodes, bipolar transistors, or diode-configured CMOS elements.

1.7.5 ESD Design and Noise

In semiconductor chips, the switching of circuitry can lead to noise generation that can influence circuit functions. In the architecture of a semiconductor chip, different domains are separated due to noise generation. Noise is generated from undershoot and overshoot

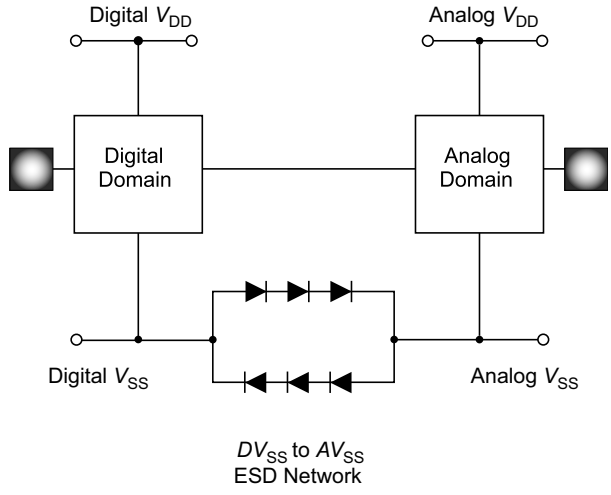

Figure 1.21 Bi-directional rail-to-rail ESD network

phenomena of signals leading to substrate injection. Noise can also be generated from switching of off-chip drivers circuitry, and large power devices.

In a semiconductor chip, there is circuitry which is sensitive to the noise generation. To avoid noise from impacting functionality of the sensitive circuitry, separate power domains are created on a common substrate. Examples of separation of power domains and semiconductor chip functions are as follows:

- Separation of peripheral circuitry from core circuitry.
- Separation of peripheral circuitry from core memory regions.
- Separation of digital and analog functions.
- Separation of digital, analog, and RF functions.
- Separation of power, digital, and analog functions.

In ESD design, the separation of different circuit domains for noise isolation can lead to ESD failures. ESD failures can occur due to the following situations:

- Lack of a forward bias current path between a first power rail and a second power rail.
- Lack of a forward bias current path between a pin of a first domain to a power rail of a second domain.
- Lack of a forward bias current path between a pin of a first domain to a pin of a second domain.

As a result, in the ESD design synthesis, the architecture of the semiconductor chip which is separated for noise, must allow for current to flow from domain to domain. As a result, there

is a tradeoff between the noise isolation and the requirement of allowance of current flow between pins and power rails of different domains. Various means have been utilized to achieve this. Examples of solutions between independent power domains are as follows:

- Symmetric and asymmetric bi-directional ESD networks between domains of $V_{DD}(i)$ and $V_{DD}(j)$.
- Symmetric and asymmetric bi-directional ESD networks between domains of $V_{DD}(i)$ and $V_{SS}(j)$.
- Symmetric and asymmetric bi-directional ESD networks between domains of $V_{SS}(i)$ and $V_{SS}(j)$.

1.7.6 Internal Signal Path ESD Networks

In ESD design, the separation of different circuit domains for noise isolation can lead to ESD failures internal to the semiconductor chip [11]. Traditionally, the majority of ESD failures occur near the signal pads, and not in internal signal lines. But, signal lines that cross power domains, where there is no current path through the power grid, leads to voltage stress internal to the semiconductor chip. Figure 1.22 is an example of a signal line that crosses the power domain from digital to analog. The solutions are as follows:

- Internal signal line ESD networks.
- Low-voltage differential domain-to-domain ESD networks.

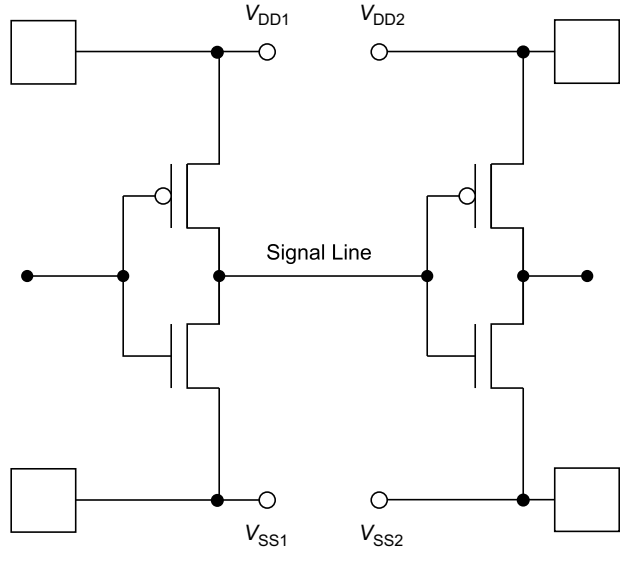

Figure 1.22 Internal signal path concern

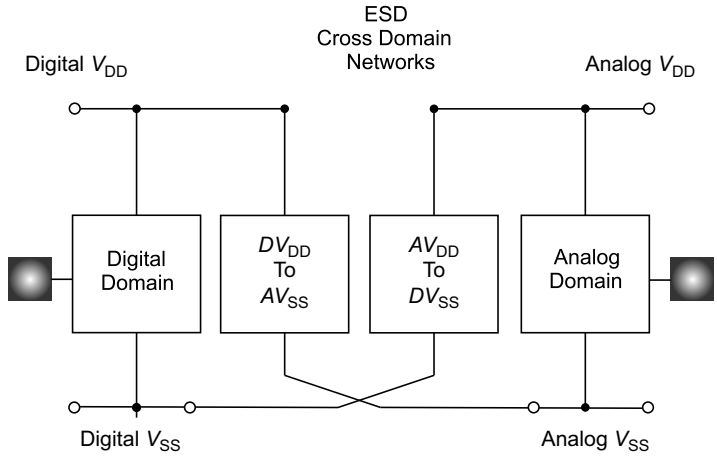

Figure 1.23 Cross-domain ESD power clamp

- Cross-domain ESD networks.
- Third-party networks between the power domains.

1.7.7 Cross-Domain ESD Networks

With the separation of power domains, the lack of a bi-directional current path through the power grid from domain to domain can lead to ESD failures. In addition, ESD failures can occur due to internal signal lines that cross domains. A solution to address this issue is to create ESD power clamp networks that cross the domains. Figure 1.23 shows an example of a cross-domain ESD network. Cross-domain ESD networks establish an electrical connection of:

- Symmetric and asymmetric bi-directional ESD networks between domains of $V_{DD}(i)$ and $V_{SS}(j)$.
- Symmetric and asymmetric bi-directional ESD networks between domains of $V_{DD}(j)$ and $V_{SS}(i)$.

1.8 ESD NETWORKS, SEQUENCING, AND CHIP ARCHITECTURE

In product applications, the sequence of power supplies and signal pins is an issue for ESD design synthesis. In some products the sequence of power to the power rails and signal pins is defined, and in others it is not. The decision whether a semiconductor chip is sequence dependent or sequence independent can influence the type of ESD networks that are used in the implementation [7].

In sequence-dependent applications, where the sequence of pins and power supplies is dependent, ESD circuits on signal pins can include the following:

- Diodes.
- Series diodes.
- Triple-well series diodes.
- MOSFETs.
- Series cascode MOSFETs.
- Silicon controlled rectifiers.

In sequence-dependent applications, the sequence of power supplies can be specified allowing usage of ESD diodes between power supplies. ESD series diodes can be placed between power supplies with different voltage levels or the same voltage level when the application specifies the procedure for power-up and power-down. ESD diodes can be placed on signal pins when the power is supplied to the power rails prior to signal pins.

In sequence-independent applications, where the sequence of pins and power supplies is not specified, ESD circuits on signal pins can include the following:

- MOSFETs.
- Series cascode MOSFETs.
- Silicon controlled rectifiers.

Sequence-independent networks that use control networks can be utilized on the power supplies and signal pins ESD circuits. Control networks and switch networks can be utilized to sense the voltage state of the signal pin or power supply to prevent forward biasing of ESD networks. Control networks can be utilized for both non-isolated and isolated epitaxial and well regions.

1.9 ESD DESIGN SYNTHESIS – LATCHUP-FREE ESD NETWORKS

In ESD design synthesis, ESD networks can lead to CMOS latchup. Latchup can be initiated in a powered state of the functional semiconductor chip [9,12].

In ESD design, it is an objective to provide an ESD network that is “activated” when an ESD event occurs, and disabled during functional operation. Functional operation leads to a powered state which includes the following:

- Power-up.
- Power-down.

- Sequencing of the independent power supplies.
- Direct current (DC) operation.
- Alternating current (AC) operation.

Additional conditions also exist that are of concern:

- System-level transient excursions.
- Board-level transient excursions.
- Reliability stress conditions.
- Latchup simulation stress testing.

During the release of a product, the ESD network must not latchup during any of these conditions. ESD networks that have a tendency to latchup are the following [9,12,14]:

- High-voltage silicon controlled rectifiers (HV-SCR).
- Medium-voltage silicon controlled rectifiers.
- Low-voltage triggered silicon controlled rectifiers (LVTSCR).
- Grounded gate silicon controlled rectifiers (GG-SCR).
- PNP-triggered SCR (PNP-SCR).
- PMOS-triggered SCR (PMOS-SCR).

To avoid CMOS latchup, in the ESD network design synthesis, the following requirements must exist:

- **Minimum Voltage Condition:** The ESD SCR network must have a "trigger voltage" condition above the worst case power supply condition, and above the reliability stress voltage requirements.
- **Maximum Voltage Condition:** The ESD SCR network must have a "trigger voltage" condition below the absolute maximum voltage condition (maximum condition without electrical damage to the component).
- **Minimum Current Condition:** The ESD SCR network must have a "holding current" condition above the latchup specification current condition (e.g., 100 mA).
- **Maximum Current Condition:** The ESD SCR network must have a "holding current" condition below the maximum current condition (maximum current condition without electrical damage to the component).

Figure 1.24 shows an example of an ESD design box for an ESD network SCR that demonstrates the above voltage and current requirements. In the figure, the trigger voltage of the ESD element exceeds the latchup specification current magnitude.

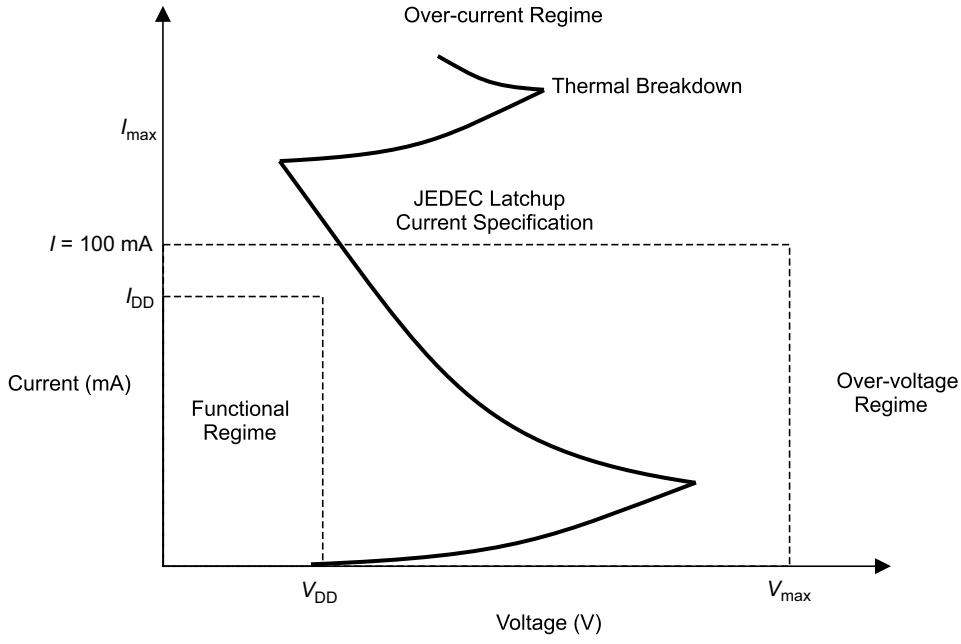

Figure 1.24 ESD design box for latchup-free SCR ESD network

1.10 ESD DESIGN CONCEPTS – BUFFERING – INTER-DEVICE

In the semiconductor chip architecture, a technique to avoid current flow to the sensitive circuits is to integrate "buffering" into the circuit net [7]. Adding series impedance in the signal path provides margin to transfer the current to the alternative current loop established by the ESD networks. In digital and analog circuits, adding resistance in series is a well-established practice. In RF circuits, capacitive and inductive elements can be introduced to avoid current flow to the sensitive active elements.

Buffering elements can serve the following roles:

- **Current:** Lower the current flow through the signal path.
- **Voltage:** Lower the voltage at the signal pin node with formation of a "resistor divider" network.
- **Impedance Matching:** Impedance matching of signal pins.

Buffering elements can be resistors that are inherent in the signal pin, or added resistance. The resistor elements can be as follows:

- Metal layer interconnects (e.g., aluminum or copper).
- Local metal interconnects (e.g., tungsten "M0" wiring layer).
- Polysilicon resistor.

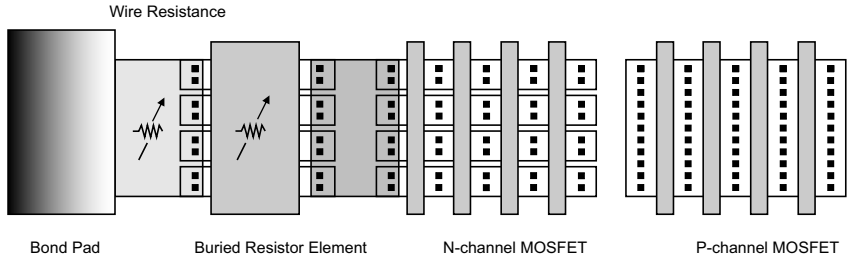

Figure 1.25 ESD design synthesis of buffering and impedance matching resistor element

- Diffused resistors (e.g., n-diffusion, n-well, buried resistors).
- Active elements (e.g., MOSFET or bipolar transistor).

The series resistor "buffering element" can be integrated inside or outside the ESD network. It is common practice to integrate the buffering element in a multi-stage ESD network. With integration of the resistor into a multi-stage ESD network, the resistor element can also reduce the voltage at the signal pin node by formation of a "resistor divider" with an ESD shunt element.

The integration of buffering can also be placed in sophisticated design methodologies to address impedance matching and ESD protection (Figure 1.25). A high-performance design methodology is to impedance match all identical pins independent of the wiring to the specific pin. In an "array I/O" architecture, each pin may be located in a different location. Hence, it is a design methodology to place a resistor that is adjustable so that the sum of the wire interconnect resistance and the series resistance is a constant. In this fashion, the impedance of all identical pins is the same. This design methodology is also satisfactory for ESD development as well, since it will reduce the ESD variation based on pin location.

1.11 ESD DESIGN CONCEPTS – BALLASTING – INTER-DEVICE

In the ESD design synthesis techniques, ballasting is utilized to both limit and distribute the ESD current within a circuit [7]. In a circuit with parallel circuit elements, ballasting is utilized to prevent a single element undergoing over-voltage or thermal runaway. By limiting the current flow through a given element, the current will re-distribute through the parallel elements.

Ballasting is utilized in both functional circuits and ESD networks [7]. In semiconductor technology, ballasting is a common practice within output circuits and power circuits. Ballasting techniques are used in an output circuit that has multiple parallel elements to improve the current distribution through the elements. Ballasting is used in output circuits, such as off-chip driver (OCD) elements. Ballasting techniques can be used in both bipolar transistors and MOSFET transistors. Ballasting is also utilized in LDMOS technology, to improve the power distribution in large power devices [14,26–30].

Ballasting is also utilized within an ESD network. Inter-device ballasting is commonly used in the following ESD networks:

- Grounded gate n-channel MOSFET networks.
- Grounded base bipolar collector-to-emitter networks.

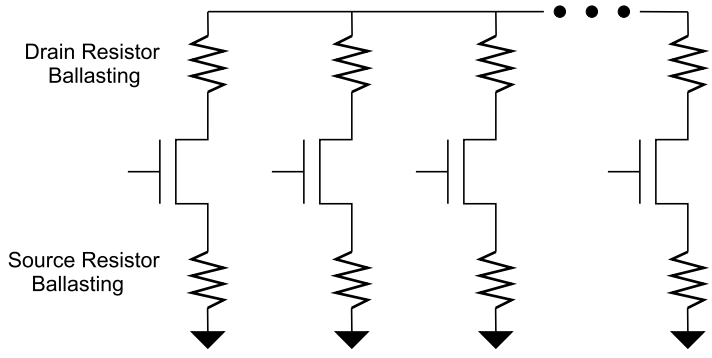

Figure 1.26 Multi-finger MOSFET with resistor ballasting

Ballasting is achieved using series resistor elements. These resistor elements can be independent resistor elements, or integrated with the bipolar or MOSFET element. Resistor elements used for ballasting are as follows:

- N-well resistors.
- Buried resistor (BR) elements.
- N-diffusion resistor MOSFET source/drain with silicide block mask.
- P-diffusion resistor MOSFET source/drain with silicide block mask.
- Polysilicon resistor.
- Bipolar base resistor.

Figure 1.26 shows an example of a MOSFET circuit with introduction of ballasting. Ballast resistors are introduced in series with the MOSFET element. The ballast resistor can be placed in series with the MOSFET drain or source region. It is common to introduce the MOSFET ballast resistor in the drain region.

Figure 1.27 shows an example of a bipolar circuit with the introduction of ballasting [8]. Ballast resistors are introduced in series with the bipolar element. The ballast resistor can be

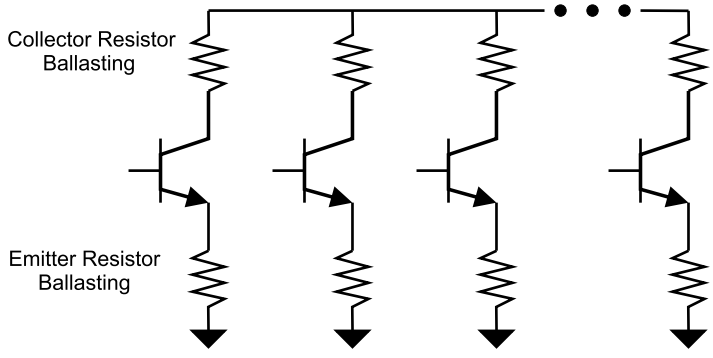

Figure 1.27 Bipolar circuit with resistor ballasting

placed in series with the bipolar base, collector, or emitter region. It is common to introduce the bipolar ballast resistor in the emitter region to provide ballasting between the bipolar collector and emitter in off-chip driver circuitry.

1.12 ESD DESIGN CONCEPTS – BALLASTING – INTRA-DEVICE

In the ESD design synthesis techniques, ballasting can be introduced into a single device element to improve current distribution along the width of the physical structure [7,8]. Ballasting is utilized to both limit and distribute the ESD current within a circuit element. Within a single device element, ballasting can be achieved through semiconductor process features or physical layout.

In a circuit with parallel circuit elements, ballasting is utilized to prevent a single element undergoing over-voltage or thermal runaway. Ballasting within a single element prevents electro-current constriction within a given physical element and re-distributes the current spatially within that physical element.

Ballasting can be introduced by semiconductor process solutions. Physical regions which can lead to improvement in ballasting are as follows:

- N-well sheet resistance.
- Buried-layer sheet resistance.
- Sub-collector sheet resistance.

Lateral resistance can be improved by the introduction of silicide blocking masks. Silicide blocking masks can be used as follows:

- MOSFET source/drain region.
- Bipolar extrinsic base region.

1.13 ESD DESIGN CONCEPTS – DISTRIBUTED LOAD TECHNIQUES

In semiconductor chip design, a concern of circuit designs is the loading capacitance of an ESD circuit and its impact on circuit performance on signal pins. Most ESD elements contain silicon junctions, leading to an increase in the capacitance on a signal pin. An ESD design practice of using a distributed ESD structure leads to a reduction in the loading effect on the signal pins [8]. This can be achieved using a multi-stage ESD network; this ESD design practice can be implemented in both high-speed digital and RF applications. Using series resistor elements, the ESD network can form a resistor–capacitor (RC) transmission line. Using a series inductor, the ESD network can form an inductor–capacitor (LC) transmission line. Figure 1.28 provides an example of a multi-stage network. Some examples of multi-stage ESD networks are as follows:

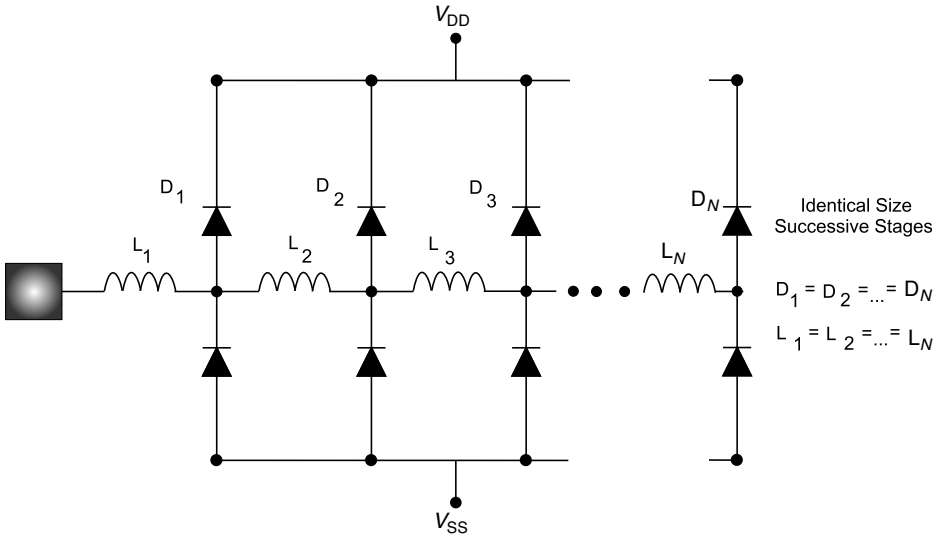

Figure 1.28 ESD distributed load techniques

- Primary dual-diode network, series resistor, and secondary dual diode network, ad infinitum.
- Primary dual-diode network, series inductor, and secondary dual-diode network, ad infinitum.
- Grounded gate MOSFET, series inductor, grounded gate MOSFET, ad infinitum.

1.14 ESD DESIGN CONCEPTS – DUMMY CIRCUITS

An ESD design discipline technique is the usage of auxiliary circuits for improved ESD robustness [7,8,11]. Auxiliary circuits, or "dummy circuits," can be used in ESD design for the following applications:

- De-coupling from signal pins.
- Disabling of feedback networks on signal pins.
- Disabling of well and tub structures.
- De-coupling from power supply rails.
- Disabling of feedback networks connected to power rails.
- Connections to "floating" structures.
- Impedance matching to an active circuit.

Auxiliary circuits can be used to de-couple elements or sub-circuits from a signal pin during electrical overstress or ESD events. De-coupling can be achieved through resistor elements,

capacitor elements, or active ESD dummy networks. In addition, dummy circuits can disable or de-couple feedback networks that can be "pinned" during ESD stress.

Auxiliary circuits can be used to de-couple elements or sub-circuits from a power rail during electrical overstress or ESD events. De-coupling can be achieved through passive elements or active ESD dummy networks.

Dummy circuits can be used to connect to "floating" structures that can undergo ESD stress. Bond wire pads, metal structures, MOSFET gate structures, and wafer substrates are left "floating" in some semiconductor applications that lead to ESD failures. An ESD design practice is to connect these structures to passive elements, active circuits, or ESD networks to avoid electrical overstress.

Dummy circuits are also used to provide "impedance matching" between parallel circuit elements. This ESD design discipline practice is used in OCD circuitry.

1.15 ESD DESIGN CONCEPTS – POWER SUPPLY DE-COUPLING

An ESD design concept is the usage of a means to de-couple the ESD power supply [7,8,11]. This is achieved by de-coupling of elements in the ESD current path. Circuit elements can be introduced which lead to the avoidance of current flow to those physical elements. The addition of "ESD de-coupling switches" can be used to de-couple sensitive circuits as well as to avoid the current flow to these networks or sections of a semiconductor chip. ESD de-coupling elements can be used to allow elements to undergo "open" or "floating" states during ESD events. This can be achieved within the ESD network, or within the architecture of a semiconductor chip.

De-coupling of sensitive elements or de-coupling of current loops can be initiated by the addition of elements that allow the current loop to "open" during ESD events [7]. During ESD testing, power rails and ground rails are set as references. The de-coupling of nodes, elements, or current loops relative to the grounded reference prevents over-voltage states in devices, and eliminates current paths. These de-coupling elements can avoid "pinning" of electrical nodes. Hence, integration of devices, circuit elements, or circuit functions that introduce de-coupling of electrical connections to ground references, and power supply references, is a key unique ESD design practice.

During ESD testing, it is a requirement to ground every independent power supply reference. As a result, unanticipated current paths are created to the reference ground power supply rail, which can lead to ESD failures.

1.16 ESD DESIGN CONCEPTS – FEEDBACK LOOP DE-COUPLING

During ESD testing, feedback can lead to unanticipated ESD failures. An ESD design concept is the usage of a means to de-couple feedback networks [7,8,11]. Feedback loops can lead to unique ESD failures and lower ESD results significantly. The de-coupling of nodes, elements, or current loops relative to the grounded reference prevents over-voltage states in devices, and eliminates current paths initiated by the feedback elements. These de-coupling elements can avoid "pinning" of electrical nodes. Hence, integration of devices, circuit elements, or circuit

functions that introduce de-coupling of electrical connections to ground references, and power supply references of the feedback elements during ESD testing, is also a key unique ESD design practice.

1.17 ESD LAYOUT AND FLOORPLAN-RELATED CONCEPTS

1.17.1 Design Symmetry

Design symmetry is an ESD design practice to maximize the ESD robustness [45]. Design symmetry is also a design practice of analog and power technologies [31–38]. The capability of the ESD network to dissipate high-current pulse events is directly related to the network's topology and its design symmetry. The more uniform the current distribution is through the ESD network during a discharge, the better the utilization of the area of the structure, and as a consequence, the greater the robustness of the circuit design.

The distribution of current during an ESD event is dependent upon the design symmetry of the ESD network and its components.

From experience, to the degree that the design of the ESD network (or structure) on all levels of the integrated circuit departs from a symmetric configuration, the greater is the current localized or non-uniformities in the ESD network. With a symmetrical distribution of the current, the peak power-to-failure per unit area is lowered, producing superior results. Additionally, the more uniform the current distribution, the more uniform the thermal field as well. Since semiconductor element electrical and thermal parameters are temperature dependent (e.g., mobility, electrical conductivity, thermal conductivity), the more uniform the current distribution, the more symmetrical the temperature distribution within the device.

In integrated circuit design, a key ESD design concept is to maintain a high degree of design symmetry within a structure on all design levels. In both the ESD network and I/O driver circuit, an evaluation of the power distribution of an ESD event within the circuit is an indicator of the robustness of the integrated circuit. Hence, physical layout design symmetry can be used as a heuristic determination of the power distribution within a physical structure [45].

To evaluate ESD design symmetry, this can be done visually in a design review, or through means of an automated computer aided design (CAD) tool [45].

Integrated circuits are produced on a uniform substrate, which is the subject of numerous mask operations. The masks create, from lines and shapes, individual devices on the layers of the integrated circuits. Hence, the mask physical layout features can be used to quantify the ESD design symmetry. This can be done on each of the layout design levels of the ESD structure.

To define ESD design symmetry, an axis of symmetry can be defined in the ESD design. Semiconductor design layout is two-dimensional, allowing us to define an axis of symmetry in the x- and y-direction. In this fashion, "moments" can be defined about the axis of symmetry as a means of quantifying the degree of symmetry, and identify non-symmetric features.

Before manufacturing the integrated circuit in silicon, the data file which defines the lines and shapes of each mask is available for evaluating the design to be implemented in silicon. In this methodology, a method can define the symmetry which evaluates on a level-by-level basis (Figure 1.29).

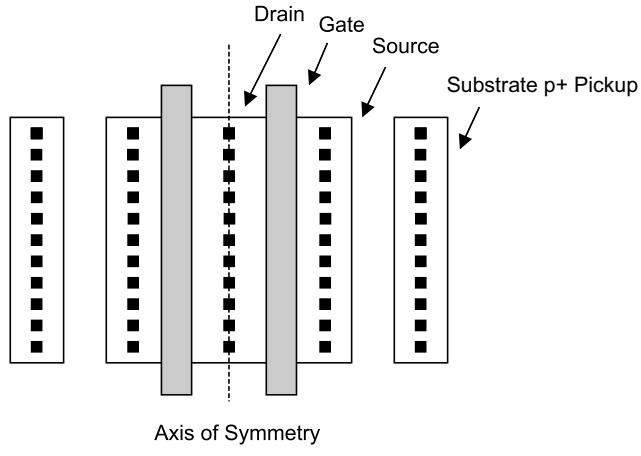

Figure 1.29 Design symmetry

In this design methodology, the method provides for evaluating the degree of design symmetry of the proposed semiconductor device, by considering various topological features of the design such as the directional flow of current into and out of the device, circuit element design symmetry, metal and contact symmetry, and other design features which reduce the robustness of an ESD protection network.

The semiconductor design can be "checked" before implementing in silicon by evaluating each ESD shape. In the event that any level fails the check, the level can be redesigned before implementing in silicon.

1.17.2 Design Segmentation

In the ESD design synthesis techniques, a form of ballasting is known as segmentation. Segmentation in essence is a means of ballasting where a device is "cut" into multiple parallel devices or elements [6–8]. The segmentation process may be initiated with a single element, or multiple elements, and then "cut" into more elements. The goal of the segmentation process is to improve current distribution along the width of the physical structure or multiple structures by physical separation using design layout techniques, which does not significantly increase the design area.

Segmentation can be utilized in any region of the semiconductor device that improves the current uniformity in the structure leading to high ESD robustness. In a MOSFET structure, segmentation can be introduced in the following regions:

- Introduction of isolation in the MOSFET source or drain regions.

In a silicon controlled rectifier, segmentation can be introduced in the following regions:

- Introduction of isolation in the anode region.
- Introduction of isolation in the cathode region.
- Introduction of masking in the sub-collector, body, well, and tub regions.

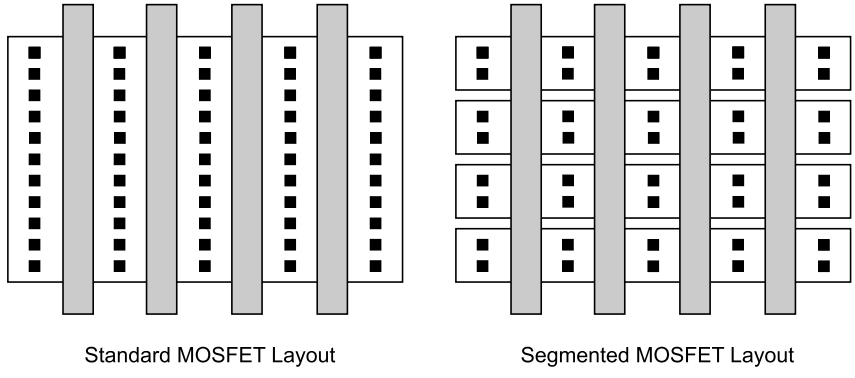

Figure 1.30 Multi-finger MOSFET structure with and without introduction of segmentation

In a bipolar transistor, segmentation can be introduced in the following regions:

- Introduction of isolation in the emitter.
- Introduction of isolation and separation in the collector or sub-collector regions.

Segmentation can be introduced in a single-finger MOSFET or multi-finger MOSFET. In a single-finger MOSFET, the segmentation will improve the current uniformity along the MOSFET width.

Figure 1.30 shows an example of a multiple-finger MOSFET structure with and without introduction of segmentation. The first device layout has a continuous MOSFET source and drain region. In the second device layout, the MOSFET source and drain regions were separated into four segments; this is an example of segmentation of a multiple-finger element.

In essence, the concept of segmentation is the reduction of a device into multiple devices to improve the ESD robustness. In order for this ESD design methodology to be successful, it is important to maintain layout symmetry.

1.17.3 ESD Design Concepts – Utilization of Empty Space

In ESD design synthesis, sections of the semiconductor chip area have no physical structures in the area. These "white space" regions exist in the semiconductor chips. White space regions in semiconductor chip design occur in the following areas:

- Area in the corners of the semiconductor chip.
- Area between the bond pads.
- Area under the signal bond pads.

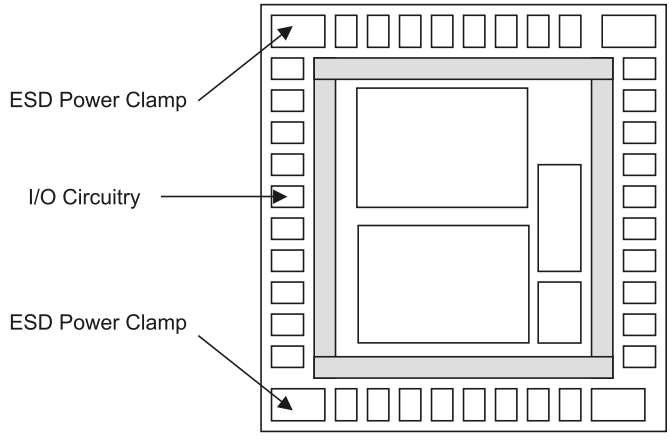

Figure 1.31 Utilization of semiconductor chip corners for ESD protection circuitry

- Area under power bond pads.
- Area under buses or "wiring bays."
- Area between power domains.

It is common practice in ESD design synthesis to utilize the area not used for functionality. Utilization of the area can be used for ESD protection in the following fashion:

- Placement of ESD power clamps in the corners of the semiconductor chip.
- Placement of ESD signal pad ESD elements or ESD power clamps in the area between the bond pads.
- Placement of the ESD signal pad ESD elements or ESD power clamps under the bond pads.
- Placement of de-coupling capacitors to increase chip capacitance.
- Placement of "back-up" ESD designs or experimental ESD designs in the unused area.

Figure 1.31 shows the usage of the semiconductor chip corner for ESD protection. This is a common practice in semiconductor design synthesis.

1.17.4 ESD Design Synthesis – Across Chip Line Width Variation (ACLV)

In semiconductor development, semiconductor process variation can introduce structural and dimensional non-uniformity. Photolithography and etch tools can introduce these non-uniformities that exist on a local and global design level. These variations can manifest themselves by introducing variations in both active and passive elements. For MOSFET

transistors, variation in the MOSFET channel length in single-finger and multiple-finger MOSFET layouts can lead to non-uniform "turn-on"; this effect can influence both active functional circuits and ESD networks [46]. In bipolar transistors, the line width variation can lead to different sizes in emitter structures, leading to non-uniform current distribution in multi-finger bipolar transistors. For resistor elements, resistor elements that are utilized for ballasting in multi-finger structures can also lead to non-uniform current in the different fingers in the structure.

Design factors that influence the lack of variation are the following semiconductor process and design variables:

- Line width.
- Line-to-line space.
- "Nested-to-isolated" ratio.
- Orientation.
- Physical spacing between identical circuits.

It is a circuit design practice and an ESD design synthesis practice to provide a line width which is well controlled. For line-to-line space, in an array of lines, the spacing is maintained to provide maximum matching between adjacent lines. For example, in a multi-finger MOSFET structure, the spacing between the polysilicon lines is equal, to provide the maximum matched characteristics.

Given any array of parallel lines, the characteristics of the "end" or edges of the array can have different characteristics from the other lines. In an array of lines, whereas one edge is adjacent to another line, the other edge is not; this leads to one line-to-line edge space appearing "nested" and the outside line-to-line edge space appearing "semi-infinite" or "isolated." To address the problem of poorly matched edge lines, the following semiconductor process and ESD design solutions are used:

- **Process:** Cancellation technique of photolithography and etch biases.
- **Design:** Use of dummy edge lines.
- **Circuit:** Use of "gate-driven" circuitry.

Orientation can also influence the line width of identical circuits, both locally and globally. An ESD design practice is to maintain the same x–y orientation of ESD circuits in a semiconductor chip to minimize variation pin-to-pin. This is not always possible in a peripheral architecture where the ESD element is rotated on the four edges of the semiconductor chip. Note that in this case, the circuit itself (e.g., OCD) may also undergo an orientation effect. It is a good ESD design synthesis practice that addresses the orientation issue with compensation and matching issues for orientation of the ESD elements (in conjunction with the circuit it is protecting).

On a macroscopic full-chip scale, variations in the photolithography and etching can vary from the top to the bottom of a semiconductor chip. In the design of a semiconductor chip, these can be compensated with a pre-knowledge of the photolithography and etch variations of a technology.

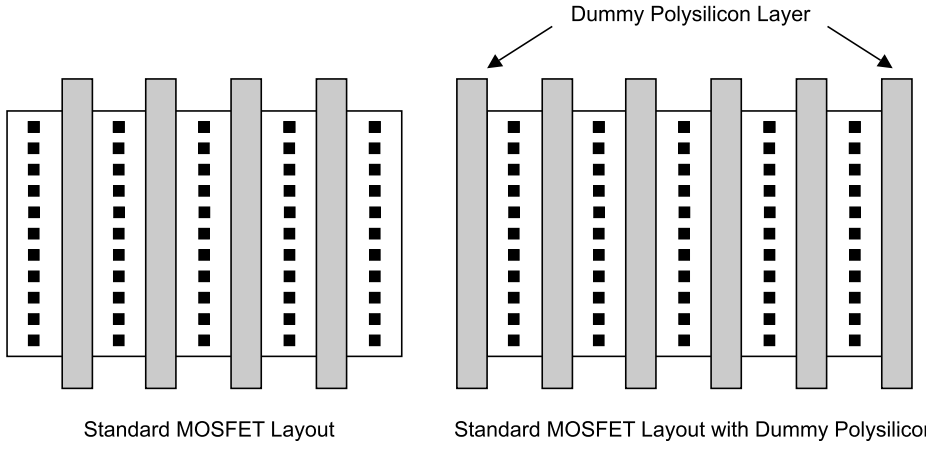

Figure 1.32 MOSFET with and without dummy shapes

1.17.5 ESD Design Concepts – Dummy Shapes

To improve uniformity in the current distribution within an output circuit (e.g., OCD network), or an ESD network, an ESD design concept is the introduction of "dummy shapes."

This technique is also utilized in advanced technologies (e.g., CMOS and bipolar), as well as circuit functions and applications that require a high degree of tolerance control or matching (e.g., analog, or high-speed digital circuits). Due to line width variations, there is a "nested" to "isolated" offset due to both photolithography and etch variations.

An ESD design concept is the introduction of "dummy shapes" adjacent to the ends of an array of active shapes. In a MOSFET structure, the polysilicon MOSFET gate line width influences the MOSFET "snapback." MOSFET "snapback" is a function of the MOSFET channel length. In a multi-finger structure, the line width variation within a given circuit can lead to non-uniform current distribution.

Figure 1.32 shows a multi-finger MOSFET structure with and without "dummy shapes." The dummy shapes are placed on the ends of the array at the same pitch as the active MOSFET fingers. With the introduction of the dummy fingers, the line width tolerance of the edge lines will improve, leading to an improved current distribution of the ESD current during MOSFET snapback.

1.17.6 ESD Design Concepts – Dummy Masks

In the ESD design synthesis, "dummy masks" are used to provide ESD design features desired in ESD design. Dummy masks used in ESD design synthesis are as follows:

- Introduction of masks to block silicide formation.
- Introduction of masks to block implants to produce non-uniform doping concentration.

Silicide "masking" can be introduced by the following processes:

- MOSFET gate structure.
- Removable MOSFET gate structure.
- Silicide block mask.
- Bipolar emitter structure masks.

MOSFET gate structures can be used in semiconductors for silicide blocking in the following devices and structures needed for ESD protection:

- Lateral "gated diodes" in bulk CMOS or SOI technologies.
- Lateral pnpn structures in bulk or SOI technology.
- Lateral buried resistor elements.

MOSFET gate structures can be removed after formation of the implants. In the above list of elements, the gate structure can be removed to avoid ESD dielectric failure mechanisms.

1.17.7 ESD Design Concepts – Adjacency

An ESD design concept is the issue of adjacency [31–33]. In the physical layout design of ESD structures, the adjacency of structures internal and external to the ESD element is a concern.

Structures adjacent to ESD structures can lead to both ESD failure mechanisms and latchup. Adjacent structures can lead to parasitic device elements not contained within the circuit schematics. Parasitic npn, pnp, and pnpn are not uncommon in the design of ESD structures. These parasitic bipolar transistor elements can occur between the ESD structure and the guard rings around the ESD structure. These parasitic elements can occur in single-well, dual-well, and triple-well CMOS, DMOS, bipolar, BiCMOS, and BCD technologies.

Figure 1.33 shows an example of two adjacent resistor elements for a differential pair circuit. For matching purposes, the resistor layouts are symmetrical about a common axis, and adjacent to each other. The figure shows a differential pair with input IN(+) and IN(−) for matching. In the case of ESD testing between the two signal pins, a lateral npn can form between the two n+ resistor elements at the input.

1.18 ESD DESIGN CONCEPTS – ANALOG CIRCUIT TECHNIQUES

In analog design, unique design practices are used to improve the functional characteristics of analog circuitry [14,31–33]. In the ESD design synthesis of analog circuitry, the ESD design practices must be suitable and consistent with the needs and requirements of analog circuitry. Fortunately, many of the analog design practices are aligned with ESD design practices.

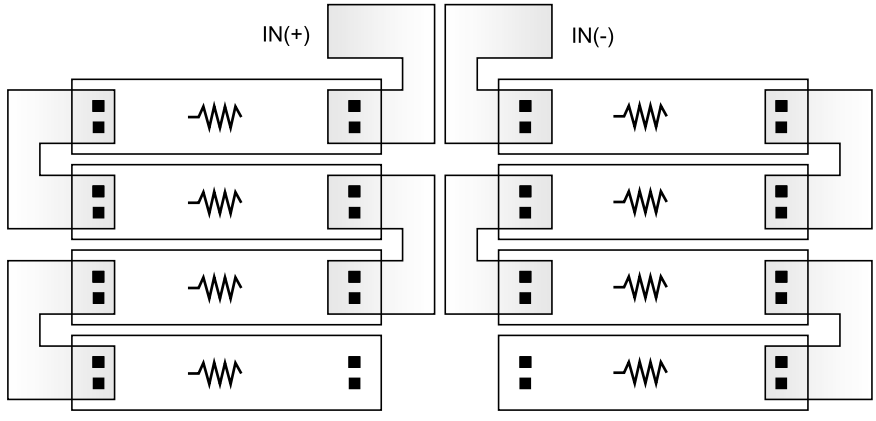

Figure 1.33 Adjacency in an RF differential pair

In the analog design discipline, there are many design techniques to improve tolerance of analog circuits. Analog design techniques include the following:

- **Local Matching:** Placement of elements close together for improved tolerance.
- **Global Matching:** Placement in the semiconductor die.
- **Thermal Symmetry:** Design symmetry.

A key analog circuit design requirement is matching [31–33]. To avoid semiconductor process variations, matching is optimized by the local placement. Placement within the die location is also an analog concern due to mechanical stress effects. In analog design, there is a concern over the temperature field within the die, and the effect of temperature distribution within the die.

Many of the analog design synthesis and practices are also good ESD design practices. The design practice of matching and design symmetry are also suitable practices for electrostatic discharge design. But, there are some design practices where a tradeoff exists between the analog tolerance and ESD; this occurs when parasitic devices are formed between the different analog elements within a given circuit, or circuit-to-circuit. Figure 1.33 demonstrates both design symmetry and matching characteristics that are suitable for RF or analog design implementations.

1.19 ESD DESIGN CONCEPTS – WIRE BONDS

In the ESD design synthesis, one must consider the packaging and wire bonds in the ESD design.

Wire bonds typically connect from the package to the bond pads. In multi-chip die, wire bonds can connect from one silicon die to another. The inductance of the wire bond is an ESD consideration. Wire bond inductance can influence the nature of the ESD event. In ESD events

which have low resistance (e.g., MM events), the inductance of the wire bond influences the impinging current waveform.

An ESD design concept is the usage of the wire bond for ESD design co-synthesis. An example of this in RF applications can serve as a matching filter, and co-integrated with ESD structures. ESD networks in RF applications integrate both capacitor and inductor elements for ESD–RF co-synthesis or as ESD networks. For RF ESD design, the wire bond inductor lead can be integrated into a T-match network comprising a first inductor, a capacitive element, and a second inductor.

1.20 DESIGN RULES

In the ESD design, a critical part of the ESD business strategy is to have ESD checking and verification methods. ESD checking and verification can evaluate both physical layout, schematic, and electrical resistances; for a successful whole-chip implementation, it is key to evaluate both layout and schematic as well as electrical parameters.

1.20.1 ESD Design Rule Checking (DRC)

As part of the process of ESD design synthesis, the semiconductor chip design layout and schematics are checked to be in conformance with the technology rules, as well as the specific ESD design rules. ESD design rule checking (DRC) is used to evaluate the layout of circuits, and ESD circuits. The ESD DRC rule sets are not standardized across the semiconductor industry. ESD DRC rule sets can evaluate the following:

- ESD network type.
- Special ESD design layers.
- ESD element layout dimensional parameters (e.g., width, length, spacing).
- Interconnects (e.g., wire and via).
- Guard rings.

ESD DRC rules are evaluated in the submission process of a semiconductor design.

1.20.2 ESD Layout vs. Schematic (LVS)

As part of the process of ESD design synthesis, the semiconductor chip design schematics are checked to be in conformance with the technology, as well as the specific ESD design rules. ESD layout vs. schematic (LVS) design checking and verification is used to evaluate the ESD schematics and circuits. ESD LVS rule sets are not standardized across the semiconductor industry. ESD LVS rule sets can evaluate the following:

- Existence of an ESD network on a given signal or power pin.
- ESD network type.

- ESD network connectivity.
- Circuit-to-ESD network compatibility.
- ESD element layout design parameters (e.g., width, length, perimeter, area).

ESD LVS rules are evaluated in the submission process of a semiconductor design.

1.20.3 Electrical Resistance Checking (ERC)

Evaluation of resistance is critical for a full-chip ESD implemenation. As part of the process of ESD design synthesis, evaluation of resistance in the alternative current loop is key to success. Electrical resistance checking (ERC) plays a key role in ESD design synthesis. ERC evaluation is used for the following:

- Bond pad to ESD series resistance.
- Signal pin series resistance.
- ESD signal pin to power rail resistance.
- ESD power rail resistance.
- ESD power rail of signal pin to the nearest ESD power clamp.
- Power rail to ESD power clamp resistance.

1.21 SUMMARY AND CLOSING COMMENTS

In this chapter, ESD concepts are introduced from layout, circuits, to design rule checking. A "sampler" of concepts is laid out for the reader, to begin viewing the ESD design synthesis from a broader perspective. ESD design synthesis extends from the smallest contact, to full-chip integration. With this awareness, it is possible to realize the extent of the ESD design discipline in semiconductor design.

In Chapter 2, the topic of ESD architecture and floorplan concepts will be highlighted. The chapter focus is on "peripheral I/O" and "array I/O" architectures, and how they influence the placement of the various elements for the whole-chip design integration. Chapter 2 also focuses on native-voltage, mixed-voltage, and mixed-signal chip integration, from digital, analog, to RF applications.

PROBLEMS

1.1. In mapping from a 5 V CMOS technology to a 3.3 V technology, what adjustments must be made in the ESD protection strategy for the ESD input circuit and a voltage-triggered ESD power clamp when the ESD input network is a grounded gate MOSFET, and the voltage-triggered MOSFET clamp contains a forward biased trigger circuit? What is the change in the power bus or ground rail (if any)?

1.2. In mapping from a 5 V CMOS technology to a 3.3 V technology, what adjustments must be made in the ESD protection strategy for the ESD input circuit and an RC-triggered ESD power clamp when the ESD input network is a series of p+/n-well diodes to V_{DD}, and n+ diffusion to ground?

1.3. Draw the SOA for a bipolar transistor. Explain each domain on the *I–V* plot. What are the limits?

1.4. Draw the SOA for a MOSFET transistor. Explain each domain on the *I–V* plot. What are the limits?

1.5. Explain the difference between the electrical safe operating area (E-SOA) and the thermal safe-operating area (T-SOA). How do these regions compare to the understanding of the functional regime of circuits? How do these relate to the ESD results? How do these relate to latent failures and hard failures?

1.6. Why is symmetry important in ESD networks? How does symmetry play a role in voltage distribution? Current distribution? Power distribution?

1.7. Why is adjacency important for matching in analog applications? Why is adjacency a problem for ESD protection? Draw matched elements of a differential receiver and draw the parasitic elements between the devices.

1.8. Draw a semiconductor chip that is 20 mm by 20 mm. Assume the bond pads for the circuits are 100 μm × 100 μm and 50 μm spacing between bond pads. Assuming a mosaic (or array) of bond pads, what is the maximum number of bond pads that can be placed on the semiconductor chip. Generalize an equation for the number of bond pads and the chip size relationship.

1.9. Draw a semiconductor chip that is 20 mm by 20 mm. Assume the bond pads for the circuits are 100 μm × 100 μm and 50 μm spacing between bond pads. Assuming the bond pads are on the perimeter, what is the maximum number of bond pads that can be placed on the semiconductor chip? Generalize an equation for the number of bond pads and the chip size relationship. If the ESD devices for each bond pad are as large as the bond pad, what is the percentage of chip area needed for ESD protection?

1.10. Draw a semiconductor chip that is 20 mm by 20 mm. Assume the bond pads for the circuits are 100 μm × 100 μm and 50 μm spacing between bond pads. Assuming a mosaic (or array) of bond pads, what is the maximum number of bond pads that can be placed on the semiconductor chip? Generalize an equation for the number of bond pads and the chip size relationship. If the ESD devices for each bond pad are as large as the bond pad, what is the percentage of chip area needed for ESD protection?

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