1

Introduction

Integrated circuits, microsensors, microfluidics, solar cells, flat-panel displays and optoelectronics rely on microfabrication technologies. Typical dimensions are around 1 micrometer in the plane of the wafer (the range is rather wide, from 0.02 to 100 μm). Vertical dimensions range from atomic layer thickness (0.1 nm) to hundreds of micrometers, but thicknesses from 0.01 to 10 μm are most typical. Microfabrication is the collection of techniques used to fabricate devices in the micrometer range.

The historical developments of microfabrication-related disciplines are shown below. The invention of the transistor in 1947 sparked a revolution. The transistor was born out of the fusion of radar technology (fast crystal detectors for electromagnetic radiation) and solid state physics. Developments of microfabrication methods enabled the fabrication of many transistors on a single piece of semiconductor and, a few years later, the fabrication of integrated circuits; that is, transistors were connected to each other on the wafer, rather than separated from each other and reconnected on the circuit board.

Microelectronics makes use of the semiconductor properties of silicon, but it is also important that silicon dioxide is such a useful material, for passivating silicon surfaces and protecting silicon during wafer processing. Silicon dioxide is readily formed on silicon, and it is high-quality electrical insulator. In addition to silicon transistors, integrated circuits require multiple levels of metal wiring, to route signals. Silicon microelectronic devices today are characterized by their immense complexity and miniaturization: a billion transistors fit on a chip the size of a fingernail.

Micromechanics makes use of the mechanical properties of silicon. Silicon is extremely strong, and flexible beams, cantilevers and membranes can be made from it. Pressure sensors, resonators, gyroscopes, switches and other mechanical and electromechanical devices utilize the excellent mechanical properties of silicon. Microelectromechanical systems (MEMS) or
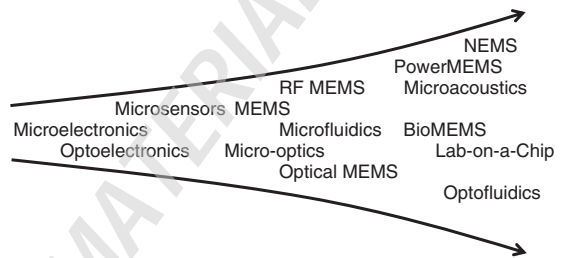

Figure 1.1 Evolution of microtechnology subfields from the 1960s onwards

microsystems, as they are also called, have expanded in every possible direction: microfluidics, microacoustics, biomedical microdevices, DNA microarrays, microreactors and microrockets to name a few. New subfields have emerged: BioMEMS, PowerMEMS, RF MEMS, as shown in Figure 1.1.

Silicon optoelectronic devices can be used as light detectors like diodes and solar cells, but light emitters like lasers and LEDs are made of gallium arsenide and indium phosphide semiconductors. Micro-optics makes use of silicon in another way: silicon, silicon dioxide and silicon nitride are used as waveguides and mirrors. MOEMS, or optical MEMS, utilize silicon in yet another way: silicon can be machined to make tilting mirrors, adjustable gratings and adaptive optical elements. The micromirror of Figure 1.2 takes advantage of silicon's smoothness and flatness for optics and its mechanical strength for tilting.

Microtechnology has evolved into nanotechnology in many respects. Some of the tools are common, like electron beam lithography machines, which were used to draw nanometer-sized structures long before the term nanotechnology was coined. Electron beam and ion beam defined nanostructures are shown in Figure 1.3. Thin films down to atomic layer thicknesses have been grown
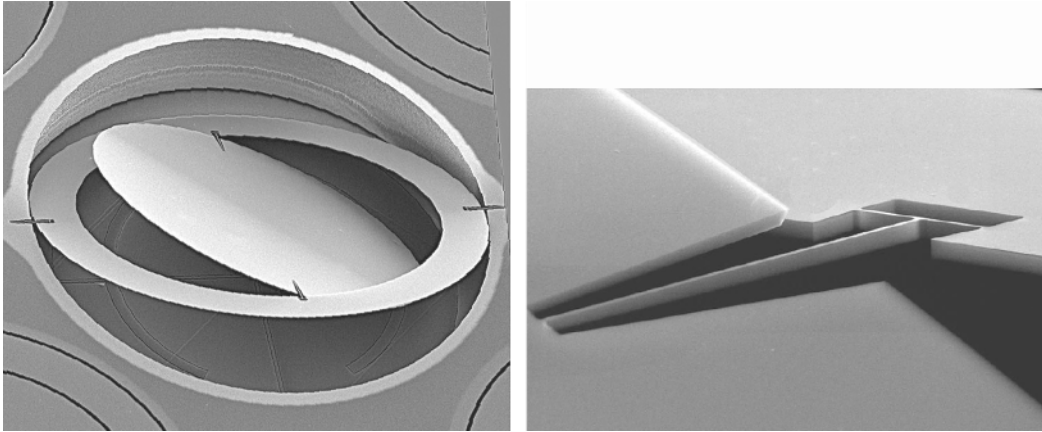
Figure 1.2   Micromirror made of silicon, 1 mm in diameter, is supported by torsion bars 1.2 μm wide and 4 μm thick (detail figure). Reproduced from Greywall *et al.* (2003), Copyright 2003, by permission of IEEE
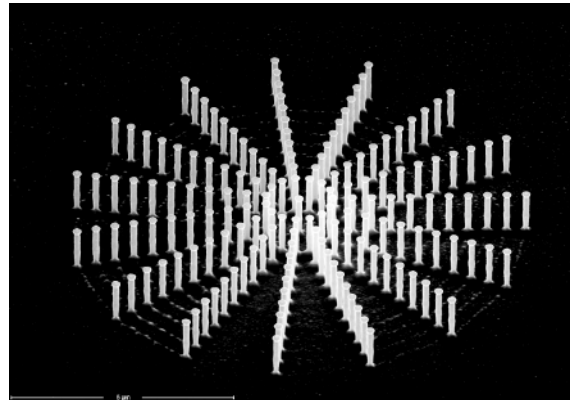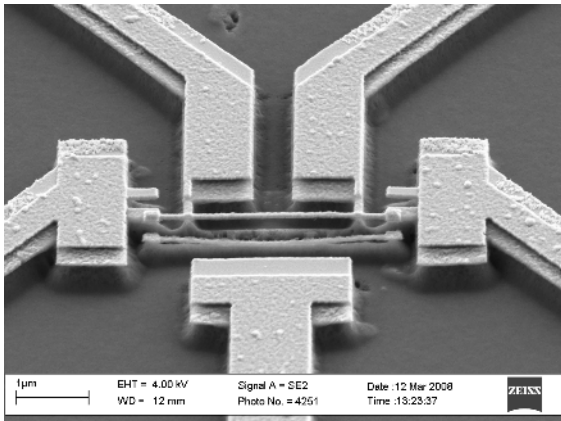

Figure 1.3   Electron microscope image of an electron beam defined gold–palladium horizontal nanobridge (courtesy Juha Muhonen, Aalto University) and vertical ion beam patterned nanopillars (courtesy Nikolai Chekurov, Aalto University); 100 nm minimum dimension in both

and deposited in the microfabrication communities for decades. Novel ways of creating nanostructures by self-assembly (self-organization) are being continuously adopted by the microfabrication community as tools to extend the capabilities of microfabrication. The tools of nanotechnology, such as the atomic force microscope (AFM), have been adopted in microfabrication as a way to characterize microstructures.

Solar cells and flat-panel displays can be large in area, but the crucial microstructures are similar to those in microdevices. Hard disks, and hard disk read/write heads especially, are microfabricated devices, with some of the

most demanding feature size and film thickness issues anywhere in microfabrication.

Listed in the references and further reading section at the end of this chapter are a number of books and review articles on microfabrication in diverse disciplines.

1.1 Substrates

Silicon is the workhorse of microfabrication. Silicon is a semiconductor, and the power of microelectronics arises strongly from the fact that silicon is available in both p-type (holes as charge carriers) and n-type (electrons as
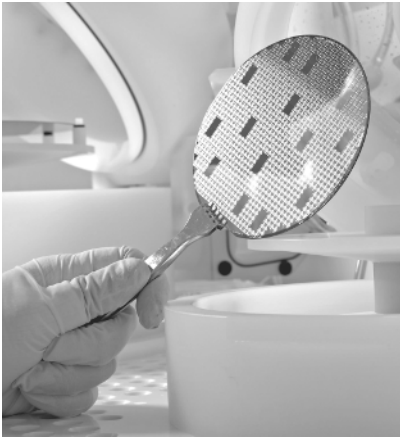
Figure 1.4   Silicon wafer, 100 mm in diameter, with about 200 device chips and a dozen test chips on it. Courtesy VTT

charge carriers), and its resistivity can be tailored over a wide range, from 0.001 to 20 000 ohm-cm. Silicon wafers are available in 100, 125, 150, 200 and 300 mm diameters and various thicknesses. Silicon is available in different crystal orientations, and the control of its crystal quality is very advanced.

Bulk silicon wafers (Figure 1.4) are single crystal pieces cut from larger single crystal ingots and polished. Silicon is extremely strong, on a par with steel, and it also retains its elasticity to much higher temperatures than metals. However, single crystalline (also known as monocrystalline) silicon wafers are fragile: once a fracture starts, it immediately develops across the wafer because covalent bonds do not allow dislocation movements.

Many microfabrication disciplines use silicon for convenience: it is available in a wide variety of sizes and resistivities; it is smooth, flat, mechanically strong and fairly cheap. Most of the machinery for microfabrication was originally developed for silicon ICs and newer technologies ride on those developments.

Single crystalline substrates include silicon, quartz (crystalline SiO_2), gallium arsenide (GaAs), silicon carbide (SiC), lithium niobate ($LiNbO_3$) and sapphire (Al_2O_3). Polycrystalline silicon is widely used in solar cell production. Amorphous substrates are also common: glass (which is SiO_2 mixed with metal oxides like Na_2O), fused silica (pure SiO_2; chemically it is identical to quartz) and alumina (Al_2O_3) are used in microfluidics, optics and microwave circuits, respectively. Sheets of polyimides, acrylates and many other polymers are also used as substrates. Substrates must be evaluated for available sizes, purities, smoothness, thermal stability, mechanical strength, etc. Round substrates are compatible with silicon, but square and rectangular ones need special processing because tools for microfabrication are geared for round silicon wafers.

1.2 Thin Films

More functionality is built on the substrates by deposition (and further processing) of thin films: various conducting, semiconducting, insulating, transparent, superconducting, catalytic, piezoelectric and other layers are deposited on the substrates. Thin films for microfabrication include a wide variety of elements: metals of common usage include aluminum, copper, tungsten, titanium, nickel, gold and platinum. Metallic alloys and compounds commonly encountered include Al–0.5% Cu, TiW, titanium silicide ($TiSi_2$), tungsten silicide (WSi_2) and titanium nitride (TiN). The compound is stoichiometric if its composition matches the chemical formula; for example, there is one nitrogen atom for each titanium atom in TiN. In practice, however, titanium nitride is more accurately described as TiN_x, with the exact value of x determined by the details of the deposition process. The most common dielectric thin films are silicon dioxide (SiO_2) and silicon nitride (Si_3N_4). Other dielectrics include aluminum oxide (Al_2O_3), hafnium dioxide (HfO_2), diamond, aluminum nitride (AlN) and many polymers.

A special case of thin-film deposition is epitaxy: the deposited film registers the crystalline structure of the underlying substrate, and, for example, more single crystal silicon can be deposited on a silicon wafer but with different dopant atoms and different dopant concentration.

The general material structure of a microfabricated devices is shown in Figure 1.5. Interfaces between the thin film and bulk, and between films, are important for the stability of structures. Wafers experience a number
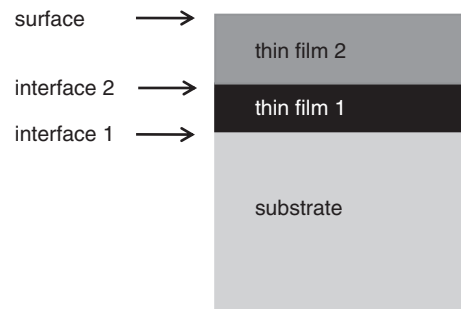

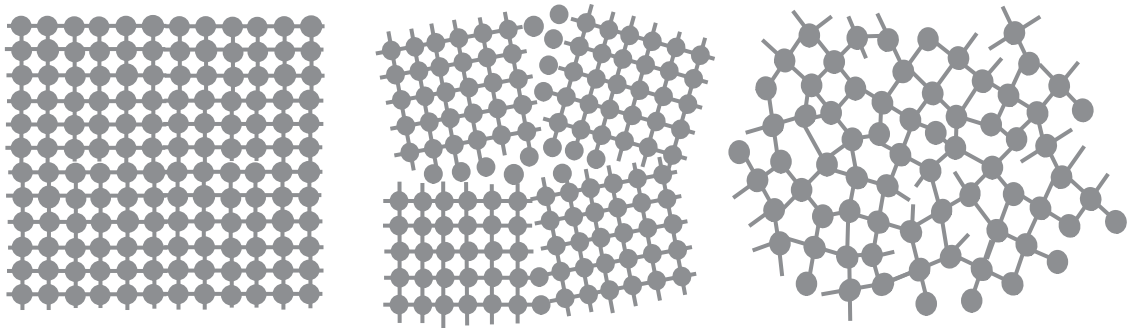**Figure 1.5** Materials and interfaces in a schematic microstructure

Figure 1.6   Single crystalline, polycrystalline and amorphous materials

of thermal treatments during their fabrication, and various chemical and physical processes are operative at interfaces, for example chemical reactions and diffusion. Sometimes reactions between films are desired, but most often they should be prevented. This can be achieved by adding extra films, known as barriers, in between films.

For example, thin film 1 might present an aluminum conductor and thin film 2 the passivation layer of silicon nitride; or films 1 and 2 are antireflective and scratch-resistant coatings in optics; or film 1 is thin tunnel oxide and film 2 a charge storage layer (as in memory cards).

Surface physical properties like roughness and reflectivity are material and fabrication process dependent. The chemical nature of the surface is important: some surfaces are reactive, others passive. Many surfaces will be covered by native oxide films if left unattended for some time: for example, silicon, aluminum and titanium form surface oxides over a time scale of hours. Water vapor adsorbed on surfaces must be eliminated before the wafers are processed further.

Thick substrates are not immune to thin films: a thin film $0.1\,\mu m$ thick may have such a high stress that a silicon wafer $500\,\mu m$ thick will be curved by tens of micrometers; or minute iron contamination on the surface will diffuse through a wafer $500\,\mu m$ thick during a fairly moderate thermal treatment.

Just like substrate wafers, the grown and deposited thin films can be

- single crystalline
- polycrystalline
- amorphous

as shown in Figure 1.6. During wafer processing, single crystal films usually stay single crystalline, but they can be amorphized by ion bombardment for example. Polycrystalline films experience grain growth, for instance during heat treatments. Foreign atoms, dopants and
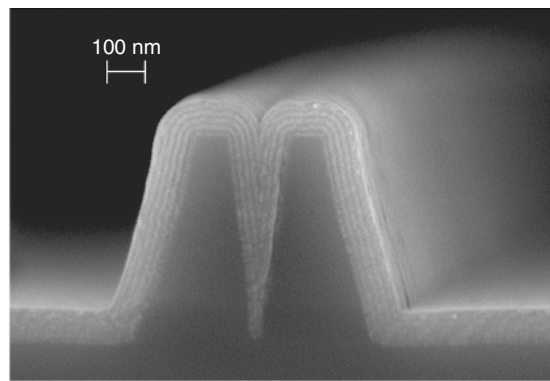

Figure 1.7   Atomic layer deposited aluminum oxide and titanium oxide thin films over silicon waveguide ridges. Courtesy Tapani Alasaarela, Aalto University

alloying atoms do not distribute themselves uniformly in polycrystalline material but aggregate at grain boundaries, which can lead to both beneficial and detrimental effects, depending on the particular materials and process conditions. Amorphous films can stay amorphous or they can crystallize during high-temperature steps, usually into the polycrystalline state.

Sometimes it is enough to deposit films on flat, planar wafers, but most often the films have to extend over steps and into trenches (Figure 1.7). These severe topographies introduce further deposition process-dependent subtleties.

Note on notations

<Si>	single crystal material
c-Si	single crystal material
α-Si/a-Si	amorphous material
a-Si:H	amorphous material with imbedded hydrogen (atomic % sometimes given)

nc-Si	nanocrystalline material (grain size a few nanometers)
µc-Si	microcrystalline material (grain size in the range of tens of nanometers)
mc-Si	multicrystalline (large-grained polycrystalline, grain size $\gg$ film thickness)
Al–0.5% Cu	aluminum alloy with 0.5% copper
W_2N, Si_3N_4	stoichiometric compounds
SiN_x, $x \approx 0.8$	non-stoichiometric compound
W:N	stuffed material, nitrogen at grain boundaries (non-stoichiometric)
WF_6 (g)	material in gas phase (for WF_6, boiling point $17\,^{\circ}C$)
WF_6 (l)	material in liquid phase
W (s)	material in solid phase
H_2SiOF_6 (aq)	aqueous solution
SiH_2 (ad)	material adsorbed on a surface
$Si/SiO_2/Si_3N_4$	film stacks are marked with substrate or bottom film on the left

1.3 Processes

Microfabrication processes consist of four basic operations:

1. High-temperature processes to modify the substrate.
2. Thin-film deposition on the substrate.
3. Patterning of thin films and the substrate.
4. Bonding and layer transfer.

Under each basic operation there are many specific technologies, which are suitable for certain devices, substrates, linewidths or cost levels. Some techniques work well in research, producing a few devices with elaborate features, but completely different methods may be required if those devices are to be mass produced.

Surface preparation and wafer cleaning could be termed the fifth basic operation but, unlike the other four, no permanent structures are made. Surfaces are modified by etching away a few atomic layers, or by depositing one molecular layer. Surface preparation requirements are widely different in different process steps: in wafer bonding it is paramount to eliminate particles that would create voids if left between the wafers, while in oxidation it is important to eliminate metallic contamination and in epitaxy to ensure that native oxides are removed.

High-temperature steps are used to oxidize silicon and to dope silicon by diffusion, and they are crucial for making transistor, diodes and other electronic devices.
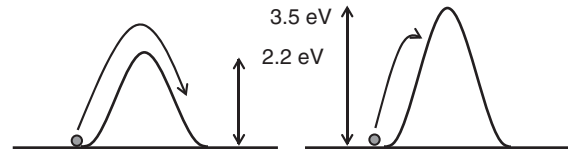

Figure 1.8 Diffusion process: the 2.2 eV barrier can be crossed at ease at $900\,^{\circ}C$ but the frequency of crossing the 3.5 eV barrier is low. A higher temperature, for example $1050\,^{\circ}C$, would be needed for the 3.5 eV barrier to be crossed at ease

Devices like piezoresistive pressure sensors also rely on high-temperature steps, with epitaxy and resistor diffusion as the key processes. High-temperature steps can be simulated extensively, by solving diffusion equations on a computer. The high-temperature regime in microfabrication is ca. $900\,^{\circ}C$ to $1200\,^{\circ}C$, temperatures where dopants readily diffuse and the silicon oxidation rate is technically relevant.

Many chemical and physical processes are exponentially temperature dependent. The Arrhenius equation (Equation 1.1) is a very general and very useful description of the rates of thermally activated processes. Activation energy can be illustrated as a jumping process over a barrier (Figure 1.8). According to the Boltzmann distribution, an atom at temperature T has an excess of energy E_a with a probability $\exp(-E_a/kT)$. Higher temperature leads higher barrier crossing probability:

$$\text{rate} = z(T)\, e^{(-E_a/kT)}$$

$$k = 1.38 \times 10^{-23}\,\text{J/K} = 8.62 \times 10^{-5}\,\text{eV/K} \quad (1.1)$$

The magnitude of the pre-exponential factor $z(T)$ and the activation energy E_a vary a lot.

In etching reactions, the activation energy is below 1 eV, in polysilicon chemical vapor deposition E_a is 1.7 eV, in substitutional dopant diffusion it is 3.5–4 eV and in silicon self-diffusion 5 eV. For a silicon etching process with 0.7 eV activation energy, raising the temperature from 20 to $40\,^{\circ}C$ results in a rate six times higher.

A great many microfabrication processes show Arrhenius-type dependence: etching, resist development, oxidation, epitaxy, chemical vapor deposition (which are chemical processes) are all governed by exponential temperature dependencies, as are diffusion, electromigration and grain growth (which are physical processes).

Low-temperature processes leave metal-to-silicon interfaces stable, and generally $450\,^{\circ}C$ is regarded as the upper limit for low temperatures. Between 450 and $900\,^{\circ}C$ there

is a middle range which must be discussed with specific materials and interfaces in mind.

The high-temperature regime is also known as the front-end of the line (FEOL) in the silicon IC business and the low-temperature regime as the back-end of the line (BEOL). But these terms have other meanings as well: for many people in the electronics industry outside silicon wafer fabrication, front-end includes all processing on wafers, and back-end refers to dicing, testing, encapsulation and assembly. We will use the first definition.

Many thin-film steps can be carried out identically on silicon wafers and other substrates; by definition they are layers deposited on top of a substrate. Thin-film steps do not affect the dopant distribution inside silicon; that is, diodes and transistors are unaffected by them.

Processes act on whole wafers – this is the basic premise. The whole wafer is subject to, for instance, diffusion from the gas phase, and metal is evaporated everywhere. Either selected areas must be protected by masks before the process, or else the material must be removed from selected areas afterward, by etching or polishing.

Patterning processes define structures usually in two steps: polymer processing to form an intermediate pattern which then acts as a mask for etching, deposition, ion implantation or other modification of the underlying material; and after the pattern has been transferred to solid material, the intermittent polymer mask is removed.

The main patterning technique in microfabrication is optical lithography, also known as photolithography. In Figure 1.9 photolithography is shown side by side with the thermal imprint/embossing process. In both processes a polymer film is modified locally to create patterns. In lithography, photosensitive polymer film is exposed to UV light, which hardens the polymer by crosslinking (so-called negative resists). In imprinting, a thermoplastic polymer softens upon heating, and a master stamp is pressed against it. The system is allowed to cool down before the stamp is released, and then the polymer retains its imprinted shape.

Many old methods have been successfully scaled down to micrometer and nanometer scales. Etching was once used by knights to engrave their armor with their coats-of-arms, and metal etching with similar acidic solutions can make aluminum patterns in the micrometer range. Once an original microstamp or nanostamp has been made, its replication into polymers is fairly easy (it is actually the detachment that is difficult). Electroplating is likewise easily applicable to nanometer structures. Casting polymers into micromolds is also popular in microfabrication: the elastomeric (rubber-like) material PDMS (poly(dimethyl)siloxane) is a favorite material for simple microfluidic devices.
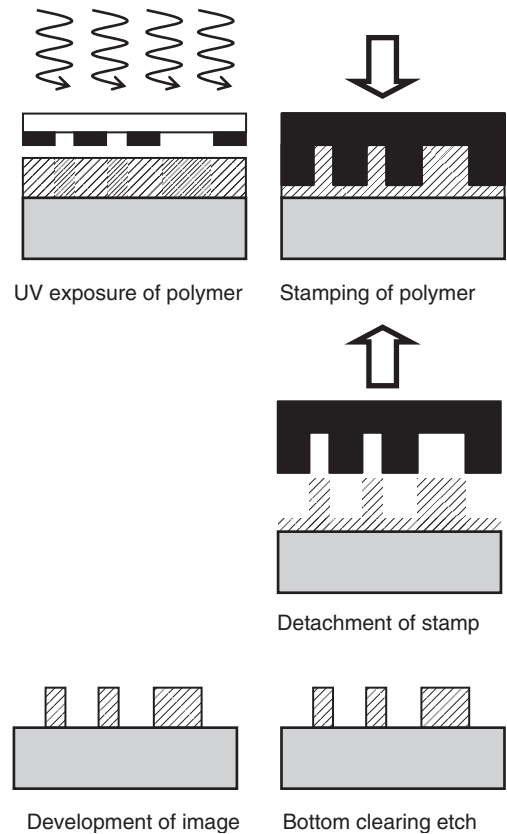

UV exposure of polymer   Stamping of polymer

Detachment of stamp

Development of image   Bottom clearing etch

Figure 1.9   Optical lithography (left) and thermal imprint (right): UV light crosslinks photosensitive polymer, and unexposed parts are developed away (in so-called negative resists). In imprinting, softened polymer is forced to shape, and after cooling the shape is retained even though the master is removed. In imprinting, some material remains at the bottom and must be cleared by etching

Wafer bonding and layer transfer enable more complex structures to be made. Bonding a wafer on top of a trench turns it into a channel, useful for microfluidics. Bonding more wafers can lead to elaborate fluidic channel patterns, as in the burner of a flame ionization detector, Figure 1.10. Bonding two wafers with electrodes creates a capacitor, for instance for pressure sensing. Bonding two different wafers can also be used simply as a method to create a new kind of a starting wafer, with the best properties of the two wafers combined.

These elementary operations of patterning, modification, deposition and bonding are combined many times over to create devices. Process complexity is often discussed in terms of the number of lithography steps (the
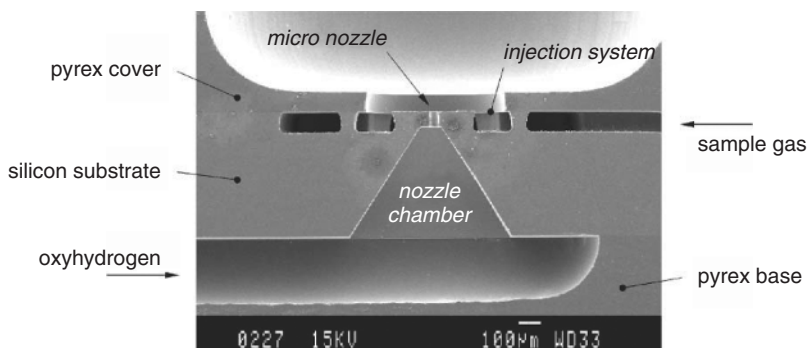
Figure 1.10   Oxyhydrogen burner of a flame ionization detector by Pyrex–glass/silicon/Pyrex–glass bonding. Reproduced from Zimmermann *et al.* (2002), Copyright © 2002 by permission of Elsevier Science Ltd

term mask levels is also used): five lithography steps are enough for a simple PMOS transistor (late 1960s' technology, and still used as a student lab process in many universities), and many MEMS, solar cell and flat-panel display devices can be made with two to six photolithography steps, but 32 nm linewidth microprocessors and logic circuits require over 30 patterning steps.

1.4 Dimensions

Microfabricated systems have minimum dimensions from 20 nm to 50 μm, depending on the device types. Advanced microprocessors and memories and the read/write heads of hard disk drives must have features <100 nm to be competitive. In Figure 1.11 the transmission electron micrograph shows the cross-section of a 65 nm MOS gate. Many other electronic devices like RF and power transistors make do with 100 nm to 1 μm dimensions. MEMS devices typically have 1–10 μm minimum lines and microfluidic devices might have 50 μm as the smallest feature.

Microfabricated device sizes are compared to physical, chemical and biological small objects in Figure 1.12, with microscopy methods capable of observing them.

Narrow individual lines can be made by a variety of methods; what really counts is resolution, the power to resolve two neighboring structures. It determines the device packing density. Resolution usually gets most attention when microscopic dimensions are discussed, but alignment between structures in different lithography steps is equally important. Alignment is, as a rule of thumb, one-third of minimum linewidth. High resolution but poor alignment can result in inferior device packing density compared to poorer resolution but tighter alignment.

As another rule of thumb, vertical and lateral dimensions of microdevices are similar. If the height-to-width
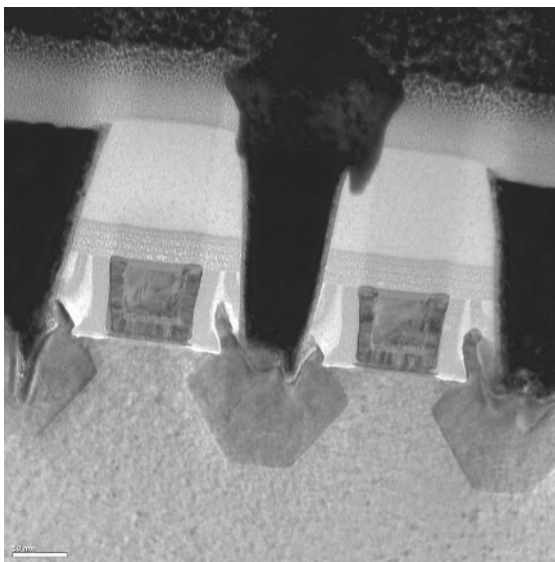

Figure 1.11   Transmission electron microscope image of 65 nm MOS transistor gates. Courtesy Young-Chung Wang, FEI Company

or aspect ratio is more than 2:1, special processing is needed, and new phenomena need to be addressed in such three-dimensional devices. Highly 3D structures are used extensively in both deep submicron ICs and in MEMS, for example in the microneedle of Figure 1.13.

Oxide thicknesses below 5 nm are used in CMOS manufacturing as gate oxides and as flash-memory tunnel oxides. Epitaxial layer thicknesses go down to the atomic layer and up to 100 μm in the thick end. There are also self-limiting deposition processes which enable extremely thin films to be made, often at the expense of deposition
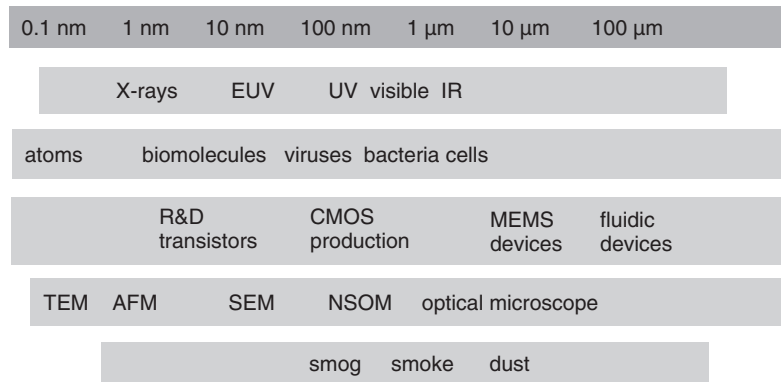
0.1 nm	1 nm	10 nm	100 nm	1 μm	10 μm	100 μm

X-rays   EUV   UV visible IR

atoms   biomolecules   viruses bacteria cells

R&D   CMOS   MEMS   fluidic
transistors   production   devices   devices

TEM AFM   SEM   NSOM   optical microscope

smog   smoke   dust

Figure 1.12 Dimensions in the microworld: electromagnetic radiation, natural objects, humanmade devices, microscopy methods and dirt
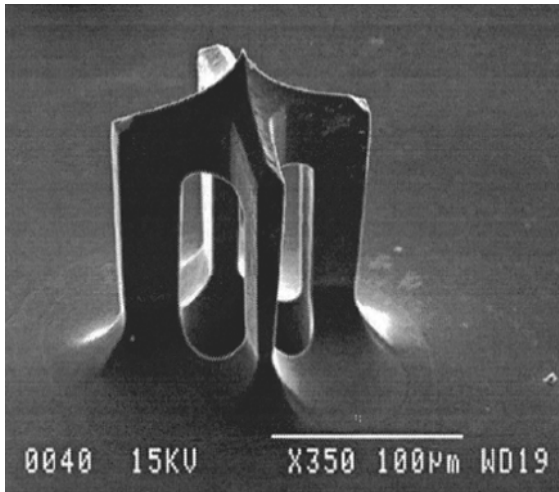

Figure 1.13 Silicon microneedle, about 100 μm. Reproduced from Griss and Stemme (2003), Copyright 2003, by permission of IEEE

rate. Chemical vapor deposition (CVD) can be used for anything from a few nanometers to a few micrometers. Sputtering also produces films from 0.5 nm to 5 μm. Spin coating is able to produce films as thin as 100 nm, or as thick as 100 μm. Typical applications include polymer spinning. Electroplating (galvanic deposition) can produce metal layers of almost any thickness, from a few nanometers up to hundreds of micrometers.

But almost every device includes structures with dimensions of about 100 μm. These are needed to interface the microdevices to the outside world: most devices need electrical connections (by a wire-bonding or bumping process); microfluidic devices must be connected to capillaries or liquid reservoirs; solar cells and power semiconductors must have thick and large metal areas to bring in and take out the high currents involved; and connections to and from optical fibers require structures about the size of fibers, which is also on the order of 100 μm.

1.5 Devices

Microfabricated device can be classified in many ways:

- material: silicon, III–V, wide band gap (SiC, diamond), polymer, glass
- integration: monolithic integration, hybrid integration, discrete devices
- active vs. passive: transistor vs. resistor, valve vs. sieve
- interfacing: externally (e.g., sensor) vs. internally (e.g., processor).

The above classifications are based on device material or functionality. In this book we are concentrating on fabrication technologies, so the following classification is more useful:

- volume (bulk) devices
- surface devices
- thin-film devices
- stacked devices.

Power transistors, thyristors, radiation detectors and solar cells (Figure 1.14) are volume devices: currents are generated and transported (vertically) through the wafer, or, alternatively, device structures extend through the wafer, as in many bulk micromechanical devices. The starting
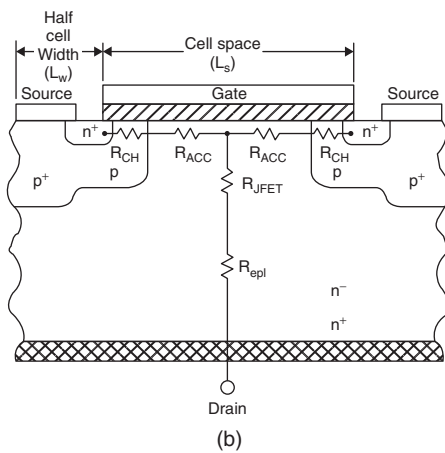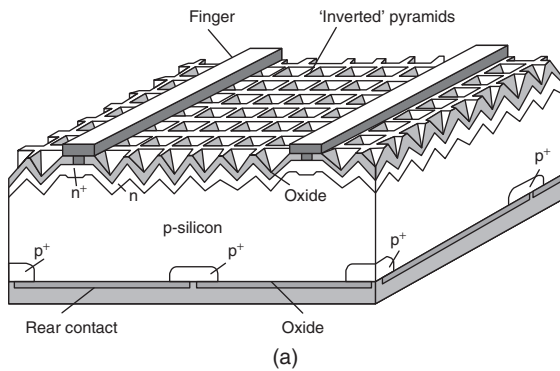
(a)

(b)

Figure 1.14   Volume devices: (a) passivated emitter, rear locally diffused solar cell, reproduced from Green (1995) by permission of University of New South Wales; (b) n-channel power MOSFET cross-section, reproduced from Yilmaz *et al*. (1991) by permission of IEEE

Figure 1.15   Surface devices: $0.5\,\mu m$ minimum linewidth CMOS in a scanning electron microscope (SEM) view

Figure 1.16   Curl switch. Reproduced from Oberhammer and Stemme (2004), Copyright 2004, by permission of IEEE

wafers for volume devices need to be uniform throughout. Patterns are often made on both sides of the wafer and it is important to note that some processes affect both sides of the wafer and some are one sided.

Surface devices make use of the material properties of the substrate but generally only a fraction of wafer thickness is utilized in making the devices. However, device structure or operation is connected with the properties of the substrate. Most ICs fall under this category: namely, MOS and bipolar transistors, photodiodes, CCD image sensors as well as III–V optoelectronic devices.

In silicon CMOS, only the top $5\,\mu m$ layer of the wafer is used in making the active devices, the remaining $500\,\mu m$ of wafer thickness being for support: that is, mechanical strength and impurity control. Shown in Figure 1.15 are CMOS polysilicon gates of $0.5\,\mu m$ width and $0.25\,\mu m$
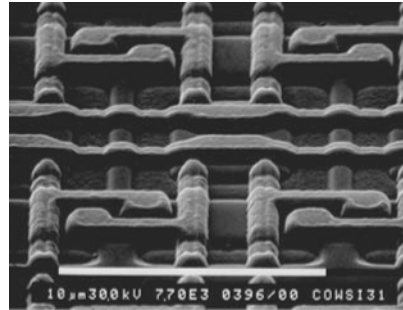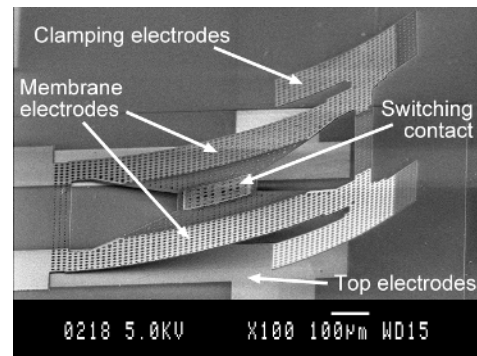
height. Surface devices can have very elaborate 3D structures, like multilevel metallization in logic circuits, which can be $10\,\mu m$ thick, but this is still only a fraction of wafer thickness; therefore the term surface device applies.

Devices can be built by depositing and patterning thin films on the wafers, where the wafer has no role in device operation. Wafer properties like thermal conductivity or optical transparency may be part of device operation, but another substrate could be used instead. Thin-film transistors (TFTs) are most often fabricated on non-semiconductor substrates of glass, plastic or steel. Devices like RF switches and relays, optical modulators or DNA arrays are often fabricated on silicon wafers for convenience, but they could be fabricated on glass or polymer substrates as well. Figure 1.16 shows a RF switch: the silicon nitride/gold thin film flap curls up because of film stresses, but can be forced flat by electrostatic actuation.

In MEMS devices with free-standing elements, membranes and cantilevers pose certain processing limitations
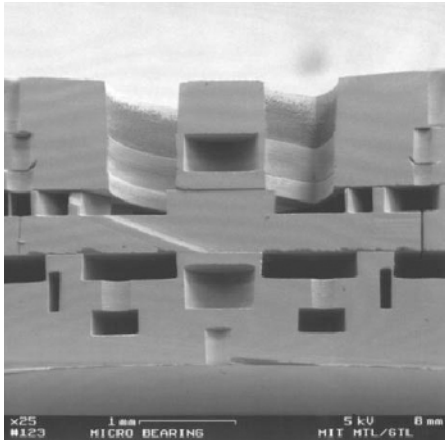
Figure 1.17 A microturbine by five-wafer silicon-to-silicon bonding. Reproduced from Lin *et al.* (1999) by permission of IEEE

of their own. Many processes cannot be done on movable, bending structures because they are not stable enough, and therefore the release step is often the very last process step. Similarly, devices with through-wafer holes pose serious limitations in many process steps.

Stacked devices are made by layer transfer and bonding techniques. Two or more wafers are joined together permanently. Devices with vacuum cavities, for example absolute pressure sensors, accelerometers and gyroscopes, are stacked devices made of bonded silicon/glass wafer pairs. Micropumps and valves are typically stacks of many wafers. Figure 1.17 shows a microturbine. It is made by bonding together five wafers. More and more layer transfer and wafer bonding techniques are being developed, and stacked devices of various sorts are expected to be appear, for example GaAs optical devices bonded to Si-based electronics, or MEMS devices bonded to ICs.

1.6 MOS Transistor

The MOS transistor is a capacitor with a silicon substrate as the bottom electrode, the gate oxide as the capacitor dielectric and the gate metal as the top electrode (Figure 1.18). The MOS transistor has been the driving force of the microfabrication industries. It is the top device by all measures: number of devices sold, the narrowest linewidths and the thinnest oxides in mass production, as well as dollar value of production. Most equipment for microfabrication was originally designed for MOS IC fabrication, and later adapted to other applications.

Despite the name MOS, the gate electrode is usually made of phosphorus-doped polycrystalline silicon, not of
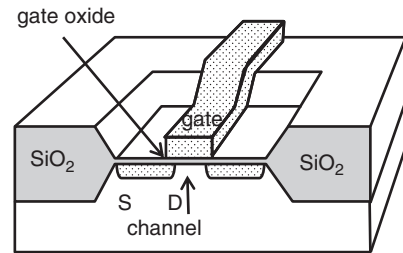

Figure 1.18 Schematic of a MOS transistor: gate, source (S) and drain (D) in an active area defined by thick isolation oxide

metal. The basic function of a MOS transistor is to control the flow of electrons from the source to drain by the gate voltage and the field it generates in the channel. In a NMOS transistor, a positive voltage on the gate pulls electrons from the p-type channel to the Si/SiO_2 interface where an overabundance of electrons inverts the region under the gate to n-type, enabling electrons to flow from the n+ source to the n+ drain.

Transistors are isolated electrically from neighboring transistors by SiO_2 field oxide areas. This isolation takes up a lot of area, and therefore the transistor packing density on a chip does not depend on transistor dimensions alone.

Scaling down MOS transistor channel length makes the transistors faster. The other main aspect is area scaling: a factor N linear dimension scaling reduces the area to A/N^2. Gate width, gate oxide thickness and source/drain diffusion depths are closely related, and the ratios are more or less unchanged when the transistors are scaled down. As a rough guide, for a gate width of L, the oxide thickness is $L/50$, and the source/drain junction depth is $L/5$.

1.7 Cleanliness and Yield

Microfabrication takes place under carefully controlled conditions of constantly circulating purified airflow, with temperature, humidity and vibrations also under strict control because micrometer-scale structures would otherwise be destroyed by particles or else the lithography process would be ruined by vibrations or temperature and humidity fluctuations. Personnel in cleanrooms wear gowns to prevent particle emissions (Figure 1.19), and work procedures have been developed to minimize all disturbances.

Wafers are cleaned actively during processing: thousands of liters of ultrapure water (UPW, as known as de-ionized water, DIW) is used for each wafer during

Figure 1.19 Working in a cleanroom, courtesy VTT

Figure 1.20 Silicon wafer with chips, alignment marks and edge exclusion. The scribe line area is reserved for dicing the chips separately

device fabrication. This is the dynamic part of particle cleanliness: the passive part comes from careful selection of materials for cleanroom walls, floors and ceilings, including sealants and paints, as well as selection of materials for design and for process equipment, wafer storage boxes and all associated tools, fixtures and jigs.

Even though extreme care is taken to ensure cleanliness in microprocessing, some devices will always be defective. As the number of process steps increases, yield Y goes down according to

$$Y = Y_0^n \qquad (1.2)$$

where Y_0 is the yield of a single process step and n is the number of steps. With 100 process steps and 99% yield in each individual step, this results in a 37% yield (representative of a 64 k DRAM chip), but a 99% yield for a 500-step process (representative of a 16 Mbit DRAM) results in a yield <1%. Clearly a 99% yield is not enough for modern memory fabrication. Chip design also affects yield through area:

$$Y = e^{-DA} \qquad (1.3)$$

where A is the chip area and D is the defect density: making small chips is much easier than making big chips.

Yield has two major components: stochastic and systematic. Stochastic (random) defects are unpredictable occurrences of pinholes in protective films, particle adhesion on the wafer, corrosion of metal lines, etc. Systematic defects come from equipment performance limitations, impurities in starting materials and design errors: two features may be placed so close to each other that they inadvertently touch, or impurities in chemicals do not allow low enough leakage currents.
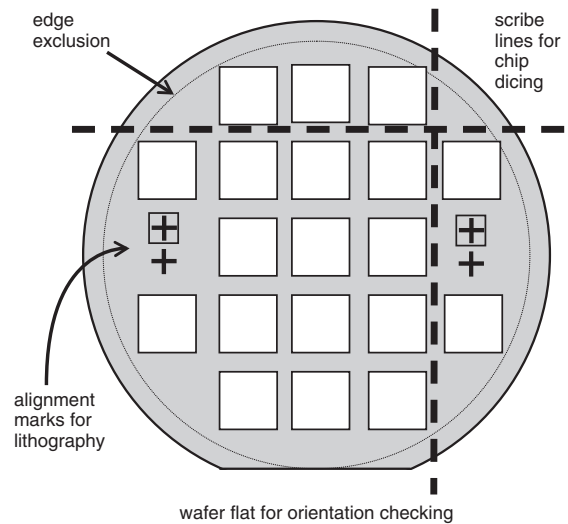
IC wafers contain typically a hundred or hundreds of chips (also called die). This is depicted in Figure 1.20. It also shows the other elements: alignment marks for registering structures on different layers to each other; and scribe lines, the space reserved for dicing the wafer into separate chips after completing the processing. The number of chips on a wafer has remained more or less unchanged for decades because chip size and wafer size have grown in parallel: $0.2 \, cm^2$ chips were made on 100 mm wafers while $2 \, cm^2$ chips are usual on 300 mm wafers. In extreme cases only one chip fits the wafer, for example a solar cell, a thyristor or a position-sensitive radiation detector. Microfluidic separation devices with channels 5 cm long and optical waveguide devices with large radii of curvature can have a handful of devices per wafer. With standard logic chips or micromechanical pressure sensors and accelerometers, thousands can be crammed together to fit a wafer.

1.8 Industries

Worldwide, about $6 billion is spent on silicon wafers annually. These are used to make $250 billion worth of semiconductor devices, which fuel the $1200 billion electronics industry. In 2009, about 10^{19} transistors were shipped, approximately 1 billion devices for each and every person on Earth. As recently as 1968 it was one transistor per year per person. Price of course explains a

Table 1.1   Wafer size and linewidth distribution in 2009

Wafer size	% of area	% of wafers
300 mm	38	15
200 mm	38	35
150 mm	17	30
<150 mm	7	20

Linewidth distribution in production:

$\geq$400 nm	10%
160–400 nm	15%
80–160 nm	20%
65–80 nm	20%
<65 nm	35%

Data from SEMI and SICAS.

lot: in 1968 transistors cost about 1$ a piece; in 2009 the cost was less than one-millionth of a cent.

Device density on chips is quadrupling every three years, a trend known as Moore's law.

Scaling has continued relentlessly for the past 50 years. Linewidths were in the 30 μm range in the early 1960s, and they are 30 nm in the year 2010. Lithographic scaling has thus improved packing density by a factor of a million (linear dimension scaling by a factor of 1000 equals area density scaling by a factor of 1 000 000). The number of transistors on a chip has increased from one to one billion, however. The other two main factors have been an increase in chip size and in circuit cleverness: new designs, new fabrication processes and novel materials use less area for the same functionality.

IC technology generations are classified by their linewidths and each new generation has dimensions roughly 30% smaller than the previous one. In 2010 the minimum linewidth in production is about 30 nm, but this represents just a small fraction of all ICs manufactured. The 200 million wafers (approximately 6 square kilometers) are distributed as shown in Table 1.1. Small wafers are used to fabricate specialty ICs, MEMS and power devices. Gigabit memories and latest generation processors are made on 300 mm wafers. When counted as silicon area, the smaller linewidths gain in importance because linewidth scaling has been accompanied by an increase in wafer size, which means that 65 nm devices are fabricated on 300 mm wafers but 1 μm devices on 100 mm wafers. Only 35% of all devices are fabricated with the latest 45 nm and 32 nm generation technologies, but the fabrication facilities for the 65 nm technology generation (commonly called

"wafer fabs" or simply "fabs") are very new: they were mostly built in 2005–2007.

The microsystems/MEMS industry as such does not exist: microsystems are more a technology than an industry, therefore statistics are erratic. Some estimates put microsystem sales at $8 billion. The flat-panel display industry has sales of close to $100 billion. The solar cell industry is growing rapidly, with sales of $30 billion. The magnetic data storage industry is similar in size but consists of a limited number of established players, while the solar industry is mostly populated by start-up companies.

Note on drawings

The z-dimension is enlarged relative to the x- and y-directions to make drawings easier to read. For example, in bulk micromechanics the diaphragm of a piezoresistive sensor is 20 μm, or 5% of wafer thickness, and the piezoresistor diffusion depth is 5% of diaphragm thickness, that is 1 μm.

1.9 Exercises

1. Silicon atom density is 5×10^{22} cm^{-3}. If the boron dopant concentration is 10^{15} cm^{-3}, how far are the boron atoms from each other?
2. IC chips are getting larger even though the linewidths are scaled down because more functions are integrated on a chip. Calculate the signal line resistance for:
   (a) aluminum conductors 1 μm thick, 3 μm wide and 500 μm long (resistivity 3 μohm-cm);
   (b) copper conductors 0.3 μm wide, 0.5 μm thick and 1 mm long (resistivity 2 μohm-cm).
3. Silicon dioxide can sustain a 10 MV/cm electric field. Calculate oxide thickness regimes for:
   (a) CMOS ICs where the operating voltages are 1–5 V;
   (b) capillary electrophoresis (CE) microfluidic chips where 500–5000 V is used.
4. DRAM memory is a capacitor. How many electrons are stored in a DRAM capacitor if it has an area of 1 μm^2 and a silicon dioxide dielectric 5 nm thick?
5. A micromechanical pressure sensor consists of a 1 mm^2 movable silicon electrode and 1 μm air gap as the dielectric. What is the capacitance? If femtofarad capacitance change can be measured, what is the corresponding displacement of the movable capacitor electrode?
6. Aluminum wires do not tolerate current densities higher than 1 MA/cm^2. What are the maximum currents that can run in micrometer aluminum wiring?

7. If a silicon etching reaction has an activation energy of 0.7 eV, and the etch rate at 80 °C is 1.3 μm/min, how much is it at 100 °C?

8. What defect densities are typical of modern IC production?

9. CMOS linewidths have been scaled down steadily by 30% every three years. In the year 2010 linewidths were in the range of 32 nm. When will the linewidths equal atomic dimensions?

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