1 RF Design and ESD

1.1 FUNDAMENTAL CONCEPTS OF ESD DESIGN

As a design discipline, the electrostatic discharge (ESD) design discipline is distinct from circuit design practices used in the development of semiconductor circuit design discipline [1,2]. Fundamental concepts and objectives exist in the ESD design of semiconductor devices, circuits, and systems in methods, layout, and design synthesis. To address the radio frequency (RF) ESD design discipline, we pose the following questions [1–3]:

- What is it that makes the ESD design discipline unique?
- How is it distinct from standard circuit design practices?
- How is RF ESD design discipline different from the RF design discipline?
- How is RF ESD design discipline different from the digital ESD design discipline?

To address the first issue of the ESD design discipline, let us first address the uniqueness of the distinction of ESD design discipline practice. Here are some of the ESD design practices [2]:

- *Device Response to External Events*: Design of devices and circuits to respond to (and not to respond to) unique current waveforms (e.g., current magnitude and time constants) associated with external environments. In ESD design, the ESD devices as well as the circuits that are to be protected can be designed to respond (and not torespond) to unique ESD current waveforms. ESD networks are typically designed to respond to specific ESD pulses. These networks are unique in that they address the current magnitude, frequency, polarity, and location of the ESD events. Hence, in ESD design, the ESD networks are designed and tuned to respond to the various ESD events. In ESD design, different stages or segments of the network can also be designed to respond to different ESD events. For example, some stages of a network can respond to human body model (HBM) and machine model (MM) events, whereas other segments respond to the charged device model (CDM)

event. These ESD events differ in current magnitude, polarity, time constant, as well as the location of the current source. Hence, the ESD circuit is optimized to respond and address different aspects of ESD events that circuits may be subjected to [2].

- *Alternate Current Loops*: Establishment of alternative current loops or current paths, that activate during high current or voltage events. A unique issue is the establishment of alternative current loops or current paths that activate during high current or voltage events. By establishing alternative current loops, or secondary paths, the ESD current can be re-directed to prevent overvoltage of sensitive circuits. In order to have an effective ESD design strategy, this current loop must respond to the ESD event and have a low impedance [2].
- *Switches*: Establishment of 'switches' that initiate during high current or voltage events. On the issue of establishment of 'switches' that initiate during high current or voltage events, the uniqueness factor is that these are at times either passive or activated by the ESD event itself. A unique feature of ESD design is that it must be active during unpowered states. Hence, the 'switches' used to sway the current into the ESD current loop are initiated passively or are initiated by the ESD event itself. Hence, the ESD event serves as the current and voltage source to initiate the circuit. These switches lead to 'current robbing' and the transfer of the majority of the current from the sensitive circuit to the alternative current loop. The ESD design discipline must use 'switches' or 'triggers' that initiate passively (e.g., a diode element) or actively (e.g., a frequency-triggered ESD network). A design objective is to provide the lowest voltage trigger allowable in the application space. Hence, a key ESD design objective is to utilize low-voltage trigger elements that serve as a means to transfer the current away from the sensitive circuit to alternative current paths. A large part of the effective ESD design discipline is the construction of these switches or trigger elements [2].
- *Decoupling of Current Paths*: Decoupling of sensitive current paths is an ESD design discipline practice. Circuit elements can be introduced that lead to the avoidance of current flow to those physical elements. The addition of 'ESD decoupling switches' can be used to decouple sensitive circuits as well as to avoid the current flow to these networks or sections of a semiconductor chip. ESD decoupling elements can be used to allow elements to undergo open or floating states during ESD events. This can be achieved within the ESD network or within the architecture of a semiconductor chip. Decoupling of sensitive elements or decoupling of current loops can be initiated by the addition of elements that allow the current loop to 'open' during ESD events. The decoupling of nodes, elements, circuits, chip subfunctions, or current loops relative to the grounded reference prevents overvoltage states in devices and eliminates undesired current paths. Decoupling elements can avoid 'pinning' of electrical nodes. Hence, integration of devices, circuits elements, or circuit functions that introduce decoupling electrical connections to ground references and power supplies references, is a unique and key ESD design practice [2].
- *Decoupling of Feedback Loops*: Decoupling of loops that initiate pinning during off condition or ESD test modes. Feedback loops can lead to unique ESD failures and lower ESD results significantly. The decoupling of nodes, elements, or current loops relative to the grounded reference prevents overvoltage states in devices and eliminates current paths

initiated by the feedback elements. These decoupling elements can avoid 'pinning' of electrical nodes [2].

- *Decoupling of Power Rails*: Decoupling of electrical connections to grounded references, and power supplies [2].
- *Local and Global Distribution*: Local and global distribution of electrical and thermal phenomena in devices, circuits, and systems is a key ESD design practice and focuses on ESD development. To provide an effective ESD design strategy, the ESD design practices must focus on the local and global distribution of electrical and thermal phenomena in devices, circuits, and systems. In order to shunt the ESD current efficiently and effectively, the distribution of the current is critical in ESD design. As the current distributes, the effectiveness of the device helps improving the utilization of the total area of the ESD network or circuit element. On a circuit and system level, the distribution of the ESD current within the network or system lowers the effective impedance and lowers the voltage condition within the ESD current loop [2].
- *Usage of Parasitic Elements*: Utilization and avoidance of parasitic element is part of the ESD design practice. ESD design either utilizes or avoids activation of these parasitic elements in the ESD implementations. Utilization of parasitic elements is a common ESD design practice for ESD operation, such as utilization of parasitic lateral or vertical bipolar transistors. It is not common to use these parasitic elements in standard circuit design, whereas for ESD design it is very prevalent to utilize the parasitic devices and is part of the ESD design practice and art [2].
- *Buffering*: Utilization of current and voltage buffering of sensitive devices, circuits, or subcircuits is a key ESD design practice. In ESD design, it is also a common practice to establish current and voltage buffering of sensitive devices, circuits, subcircuits, chip level core regions, or voltage islands. A design practice is to increase the impedance in the path of the sensitive circuit either by placing of high impedance elements, establishing 'off' states of elements, voltage and current dividing networks, resistor ballasting, or by initiating elements in high impedance states [2].
- *Ballasting*: It is a standard ESD design practice to use ballasting techniques, which involves introduction of resistance to redistribute current within a single element or a plurality of elements. In digital design, ballasting is predominately achieved using resistor elements. Resistive, capacitive, or inductive ballasting can be introduced to redistribute current or voltage within a single element or a plurality of elements, circuit, or chip segment. The usage within a semiconductor device element allows for redistribution within a device to avoid electro–thermal current constriction and poor area utilization of a protection network or circuit element. The usage of ballasting allows to redistribute the source current from the ESD event to avoid thermal heating or electrical overstress within the semiconductor network or chip. Ballasting can be introduced into a semiconductor device structures achieved by semiconductor process choices, material choices, silicide film removal, introduction of discrete resistor elements, and introduction of design layout segmentation [2].
- *Usage of Unused Sections of a Semiconductor Device, Circuit, or Chip Function*: It is an ESD design practice to utilize 'unused' segments of a semiconductor device for ESD protection, which was not utilized for functional applications [2].

- *Impedance Matching between Floating and NonFloating Networks*: It is an ESD design practice to impedance match the states of floating structures. In ESD design, it is common to utilize the 'unused' segments of a semiconductor device for ESD protection and impedance match the network segments for ESD operation; this matching of conditions during ESD testing allows for current sharing during matching between networks and common triggering voltage conditions [2].
- *Unconnected Structures*: It is a common ESD design practice to address structures not containing electrical connections to the power grid or circuitry. In semiconductor chips, there are many structures that are electrically not connected to other circuitry or power grids, which are vulnerable to ESD damage. Unique ESD solutions are used to address floating or unconnected structures [2].
- *Utilization of 'Dummy Structures and Dummy Circuits'*: In the ESD design practice it is not uncommon to utilize dummy structures or dummy circuits that serve the purpose to provide better current uniformity or distribution effects; these concepts span from the usage of dummy Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) polysilicon gate fingers to dummy inverter circuits [2].
- *Nonscalable Source Events*: Another key issue is that the ESD event is a nonscalable event. Each generation, the size of devices is scaled to smaller dimensions. The ESD design practice must address the constant source input current, and the physical scaling of the structures. A unique ESD scaling theory and strategy must be initiated to address this issue [2].

1.2 FUNDAMENTAL CONCEPTS OF RF ESD DESIGN

In the ESD design discipline of radio frequency (RF) circuits, there is a fundamental difference in the focus and methods that are required, which are distinct from the ESD design practices used in ESD protection of digital circuitry [3]. This rapidly developing ESD design practice utilizes some of the ESD digital design practices when it is possible and abandons some practices, ESD circuits, and design when they are unsuitable for RF applications. In this evolution, the ESD design discipline is shifting and adapting design practices used by microwave RF circuit designers, in addition to the new, and unique RF ESD design practices that will be established to cosynthesize RF functional application needs and ESD protection [4]. The RF ESD design discipline is presently evolving as the application frequency, which continues to increase as well. The key question is what makes this new design practice unique from ESD design practice, and how does it differ from RF design practices.

The RF fundamental concepts for the ESD protection and design of RF components are as follows:

- *RF ESD Application Frequency Dependent ESD Solutions*: In RF ESD design, the solutions and methods for the ESD protection may be a function of the application frequency. Below 1 GHz, traditional digital ESD on-chip silicon ESD circuit solutions may be sufficient. Between 1 and 5 GHz, the choice of ESD device may be a function of the tradeoffs of loading and other RF parameters. Above 5–15 GHz, RF ESD cosynthesize may be a mandatory process. Above these application frequencies, off-chip protection and nontraditional ESD solutions may be necessary (Figure 1.1).

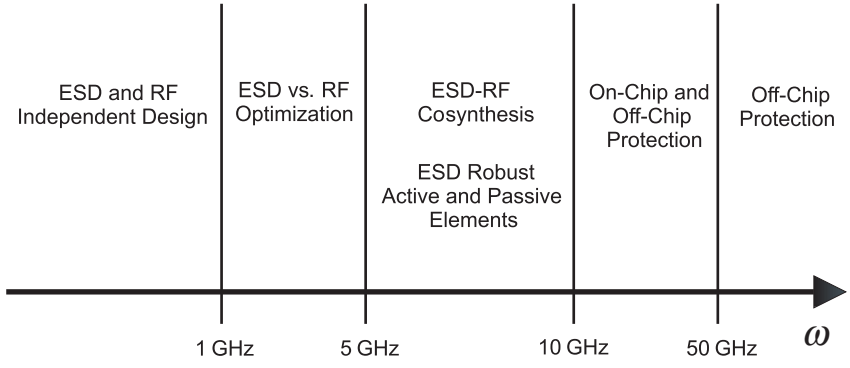

Figure 1.1 RF ESD design as a function of application frequency

- *RF Models for ESD Elements*: With RF circuits and components, d.c. and RF models are required to build RF circuits. As a result, all ESD elements must have full RF quality models. This is very different from ESD digital design practices that are not highly dependent on an ESD model. ESD design for digital design does not require a physical model. On the contrary, RF applications require some form of RF model analysis of the ESD element as it influences all of the RF functional parameters. This influences the physical design implementation.
- *RF ESD Design Methodology*: With the requirement of high-quality RF models, ESD design methodologies require full RF model support as well. As a result, the computer-aided design methodology for the ESD design methods must address this issue. As an example, it may require new computer-aided design methodologies that are not practiced in digital design and are more adaptable to the RF design environment. As an example to be discussed in a later chapter, custom fixed design sizes, growable or scalable designs, parameterized cells, and/or hierarchical parameterized cell ESD networks and methods of extraction for various size implementations may be required [5,6,7].
- *RF ESD Design Chip Subfunction Synthesis*: With RF ESD design, the synthesis of the digital, analog and RF segments may require unique structures in the substrate wafer or in the interconnect system, to isolate the electrical noise, and at the same time provide ESD protection between the various segments of the chip. This may require unique physical structures and circuits to address the circuit subfunction ESD protection. Although the same ESD networks used in digital ESD design practices are utilized, the design choices are distinct as a result of the implications on the RF application. For example, ESD diodes can be used between ground rails and between chip subfunctions. In ESD digital design, the focus may be differential voltage isolation; for the RF ESD design practice, the focus may be the capacitive coupling, and the impact on RF stability of networks [5,6].
- *RF ESD Test Methods*: In the ESD testing of RF components, unique tests need to be established on a component level and system level to evaluate the ESD degradation. Unique RF testing methods are needed that will address different d.c. and RF parametrics degradation to evaluate the pre- and post-ESD stress test conditions [8]. A distinction between digital ESD design practice and RF ESD design practice is that the digital ESD

design practice focuses on d.c. voltage shifts and leakage; whereas in RF ESD design practice, the focus is on the RF parameters and what occurs first:–d.c. or RF degradation [8]. These methods may contain RF methods such as time domain reflection (TDR) and time domain transmission (TDT) methods.

- *RF ESD Failure Criteria*: In RF applications, the functional requirements are very distinct from digital applications. Unique RF parameters and ESD failure criteria require to be established on the basis of the RF parameters, d.c. parameters, and system level requirements. This is distinct from the typical digital applications, which only require d.c. leakage evaluation [8,9].
- *RF ESD Test Systems*: To address the RF ESD test methods and failure criteria, new RF ESD test systems may be required that address product evaluation. RF ESD test systems may require ESD systems that allow extraction of the RF parameters *in situ* for noise figure (NF), gain (G), output intercept third order (OIP3) harmonics as well as d.c. leakage evaluation. This may influence the direction of ESD HBM, MM, and transmission line pulse (TLP) systems. In recent times, 50 Ω-based TLP systems are compatible with 50 Ω-based RF circuits. Additionally, future TLP systems may be influenced by the needs of RF circuits.
- *ESD Frequency Spectrum Versus Functional Applications*: In advanced RF designs, the RF circuits are significantly faster than the ESD phenomenon; this allows for frequency 'bands' for the ESD phenomenon and ESD circuit element response versus the RF functional circuit operation and application frequency. As the RF application frequency exceeds 5 GHz, the application frequency will exceed the ESD CDM energy spectrum (e.g., approximately less than 5 GHz). As the application frequency exceeds the ESD phenomenon, the RF ESD design methodology allows for the utilization of the difference in the response during ESD event time scale (e.g., frequency) and application frequency.
- *ESD Frequency Domain Load Reduction Methods*: In RF ESD design, a higher focus is used to lower the loading effects by taking advantage of the frequency response of the RF networks, which are distinct from the ESD phenomena [3].
- *ESD Method of Cosynthesis of ESD and RF Circuits*: In the RF design of ESD networks, it is necessary to design the ESD device in conjunction with the RF circuit. By cosynthesis of the network, the loading effect as well as frequency modifications can be optimized to prevent the limitation of the RF ESD network [3].
- *Utilization of Shunt RF Elements as ESD Elements for the Alternative Current Loop*: In RF design, shunt elements are needed for impedance matching. These parallel shunt elements can help to provide electrical connectivity to the ESD alternative current loop. As a result, the RF shunt serves the role of providing a path to the ESD alternative current loop and must also have ESD robustness requirements to be effective.
- *ESD Method of Utilization of ESD Element as a Capacitor in RF Design*: ESD elements can serve as capacitor elements. Hence, in the cosynthesis, a method of transfer of the capacitance from the functional circuit to the ESD element to achieve the same RF performance is achievable [3].
- *ESD Method of Series to Parallel Conversion of RF Element to ESD Element*: Given a functional RF circuit that is defined as a series configuration, the representation can be

modified to a parallel configuration. In the transformation from a series configuration to a parallel configuration, some portion of the element can be utilized for ESD protection using it as a parallel shunt to power or ground rails [3].

- *ESD Method of Utilization of ESD Element as a Shunt Capacitor*: Given a functional RF circuit, which is defined as a series capacitor configuration, the representation can be modified to a parallel configuration in order to establish a shunt capacitor equivalent circuit. Given a capacitor in series with a resistor element, this circuit can be transformed into an equivalent circuit of a resistor and capacitor in parallel for which it achieves the same quality factor (Q). The transformation of the network with a matched Q achieves the same circuit response. In this fashion, a series capacitor element can be substituted for a shunt ESD element, that serves as an ESD element in either diodic operation or breakdown mode of operation [3].
- *ESD Method of Parallel Susceptance Equivalent Load Compensation*: Capacitive loads that are in parallel configuration can be transformed as treating two parallel susceptances. In the implementation, the total susceptance load is the parallel configuration of the new load susceptance and the ESD susceptance. Hence, the transformation of the total load susceptance to an equivalent parallel configuration of an ESD susceptance load and a new susceptance load [3].
- *ESD Method of Series Inductive Decoupling of ESD Element Circuit*: Using inductor elements in series with the ESD element, the loading effect of the ESD element can be inductively isolated. A series inductor providing a low $L(\mathrm{d}i/\mathrm{d}t)$ during ESD events allows for the current to flow through the ESD element to a power rail or ground. During functional RF operation, the $L(\mathrm{d}i/\mathrm{d}t)$ allows voltage isolation of the ESD element [10,11].
- *RF ESD Method of Narrow Band Fixed Load Absorption and Resonant: Matching L-Matching Compensation Method*: ESD elements can serve as a means to provide impedance matching between the output and the load. Hence, using matching techniques, the ESD element can serve as the matching elements to provide optimum matching conditions. Using a L-match circuit, consisting of a series inductor and a shunt capacitor (e.g., ESD element), the ESD network can be used as a means to provide matching between the source and the load. The shunt capacitor must remain on a constant conductance circle on a Smith admittance chart [3].
- *RF ESD Method of Narrow Band Fixed Load ESD Absorption and Resonant Matching L-Match*: For 'absorption matching' the stray reactance are absorbed into the impedance matching network up to the maximum that are equal to the matching components. For 'resonance matching' stray reactance are resonated out with an equal and opposite reactance, providing cancellation. Hence, the stray reactance serving as an ESD element can be resonance matched to an inductor of equal reactance. An inductor element in parallel with the ESD capacitor element can null the ESD capacitance loading effect providing 'resonance matching' that hides the ESD capacitive element by matching the inductor susceptance [3].
- *ESD Method of Cancellation*: Using RF components, the loading effect of an ESD element can be hidden at the application frequency. Cancellation of the ESD loading effect can be achieved by proper loading of additional elements [12–14].

- *ESD Method of Impedance Isolation*: Using inductors in series with an ESD network, the inductors can serve as high impedance elements such that the loading effect of the ESD element is not observed at application frequencies [14–16].
- *ESD Method of Impedance Isolation using LC tank*: Using inductor and capacitor in parallel, an LC resonator tank in series with an ESD element, the loading effect of the ESD element can be reduced. The frequency of the LC tank is such that it allows operation of the ESD element but provides isolation during functional RF operation [14–16].
- *ESD Method of Lumped Versus Distributed Load*: In RF ESD design, ESD design focus on load reduction is achieved in the frequency domain by taking advantage of the distributed ESD loads instead of single component lumped elements. The 'distributed' versus 'lumped' design method can be achieved within a given element or multiple elements [17–28].
- *ESD Method of Distributed Design using Design Layout*: In RF ESD design, ESD design focus on load reduction is achieved in the frequency domain by taking advantage of the distributive nature of a single ESD element. This can be achieved through design layout by providing introducing resistance, capacitance, or inductance within a given ESD design layout. Metal interconnect design and layout distribution within diodes, MOSFETs, and bipolar transistors can introduce distributive effects. When this effect is typically undesirable in a digital operation of the ESD elements, in an RF application, it can be intentionally utilized [29].
- *ESD Methods of Distributed Design using Multiple Circuit Element Stages*: In RF ESD design, ESD design focus on load reduction is achieved in the frequency domain by taking advantage of multiple elements. This can be achieved by multiple stage designs of equal, or variable size stages with the introduction of resistance, capacitance, or inductance within a given ESD multiple-stage design. This can be achieved through introduction of RF resistor, capacitor, or inductor components into the ESD implementation; whereas, this is typically undesirable in a digital operation of the ESD elements, in an RF application, this can be intentionally utilized [17–28,30–33].
- *ESD Method of Resistive Decoupling Using Distributed Multiple Circuit Element Stages*: In RF ESD design, ESD design focus on load reduction is achieved in the frequency domain by taking advantage of multiple elements and series resistors. This can be achieved by multiple stage designs of equal, or variable size stages with the introduction of resistors within a given ESD multiple-stage design. The introduction of resistors provides an IR voltage drop isolating the successive stages during functional operation, but not during ESD operation.
- *ESD Method of Inductive Decoupling Using Distributed Multiple Circuit Element Stages*: In RF ESD design, ESD design focus on load reduction is achieved in the frequency domain by taking advantage of multiple elements and inductors. This can be achieved by multiple stage designs of equal, or variable size stages with the introduction of on-chip or off-chip inductors within a given ESD multiple-stage design. The introduction of inductors produces an $L(\mathrm{d}i/\mathrm{d}t)$ voltage drop isolating the successive stages during functional operation, but not during ESD operation [23,24,26–28,30–33].
- *ESD Methods of Distributed Design Using Coplanar Waveguides*: In RF ESD design, multi-stage implementations can place coplanar waveguides (CPW) to provide

improvements in the power transfer, matching, and to reduce the loading effect on the input nodes [26–28,30–33].

- *ESD Method of Distributed Design for Digital Semiconductor Chip Cores*: Digital chip sectors are not inherently designed for 50 Ω matching conditions. Hence, an RF design practice is a placement of a resistive element shunt for utilization of distributed design for core chip subfunctions [26–28].
- *ESD Method of Capacitive Isolation Buffering*: Using decoupling capacitors in series with RF elements can provide impedance buffering of receiver networks, allowing operation of ESD networks. Capacitor elements can be metal–insulator–metal (MIM) capacitors, vertical parallel plate (VPP) capacitors, or metal-interlevel dielectric layer metal (M/ILD/M) capacitors. This method cannot be utilized in d.c. circuits due to the blocking of d.c. currents [34].
- *ESD Method of Architecturing an ESD circuit for Improved Linearity*: ESD networks can be designed in a fashion to eliminate linearity issues in RF design. For example, diode elements and varactor structures have capacitance variation as a function of applied voltage. Using ESD elements (e.g., double diode configuration), RF circuit linearity can be improved [35].
- *RF ESD Method of Tuning an ESD circuit for Improved Linearity*: ESD networks can be designed in a fashion to improve linearity issues in RF design by tuning. For example, diode elements and varactor structures have capacitance variation as a function of applied voltage. These variations can be modified by variable tuning by utilization of tunable ESD elements with semiconductor process or design layout techniques [35].
- *RF ESD Method of Noise and ESD Optimization*: Noise in RF circuits is a large concern. This influences the chip architecture between the digital, analog and RF circuits. Additionally, noise concerns also determine the substrate doping concentration, semiconductor profile, isolation strategy, and guard ring design. Additionally, noise may determine the acceptable ESD device type due to noise concerns. Hence, the method of cosynthesis of chip architecture, chip power grids, choice of ESD elements, and choice of ESD circuits are all influenced by the noise requirements [3].
- *RF ESD Method of Quality Factor and ESD Optimization*: The quality factor, Q, is influenced by the ESD device choice. Additionally, Q degradation can occur in RF passive elements such as resistors, inductors, and capacitors from ESD events. Hence, Q optimization and the ESD current path optimization are needed to have RF degradation mechanisms associated with ESD stress of critical circuit elements [3,12,13].
- *RF ESD Method of Stability and ESD Optimization*: In RF ESD design, circuits must be designed to achieve electrical d.c. stability, thermal stability, and RF stability. Amplifier stability is a function of the stability at both the source and the load. In RF design, these are defined as source and load stability circles. The stability of the source and load is a function of the minimum resistance requirement. With the addition of ESD ballast resistance, circuit stability can be improved. Cosynthesizing the stability requirement, ESD resistance can be integrated to improve circuit stability [3].
- *RF ESD Method of Gain Stability, Noise, Q, and ESD Optimization*: In the optimization of circuits, the gain stability, noise, quality factor, and the ESD can be cosynthesized.

An ESD circuit can be designed in such a way that the ESD elements are added to a circuit to help satisfy the Stern stability criteria. For ESD optimization, the path from source to load along the gain–noise optimum contour, which has the maximum shunt capacitance will achieve this optimized solution [3].

- *ESD Circuits Which Are Nonfrequency Triggered*: The introduction of ESD circuits with frequency-initiated trigger elements, such as RC-triggered MOSFET ESD power clamps, or RC-triggered ESD input networks, can be undesirable because of the interaction with other RF circuit response. For example, the introduction of RC-triggered networks that have inductor load can introduce undesired oscillation states and functional issues. Hence, in RF technology, nonfrequency initiated trigger networks are desirable for some RF applications (e.g., voltage-triggered networks).
- *ESD System Level and Chip Level Multistage Solutions*: At radio frequency application frequencies, ESD protection loading effects have significant impact on RF performance. ESD solutions for RF application include the combination of both on-chip and off-chip ESD solutions: spark gaps, field emission devices (FED), transient voltage suppression (TVS) devices, polymer voltage suppression (PVS) devices, mechanical shunts, and other solutions. By combining both off- and on-chip ESD protection solutions, the amount or percentage of on-chip protection solutions can be reduced.
- *On-Chip and Off-Chip Protection*: In future high speed applications, a mix of off-chip and on-chip protection may be required to reduce the capacitance loading effects. The off-chip protection can be present in the electrical cables, connectors, ceramic carriers, or on the circuit boards. As the frequency increases, or the materials change, the ESD protection may shift to only off-chip protection.
- *ESD Nonsemiconductor Devices*: Spark gaps, field emission devices (FED), transient voltage suppression (TVS) devices, polymer voltage suppression (PVS) devices, mechanical package 'crowbar' shunts, and other solutions are utilized in RF applications off-chip due loading effects, space (e.g., ESD design area), cost (e.g., cost/die), or the lack of the proper material to form ESD protection circuitry (e.g., substrate material). These solutions are not typically an option in semiconductor chips with high pin-count and packaging constraints, but for low pin-count low circuit density applications, these are an option.

1.3 KEY RF ESD CONTRIBUTIONS

In the field of electrostatic discharge (ESD) of radio frequency (RF) devices, accomplishments to advance the field are in the form of development of experimental discovery, analytical models, introduction of new semiconductor devices and circuits, test equipment, and test methods. Below is a short chronological list of key events that influenced the field of radio frequency (RF) electrostatic discharge (ESD):

- 1968 A.D. D. Wunsch and R.R. Bell introduce the power-to-failure electro-thermal model in the thermal diffusion time constant regime [36].
- 1970 A.D. D. Tasca develops the power-to-failure electro-thermal model in the adiabatic and steady-state time constant regime [37].

- 1970 A.D. Y. Anand, W. J. Moroney, G.E. Morris, V. J. Higgins, C. Cook, and G. Hall evaluate the ESD robustness of Schottky diodes for microwave mixer applications [38]. This work is significant as it demonstrates some of the first measurements and failure analysis highlighting the failure of microwave components in microsecond to nanosecond time regimes.
- 1971 A.D. Vlasov and Sinkevitch develop a physical model for electro-thermal failure of semiconductor devices [39].
- 1972 A.D. W.D. Brown evaluates semiconductor devices under high amplitude current conditions [40].
- 1979 A.D. R.L. Minear and G.A. Dodson demonstrate failure mechanisms in Silicon bipolar monolithic transistors. The significance of the work lies in the introduction of butted base contacts, known as the 'phantom emitter' to provide ESD improvements in bipolar transistors [41].
- 1979 A.D. J.J. Whalen demonstrates the power-to-failure of GaAs MESFET devices due to RF power magnitude. This study also demonstrates the relationship of absorbed energy to time-to-failure in GaAs devices [42].
- 1979 A.D. J.J. Whalen and H. Domingos evaluated the inter-relationship of the power-to-failure associated with an RF oscillating signal and ESD HBM pulse waveforms on GaAs ultra-high frequency transistors. The significance of the work is in the demonstration of the relationship between RF power stressing and ESD test stressing and between the absorbed energy and the time-to-failure models [43].
- 1981 A.D. J. Smith and W.R. Littau develop an electro-thermal model for resistors in the thermal diffusion time regime [44].
- 1981 A.D. Enlow, Alexander, Pierce, and Mason address the statistical variation of the power-to-failure of silicon bipolar transistors due to semiconductor manufacturing process, and ESD event variations [45–47].
- 1983 A.D. M. Ash evaluates the nonlinear nature of the power threshold and the temperature dependence of the physical parameters establishing the Ash relationship [9]. This study also demonstrates that Silicon and Gallium Arsenide satisfy the Ash relationship, leading to accurate prediction of the power-to-failure without addressing the temperature variation [48].
- 1983 A.D. V.I. Arkihpov, E.R. Astvatsaturyan, V.I. Godovosyn, and A.I. Rudenko derive the cylindrical nature of the electro-current constriction [49]. The significance of this work lies in the development of a physical model that quantified current constriction in high resistance wafers.
- 1989 A.D. Dwyer, Franklin, and Campbell develop a three-dimensional Green's function model for explanation of power-to-failure in Gallium Arsenide structures. The significance of the work lies in the extension of the Wunsch–Bell model to address dimensional scale length variations in the three dimensions [50].
- 1986 A.D. A.L. Rubalcava, D. Stunkard, and W.J. Roesch study the effects of ESD on Gallium Arsenide MESFETs and passive structures [51].

- 1987 A.D. F.A. Buot, W.T. Anderson, A. Christou, K.J. Sleger, and E.W. Chase study the theoretical and experimental study of subsurface burnout and ESD in GaAs FETs and HEMTs [52].
- 1990 A.D. K. Bock, K. Fricke, V. Krozer, and H.L. Hartnagel study the improvements in GaAs MESFETs using alternative metallurgy, spark gaps, and field emission devices (FEDs) [53].
- 1993 A.D. L.F. DeChairo and B.A. Unger evaluate ESD degradation in InGaAsP semiconductor lasers resulting from human body model ESD [54].
- 1997 A.D. S. Voldman develops the lateral 'polysilicon-bound ESD diode' structure. The work is significant for its invention of a device used today for RF Complementay Metal Oxide Semiconductor (CMOS) ESD applications [55].
- 1999 A.D. B. Kleveland and T. H. Lee apply distributed RF concepts to ESD protection networks. This work utilizes the concepts of distributed network to ESD structures for radio frequency applications [23,24].
- 2000 A.D. S. Voldman and P. Juliano publish the first TLP measurements of a Silicon Germanium (SuGe) heterojunction bipolar transistor (HBT). They also evaluate the SiGe power-to-failure characteristics as a function of pulse width [56].
- 2000 A.D. C. Richier, P. Salome, G. Mabboux, I. Zaza, A. Juge, and P. Mortini investigate different ESD protection strategies for 2 GHz RF CMOS applications. The significance of the work lies in the choosing of ESD elements on the basis by the ESD robustness versus RF parameter characteristics. The second significant conclusion is the effectiveness of polysilicon-bound silicon lateral diodes for RF ESD applications [35].
- 2001 A.D. S. Voldman, A. Botula, and D. Hui develop the first Silicon Germanium ESD Power Clamps [57]. This work is significant because of its utilization of the high unity current cutoff frequency/low breakdown transistor as the trigger element for the low high unity current cutoff frequency/low breakdown transistor, invoking a natural scaling relationship.
- 2001 A.D. S. Voldman, L. Lanzerotti, and R.R. Johnson evaluate the emitter-base design sensitivities of the SiGe HBT device [58]. The significant finding of the work is the implications of emitter-base scaling on the ESD robustness of SiGe HBT devices.
- 2001 A.D. P. Leroux and M. Steyart utilize on-chip inductors for a 5.25 GHz low noise amplifier (LNA) applications. This work utilizes the inductors as part of RF-ESD design cosynthesis methodologies [10].
- 2002 A.D. S. Voldman, B. Ronan, and L. Lanzerotti publish the first TLP measurements of a Silicon Germanium Carbon (SiGeC) hetero junction HBT device. This is a significant study as it provides a comparison of the SiGeC HBT and the SiGe HBT [59].
- 2002 A.D. S. Voldman, B. Ronan, S. Ames, A. Van Laecke, and J. Rascoe demonstrate testing methodologies for RF single devices, products, and systems. This study demonstrates the RF degradation typically occurs prior to ESD failure based on leakage specifications and addresses RF ESD failure criteria [8].
- 2002 A.D. S. Voldman, S. Strang, and D. Jordan demonstrate an automated ESD design system methodology that allows RF ESD cosynthesis in a RF foundry system [5–7]. The

study show that the methodology achieved has the ability to provide RF-ESD cosynthesis integrated into a modern design methodology suitable for RF CMOS, and RF BiCMOS Silicon Germanium foundry environment.

- 2003 A.D. Y. Ma and G.P. Li demonstrate construction of GaAs-based ESD power clamp networks for InGaP/GaAs and GaAs technologies. The significance of the work lies in the utilization of ESD power clamps in RF GaAs applications [60].
- 2003 A.D. M.D. Ker and B.J. Kuo optimize a broadband RF performance and ESD robustness by π-model distributed ESD protection scheme. The significance of the work lies in the extension of the range of distributed networks to the 1–10 GHz RF application range [30,31].
- 2003 A.D. S. Hynoven, S. Joshi and E. Rosenbaum discuss method of resonant absorption to lower the effective loading effects of ESD, referred to as 'cancellation method.' The significance of the work is in the utilization of inductors as inductive shunts to V_{DD} or V_{SS} providing 'cancellation' of the loading effect of the diode capacitance [12,13].
- 2004 A.D. K. Shrier demonstrates ESD improvements in GaAs power amplifiers using electronic polymer off-chip protection elements [61]. This study shows the utilization of low capacitance polymer voltage suppression (PVS) devices as a solution for RF ESD protection.
- 2005 A.D. S. Hynoven and E. Rosenbaum develop single inductor/single diode ESD networks. The significance of the work is in the utilization of inductors as inductive shunts to V_{DD} or V_{SS} providing 'cancellation' of the loading effect of the diode capacitance [12,13].

1.4 KEY RF ESD PATENTS

In the past few years, a significant number of patents in the field of ESD protection of RF technologies are seen.

The patents on ESD protection of radio frequency devices address the following classes of solutions:

- RF ESD active and passive elements [61–79];
- RF ESD input circuits [80–91];
- RF ESD power clamps [92–95];
- RF ESD design integration issues [96–103];
- RF ESD design systems [7, 104–106].

1.5 ESD FAILURE MECHANISMS

ESD-induced failure mechanisms lead to both latent damage and destruction of RF semiconductor elements. ESD-induced failure mechanisms are a function of the technology

Table 1.1 ESD failure mechanisms in RF CMOS devices

RF CMOS			
Device	Test type	Polarity	Failure mechanism
RF CMOS MOSFET	HBM	Positive	MOSFET Source-Drain
	CDM	Positive	MOSFET Gate Dielectric
STI-bound p^+/n-well diodes	HBM	Positive	p^+-to-well
Poly-bound P-N diodes	HBM	Positive	p^+ to n-well
	CDM		Polysilicon Gate of diode structure
Inductors	HBM	Positive or negative	Inductor Vias and metal underpass
MIM capacitors	HBM	Positve or negative	MIM dielectric
Polysilicon resistors	HBM	Positive or negative	Polysilicon film

type, device, circuit topology, and RF chip architecture. In this section, a brief tabulation of ESD failure mechanisms will be highlighted for RF CMOS, RF Silicon Germanium, RF Silicon Germanium Carbon, Gallium Arsenide, and Indium Gallium Arsenide technologies. The primary distinction between digital CMOS ESD failure mechanisms and RF failure mechanism is not the RF environment but the utilization of different technologies, circuit topologies, and extensive use of RF passive elements.

1.5.1 RF CMOS ESD Failure Mechanisms

Table 1.1 contains a brief summary of the ESD mechanisms observed in RF CMOS devices. The key distinction in this table is that in RF CMOS, there is a greater use of RF CMOS passive elements. In a RF CMOS technology that uses standard thin oxide MOSFET capacitors and RF inductors from standard CMOS film thickness, ESD failures will occur in the passive elements.

In Table 1.2, a listing of RF ESD circuit failure mechanisms is tabulated. In RF CMOS, ESD networks consist of shallow trench isolation (STI) bound diode networks,

Table 1.2 RF CMOS ESD network failure mechanisms

RF ESD Circuits			
Circuit type	Test type	Polarity	Failure mechanism
RF CMOS Grounded Gate NFET	HBM	Positive	MOSFET Source-Drain
RF CMOS STI-Bound dual diodes	HBM	Positive	p^+/n-well diode
	HBM	Positive	p^+/n-well diode
RF CMOS poly-bound dual diodes	HBM	Positive	p^+/n-well
	CDM		Polysilicon Gate of diode structure
RF CMOS inductor/diode	HBM	Positive	Inductor
	HBM	Negative	Diode
RF CMOS diode/inductor	HBM	Positive	Diode
		Negative	Inductor

Table 1.3 HBM ESD failures in Silicon Germanium-based devices

Silicon Germanium				
Device	Structure	ESD test	Polarity	Failure mechanism
SiGe SA npn HBT	Epitaxial SiGe film	HBM, MM	Positive, negative	Emitter–Base junction
SiGe NSA npn HBT	Epitaxial SiGe film	HBM, MM	Positive, negative	Emitter–Base junction
SiGe Raised Extrinsic Base npn HBT	Epitaxial SiGe film	HBM, MM	Positive, negative	Emitter–Base junction
SiGe Base-Collector Varactor	SiGe Base /Si Sub-collector	HBM, MM	Positive, negative	Base–Collector junction

polysilicon-bound diode networks, diode/inductor elements, impedance isolation LC tank/diode networks, and grounded gate RF MOSFET networks. The table contains a listing of the known failure mechanisms.

1.5.2 Silicon Germanium ESD Failure Mechanisms

Table 1.3 contains a brief summary of the ESD mechanisms observed in RF Silicon Germanium devices. RF BiCMOS Silicon Germanium technologies contain both bipolar devices, CMOS devices and hybrid structures. As in RF CMOS, ESD failures will occur in the RF CMOS active and passive elements. Table 1.3 addresses the additional RF Silicon Germanium device element ESD-induced failures.

1.5.3 Silicon Germanium Carbon ESD Failure Mechanisms in Silicon Germanium Carbon Devices

Table 1.4 contains a brief summary of the ESD mechanisms observed in RF Silicon Germanium Carbon devices. RF BiCMOS Silicon Germanium Carbon technologies contain both bipolar devices, CMOS devices, and hybrid structures. As in RF CMOS, ESD failures will occur in the RF CMOS active and passive elements. Table 1.4 addresses the additional RF Silicon Germanium device element ESD-induced failures. At this point, there is no known distinction between the ESD failure mechanisms in Silicon Germanium Carbon and Silicon Germanium devices, other than the ESD failure levels.

Table 1.4 HBM ESD failures in Silicon Germanium-based devices

Silicon Germanium Carbon				
Device	Structure	ESD test	Polarity	Failure mechanism
SiGeC SA *npn* HBT	Epitaxial SiGe film		Positive, negative	Emitter–Base junction
SiGeC raised extrinsic base *npn* HBT	Epitaxial SiGe film		Positive, negative	Emitter–Base junction

Table 1.5 HBM ESD failures in Gallium Arsenide-based devices

Gallium Arsenide				
Device	Length (μm)	Width (μm)	HBM Failure level (V)	Failure mechanism
MESFET	0.8 (Gate)	1500	+100	Gate-to-Source
	1.0 (Gate)	2800	+350	Gate-to-Source
	2.0 (Gate)	220	+50	Gate-to-Source
HEMT	0.5 (Gate)	280	+90	Gate-to-Source
HBT		20	+120	Emitter-Base
		6 × 20	+480	Emitter-Base

1.5.4 Gallium Arsenide Technology ESD Failure Mechanisms

Gallium arsenide technology has unique ESD-induced failure mechanisms distinct from RF CMOS and RF Silicon Germanium technology because of the different materials (e.g., substrate, dopants, and metallurgy), structures, and device types. These types of devices vary from MESFETs, HEMT, to HBT devices. As a result, the ESD failure levels and failure mechanisms are very different. In Table 1.5, a brief list of GaAs ESD-induced failure mechanisms are tabulated.

1.5.5 Indium Gallium Arsenide ESD Failure Mechanisms

Indium Gallium Arsenide (InGaAs) based devices are used from lasers, photodetector to PIN diode applications. Table 1.6 shows some experimental data of ESD failure levels and failure mechanisms.

Table 1.6 HBM ESD failures in Indium Gallium Arsenide-based devices

InGaAs				
Device	Structure	Width (mil)	HBM failure level (V)	ESD Failure mechanism
InGaAs Laser	GaAs substrate	10	−1500	
		20	−4000	
		30	−5500	
GaInAs/GaAlAs MODFET	GaAs substrate InGaAs Channel			Gate burnout
InGaAs/InP Photodetectors		50–80 μm	700	
InGaAs PIN	InGaAsP Substrate		−200	

Table 1.7 RF bipolar receiver circuits failure mechanisms

RF bipolar circuits				
Circuit type	Test type	Polarity	Test mode	Failure mechanism
Single ended common emitter	HBM, MM	Positive or negative	Input-to-V_{SS}	Emitter–Base junction
Single ended C-E receiver with MIM series capacitor	HBM, MM	Positive or negative	Input-to- V_{SS}	Capacitor Element
Single ended C-E receiver with resistor feedback	HBM, MM	Positive or negative	Output-to-input	Feedback resistor element
Single ended C-E receiver with resistor and capacitor feedback	HBM, MM	Positive or negative	Output-to-input	Feedback resistor and capacitor element
Single ended C-E receiver with emitter resistor degeneration	HBM, MM	Positive or negative	Input-to-V_{SS}	Emitter–Base junction
Single ended C-E with Balun output	HBM, MM	Positive or negative	Output-to-output	Balun or d.c blocking capacitor failure
Differential Common-Emitter receiver	HBM, MM	Positive or negative	Input-to-input	Emitter–Base junction
Bipolar Current mirror	HBM, MM	Positive or negative	Input-to-ground	Collector-to-Base

1.5.6 RF Bipolar Circuits ESD Failure Mechanisms

RF bipolar circuits have failure mechanisms that are associated with the RF homo-junction bipolar junction transistor (BJT) or HBT, and the passive derivatives. Circuit topology plays a large role in the ESD-induced failure mechanisms observed in RF bipolar circuits. For example, failure mechanisms between single-ended mode and differential mode receiver networks are very different. Table 1.7 shows some examples of RF bipolar ESD-induced failure mechanisms.

1.6 RF BASICS

In RF ESD design, there are many RF metrics of interest. The metrics are important to understand the language and concerns of RF designers. Additionally, from an ESD perspective these RF metrics are important to understand the ESD failure mechanisms, and how they manifest themselves in RF semiconductor components and products.

Reflection Coefficient

The reflection coefficient represented as a function of characteristic impedance and load impedance,

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$$

This can also be expressed as a function of the characteristic admittance, $Y_o = Z_0$,

$$\Gamma = \frac{Y_0 + Y_L}{Y_0 + Y_L}$$

Normalized Reflection Coefficient

The normalized reflection coefficient can be expressed as normalized to the characteristic impedance. In this form it can be expressed as follows:

$$\Gamma = \frac{(Z_L/Z_0) - 1}{(Z_L/Z_0) + 1}$$

Load Relationship as a Function of Reflection Coefficient

Expressing the load as a function of the reflection coefficient, Γ,

$$Z_L = Z_0 \frac{1 + \Gamma}{1 - \Gamma}$$

Return Loss

$$\mathrm{RL(dB)} = -10 \log |\Gamma \times \Gamma| = -20 \log |\Gamma|$$

Voltage Standing Wave Ratio

The voltage standing wave ratio (VSWR) is a measure of the forward and reflected wave conditions between the maximum voltage and the minimum voltage conditions. This can be expressed as a function of the maximum and minimum voltage, or the reflection coefficients.

$$\mathrm{VSWR} = \frac{V_{\mathrm{MAX}}}{V_{\mathrm{MIN}}} = \frac{|V_f| + |V_r|}{|V_f| + |V_r|}$$

$$\mathrm{VSWR} = \frac{1 + |\Gamma|}{1 - |\Gamma|}$$

The reflection coefficient can also be expressed as a function of the VSWR,

$$\Gamma = \frac{\mathrm{VSWR} - 1}{\mathrm{VSWR} + 1}$$

Mismatch Loss (ML)

Mismatch loss is associated with the loss of signal between two terminations. These terminations can be expressed as a source and a load. The mismatch loss is related to the ability to deliver power to the load.

In the general case, where the reflection coefficient on the source and load is nonzero (e.g., both the source and load are not equal to Z_0), the expression for mismatch loss can be expressed as

$$\mathrm{ML} = \frac{|1 - \Gamma_S \Gamma_L|^2}{[1 - |\Gamma_S|^2][1 - |\Gamma_L|^2]}$$

In the case of a source with characteristic impedance, Z_0, and with a zero reflection coefficient (e.g., $\Gamma = 0$), the mismatch loss can be expressed as

$$\mathrm{ML} = \frac{1}{1 - |\Gamma_L|^2}$$

After ESD stress, given the device-under-test (DUT) is the load, changes in the reflection coefficient in the load due to degradation can lead to changes in the mismatch loss.

Quality Factors

The quality factor, QF, or simply the 'Q' of the element is a metric associated with the ratio of the desired to the undesired electrical characteristics. In any physical element, there exists undesirable parasitics that degrade the nature of a element. For example, in a capacitor, there is resistance associated with the metal interconnects. With an inductor, there is also resistance associated with the coil wire itself. These nondesired features degrade the nature of the physical element. From an ESD perspective, the change in these ideal elements can impact circuit functionality. For example, amorphous or metal grain structure changes can lead to changes in the resistance after ESD stress. This can lead to changes in the 'Q' of the physical elements [3].

In the series expression, it is expressed as the ratio between the series reactance, X_s, and the series resistance R_s.

$$Q = \frac{X_s}{R_s}$$

For a parallel configuration, the form of the quality factor, Q, is expressed as a function of the equivalent parallel circuit expressed as susceptance, B_p, and the conductance, G_p,

$$Q = \frac{B_p}{G_p} \qquad Q = \frac{R_p}{X_p}$$

Noise Figure

The noise figure (NF) is the actual noise power to thermal noise power ratio,

$$\mathrm{NF(dB)} = 10 \log \left[\frac{P_N}{(kT)B} \right]$$

where P_N is the actual noise power, B is the bandwidth, k is the Boltzmann constant, and T is the temperature. ESD-induced degradation can change the actual noise power owing to the changes in the material properties, leading to an increase in the NF.

Output Intercept Point Third Order Harmonic

The OIP3 is the extrapolated power level where the third order inter-modulation product equals the fundamental power level (e.g., also referred to as P_{3IP}). ESD degradation in the fundamental output power can lead to a lowering in the intersection point of the fundamental power and the third order harmonics. As a result, ESD-induced degradation that degrades the fundamental power transfer curve (e.g., power output divided by power input) leads to OIP3 degradation and ESD-induced RF degradation.

Gain Compression Point

The gain compression point is a point on the output power (P_{OUT}) versus input power (P_{IN}) plot where the actual power curve deviates from the fundamental harmonic linear slope. In a linear system, the characteristic is a linear slope on the P_{OUT} versus P_{IN} plot. Power exists in the nonfundamental harmonics, which leads to an output power roll-off with increasing input power.
When the actual output power is 1 dB below the fundamental output power, a typical RF metric is 1 dB Gain Compression; this can be denoted as the P_{1dB}.

During ESD stress, the output power level of a semiconductor device or circuit can be degraded as a result of transistor degradation and impedance degradation. In a multifinger structure, or where parallel elements exist, ESD-induced interconnect failure can also lower the output power levels. This can be apparent by the 1 dB Gain Compression metric.

Dynamic Range

The dynamic range (DR) is the range of system a signal power can handle without significant noise distortion. This is evaluated by the difference between the compression gain and the output noise floor.

$$\mathrm{DR} = P_{1\mathrm{dB}} - (\mathrm{k}TB + \mathrm{NF} + G_A)$$

where DR is the dynamic range (at the output), P_{1dB} is the 1 dB gain compression point, B is the noise bandwidth, NF is the noise figure, and G_A is the available gain of the amplifier.

Spurious Free Dynamic Range

Spurious free dynamic range is the output power level where the inter-modulation product terms reach the noise floor. This can be expressed as a function of the DR and the third order intercept output power, P_{3IP}.

$$\mathrm{SFDR} = \frac{2}{3}[P_{3IP} - \mathrm{DR}]$$

Transmission Line Characteristic Impedance

Characteristic impedance of a lossy transmission line

$$Z_{TL} = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

Transmission Line Electrical Length

The electrical length is the ratio of the transmission line physical length and the wavelength in the medium at a given frequency.

$$E = 360\frac{\ell}{\lambda_G}$$

Phase constant

$$\beta = \frac{360}{\lambda_G}$$

Transmission Line Propagation constant

$$\gamma = \alpha + j\beta$$

1.7 TWO-PORT NETWORK PARAMETERS

In RF analysis, signal characterization is approached as a 'two-port network' where there are two input signals and two output signals. From an ESD perspective, ESD measurements on TLP test evaluation is also similar to this perspective. Hence, evaluation of RF ESD networks from a two-port perspective leads to a natural synergism between signal analysis and ESD TLP testing. In a two-port network, the voltage–current relationships of the terminals can be expressed where the voltages on the input and the output are expressed as a function of the currents on the input and output.

1.7.1 *Z*-Parameters

In a two-port network, the voltage–current relationships of the terminals can be expressed where the voltages on the input and the output are expressed as a function of the currents on the input and output. Two voltage equations are established that are coupled through the current terms, and the coefficients are the impedance terms, known as z-parameters

$$v_1 = z_{11}i_1 + z_{12}i_2$$
$$v_2 = z_{21}i_1 + z_{22}i_2.$$

This can be expressed in matrix form, where the output vector is the terminal voltages, the input vector is the terminal currents,

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}.$$

1.7.2 *Y*-Parameters

In a two-port network, the voltage–current relationships of the terminals can be expressed where the currents on the input and the output are expressed as a function of the terminal voltages on the input and output. Two current equations are established that are coupled through the voltage terms, and the coefficients are the admittance terms, known as y-parameters

$$i_1 = y_{11}v_1 + y_{12}v_2$$
$$i_2 = y_{21}v_1 + y_{22}v_2$$

This can be expressed in matrix form, where the output vector is the terminal currents, the input vector is the terminal voltages:

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

1.7.3 *S*-Parameters

In a two-port network, the voltage–current relationships of the terminals can be expressed where the currents on the input and the output are expressed as a function of the terminal voltages on the input and output using z- and y-parameters. But, in system environments, access to the both input and output terminals are not accessible.

During ESD testing, in many cases, only two terminals are available to determine ESD degradation in RF components. Using reflected, absorbed, and transmitted signal information is of greater value. Transmission line pulse testing also is done as a 'two-pin' test. An electrical pulse is launched from the ESD test system to the DUT. The response of the device is defined by the voltage and current response of the device. The time of electrical failure and the power-to-failure can be deconvolved from the pulse response information.

Scatter parameters, also known as s-parameters, allow to quantify the reflected signal. Two equations are established in which the reflected signals, are coupled through the injected signals, and the coefficients, known as s-parameters, are the scatter terms.

$$b_1 = s_{11}a_1 + s_{12}a_2$$
$$b_2 = s_{21}a_1 + s_{22}a_2.$$

This can be expressed in matrix form, where the matrix is the scattering matrix (e.g., *S*-matrix),

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

where

$$S = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix}$$

In this form, the terms in the *S*-matrix have physical meaning associated with reflection and transmission. The first term on the main diagonal is s_{11}, which is the input reflection coefficient, and the second term on the main diagonal is s_{22} is the output reflection coefficient. The off-diagonal terms, s_{21} and s_{12}, are the forward transmission coefficient and the reverse transmission coefficient, respectively.

S-parameters are used in the evaluation of RF semiconductor devices. Additionally, these can be used to quantify the ESD degradation after ESD stress.

1.7.4 *T*-Parameters

Another representation that is useful for RF analysis is the scattering transfer matrix. This has the advantage of relating scattering and transmission information as an output vector and an input vector.

Scatter transfer parameters, also known as t-parameters, allow to quantify the reflected signal and transmitted signals. Two equations are established

$$a_1 = T_{11}b_2 + T_{12}a_2$$
$$b_1 = T_{21}b_2 + T_{22}a_2$$

This can be expressed in matrix form, where the matrix is the scattering transfer matrix (e.g., *T*-matrix),

$$\begin{bmatrix} a_1 \\ b_1 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} b_2 \\ a_2 \end{bmatrix}$$

where

$$T = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix}$$

To convert from *S*-matrix to *T*-matrix, we can obtain the parameters as follows:

$$T_{11} = \frac{1}{S_{21}}$$

$$T_{21} = \frac{S_{11}}{S_{21}}$$

$$T_{12} = -\frac{S_{22}}{S_{21}}$$

$$T_{22} = -\frac{\det[S]}{S_{21}}$$

and the determinant of the *S*-matrix is

$$\det[S] = S_{11}S_{22} - S_{12}S_{21}.$$

The conversion from the *T*-matrix back to an *S*-matrix is as follows:

$$S_{11} = \frac{T_{21}}{T_{11}}$$

$$S_{21} = \frac{1}{T_{11}}$$

$$S_{12} = -\frac{\det[T]}{T_{11}}$$

$$S_{22} = -\frac{T_{12}}{T_{11}}$$

and the determinant of the *T*-matrix is as follows

$$\det[T] = T_{11}T_{22} - T_{12}T_{21}$$

1.8 STABILITY: RF DESIGN STABILITY AND ESD

In RF design, circuit stability is an important design parameter. In RF ESD design, circuit stability can be influenced by ESD protection networks. A design synthesis of the RF source stability and the ESD sensitivity of the base resistance can be understood from Smith chart analysis. Different stability metrics exist for evaluation of RF circuit stability. From the Stern stability criteria, $K > 1$ achieves unconditionally stable two port networks where

$$K = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\det S|}{2\,|s_{12}s_{21}|}$$

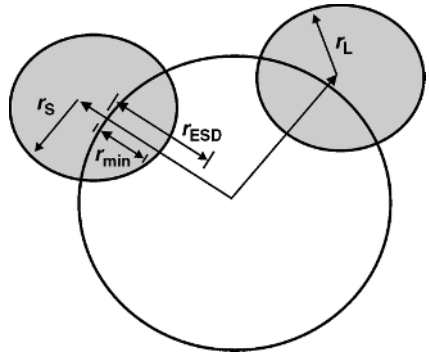

Figure 1.2 Unity radius smith chart with source and load stability circles. Region outside the Unity radius Smith chart is unstable source. Stability and ESD improvement achieved with shift along axis toward radial center

This condition initiates a specific value for the scattering parameters where stability can occur for a two-port network. This can be visualized on a Smith chart.

Source stability requirements will determine a minimum resistance, $R_{\min}$, in order for a source connected to a bipolar base is unconditionally stable. By modification of the base resistance, it is possible to achieve both unconditionally stable circuits and ESD robust circuitry. If the additional resistance added to a bipolar device for ESD robustness improvements exceeds the minimum base resistance, both ESD and the stability criteria can be achieved. Adding resistance beyond $r_{\min}$ can exceed the minimum stability requirement with further improved ESD protection levels (Figure 1.2).

As an example, to optimize power amplifiers or other applications, this can be achieved by evaluating the unilateral constant gain and noise circles on a Smith chart. Plotting the source and load circles on the normalized chart, stability of the circuit can be evaluated.

For example, source and load stability circles can be defined by their radius and center. The radius, r, and center, C, for the source are defined as follows:

$$r_s = \frac{|s_{12}s_{21}|}{||s_{11}|^2 - |\det S|^2|}$$

and

$$C_s = \frac{s_{11}|\det S|s_{22}}{|s_{11}|^2 - |\det s|^2}$$

If the source stability circle center is contained outside the Smith chart, there are conditions that unconditional stability is not achieved.

In this case, a minimum resistance $r_{\min}$ can be defined as the one that moves the source stability circle within the boundary of the Smith chart. In this case, adding resistance $R_{\min}$ to the base of an NPN amplifier can place the amplifier into a metastable condition. Improved stability is achieved by adding a resistance R_{ESD} where

$$R_{\mathrm{ESD}} = R_{\min} + \mathrm{R}_{\mathrm{ESD}}$$

where the first term is for unconditional stability and the second term is additional resistor ballasting for the base region. This method can also be applied to the load stability circles to provide a stable output and identifying a G_p (min) on the constant conductance circles.

As stated above, Stern stability criteria, $K > 1$ achieves unconditionally stable two port networks where

$$K = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\det S|}{2|s_{12}s_{21}|}$$

To achieve stability and design margin, designers should know to have $K > 1.2$. A circuit can be designed such that ESD elements are added to satisfy the Stern criteria and an additional ESD element can be added to provide the extra stability margin.

1.9 DEVICE DEGRADATION AND ESD FAILURE

1.9.1 ESD-Induced D.C. Parameter Shift and Failure Criteria

In the evaluation of ESD failure of RF devices, there are both d.c. and a.c. parameters that are important to determine the presence of latent mechanisms, device shifts, or destructive damage. The ESD failure criteria will be a function of the allowable change for the given product specification or application. For d.c. parameters, the following d.c. parameters are of interest:

- transistor emitter, base or collector leakage;
- transistor emitter-base ideality factor;
- MOSFET threshold voltage shifts;
- MOSFET gate-dielectric leakage current.

Bipolar Transistor Leakage Current

Transistor emitter, base or collector leakage current can be indicative of metallurgical junction dopant movement from thermal stress, transistor 'pipes', silicide penetration of metallurgical junction, or interconnect metallurgy poisoning of the metallurgical junction. From the ESD pulse event, the increase in temperature at the metallurgical junction can lead to a motion of the dopant materials; this will change the junction leakage current. ESD-induced transistor 'pipes' occur between the emitter and collector region, influencing the leakage characteristics. ESD-induced silicide penetration near the metallurgical junction can lead to changes in the leakage characteristics [1]. Leakage current in metallurgical junctions can increase with junction regions that use refractory metals such as titanium salicide, titanium molybdenum, and cobalt salicide. Evaluation of the d.c. shifts can be evaluated as follows:

- emitter-base reverse bias current as a function of the emitter-base voltage;
- collector-base reverse bias current as a function of the collector-base voltage;

- collector-to-emitter reverse bias current as a function of the collector-to-emitter voltage;
- collector-to-substrate reverse bias current as a function of the collector-to-substrate voltage.

Bipolar Transistor Ideality

Transistor emitter-base ideality factor can be altered as a result of ESD stress. Post-ESD stress, the transistor emitter-base ideality factor can be altered as a result of an increase in bulk or surface recombination centers in the emitter–base junction. Transistor emitter-base ideality factors can be observed from the following measurements:

- Gummel plot of base current as a function of the emitter-base voltage and extraction of the base current slope;
- Gummel plot ratio of collector-to-base current as a function of emitter-base voltage;
- extraction of the leakage current scaling with increased temperature;
- direct current bipolar gain characteristics;
- model extraction from Gummel-Poon model at low currents.

As an example, in the work of R.L. Minear and G.A. Dodson, in a CBE bipolar homojunction transistor, it was observed that the pre-ESD stress collector and base ideality factors were $n = 1.02$ and $n = 1.17$ prior to ESD stress, respectively [41]. Base and collector currents were measured for a base-emitter voltage from 0.3 to 1.0 V, with preforward bias current levels from 1×10^{-9} to 1×10^{-3} A levels. After HBM ESD stress of the emitter–base junction, the Gummel plot base characteristic (e.g., log I_B versus V_{BE}) showed a change in the slope with a new ideality factor of $n = 2.02$; no change was observed in the Gummel plot collector current characteristic [41]. In this result, the Gummel plot slope changed by $2\times$ from an ideal device (e.g., $n = 1$); this indicates that the ESD stress generated mid-band gap recombination centers in the emitter–base junction region. The recombination centers can be associated with bulk recombination centers or surface recombination centers. The recombination centers would satisfy a forward bias characteristic of

$$I_B \propto \exp\left\{\frac{qV_{BE}}{2kT}\right\}$$

MOSFET Threshold Voltage Shifts

In RF MOSFET devices, the evidence of ESD-induced degradation may be evident by an observation of the MOSFET threshold voltage shift. In a MOSFET structure, MOSFET threshold voltage shifts can occur due to MOSFET gate dielectric surface state generation, MOSFET hot-electron injection, MOSFET negative bias temperature instability (NBTI), MOSFET gate-induced drain leakage (GIDL), and MOSFET parasitic current devices. ESD-stress can lead to changes in the spatial location of fixed charge in the isolation materials (e.g., LOCOS isolation, or shallow trench isolation), or generate additional charge

due to charge injection. From the d.c. MOSFET threshold measurements, ESD-induced degradation can be evaluated.

MOSFET gate dielectric leakage

Evaluation of the d.c. MOSFET gate dielectric leakage is important to determine d.c. degradation issues with RF MOSFETs. MOSFET gate dielectric leakage can be observed as 'soft breakdown' or 'hard breakdown.' MOSFET 'soft breakdown' can be induced by ESD electrical overstress. In MOSFET gate dielectric breakdown theory, evidence today demonstrates that MOSFET 'soft breakdown' is an early stage of MOSFET 'hard breakdown'. Hence, observed ESD-induced MOSFET gate leakage current may be regarded as a latent failure mechanism, which can lead to MOSFET device failure.

Additionally, it has been found that the location of the MOSFET dielectric damage can influence the d.c. characteristics of the MOSFET. MOSFET dielectric failure can occur MOSFET gate-to-drain, MOSFET gate-to-source, and MOSFET gate-to-channel; the location has an influence on the d.c. characteristics of the MOSFET device.

1.9.2 RF Parameters, ESD Degradation, and Failure Criteria

With ESD-induced degradation, the RF parameter shifts can lead to RF product failure. For example, these degradation will manifest themselves in the key RF metrics.

Reflection Coefficient ESD-induced Degradation

ESD-induced impedance changes can influence the reflection coefficient, and the power transfer into an RF component. Assuming the load is the circuit elements, the change in the reflection coefficient represented as a function of characteristic impedance and load impedance,

$$\Gamma + \Delta\Gamma = \frac{Z_L + \Delta Z_L - Z_0}{Z_L + \Delta Z_L + Z_0}$$

This can also be expressed as a function of the characteristic admittance,

$$\Gamma + \Delta\Gamma = \frac{Y_0 - (Y_L + \Delta Y_L)}{Y_0 + (Y_L + \Delta Y_L)}$$

With the ESD-induced shift in the reflection coefficient, many RF metrics will be influenced:

- load reflection coefficient;
- return loss (RL);
- mismatch loss (ML);
- voltage standing wave ratio (VSWR).

With changes in the resistance characteristics, quality factor degradation will also occur.

$$Q + \Delta Q = \frac{X_s}{R_s + \Delta R_s},$$

Changes in the RF parameters will play a role in the definition of RF product failure. In the following sections, discussion of RF ESD testing techniques and degradation in the RF parameters will be highlighted. The changes in both the d.c. and RF parameters will lead to the definition of ESD failure in the RF product.

1.10 RF ESD TESTING

Now a days, ESD testing and qualification of semiconductor components is performed using a variety of ESD models. The device level ESD testing models and methods are as follows [1,2,107–132]:

- human body model (HBM);
- machine model (MM);
- charged device model (CDM);
- charged cable model (CCM);
- cable discharge event (CDE);
- cassette model;
- transmission line pulse (TLP);
- very-fast transmission line pulse (VF-TLP).

1.10.1 ESD Testing Models

Human Body Model (HBM)

The HBM ESD pulse was intended to represent the interaction of the electrical discharge from a human being, who is charged with a component, or object [107–110]. The model assumes that the human being is initially charged. The charged human source then touches a component or object using a finger. The physical contact between the charged human being and the component or object allows for current transfer between the human being and the object. A characteristic time of the HBM model is associated with the electrical components used to emulate the human being. In the HBM standard, the circuit component to simulate the charged human being is a 100 pF capacitor in series with a 1500 Ω resistor. This network has a characteristic rise time and decay time. The characteristic decay time is associated with the time of the network

$$\tau_{HBM} = R_{HBM} C_{HBM}$$

where R_{HBM} is the series resistor and C_{HBM} is the charged capacitor. This is a characteristic time of the charged source. The HBM characteristic time constant is physically interesting as the time of the pulse is on the order of the thermal diffusion time of many materials used in the semiconductor industry. In recent times, the RC time of the HBM pulse is significantly slower than RF microwave application frequencies.

Machine Model

Another fundamental model used in the ESD industry is known as the MM pulse [111–114]. The model was intended to represent the interaction of the electrical discharge from a conductive source, which is charged with a component or object. The model assumes that the 'machine' is charged as the initial condition. The charged source then touches a component or object. In this model, an arc discharge is assumed to occur between the source and the component or object allowing for current transfer between the charged object and the component or object. In the MM industry standard, the circuit component is a 200 pF capacitor with no inherent resistor component. An arc discharge fundamentally has a resistance on the order of 10–25 Ω. The characteristic decay time is associated with the time of the network

$$\tau_{HBM} = R_{HBM} C_{HBM}$$

where R is the arc discharge resistor and C is the charged capacitor. This is a characteristic time of the charged source. The MM characteristic time scale is significantly faster than the HBM characteristic time scale due to the lack of a resistive element. The MM response is oscillatory and has significantly higher currents than the HBM ESD event, faster than the HBM ESD events, but still significantly lower than today's RF application frequencies.

Charged Device Model (CDM)

The CDM represents an electrostatic discharge interaction between a chip and a discharging means where the chip is precharged [115–117]. The charging process can be initiated by a direct charging, or field-induced charging. The discharge process initiated as contact is initiated between the charged device and the discharging means. The CDM discharge phenomenon occurs at less than 5 ns where typically the rise time of the event is on the order of 250 ps. The CDM event is the fastest of the ESD phenomenon. With a 250 ps rise time, the energy spectrum of the CDM discharge event extends to 5 GHz frequencies. For RF application frequencies below 5 GHz, this ESD event is on the same order as the RF product application. As the RF application frequencies exceed 5 GHz, the RF application frequency extends beyond the ESD phenomena of concern.

Charged Cable Model

Another fundamental model used in the ESD industry is known as the charged cable model or cable model pulse. The model was intended to represent the interaction, the electrical discharge of a charged cable, discharging to a chip, card, or system. To initiate the charging process, a transmission line or cable source is charged through a

high-voltage source or tribo-electrically. The model assumes that the cable is charged as the initial condition. The charged cable source then touches a component or an object. A characteristic time of the cable model is associated with the electrical components used to emulate the discharge process. In the charged cable model, the cable acts as a capacitor element. The characteristic decay time is associated with the time of the network

$$\tau_{CCM} = R_{CCM} C_{CCM}$$

where R is the discharge resistor and C is the charged cable. The capacitance used for this model is 1000 pF. Studies are also completed using a ESD gun, which is discharged through a cable to evaluate the system level events.

Akin to this model, the CDE model is of interest [118–123]. In this case, a transmission lineis used as a source (e.g., instead of a lumped capacitor). The cable is charged, where the pulse length is a function of the length of the cable. This CDE model is very important today because of the wide usage of laptops, servers, and wireless applications. In these cases, the length of the events are significantly longer than the RF application frequencies for long cables.

Charged Cassette Model

The charged cassette model is a recent model associated with consumer electronics and game industry. In consumer electronics there are many applications where a human plugs a small cartridge or cassette into an electronic socket. These are evident in popular electronic games. In today's electronic world, there are many palm size electronic components that must be socketed into a system for nonwireless applications. To verify the electronic safety of such equipment, the cassette itself is assumed as a charged source. The 'cassette model' assumes a small capacitance and negligible resistance. This model is equivalent to a machine model type current source with a much lower capacitor component. The model assumes the resistance of an arc discharge and a capacitance of 10 pF. For RF applications that utilize charged cassettes, charged memory sticks, or other small charged items, the ESD-induced field failures may be best understood using the charged cassette model.

Transmission Line Pulse (TLP)

TLP testing has become an established methodology for the ESD design discipline [125–129]. The popularity of the TLP method is due to semiconductor and circuit engineers, interest in observing the pulsed I–V characteristic response. Historically, pulse testing is focused on the pulse waveform with the focus on the power-to-failure and energy-to-failure. In this form of ESD testing, a transmission line cable is charged using a voltage source. The TLP system discharges the pulse into the device under test (DUT). The characteristic time of the pulse is associated with the length of the cable. The pulse width of a transmission line pulse is a function of the length of the transmission line and the propagation velocity of the transmission line. The propagation velocity can be expressed relative to the speed of light, as a function of the effective permittivity and

permeability of the transmission line source

$$\tau_{\mathrm{TLP}} = \frac{2L_{\mathrm{TLP}}}{v} = \frac{2L_{\mathrm{TLP}}\sqrt{\mu_{\mathrm{eff}}\varepsilon_{\mathrm{eff}}}}{c_0}$$

As a standard practice in recent times, the TLP cable length is chosen to provide a TLP pulse width of 100 ns with less than 10 ns rise time. This choice was intended to find a pulsed waveform that was closest in total energy of a HBM pulse. As a result, the RF application frequencies today are significantly higher than this TLP method. TLP systems are designed in different configurations. TLP system configurations include current source, TDR, TDT, and time domain reflectometry and transmission (TDRT). In all configurations, the source is a transmission line whose characteristic time constant is determined by the length of the transmission line cable. The various TLP configurations influence the systems characteristic impedance, the location of the device under test, and the measurement of the transmitted or reflected signals.

An interesting synergy of TLP testing techniques and RF design is the focus on 50 Ω impedance. The TLP systems methods for TDR, TDT, and TDRT configurations are akin to the reflection and transmission methods used by RF engineers for evaluation of RF parameters. As a result, the ESD testing practice of using 50 Ω TLP systems will be similar to the RF parameter characterization needed to evaluate RF circuits and RF systems.

A second interesting point in the TLP testing method is a two-pin test (unlike the HBM and MM ESD testing methodology). As a result, the method also is closer to the two-port methodology for RF evaluation.

Very Fast Transmission line Pulse (VF-TLP)

The VF-TLP test method is similar to the TLP methodology [125–133]. The interest in the VF-TLP is driven by our understanding of the semiconductor devices in a time regime similar to the CDM time constant. The characteristic time of interest is again determined by the propagation characteristics of the transmission line cable source and the length of the transmission line cable

$$\tau_{\mathrm{VF-TLP}} = \frac{2L_{\mathrm{VF-TLP}}}{v} = \frac{2L_{\mathrm{VF-TLP}}\sqrt{\mu_{\mathrm{eff}}\varepsilon_{\mathrm{eff}}}}{c_0}$$

The VF-TLP pulse width of interest is a pulse width of less than 5 ns and a less than 1 ns rise time. As a result, the VF-TLP characteristic time is on the same order as 1–10 GHz RF application pulses. Hence, this method has potential suitability to evaluate the power-to-failure of RF components. This is a key point. Of all the ESD test methodologies, one of the key values of the VF-TLP test is its pulse width that is closest to the RF source frequency.

Figure 1.3 shows the time constant hierarchy of the ESD phenomenon on a frequency axis. As the application frequency increases, the RF application frequency separates from the ESD pulse phenomena. A key point is that the RF application frequency extends beyond the fastest of the ESD phenomena and hence separates from the ESD pulse waveforms. As the application frequency exceeds 5 GHz, the application frequency exceedes all ESD phenomena of interest.

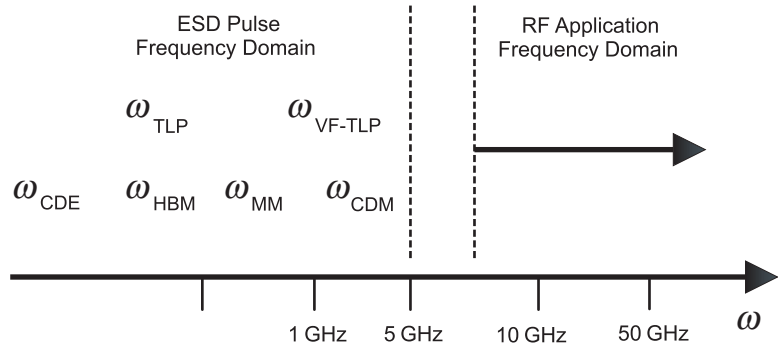

Figure 1.3 Frequency domain plot of ESD phenomena and RF application frequencies

1.10.2 RF Maximum Power-to-Failure and ESD Pulse Testing Methodology

The power-to-failure and the ability of a semiconductor device to survive electrical overstress (EOS), and ESD is important for radio frequency components. In RF components, receiver networks are subjected to electrical stimulus of different power magnitudes, and of different pulse forms and pulse widths. As a result, it is valuable to evaluate both the power-to-failure and the ESD sensitivity of RF components.

Whalen and Domingos [43] evaluated both the response of RF components to RF pulse power and ESD events. Two different independent test methodologies were utilized. A first test system addressed the RF power-to-failure using a RF pulse source. In a second test system, a square pulse test system was utilized.

Figure 1.4 shows the RF pulse system for the evaluation of the electrical overstress of a RF component. For the evaluation of the RF power-to-failure, a system was established that could evaluate the incident, reflected and transmitted power through a RF DUT. An ultra-high frequency source signal was transmitted through a 0–30 dB attenuator. The RF signal was passed through the first directional coupler for the incident power, and the second directional coupler for the reflected power evaluation. A switch followed by a load is placed after the directional couplers to allow for isolation of UHF RF source from the RF DUT. In the TDRT system, the DUT is placed in series with the incident and the transmitted signals. A directional coupler is also utilized to evaluate the transmitted power through the DUT. The three directional coupler elements are followed by crystal detectors and 50 Ω terminations, whose signals are transferred to oscilloscopes and camera sources; these diagnostics capture the incident power, reflected power, and transmitted power waveforms in time.

In this RF test system, the incident power, reflected power and transmitted power waveforms were captured. Whalen and Domingos [43] showed that at the time of failure is observable in the reflected power waveform prior to the end of the applied pulse waveform. In the case of the incident power pulse, a constant power pulse is observable. But, in the reflected power waveform, variation can be observed in the peak power as a function of time. It was noted that a transition occurs in the reflected power waveform, indicating a change in the power absorption and a reduction in the reflected power, followed by an abrupt increase in the reflected power characteristic. This was not observed in power waveforms of RF devices that did not fail at lower power levels.

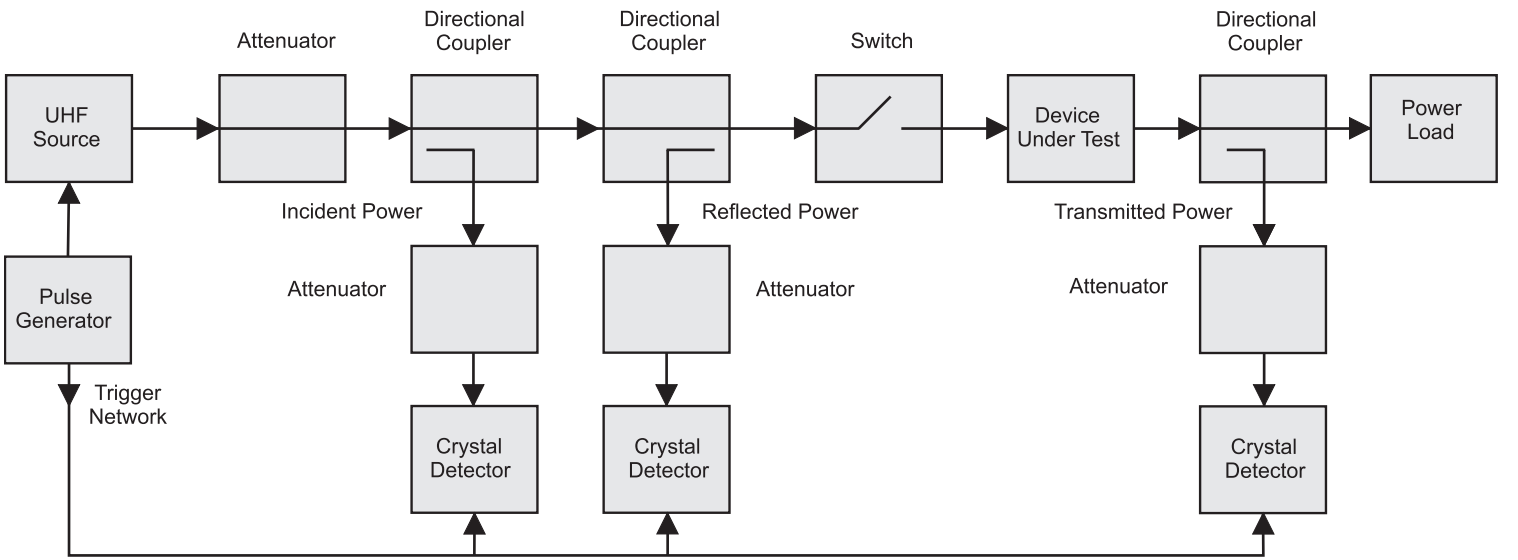

Figure 1.4 RF pulse test system

To evaluate the absorbed energy of the RF device, this can be calculated by the difference between the incident energy and the sum of the reflected and transmitted energy

$$E_A = E_I - E_R - E_T$$

where the incident energy is

$$E_I = \int P_I(t)\mathrm{d}t$$

and the reflected energy is

$$E_R = \int P_R(t)\mathrm{d}t$$

and the transmitted energy is

$$E_T = \int P_T(t)\mathrm{d}t.$$

In the case of RF component failure, the integration is terminated at the time of failure, t_f. From this test methodology, the energy to failure from an RF pulse source can be determined.

Whalen and Domingos also performed a square pulse test that could vary the polarity of the pulse waveform to either positive pulses or negative pulses. Figure 1.5 shows the square pulse system utilized. As in a transmission line pulse test system, this system utilized a square pulse waveform, and was able to capture the voltage and current characteristic across the DUT. In this square pulse test system, the test system integrated a pulse source with a manual trigger, a resistor matching network, and the RF DUT. To capture the voltage characteristic across the RF DUT, a voltage probe was placed across the device, whose output was transferred to an oscilloscope. Additionally, a current probe was placed over the

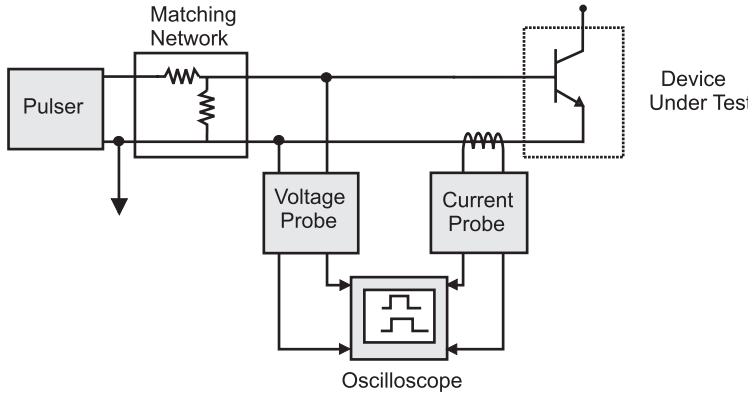

Figure 1.5 Square pulse source ESD test system

ground return line, observing the current that flowed through the RF DUT. The output of the current probe was transferred to an oscilloscope to observe the current waveform. From the voltage and current waveforms, the voltage and current across the RF DUT are evaluated. From these characteristics, the time of failure is also observable by the change in the forward bias value across the RF transistor (e.g., reduction of V_{BE}).

From the test system, the power-to-failure can be evaluated as the product of the current and voltage across the device prior to the collapse of the emitter-base voltage,

$$P_f = I_B V_{BE}$$

whereas the absorbed energy to failure is the product of the power-to-failure and time of failure,

$$E_A = P_f t_f = \{I_B V_{BE}\} t_f$$

From the test system, the voltage, current, and the time of failure are obtainable from the waveforms.

Comparison of the RF pulse system and the square pulse (e.g., TLP-like) test system shows the absorbed energy versus the time-to-failure. The absorbed energy is calculated of the power to failure up to the time of the failure. Whalen and Domingos [43] showed that during the test of RF bipolar transistors, the absorbed power-to-failure is the lowest for negative square pulses, then RF pulse events, and then positive square pulses (Figure 1.6). The results show that the forward biasing of the emitter–base junction leads to a higher absorbed energy-to-failure in comparison to any event that undergoes reverse bias of the emitter–base junction.

An RF ESD design and test methodology is as follows:

- Using a RF pulse system, electrical overstress of an RF component can be evaluated by calculating the incident, transmitted, and reflected energy. The absorbed energy-to-failure

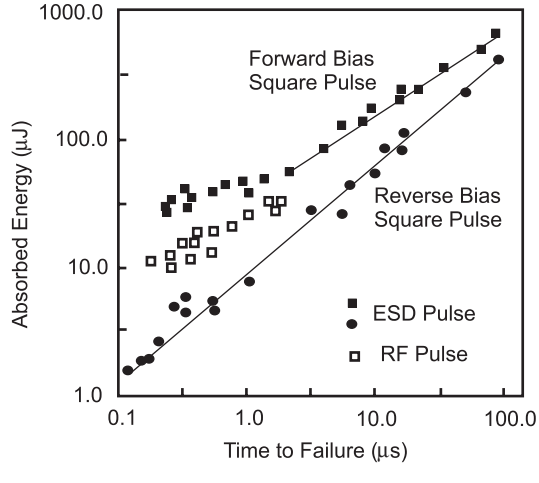

Figure 1.6 Absorbed energy-to-failure versus time-to-failure for RF pulse system and square pulse TLP system (with square pulse is for positive and negative polarity pulses)

can be calculated by the difference between the incident energy and the sum of the transmitted and reflected energy, calculated up to the time of failure.

- Using a square pulse system, electrical overstress can be evaluated in an RF component by evaluating the current and voltage across the device under test and determining the time of failure from the characteristics.
- A correlation exists between the absorbed energy-to-failure from a RF pulse system and a square pulse TLP-type system.
- The absorbed energy-to-failure versus the time-of-failure plot provides a linear plot, with the slope associated with the power-to-failure.

1.10.3 ESD-Induced RF Degradation and *S*-Parameter Evaluation Test Methodology

For the evaluation of ESD-induced degradation to RF components and system, scattering parameters (*S*-parameters) can be used as a measurement diagnostic and serve as an ESD metric for failure criteria [8]. At high frequencies, ESD-induced degradation to RF components that impact signal integrity can lead to impact the system reliability concerns. In high-speed communication systems and high-speed components, the transmission characteristics are important for the transference of signals. The transmission and reflection coefficients are the key measures of the operation and functionality of the system. As the transmission and reflection coefficients are altered, this will also be apparent from the *S*-parameter terms. Shifts in the *S*-parameters or transmission coefficients can be quantified using the TDR methodology.

An RF ESD test method can be established as follows [8]:

- *Prestress evaluation*: Evaluation of all *S*-parameter parameters terms of the RF component using a TDR methodology as a function of frequency;
- *S-parameter matrix*: Formulation of the *S*-parameter matrix terms (e.g., two-port matrix terms are S_{11}, S_{12}, S_{21}, S_{22});
- *ESD step-stress*: Apply an ESD stress between two terminals of the RF component; one of the terminals has an ESD stress applied, whereas a second terminal is the reference ground. A given ESD model waveform shape, waveform polarity, and pulse magnitude is chosen (e.g., HBM, MM, CDM, CDE, TLP, or VF-TLP);
- *Post-stress S-parameter evaluation*: Evaluation of all *S*-parameter parameters terms of the RF component using a TDR methodology as a function of frequency;
- *Post-stress S-parameter matrix formulation*: Formulation of the *S*-parameter matrix terms (e.g., two-port matrix terms are S_{11}, S_{12}, S_{21}, S_{22}) post-ESD stress;
- *ESD step-stress*: The pulse magnitude of the defined ESD stress is increased on the same RF component, and the above procedure is repeated, where the *S*-parameters are reevaluated.

This test procedure can be applied to any two ports of the RF component. Depending on the intended application of the RF component, whether a receiver element, or a transmitter

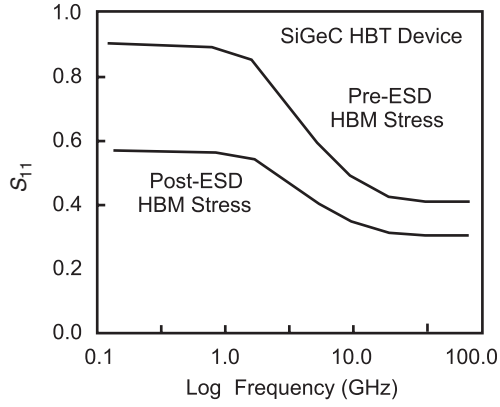

Figure 1.7 *S*-parameter S_{11} comparison as a function of frequency for a SiGeC HBT device before and after ESD HBM stress

element, some configuration will have more value and relevance to evaluate utilization of the component in a system environment. For RF CMOS MOSFET transistors, the ESD stress can be applied to gate-to-drain, gate-to-source, drain-to-source, and drain-to-substrate. The *S*-parameter values of the RF MOSFET in a given configuration are extracted, and then the ESD stress is established between any two terminals. As a RF MOSFET receiver network, ESD-induced *S*-parameter degradation associated with the RF MOSFET gate may be of higher interest; as a RF MOSFET transmitter the ESD-induced *S*-parameter degradation from drain-to-source may be of greater interest.

For a RF bipolar transistor, the ESD stress can be applied to base-to-emitter, base-to-collector, collector-to-emitter, and collector-to-substrate terminal combinations. For RF receivers, the ESD stress of the base region is of interest, whereas as a RF transmitter, the collector-to-emitter configuration *S*-parameter degradation may be more relevant.

Figure 1.7 shows an example of *S*-parameter S_{11} versus frequency before and after HBM ESD stress. The RF test structure is a RF SiGeC hetero-junction bipolar transistor placed in an *S*-parameter wafer-level pad set [8]. The RF SiGeC HBT device is configured in a common-emitter configuration where the two-port input terminals are between the base and the emitter, and the two-port output terminals are between the collector and the emitter.

In the test procedure, the *S*-parameter was extracted on a full RF functional test system and the measurements were performed on a wafer level. The HBM stress was applied using a wafer-level HBM test system. A single HBM ESD pulse was applied between the SiGeC HBT base and emitter pads. Post-ESD stress, the test wafer was reevaluated for *S*-parameter extraction. In Figure 1.7, the *S*-parameter S_{11} results are shown before and after HBM ESD stress; it can be observed that the S_{11} parameter magnitude is lower for all frequencies after ESD stress.

From this discussion, an ESD RF test method and test technique teaches the following:

- *S*-parameter evaluation can be used to determine the ESD-induced degradation of RF components.
- For single components, RF components or RF ESD elements are to be placed in *S*-parameter pad sets and accompanied with open and short pad sets for deembedding procedures and *S*-parameter extraction.

- ESD applied stress is established across two terminals of the two-port structure where one of the terminals has the pulse applied, and the second terminal serves as the grounded reference.
- RF functional testing and *S*-parameter evaluation before and after ESD stress can be performed within a single pulse or step-stress process to evaluate single pulse or cumulative degradation effects.
- *S*-parameters shifts and degradation can be utilized for the ESD failure criteria for a single component or system.

1.11 TIME DOMAIN REFLECTOMETRY (TDR) AND IMPEDANCE METHODOLOGY FOR ESD TESTING

Signal integrity is important to both digital systems and RF communication systems as clock frequencies and data transmission rates increase. For RF and high-data rate transmission systems, new testing techniques are needed to evaluate the impact of ESD on components. At these high-data transmission rates, ESD-induced changes to the electronics that impact signal integrity can lead to impact the system reliability. ESD damage, either permanent or latent, can lead to chip or performance issues. ESD-induced damage influences the gain, the transconductance, and the *S*-parameters; a new methodology and failure criterion may be needed to evaluate the ESD impacts. This can occur to circuitry on the transmission or receiving end of a system leading to unacceptable degradation levels. ESD-induced damage can include the following circuit and system issues:

- signal rise time;
- pulse width;
- timing;
- jitter;
- signal-to-noise ratio.

In high-speed communication systems and high-speed components, the transmission characteristics are important for the transference of signals. The transmission and reflection coefficients are the key measures of the operation and functionality of the system. The transmission coefficients, the *S*-parameters, and the impedance play a major role in the functionality of the system. Shifts in the *S*-parameters or transmission coefficients can be quantified using the TDR methodology.

The TDR method can be used to verify ESD failures and implications to functional system. The TDR method is a common practice in high-speed system development. The functional test requires a launching of a signal and the reflected wave is measured to evaluate the transmission, the reflection, and impedance of the port tested. Time domain reflectometry measures the reflections that occur from a signal, which is traveling through a transmission environment. The transmission environment can be a semiconductor circuit, a connector, cable, or circuit board. The TDR instrumentation launches a signal or pulse through the system to be evaluated and compares the reflections of a standard impedance to that of the unquantified transmission environment.

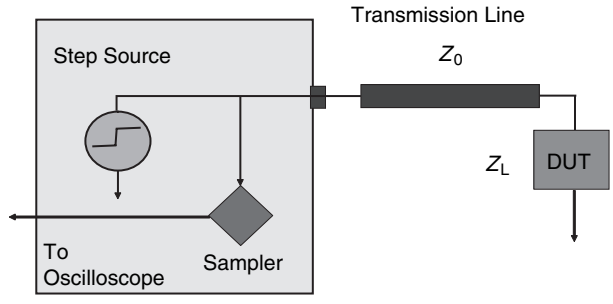

Figure 1.8 A time domain reflectometry (TDR) test methodology

Figure 1.8 shows an example of a TDR measurement system [8]. A TDR measurement sampling module consists of a step source, a 50 Ω connection, followed by a transmission line to the load. The TDR sampling module also contains a sampler circuit, which draws a signal off of a 50 Ω transmission line, whose signal is fed back to the oscilloscope. The TDR display is the voltage waveform that is reflected when a fast voltage step signal is launched down the transmission line. The waveform, which is received at the oscilloscope, is the incident step as well as the set of reflections generated from impedance mismatch and discontinuities in the transmission system.

The mathematics of the TDR method is based on the impedance ratios and a reflection coefficient ρ. The reflection coefficient ρ is equal to the ratio of the reflected pulse amplitude to the incident pulse amplitude

$$\rho = \frac{V_{\text{reflected}}}{V_{\text{incident}}}$$

The reflection coefficient can be expressed as a function of the transmission line characteristic impedance Z_0 and the fixed termination impedance Z_L. In this form, the reflection coefficient can be expressed as

$$\rho = \frac{Z_L - Z_0}{Z_L + Z_0}$$

The fast-step stimulus waveform is delivered to the DUT after propagation through the sample head, the transmission line, connectors, and the test fixture connections. The waveform, which is reflected from the device under test, is delayed by the two electrical lengths at the oscilloscope – the time of flight through all the interconnects and the return flight time. This signal is superimposed on the incident waveform at the TDR sampling head. The TDR sampling heads typically allow evaluation of the voltage waveform, the reflection coefficient, or the impedance on the TDR oscilloscope.

1.11.1 Time Domain Reflectometry (TDR) ESD Test System Evaluation

TDR is valuable for the analysis of ESD-induced failure in both components and systems. This TDR methodology can be valuable when only the input is available for analysis. As an

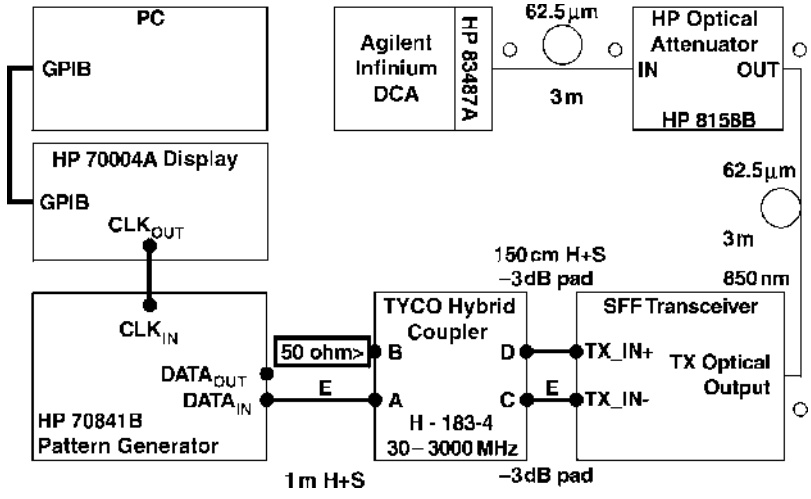

Figure 1.9 Electro-optical test system

example of application of the TDR system and ESD-induced degradation, a high-speed optical interconnect system is shown [8].

Figure 1.9 shows a high-level diagram of the optical interconnect system. The system consisted of a transmitter/receiver module, a short-wave vertical cavity surface emitting laser (VCSEL), an optical wave guide, an optical photo-detector, and an optical-to-electrical (O/E) converter. The data input signal stream is produced at approximately 2 Gb/s in a fiber channel pattern (FCPAT). The data pattern is generated by the pattern generator and converted to a differential signal via the hybrid coupler. The hybrid coupler element is connected electrically to the transceiver (TX) differential inputs. The SFF transceiver receives the data pattern and modulates the laser diode. The optical output from the SFF transceiver is connected to a multimode fiber, which conveys the signal to an optical attenuator before making its way to the optical input of the DCA. The O/E converter in the DCA filters the waveform by limiting the bandwidth and projects the displayed waveform on screen.

Optical-to-electrical conversion in the transceiver is a very precise function requiring tight control of parameters for gigabit data transfer. The electrical path from the connector to the MICC chip is a controlled 50 Ω single-ended impedance. A transceiver having this form factor has transmitter input pins exposed to ESD events. ESD events can damage the circuits and destroy the circuit integrity. Testing the O/E conversion before and after ESD events is a way to monitor the robustness of the ESD protection circuits.

The ESD test methodology for evaluation of the system comprises the following steps [8]:

- Functional characterization of the system is performed prior to ESD stress.
- The input TDR signal is evaluated in an unpowered state.
- System power is applied.
- Optical ‘eye’ patterns are recorded prior to ESD testing.

- ESD stress is applied to the transceiver chip input signals.
- An 'ESD gun' or ESD pulse system is directly connected to the subject pin, and the stimulus is applied.
- Each pin on the evaluation card is connected to signals, power, and grounds in the transceiver.
- Differential input TX_IN pins would be the source signal, and the return signal path was either the power or the ground pin. Both positive and negative polarities are tested.
- TDR measurements were evaluated post-ESD stress. An ESD impulse is applied to the port when the system is unpowered; the system is then retested using the TDR test methodology.
- Post-ESD stress output 'eye' test is evaluated to observe system level degradation effects.

Prior to ESD testing, the functional system is characterized. The experiment is started by observing the input TDR signal when the system is powered down. The TDR system consists of a Tektronix SD24 TDR Sampling head in a Tektronix 11801C oscilloscope. The Tektronix 20 GHz SD24 TDR sampling plug-in has a 15 ps rise time into a load and a 35 ps reflected wave rise time. The Tektronix 11801C has a 50 GHz sampling rate. After power-up the data input signal stream is initiated, and the output optical eye patterns are recorded prior to any ESD testing. The transceiver/receiver chip was first analyzed followed by full system evaluation.

The ESD test method establishes a procedure to apply ESD pulses to all pads on the transceiver via externally placed pins. An 'ESD gun' Mini-Zap 2000 is directly connected to the subject pin and the stimulus is applied in accordance to the JEDEC Standard (JESD22-A114-B). The ESD gun Mini-Zap 2000 is wired to the desired pins for source and return. Each pin on the evaluation card is connected to signals, power, and grounds in the transceiver. In this particular test, one of the TX_IN pins would be the source signal, and the return signal path was either the power or the ground pin. Note that both positive and negative ESD pulse polarities can be evaluated. The source/return path from the 'ESD gun' Mini-Zap 2000 lead is in the following order: stimulus pin, card trace, card connector, transceiver connector, transceiver trace/component, and finally MICC chip input (TX_IN). An ESD pulse stress is applied to the port when the system is unpowered; the system is then retested using the TDR test methodology. An example of the results below shows the characteristics of a system of a 1 GHz path for stress at 2000 V and at more than 2000 V.

In the test system, the semiconductor chip that may be vulnerable to ESD events is the SFF transceiver chip, which consists of RF components. In this application, a 45 GHz f_T SiGe hetero-junction bipolar transistor technology is used in the transceiver chip. Figure 1.10 shows a high-level diagram of the transceiver chip architecture. In the diagram, the differential inputs, the amplifiers, and the diode laser signals are shown.

Measurements were taken at different stress levels, evaluating the TX-pin distortion. HBM stressing was performed on the transceiver chip to determine the ESD sensitivity of the signal pins. Table 1.8 shows a table of transmission and reflection signal magnitudes at a magnitude of 2000 V HBM ESD stress. Each line in the table represents a different module placed under ESD stress. Various system level parameters of amplitude and loss are recorded

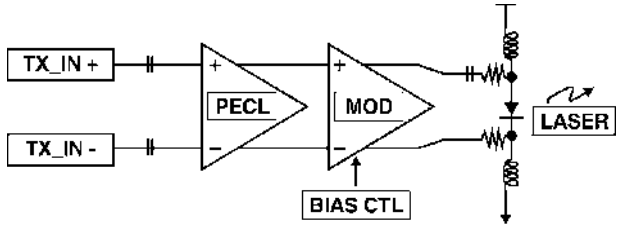

Figure 1.10 Transceiver chip architecture

for the transmitted and reflected signals. Below a 2000 V HBM level, distortions in the TX amplitude is not observed in the 1 GHz signal path. In Table 1.9, the ESD stress was increased above 2000 V HBM. From the TDR method, various parameters begin to distort as the ESD stress increases. Above 2000 V, shifts occur in the transmission port tested. Distortion of the transmitter is noted in the TX pin with a 2X increase in TX DJ (TX DJ increased from levels of 30 to 72 and 131). Hence, from this TDR methodology, the metrics are evaluated for the various signal level parameters [8].

A second means of observation is the output 'eye' test. After the input transmitter/receiver circuit has its TDR measurement, the system is repowered and cycled at the 2 Gb/s data rate. From the output 'eye' the distortion of the output characteristics is another way of evaluation of the ESD impacts. The timing of the optical network is impacted by the ESD pulse as a result of the impact on the differential input of the input SFF chip. Experimental observations showed that, in some cases, it was hard to determine the change in the TDR input characteristic before and after ESD stress, yet observations were visible in the subtle changes in the output 'eye test' [8].

Table 1.8 TDR method results at 2000 V HBM ESD stress

Type	Serial	FCP	TX ER	TX DJ	1e-12 RX sensitivity	RX amplitude	TX fault	Rx loss
1 GHz f_c path	1505	−5.69	7.40	34.78	−18.7	756.06	OK	OK
	2735	−5.64	6.62	22.17	−19.2	761.03	OK	OK
	2779	−6.12	7.25	24.01	−19.7	743.39	OK	OK
	2750	−6.48	5.96	18.3	−18.7	717.93	OK	OK
	1502	−5.82	8.82	45.45	−19.8	749.10	OK	OK

Table 1.9 TDR method results above 2000 V HBM ESD stress

Type	Serial	FCP	TX ER	TX DJ	1e-12 RX sensitivity	RX amplitude	TX fault	Rx loss	Comments
1 GHz path	1505	−5.69	7.97	131.48	−18.8	770.85	OK	OK	TX-distorted
	2735	−5.64	6.98	24.58	−19.4	771.89	OK	OK	TX-OK
	2779	−6.12	6.75	28.85	−19.6	767.84	OKOK	OK	TX-OK
	2750	−6.48	7.25	30.57	−18.8	786.23	OK	OK	TX-OK
	1502	−5.82	7.68	72.53	−19.8	787.76	OK	OK	TX-hi crossing

Hence, using a TDR technique, and system level 'eye test,' the impact on a RF chip at the input and the output of the system can be evaluated. The TDR method, using state-of-the-art oscilloscopes with TDR sampling heads, can evaluate the reflection coefficients, the impedance, and voltage level response. Using the methodology of TDR measurements of the system input (in an unpowered state) pre- and post-ESD allow for a comparison evaluation of the stress on the TDR waveform. It was also found that the 'eye test' can also observe low-voltage degradation effects not observed from the TDR method only. With a trained eye, the subtle variations in the 'eye test' can allow a test engineer the means of observing distortions, which may impact the data transmission system.

1.11.2 ESD Degradation System Level Method – Eye Tests

In system level quantification of ESD degradation, it is not always possible to determine the ESD-induced degradation at the semiconductor chip, or at low-speed characterization. Using the 'eye test', it is possible to provide quantification of the system level impact of ESD degradation. A means of observation is the output 'eye' test. From the comparison of the output 'eye' before and after ESD degradation, a system level failure criteria can be established. From the output 'eye' the distortion of the output characteristics is another way of evaluating the ESD impacts. The eye test is a measure of the timing of signals to evaluate the worst case operational means. Figure 1.11 is a pictorial example of the 'eye' before and after ESD stress. The 'eye' is formed by the overlaying of two signals of interest where one signal is inverted. When the timing is sound, the 'eye' is open and wide. When distortion or poor timing the overlapping of the signal leads to a small eye opening. An example of an 'eye test' whose iris has been degraded as a result of ESD-induced degradation is shown in Figure 1.11.

Figure 1.12 shows an example of an 'eye test' with a system with good functional characteristics. Figure 1.13 shows the results of the output 'eye' after ESD testing. The parameters of interest from the system level from the analysis are as follows:

- rise time;
- fall time;
- jitter.

In the 'eye test' study, a range of parameter variations is shown. Prior to ESD testing, the rise time range varied from 95.6 to 97.8 ps. The fall time range varied from 113.3 to 115. 6 ps. The range of the jitter parameter is 9.4–9.9 ps.

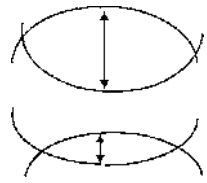

Figure 1.11 Functional eye test before and after ESD testing. The first characteristic represents a 'good eye' and the second represents a 'bad eye'

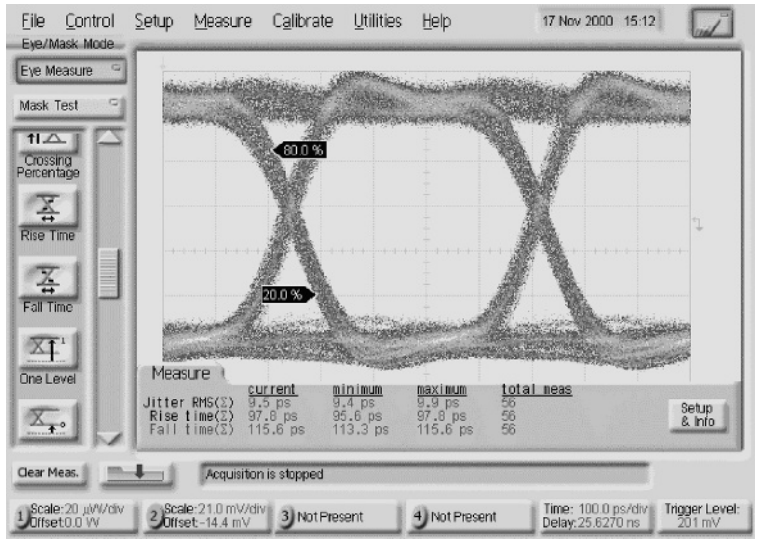

Figure 1.12 Eye diagram prior to ESD testing

Experimental observations will show that in some chip applications it will be difficult to determine the change in the semiconductor chip input characteristics, before and after ESD stress. At low current stress levels, d.c. characteristics shifts, and small degradations in the device characteristics may not appear to have significant impact on the semiconductor chip. But, on a system level these can lead to system failure. In some applications, the

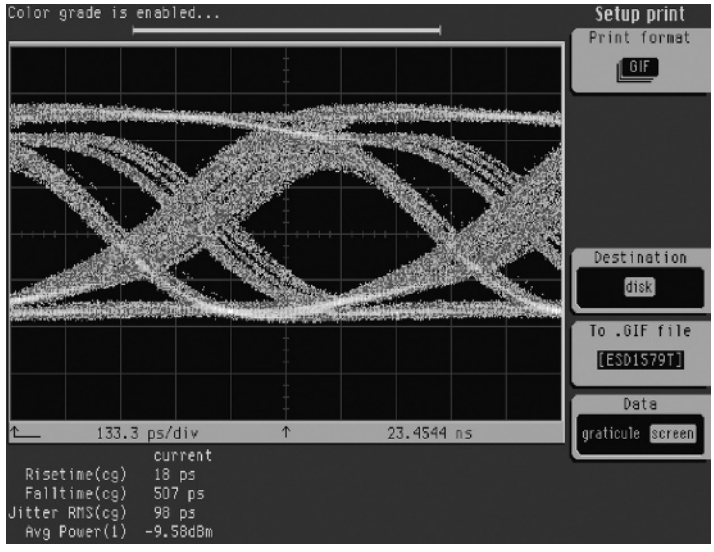

Figure 1.13 Eye test post-ESD testing

semiconductor chip level ESD degradations may not be apparent but observations are visible in the subtle changes in the output 'eye test'. At high ESD stress levels where significant change can be evident in the d.c. device characteristics, or a TDR test, the optical eye distortion will be clearly visible in the receiving output oscilloscope signals. In the 'eye test' study, a range of parameter variations is shown.

As previously shown, before ESD testing, the rise time range varied from 95.6 to 97.8 ps; the fall time range varied from 113.3 to 115.6 ps and the range of the jitter parameter was 9.4 to 9.9 ps. Post electrical stress, the rise time, fall time, and jitter was impacted to the values of range of 18, 507, and 98 ps, respectively. Large shifts were evident in the rise, fall, and jitter parameters demonstrating significant impact to the system response after ESD stress, the three parameters functional parameters (rise time, fall time and jitter) were impacted. In this system, the ideal ESD failure criteria will be defined on a system level on the basis of the timing impact (e.g., rise time and fall time), as well as in the jitter value specifications, but not on a component level. In a given system, a relationship can be established between the system level response and the internal damaged component. Hence, using the output eye test provides a qualitative way to observe distortion of the device characteristics of the input devices [8].

These results indicate that for high-speed communications systems, new criteria and test techniques may be needed to define the impact of ESD stress. Traditional ESD testing looks at the d.c. parameter shifts of the semiconductor device or input pin chip characteristics may be inadequate to quantify the system level impacts. In the future, ESD degradation may be best quantified using quantitative time-domain reflection techniques, and evaluate the impedance shifts, reflection characteristics, and transmission characteristics in determining device failure. At the same time, this can be further understood using the output 'eye' test in evaluation of the true system impact.

1.12 PRODUCT LEVEL ESD TEST AND RF FUNCTIONAL PARAMETER FAILURE

For product level evaluation, a comparison of the product level failure point anticipated by the ESD tester and the evaluation based on RF parameters is required. A key question that was being addressed is whether the ESD HBM failure levels reported from ESD HBM testers is valid for prediction of the ESD robustness of RF products. To address the question of whether ESD data from commercial HBM stress systems is valid in predicting the failure of RF products, a method was first initiated by Van Laecke, Rascoe, and Voldman [8]. In this application, a product with a 45 GHz f_T Silicon Germanium HBT technology was used for the evaluation. The ESD test method is as follows:

- A first test chip is placed on the HBM commercial test system.
- Failure criteria are defined on the basis of a d.c. shift in the *I–V* characteristics.
- ESD step-stress is applied with pre- and post-ESD pulse leakage evaluation.
- ESD pulse step-stress is completed in 100 V HBM test increments.
- ESD failure is defined as the first pin to satisfy the 50% shift in the *I–V* characteristic. This sets the failure level on the basis of the d.c. shift criteria, used for the second study.

- A second set of test chips are d.c. and RF characterized prior to ESD testing using a fully functional RF test system.
- A second set of test chips are stressed with a single HBM ESD pulse magnitude where the highest pulse level is the same as achieved in the prior ESD step-stress (e.g., failure level as defined by the first test). The modules are tested from zero to the highest pulse level where each module has a single pulse stress applied.
- RF characterization and full functional characterization are evaluated for the second set of modules.
- RF metrics are plotted to determine where the failure criterion is first encountered. The lowest encountered RF parameter determines the HBM stress level for 'failure.'

As an example, the HBM ESD test was applied to a first module. The HBM ESD test is done in 100 V step increments. In this application, the HBM testing of the test chip has an HBM worst-case pin-to-rail of 5000 V. This set the upper limit for the second study. In the second study, testing is completed at different ESD stress levels where the testing is stopped prior to the worst case functional failure level (of the first study). Different sample parts are tested with at a single ESD HBM stress level at 0–5000 V. Full-functional RF testing is then completed on the product chip on all the ESD stressed parts [8].

Figure 1.14 shows the OIP3 magnitude as a function of the single pulse HBM stress condition. With no ESD stress applied the OIP3 magnitude remained the same until after a stress level of 3000 V. No degradation was observed between 0 and 3000 V HBM stress levels. The modules that were stressed at 4000 V demonstrated a degraded OIP3. At an ESD stress level of 4500 V, the OIP3 is degraded with an OIP3 magnitude of 5–20. Hence, the OIP3 RF metric demonstrated degradation prior to the 5000 V HBM level reported from the commercial HBM test system (based on a 50% failure d.c. shift failure criteria).

Figure 1.15 shows the conversion gain results from the identical study. At a HBM stress level of 3000 V, the conversion gain magnitude is 8.55. As the HBM ESD stress level increased, the conversion gain characteristics decreased below 8, with a conversion gain roll-off toward zero at stress levels of 4500 V HBM. As is observed in the OIP3 metric, the RF

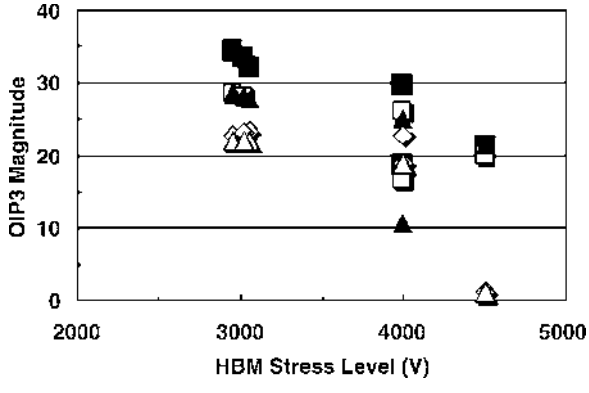

Figure 1.14 Ouput intercept point third-order harmonic (OIP3) magnitude as a function of HBM stress level

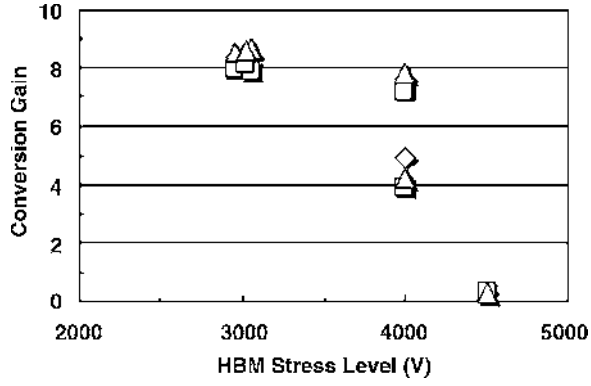

Figure 1.15 Conversion gain as a function of the HBM ESD stress

parameters degraded prior to the predicted level on the basis of the ESD HBM step-stress (e.g., the d.c. *I–V* shift failure criteria) [8].

From this product level ESD stress study, the failure criteria of RF components must address evaluation of all the RF parametrics. Using the ESD test system for d.c. characterization, this study can be used to define the upper limit of the second RF characterization study.

As was done in the single component ESD study, a relationship does exist between the d.c. characterization and the RF degradation. First, in both cases, RF degradation does occur prior to full ESD 'failure' based on a d.c. parameter. In the single component case, a clear relationship was established between transistor RF parameter degradation and the d.c. shift of the forward bias voltage (e.g., in the emitter-base study). In this product level study, the upper level of HBM failure, based on a d.c. shift criteria, was used only as an upper limit to define the stress conditions for the second full RF evaluation. In the product evaluation, there are a significant number of RF parameterics, which is dependent on the product application. Hence, the method discussed is a useful method to utilize the commercial ESD testers and establish limits for the RF ESD evaluation [8].

1.13 COMBINED RF AND ESD TLP TEST SYSTEMS

For the ESD evaluation of RF components, it is important to evaluate the RF parameters pre- and post-ESD stress in the case where there is no correlation to d.c. parameters. In ESD testing of radio frequency components, the evaluation of the RF parameters pre- and post-ESD stress can be provided by the integration of RF characterization test equipment into ESD test systems. RF parameters can be evaluated during ESD testing by the integration of RF test equipment within the testing systems. Alternatively, a second methodology would be to integrate ESD pulse sources into RF test systems. In RF test systems, the latter method would not be desirable due to potential damage or time constraints to high-cost sensitive RF test systems.

In today's commercial ESD test systems, the ability to evaluate the d.c. parameters as well as the RF parameters is not offered. For the evaluation of ESD degradation influence on

RF components, the integration of RF characterization equipment into HBM, MM, and TLP and VF-TLP test simulators is possible with providing 'switches' that allow the RF characterization between ESD pulse stress.

Hynoven, Joshi, and Rosenbaum integrated RF characterization equipment into a TLP system by applying a second single-pole double-throw (SPDT) switch to measure the RF parameters before and after application of the TLP stress [9]. Figure 1.16 shows the TLP system with integrated RF characterization.

The test system for characterization and electrical connections includes an oscilloscope, a parameter analyzer, noise figure meter, noise figure test set, signal generators, preamplifiers, relays, and SPDT switches. For the ESD pulse source, the test system includes a high-voltage generator, an ESD pulse generator source (e.g., a commercial pulse generator or a transmission line cable of predefined length) and associated electrical connections. As an example of the test equipment, the following equipments were used by Hynoven, Joshi, and Rosenbaum [9]:

- 50-Ω 40-GHz coplanar waveguide probes with ground-signal-ground (GSG) footprints.
- Bertan Series 225 High Voltage Generator.
- HP 54510B (300 MHz) Oscilloscope.
- HP 4145B Semiconductor Parametric Analyzer.
- CP Clare relays MSS41A05 (SPST) and HGJM51111K00 (SPDT).
- HP 8761A RF SPDT switch (DC-18GHz).
- HP 8970B NF Meter (1.6 GHz bandwidth).
- HP 8971B NF Test Set (mixer with control logic, up to 18 GHz).
- Agilent PSG-E8241A Signal Generator (up to 20 GHz).
- Amplifier Research LN1G11 Pre-Amplifier (<6 db NF, 27 dB gain).
- HP 8114A Pulse Generator (for relay control).
- HP E3631A Power Supply (for relay control).
- Transmission line cable.

In TLP systems, a common design are the 50 Ω impedance systems. In this RF/TLP integrated system, the SPDT relays isolate and select between the ESD pulse source (e.g., charged transmission line), the d.c. measurement equipment (e.g., parametric analyzer) and the RF test equipment. Hynoven, Joshi, and Rosenbaum [9] integrated the first relay as a conventional mercury-wetted relay used in high voltage ESD systems. The second relay utilized is a high-frequency RF switch. In both cases, the activation of the relays are controlled and initiated by programmable voltage sources. In the construction of these test systems, the RF components and cables should allow for RF characterization at the operational frequency of the semiconductor component or semiconductor chip under evaluation. Hence a key issue is that the ESD system and the RF characterization sector must be suitable to allow accurate RF characterization of the component. As a result, this may place limitation on the type of TLP test system and the impedance. TLP systems can

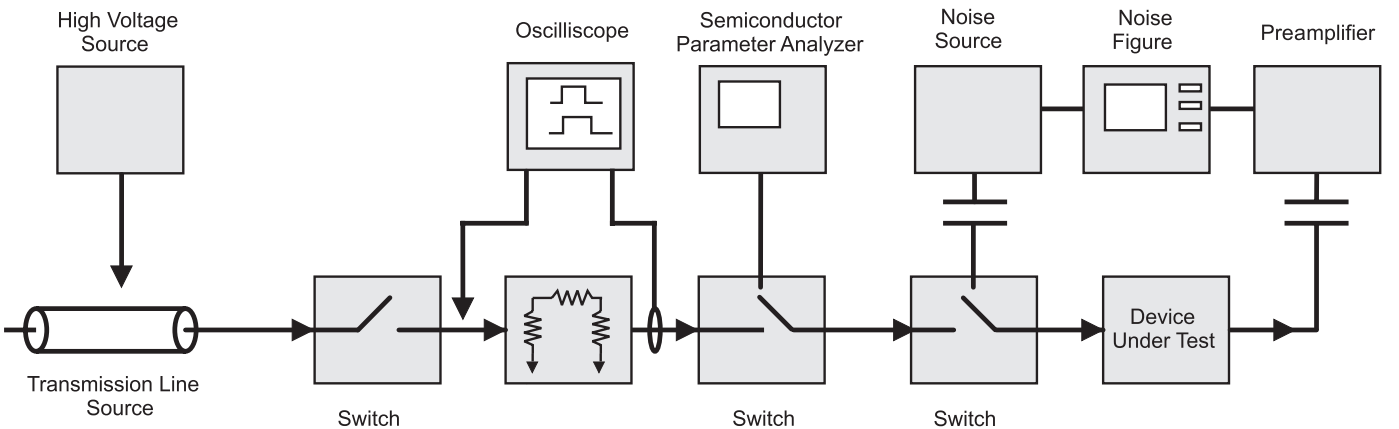

Figure 1.16 Transmission line pulse (TLP) test system with integrated RF characterization

have four classifications: TLP current source, TDR, TDT, and TDRT. For RF measurements, a 50 Ω impedance level must exist in the measurement path, limiting the classes of TLP systems that may be suitable. Additionally, with the integration of the RF characterization and the TLP measurements, the TLP pulse current level must remain under the current limit of the microwave RF probes.

It was noted by Hynoven that one must be conscious of ground loops and ground references in the combined RF/TLP test system. RF measurements require the use of coaxial cables and ground-signal-ground probes to establish a ground plane reference for the signals. Hynoven and Rosenbaum [9] noted that the RF ground establishes an undesired return path for the ESD pulse. This issue is addressed by d.c. blocking capacitors and switches. With the addition of switches and d.c. blocking capacitors, a test sequence can be established that avoids this issue.

An RF ESD test procedure for ESD TLP-stressing of an RF component can be as follows [9]:

- Initialize the state of the system.
- Initiate the charging of the transmission line cable outer conductor.
- Discharge the outer conductor potential to ground.
- Establish the state for launching TLP current pulse.
- Apply the TLP current pulse to the DUT.
- Close the TLP source switches.
- Establish switch states to initiate power to the DUT.
- Apply power to the DUT and enable RF measurement diagnostics.
- Complete RF measurements.
- Re-initiate the test sequence.

1.14 CLOSING COMMENTS AND SUMMARY

In Chapter 1, the text opens with the discussion of ESD and EOS in RF technology. The chapter discusses patents, RF parametrics, the fundamental design techniques, RF ESD metrics, and new RF ESD testing methodologies. Early contributions are reviewed to place today's efforts in the historical context and to highlight the excellent work performed in evaluation of the RF power-to-failure and ESD power-to-failure of microwave electronic components; this was intentionally done to demonstrate that the early work testing techniques, measurements, and modeling are relevant to today's rapid interest in the field of ESD in RF devices. Some things have changed since the 1970s. First, new technologies emerged. Second, the device themselves changed within a technology type. Third, the devices became faster. Fourth, testing methodologies will evolve addressing more application-specific ESD failure criteria. Fifth, there will be larger emphasis on the utilization of RF design techniques, and cosynthesizing the ESD and RF characteristics for optimization.

A plethora of cosynthesis methods of ESD and RF component design is shown for the first time to define an 'RF ESD design practice.' This RF ESD design practice is a blending of the

traditional methods used in digital CMOS ESD design practices with RF design practice methods; whereas, in the case of digital ESD solutions both devices and methods may be abandoned when unsuitable for RF design. In digital design, there is a significant usage of resistors; in RF ESD design we will see the significant usage of inductors and capacitors.

Another key point is that the TLP and VF-TLP methodologies are a natural testing method for RF circuits for a few reasons. First, the TLP method is a 50 Ω-based methodology. Second, it is a two-pin test whereas RF parameter extraction are also two-port methodologies. Additionally, the device, circuit and systems can be analyzed in a common method. For future ESD test methods such as the VF-TLP, whereas its original goal was to characterize CDM failure mechanisms, the new value of this method may be for RF components where it may be the utilization for evaluation of short-pulse phenomenon akin to the RF power-to-failure methods utilized by Whalen thirty years ago. As a result, a testing synergy has begun toward the ESD testing using the TLP and VF-TLP methods, with RF characterization.

In Chapter 2, we will discuss RF codesign methods and techniques, as well as address ESD design integration in mixed signal chips that contain digital, analog, and RF subfunctions, within a common chip. In Chapter 2, we will discuss in more depth the specific methods of ESD RF cosynthesis—inductive shunts, impedance isolation, cancellation, linearity optimization, distributed loads, and matching. These practices have been only recently utilized for today's RF technologies. In Chapter 2, we will also discuss how to architecture and floor plan mixed signal chips for ESD. Additionally, some special topics on structure under pads and pad-ESD integration will be briefly discussed.

PROBLEMS

1. Given a diode element, of the width, W, the length, L, and spacing of shallow trench isolation between the $p+$ to $n+$ of spacing, $W_{STI,}$ and well sheet resistance, ρ_W, derive the series resistance of the diode element. Assuming the capacitance assuming a capacitance per unit area, C_0, develop a diode model for the series capacitor and series resistor.

2. Assume two-diode elements, where one serves as a low-impedance shunt, and the other is reverse-biased serving as a load. Assume the diode element is a low-impedance shunt of zero capacitance, whereas the second diode element is a capacitive load. Derive the figure of merit (FOM) for the 'dual diode network' using the dimensions of the prior derivation. Assume an ESD robustness per unit micron of V_0 (HBM volts per unit micron).

3. Derive the *S*-parameters for a diode element between an input and an output terminal. Derive the *T*-, *Y*- and *Z*-parameters.

4. Assuming an ideal HBM source of capacitor C and series resistor R, derive the discharge through a resistor load R_L. Assume the capacitor is pre-charged to voltage V_0, and a switch is between the series resistor and the load resistor.

5. Assuming an ideal HBM source of capacitor C, and series resistor R, derive the discharge through a capacitor load C_L. Assume the capacitor is pre charged to voltage V_0, and a switch is between the series resistor and the capacitor load.

6. Assuming an ideal HBM source of capacitor C, and series resistor R, derive the discharge through an inductor load C_L. Assume the capacitor is pre-charged to voltage V_0, and a switch is between the series resistor and the inductor load.

7. To evaluate the absorbed energy of the RF device, this can be calculated by the difference between the incident energy, and the sum of the reflected and transmitted energy.

$$E_A = E_I - E_R - E_T$$

where the incident energy is

$$E_I = \int P_I(t)\,dt$$

and the reflected energy is

$$E_R = \int P_R(t)\,dt$$

and transmitted energy is

$$E_T = \int P_T(t)\,dt$$

Assuming a transmission line pulse system, derive the power from a TLP pulse assuming a trapezoidal pulse wave form. Assume a perfect 50 Ω impedance through the system. Derive the general relation where there is an impedance mismatch at the device under test.

8. Given an inductor, ESD degradation can induced degradation in the quality factor due to resistance changes. Derive the quality factor of an inductor where a resistance degradation occurs due to an ESD events.

9. Given a capacitor, ESD degradation can induce resistance degradation due to impedance pin–holes. Derive a quality factor of a capacitor assuming a conductance variation due to an ESD event.

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technology for mixed signal applications. *Proceedings of the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium*, October 2002. p. 296–305.
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