CHAPTER 1

INTRODUCTION

This book is a continuation of *Frequency Synthesis by Phase Lock*, 2nd edition (*FS2*) [Egan, 2000] with significant emphasis on the study of sigma–delta (ΣΔ) frequency synthesis. Although ΣΔ synthesis has already been introduced in *FS2* (Section 8.3), there is much more to learn, so much that there is a danger of the reader being overwhelmed. For this reason, we will proceed with experimental observation, one experiment at a time, picking up information as we go. We will depend on *FS2* to define a level of knowledge about frequency synthesis that precedes this new study. It will provide a ready reference for background, but we will provide enough information to make referral unnecessary, albeit helpful, for the reader who has acquired basic knowledge about frequency synthesis elsewhere.

The experimental observations will be based on Simulink® simulations. While it is not necessary to use the Simulink program to follow the results that will be discussed, models and discussions will be subsequently provided to enable the reader to perform the Simulink simulations and to progress from there to new simulations to answer new questions. Some books and papers are largely based on development of one or more ICs or delve into monolithic circuit realizations. These have advantages, but the use of simulations permits easier demonstration of a large variety of different configurations and effects.

Following our discussion of ΣΔ synthesis, we will consider two topics that are important when simultaneous wide bandwidth and small frequency steps are to be

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achieved without the use of ΣΔ synthesis. Finally, we will introduce an area of current intense interest, all-digital frequency synthesis. This has become important because the deep submicron CMOS technology that is being used to achieve advances in digital circuits is increasingly incompatible with analog circuits.

In order not to interrupt the main flow, many developments are included in Appendices. This also allows the information to be easily accessed from multiple places in the main text. Each appendix is designated by a letter, and an attempt has been made to choose a letter that could be associated with the content (e.g., L for loop, N for noise) as an aid to recalling the location of the material. Equations, figures, sections, and so on in Appendix Z are numbered Z.*n*, where Z is the letter designation for that appendix [e.g., Eq. (C.3.2) for an equation in Appendix C]. Such items in *FS2* are referred to by a designator F.*n*, as if *FS2* were an appendix, but the corresponding designator in *FS2* is just *n* [e.g., Eq. (F.4.5) refers to Eq. (4.5) in *FS2*]. A more detailed explanation is given in Appendix F.

1.1 PHASE-LOCKED SYNTHESIZER

The basic phase-locked frequency synthesizer is illustrated in Fig. 1.1*a*. The reference for the loop is a source at a fixed frequency f_{ref}. It is commonly derived by frequency division from a fundamental reference at frequency f'_{ref}. The phase of the fixed signal at f_{ref} is compared with the phase of the signal at frequency f_{out}/N from the frequency

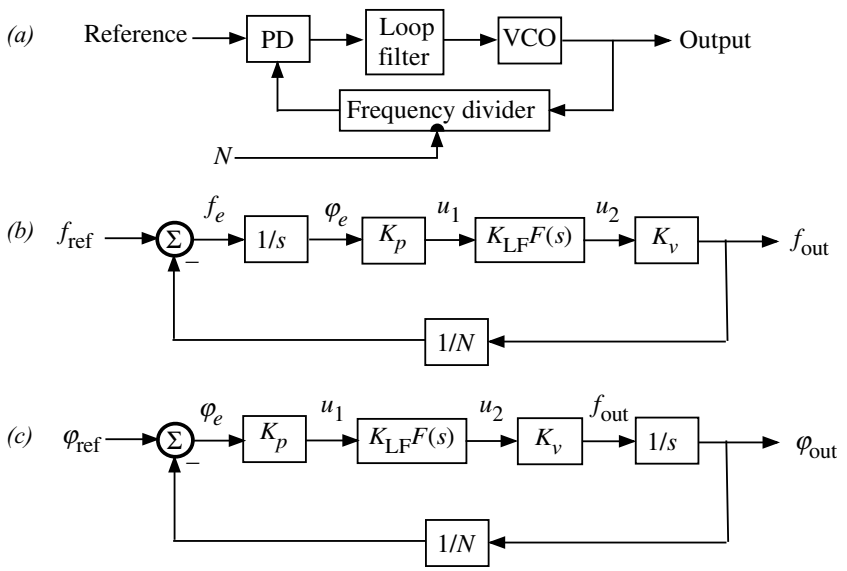

FIGURE 1.1 Basic phase-locked frequency synthesizer: (*a*) function block diagram and (*b* and *c*) mathematical block diagrams.

divider, where f_{out} is the frequency of the VCO and the loop output and N is the divider ratio. The phase comparison occurs in the phase detector (PD). The output of the PD is passed through the loop filter to drive the VCO, completing the loop.

Figure 1.1*b* is the mathematical block diagram representing this process. An integration is required to convert the frequency difference between the reference and divider output to a phase difference, so the Laplace representation for integration, $1/s$, must be placed in the loop. It can be placed after the frequency difference, as in Fig. 1.1*b*, or after the VCO, as in Fig. 1.1*c*. The representation chosen depends on whether we wish to consider frequency or phase at the terminals of the synthesizer. We will see that the representation of the all-digital phase-locked synthesizer differs in one significant way from Fig. 1.1.

1.2 FRACTIONAL-N FREQUENCY SYNTHESIS

The steady-state value of the frequency from a locked loop is

$$F_{out} = F_{ref}N. \tag{1.1}$$

The ratio N is inherently a whole number. Sometimes it is advantageous to employ a value of N that contains a fraction,

$$\overline{N} = N_{int} + n_{fract}. \tag{1.2}$$

To do this, we can let $N = N_{int}$ sometimes and $N = N_{int} + 1$ other times, so the average value $\overline{N}$ is given by Eq. (1.2). This is called fractional-N synthesis. We can also use $\Sigma\Delta$ synthesis to obtain improved noise characteristics through the use of other particular sequences of N-values that average to $\overline{N}$.

1.3 REPRESENTING A CHANGE IN DIVIDE NUMBER

The most common transient expected in frequency synthesis results from a change in divider ratio N. We need a way to represent this transient, which results from a change *to a loop parameter*, in a manner that permits us to obtain the loop response by analysis of a linear time-invariant circuit.

Figure 1.2*a* illustrates a change in N, which results in a transient at the output of the summer (e). The frequency there changes from $f_{out}(0)/N_1$ before switching to $f_{out}(0)/N_2$ after switching, where $f_{out}(0)$ is the output frequency at the moment of switching. The same transient could be caused by a frequency change, injected into the time-invariant loop shown in Fig. 1.2*b*, of

$$\Delta f_d(0) = f_{out}(0)\left(\frac{N_2}{N_1} - 1\right). \tag{1.3}$$

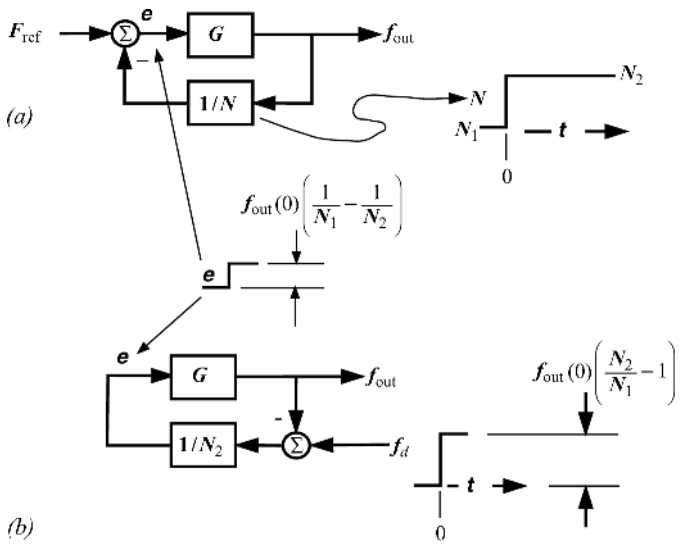

FIGURE 1.2 Representation of a change in divide number N.

If the loop is initially at steady state,

$$f_{\text{out}}(0) = N_1 F_{\text{ref}} \tag{1.4}$$

and Eq. (1.3) becomes

$$\Delta f_d(0) = F_{\text{ref}}(N_2 - N_1) = F_{\text{ref}}\Delta N, \tag{1.5}$$

which is also the eventual size of the output frequency change. Since $N = N_2$ after switching, the loop response is analyzed using that value of N. This is further illustrated in Fig. F.2.19. Thus, we can analyze the response to a change in the parameter N as if it were the response of a time-invariant circuit to a step signal at f_d, so long as the loop is initially at steady state.

During $\Sigma\Delta$ modulation, the parameter N undergoes continual changes but the output is relatively steady at the synthesized frequency,

$$f_{\text{out}}(0) = \overline{N} F_{\text{ref}}, \tag{1.6}$$

so Eq. (1.3) then becomes

$$\Delta f_d(0) = F_{\text{ref}}\overline{N}\left(\frac{N_2}{N_1} - 1\right) = F_{\text{ref}}\frac{\overline{N}}{N_1}\Delta N \tag{1.7}$$

[compare with Eq. (1.5)]. Since this now applies to the individual steps at each reference period, we can also write

$$f_d(nT_{\text{ref}}) = F_{\text{ref}} \frac{\overline{N}}{N_1} N_{\text{mod}}(nT_{\text{ref}}), \tag{1.8}$$

where N_{mod} is the modulated divider ratio.

Looking at the various frequency components in the sequence of N_{mod} values, the low-frequency components will be affected by the average value of N_1 (i.e., $\overline{N}$); so, for $f_m \ll f_{\text{ref}}$, Eq. (1.8) suggests

$$f_d(f_m \ll f_{\text{ref}}) \approx F_{\text{ref}} N_{\text{mod}}(f_m \ll f_{\text{ref}}), \tag{1.9}$$

implying that N_{mod} can be represented as an equivalent frequency deviation injected at f_d in Fig. 1.2*b*. However, such averaging cannot be applied to the higher frequency components. Thus, we can expect the response for $f_m \ll f_{\text{ref}}$ to be as if $f = f_{\text{ref}} N_{\text{mod}}$ were injected at the divider input [Eq. (F.8.75)], but the exact response, including the higher modulation frequencies, usually those beyond the loop bandwidth, will differ. That response is developed in Appendix Q (and its form supports the treatment of the low-frequency components that we have just described).

1.4 UNITS

We will try to use units everywhere, which may lead to some unfamiliar looking expressions. For example, rather than writing $f = 1/T$, we relate frequency f to period T by

$$f = \text{cycle}/T. \tag{1.10}$$

However, we drop or add radian units, and only radian units, at will (see Section F.1.1.4 for an explanation).

1.5 REPRESENTING PHASE NOISE

Sinusoidal frequency modulation of a signal at frequency f_m with a peak deviation Δf produces a sinusoidal phase deviation at the same frequency with a peak phase deviation of m, called the modulation index,

$$m(f_m) = \Delta f(f_m)/f_m, \tag{1.11}$$

in radians (Section F.3.1). This causes sidebands on the signal, spaced at multiples of f_m from the central spectral line. When m is small relative to 1 rad, the central spectral line is reduced little from its level without modulation, the sidebands fall off rapidly, and the first sideband has an amplitude of $m/2$ relative to the central line. If there are many modulating frequencies and if they are spaced very closely, or continuous, we can treat them as a phase power spectral density (PPSD) S_φ with units of rad^2/Hz

(Section F.3.7). The units of

$$S_\varphi|_{\text{dB}} = 10\,\text{dB}\log_{10} S_\varphi \tag{1.12}$$

are decibels relative to a radian squared per hertz, dBr/Hz.

This relationship between the first sidebands and the discrete phase deviation implies a similar relationship between $S_\varphi(f_m)$ and the relative single-sideband power spectral density (PSD) $L_\varphi(\Delta f)$ at an offset of $\Delta f = \pm f_m$ from spectral center (which we see when observing the signal on a spectrum analyzer), requiring still that m be small, in which case (Section F.3.7)

$$L_\varphi(\Delta f = \pm f_m) = S_\varphi(f_m)/2. \tag{1.13}$$

If the restriction on m is not met, Eq. (1.13) *is not valid*. However, by definition,

$$\mathcal{L}_\varphi(\Delta f = f_m) \triangleq S_\varphi(f_m)/2. \qquad \text{(F.3.41)}\ (1.14)$$

The density $\mathcal{L}_\varphi$ is a popular measure of oscillator phase noise because at sufficiently large $\Delta f = f_m$, the modulation index *is* small, so $\mathcal{L}_\varphi \approx L_\varphi$ at those offsets. Thus, $\mathcal{L}_\varphi$ indicates what the power spectrum of a signal looks like, except close to the center, where S_φ (and thus $\mathcal{L}_\varphi$) continue to climb with decreasing Δf, even as L_φ approaches a peak at $\Delta f = 0$. As $f_m \Rightarrow 0$, the measurement of S_φ requires ever narrower filters and takes ever longer times, causing a practical limit on the minimum f_m at which it is measured, but no such limit exists for L_φ.

The density $L_\varphi(\Delta f = \pm f_m)$ is called single-sideband density because it is the relative density on either side of the spectral center, $L_\varphi(\Delta f = +f_m)$ or the equivalent $L_\varphi(\Delta f = -f_m)$. We will not use double-sideband density.

The alternative use of $\mathcal{L}_\varphi$ or S_φ should present no problem because of the simple relationship Eq. (1.14), which can also be expressed as

$$\mathcal{L}_\varphi|_{\text{dBc/Hz}} \equiv S_\varphi|_{\text{dBr/Hz}} - 3\,\text{dB}. \tag{1.15}$$

In the Fourier domain, positive and negative frequencies are used, and the power densities are divided evenly between the positive and negative frequencies. We will generally use one-sided densities and will designate two-sided (Fourier) densities by using a subscript 2. Thus,

$$S_{2,\varphi}(f_m) = S_\varphi(f_m)/2 \tag{1.16}$$

and

$$\mathcal{L}_\varphi(\Delta f = f_m) = S_{2,\varphi}(f_m). \tag{1.17}$$

A relationship similar to Eq. (1.16) holds also for power spectral density, but $L_\varphi(\Delta f = \pm f_m)$ is the *relative* PSD, normalized to the signal power, so it is the same

one-sided as two-sided, since both the signal power and PSD are changed by the same factor of 2.

1.6 PHASE NOISE AT THE SYNTHESIZER OUTPUT

The various noise sources in the synthesizer and their effects on the output spectrum are covered extensively in *FS2*, especially in Chapters 3 (density) and 5 (discrete). We will further consider some of these and some additional noise source in Chapter 4, in particular as they relate to synthesizer ICs and to ΣΔ synthesizers.

1.7 OBSERVING THE OUTPUT SPECTRUM

We will observe the effects of fractional-N synthesis on the synthesizer's output spectrum using a Simulink model of a type-2 PLL with a 58 kHz unity gain bandwidth f_L. See Section L.1 for details. We will initially use a sample-and-hold (S&H) phase detector (Appendix P) to make the phase values easier to observe. Eventually, we will change to the more common phase frequency detector (PFD).