Chapter 1

Introduction and Overview of Microelectronic Packaging

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1.1 INTRODUCTION

An exact date for the advent of *electronic packaging* is difficult, if not impossible, to establish due to the diversity of opinion on what constitutes an electronic package. However, there is no doubt that, in general, nearly all structures that are involved in the generation, transmission, and utilization of electrical signals are packaged in some manner, even if the packaging method and material are somewhat primitive. For example, the insulation surrounding a wire is technically a package. Thus, an *electronic package* might be defined as that portion of an electronic structure that serves to protect an electronic/electrical element from its environment and the environment from the electronic/electrical element. However, in addition to providing encapsulation for environmental protection, a package must also allow for complete testing of the packaged device and a high-yield method of assembly to the next level of integration [1–3].

With the commercialization of the silicon transistor in the 1950s, electronic packaging technology development took on a new level of intensity resulting in the proliferation of standard electronic packages, a few of which are shown in Figure 1.1. However, for several years, the performance of packaged electronic components was limited by the component itself and was impacted little, if any, by packaging technology. At some later date, parasitics associated with the package housing the component began to adversely affect the performance of the device. Consequently, packaging of electronic components, in particular integrated circuits (ICs), became the focus of an intense developmental effort and continues to challenge the microelectronics industry today [4]. Essentially, the point has been reached where advancement in IC performance now drives packaging technology. No matter what approach is taken to package an IC, the primary objective is to realize maximum performance from the IC, and, thereby, electronic systems, by minimizing the impact of the package. It is the intent of this book to discuss all aspects of electronic packaging that impact the performance of electronic devices that they house.

This book addresses all aspects of electronic packaging beginning with an introduction and overview of packaging including definitions, functions, and classifications of microelectronics packaging. Subsequent chapters provide a thorough treatment of technical subject

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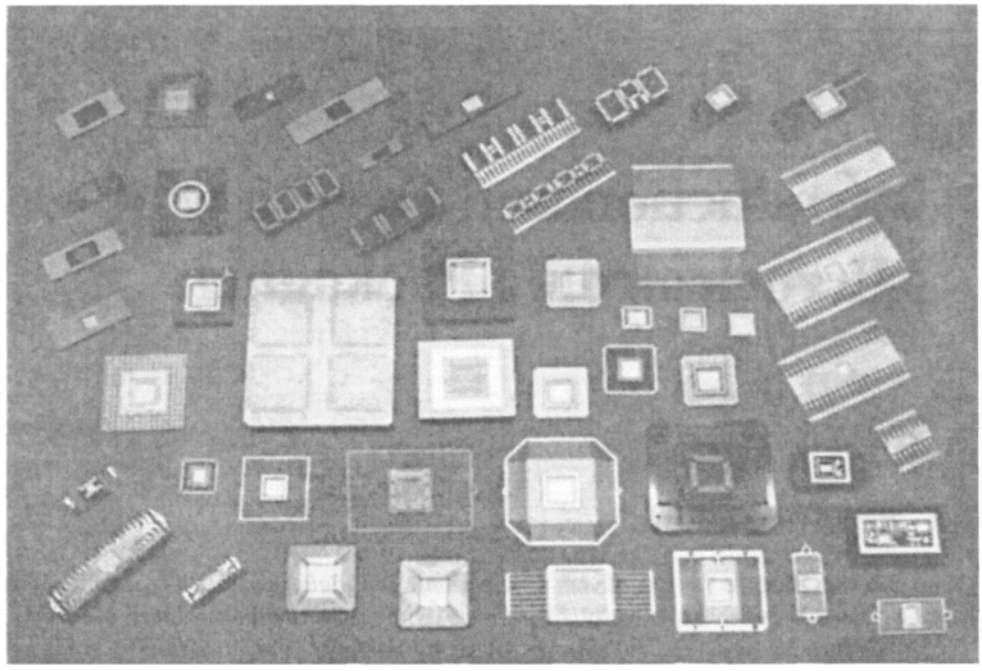

Figure 1.1 Photograph of a number of standard electronic packages (courtesy of Kyocera).

matter important to both the package designer engaged in developing custom packages and the design engineer who must choose from the available standardized packages. The fundamental topics covered include packaging materials and applications, processing technologies, electrical fundamentals, design considerations, thermal considerations, mechanical considerations, package assembly, reliability, and cost evaluation and analysis. Other chapters address electrical modeling and simulation, discrete and integrated passive devices, radio frequency (RF) and microwave packaging, power electronics packaging, multichip and three-dimensional (3D) packaging, and microelectromechanical system (MEMS) and optoelectronic packaging. The final chapter discusses analytical techniques for materials characterization, a subject of considerable interest since materials, and particularly, new materials, have played such an important role in the evolution of electronic packaging technology.

1.2 FUNCTIONS OF AN ELECTRONIC PACKAGE

In the previous section, a very simple definition of an electronic package was given. If we restrict the definition of an electronic package to the housing and interconnection of integrated circuits (also referred to as ICs, silicon chips, chips, or die) to form an electronic system, then we can restrict the discussion to a subset of the multitude of electronic packages that would otherwise have to be considered. For this reduced set of packages, the functions that the package must provide include a structure to physically support the chip, a physical housing to protect the chip from the environment, an adequate means of removing heat generated by the chips or system, electrical connections to allow signal and power access to and from the chip, and a wiring structure to provide interconnection between the chips

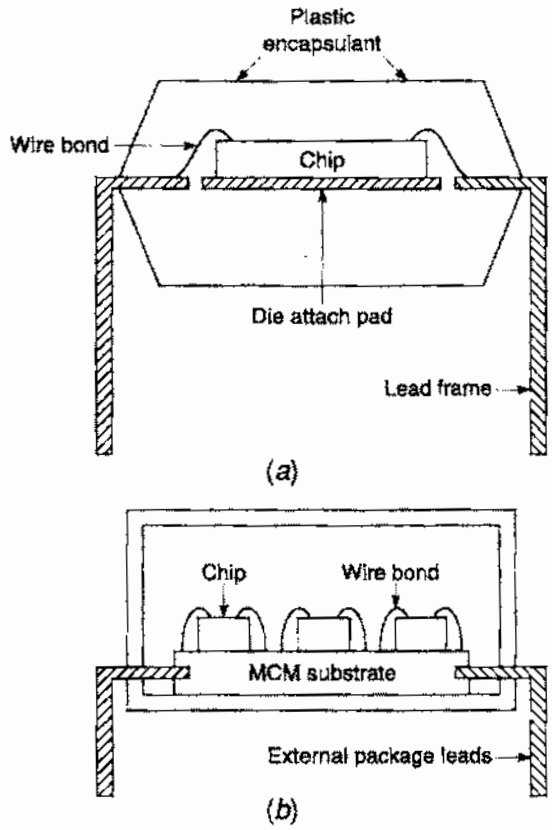

Figure 1.2 (*a*) Single- and (*b*) multichip packages illustrating signal distribution, heat dissipation, power distribution, and circuit support and protection (signal and power distribution are accomplished through leads and wire bonds, heat dissipation is accomplished through leads and chip support, and support and protection are accomplished through the lead frame, substrate, and external package).

of an electronic system [5]. Thus, the package must provide for:

- Signal distribution
- Heat dissipation
- Power distribution
- Circuit support and protection

Figure 1.2 illustrates these various functions for both single-chip and multichip packaging schemes.

In addition to providing the four basic requirements listed above, an electronic package must also function at its designed performance level while still allowing for a product that is high quality, reliable, serviceable, and economical [5]. The rearrangement or addition of functional features, such as upgrading the memory of a computer, is also a desirable feature of an electronic packaging technology.

1.3 PACKAGING HIERARCHY

Typical electronic systems are made up of several layers or levels of packaging, and each level of packaging has distinctive types of interconnection devices associated with it. One

way in which this hierarchy of interconnection levels can be divided is as follows:

Level 0 Gate-to-gate interconnections on a monolithic silicon chip.

Level 1 Packaging of silicon chips into dual-in-line packages (DIPs), small outline integrated circuit (SOICs), chip carriers, multichip packages, and so on, and the chip-level interconnects that join the chip to the lead frames. Occasionally, this level is skipped when tape-automated bonding (TAB) or chip on-board (COB) technologies are utilized.

Level 2 Printed wiring board (PWB), also referred to as a printed circuit board (PCB), level of interconnection. Printed conductor paths connect the device leads of components to PWBs and to the electrical edge connectors for off-the-board interconnection.

Level 3 Connections between PWBs. This may include PWB-to-PWB interconnections or card-to-motherboard interconnections.

Level 4 Connections between two subassemblies. For example, a rack or frame may hold several shelves of subassemblies that must be connected together to make up a complete system.

Level 5 Connections between physically separate systems such as host computer to terminals, computer to printer, and so on.

The various levels of interconnection are illustrated in Figure 1.3.

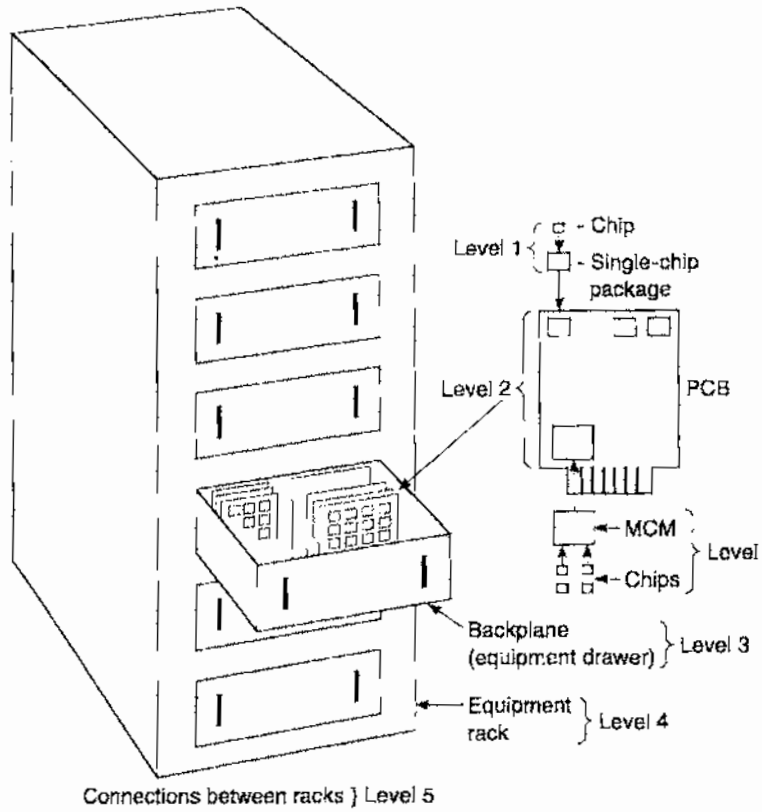

Figure 1.3 Electronic packaging hierarchy.

Gate-to-gate interconnections categorized as level 0 are formed during IC fabrication. They will not be discussed in this text. Persons interested in learning more about this level of interconnection should consult one of the many books on IC fabrication. Likewise, levels 3 through 5 are not pertinent to IC packaging, so they will not be discussed either. Although not considered a part of the packaging hierarchy, die attach (or die bonding) is a crucial step in packaging technology, so it is discussed prior to addressing levels 1 and 2.

1.3.1 Die Attach

An IC must be mounted on a substrate or metal lead frame by a die attach material, which permits heat conduction while assuring mechanical stability. The die attach may also provide for electrical grounding if the material used to secure the chip is sufficiently conductive. The three primary types of die attach materials used are soldering (both soft and hard solders can be used), which is also referred to as eutectic bonding, metal-filled polymers (epoxies), and metal-filled glasses. Hard solders, such as a silicon–gold alloy, can present reliability problems due to mismatched thermal expansion coefficients. Soft solders generally do not suffer from this problem because they exhibit plastic flow, which prevents chips from seeing high stresses. However, they can result in failure due to fatigue and creep.

Metal-filled epoxies and polyimides are another alternative for die bonding. As a general rule, they are less expensive, produce lower stress levels, and require significantly lower processing temperatures. Metal loading, generally silver, yields acceptable values of electrical and thermal conductivity, although normal thermal cycling during use can cause drift in these parameters over time. Polyimides require higher processing temperatures for complete curing but also exhibit a higher stability at high temperatures than materials containing metal fillers.

Glass adhesives have also been used for die attach. The primary problems with glasses are the excessively high processing temperatures and the possible presence of oxidizing agents, which can corrode the IC. Silver-loaded glass adhesives have been used in ceramic packages.

1.3.2 First-Level Interconnection

First-level packaging (or interconnection) refers to the technology required to get electrical signals into and out of a single transistor or IC; in other words, the connections required between the bonding pads on the IC and the pins of the package. This is generally accomplished by wire bonding, flip-chip bonding, or TAB, all of which are illustrated in Figure 1.4.

1.3.2.1 Wire Bonding

Wire bonding is the oldest method used for first-level interconnection and is still the dominant method used today, particularly for chips with a moderate number of inputs/outputs (I/O) (i.e., 200). This technique involves connecting gold or aluminum wires between the chip bonding pads, located around the periphery of the chip, and contact points on the package. Although this process has been automated for many years, it is still time consuming because each wire, requiring two bonding operations, must be attached individually. Limitations of wire bonding include the requirement for minimum spacing between adjacent bonding sites to provide sufficient room for the bonding tool, the number of bonding pads

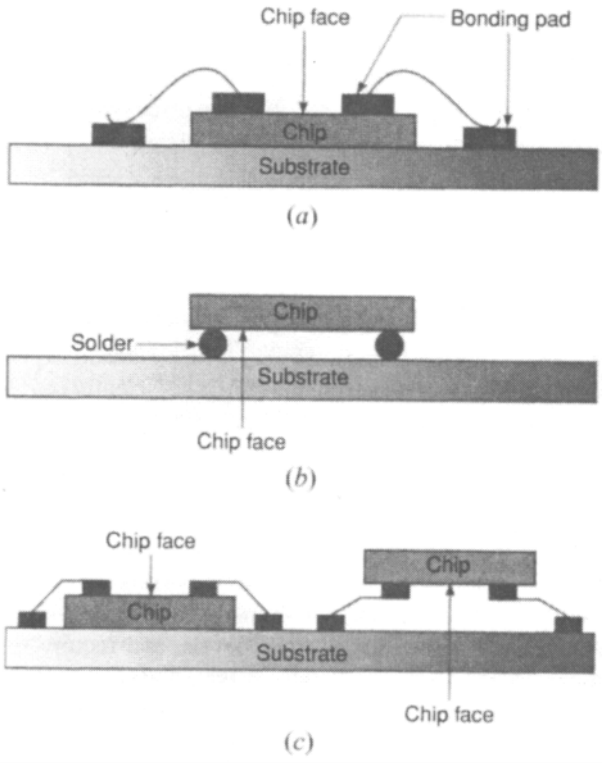

Figure 1.4 Illustrations of (*a*) wire, (*b*) flip-chip, and (*c*) tape-automated bonding.

that can be located around the periphery of the chip, signal delay, and crosstalk between adjacent wires.

1.3.2.2 Flip-Chip Bonding

In this interconnection technology, the chip is mounted upside down onto a carrier, module, or PWB. Electrical connection is made via solder bumps much like those used in TAB, which is discussed in the next section. The solder bumps are located over the surface of the chip in a somewhat random pattern or an array so that periphery limitation, such as that encountered in wire bonding, does not limit the I/O capability. The I/O density is primarily limited by the minimum distance between adjacent bonding pads on the chip and the amount of chip area that can be dedicated to interconnection. Additionally, the interconnect distance between chip and package is minimized since bumps can essentially be located anywhere on the chip. Although this technique is attractive for use in multichip packaging technology because chips can be located very close together, fatigue of solder joints due to thermal expansion mismatch of the chip–bond–substrate, heat removal from the back of the chip, and difficulty inspecting the solder joints after the chip has been attached to the substrate offer special challenges to the packaging specialist.

1.3.2.3 Tape-Automated Bonding

Tape-automated bonding, developed in the early 1970s, is a third method for accomplishing first-level interconnection. It is most often used with chip carriers or PWBs. In this technique,

ICs are first mounted on a flexible polymer tape, such as polyimide, containing repeated, flat, wide copper interconnection patterns formed lithographically from a metal laminate. Each pad on the IC is aligned to a metal interconnection stripe on the tape and attachment is effected by thermocompression bonding. All bonds are formed to the IC at the same time by a process called gang bonding. This is referred to as inner lead bonding (ILB). At this point, the IC can be tested and burned-in, allowing poorly bonded or defective chips to be eliminated prior to packaging. Good chips are then outer lead bonded (OLB) to lead frames or PWBs using the thermocompression process. The shape of the interconnections and the use of copper with its lower resistivity results in low inductance and low resistance that minimizes signal distortion. However, TAB requires the use of complex metallurgy, multilayer solder bumps either on the tape or IC or both in order to effect a bond. Generally, the bumps utilize gold or copper as the primary constituent, along with titanium or tungsten as a diffusion barrier to prevent alloying. Finally, a TAB tape can only be used for a chip and package that matches its interconnection pattern. Thus, each TAB tape is, in effect, a custom tape. However, TAB will likely continue to gain popularity as a method for bonding chips directly to a PWB and for large chips with high I/O requirements.

1.3.3 Package Lid and Pin Sealing

Lid and pin sealing generally utilize materials that are similar or identical to those used elsewhere in packaging technology. Low-melting-temperature glasses are used for sealing both the lid and I/O pins in hermetic packages. Required properties of these sealing glasses include (1) the ability to form a hermetic seal, (2) temperatures required to effect the seal must be compatible with the other materials in the package, (3) must adhere well to the materials being sealed, (4) must have a thermal coefficient of expansion compatible with the materials being sealed, and (5) the sealing glass must be electrical insulating. The primary problems encountered with glass seals are low strength and brittleness.

Metal hermetic lid seals are effected by low-melting-temperature brazing, alloy soldering, or welding. Solders used for lid sealing are dictated by the temperature hierarchy of the processes that precede and follow the sealing operation, the required seal strength, and cost. It is less desirable than brazing because of its lower strength, tendency to become embrittled by intermetallic formation, and the use of fluxes. Brazing, which consists of reflowing a preform of a eutectic, for example, Au–Sn (80–20), yields a stronger, more corrosion-resistant seal, although it is a little more difficult to perform consistently. On the other hand, welding is still the most popular method of realizing high-reliability hermetic seals because of the high yield and the fact that the high-current pulses used to effect the weld produce only local heating.

1.3.4 Second-Level Interconnection

As noted previously, level 2 interconnection refers to the electrical connection of an IC to a circuit board, the most common one being a conventional PWB. Following level 1 interconnection, single IC chips normally undergo encapsulation in either plastic or ceramic-based packages prior to connection to a PWB. In other cases, the IC is bonded directly to a PWB either by a die attach/wire bonding scheme or using TAB. The chip is then protected by a "glob-top" encapsulant such as a topical epoxy or a silicone. This interconnection technique, referred to as chip on board (COB), has the advantages of reduced PWB area and cost because of the elimination of an extrinsic package. For multichip packages,

second-level interconnection is the connection between a package containing more than one chip, which are interconnected via an imbedded conductor network in a substrate, and a PWB. However, the substrate on which the chips are mounted prior to being inserted into a package actually qualifies as a PWB in the broadest sense of the definition of a PWB.

1.4 BRIEF HISTORY OF MICROELECTRONIC PACKAGING TECHNOLOGY

It is probably impossible to determine the exact date that electronic packaging began to be viewed as an engineering and science technology. However, microelectronics packaging technology began in earnest in response to the discovery of the transistor in the late 1940s and has continued to evolve to serve the increasing complexity and performance of ICs since that time. Early transistors were of the alloy structure and were housed in plastic packages, providing little in the way of protection for the device. However, once the military became interested in these new devices for high-reliability applications, the need for hermeticity to prevent transistor gain degradation and junction leakage current due to contamination and moisture led to the development of the metal transistor outline (TO) packages shown in Figure 1.5. These packages consist of a gold-plated metal base containing external leads (generally three or four leads for discrete transistors), commonly referred to as a header, and a metal lid that is sealed to the header by welding in an inert atmosphere, such as nitrogen or argon, to ensure that moisture and other contaminants are excluded from the ambient in which the electronic device must operate.

With the development of silicon planar technology, electronic packages were developed to accommodate the large number of I/O leads of ICs. Initially, ICs were merely packaged in higher pin count versions of the TO can, which quickly became inadequate to handle the more complex and higher I/O integrated circuits. Consequently, the 1960s saw a rapid proliferation of new packages for ICs. Because of cost considerations, the lack of standards for package design, and difficulty in mounting some packages onto PWBs, only

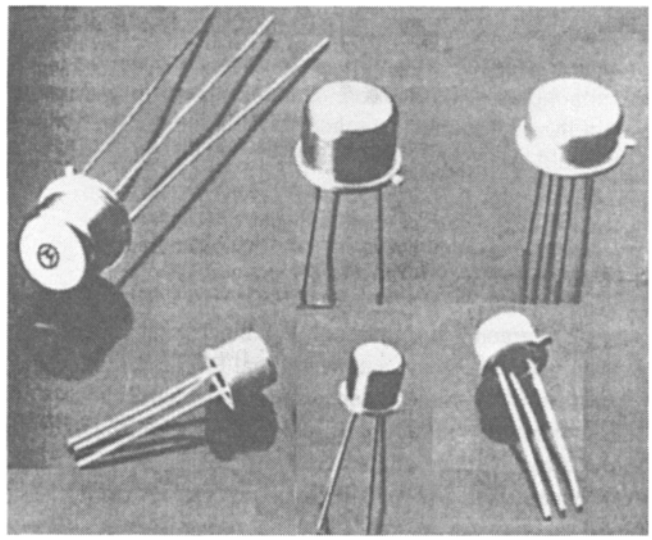

Figure 1.5 Photograph of a selection of TO packages.

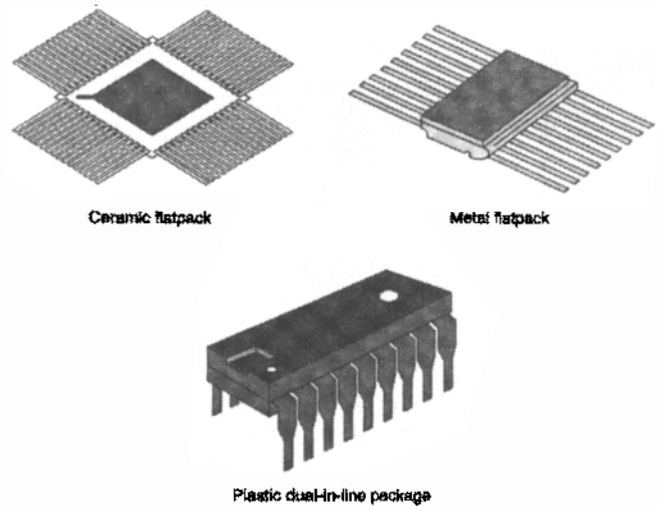

Figure 1.6 Dual-in-line and flatpack packages.

the "flatpack" and dual-in-line package (DIP) survived. Examples of these two major types of IC packages are shown in Figure 1.6. It should be noted that the flatpack leads, which extend from all four sides, are essentially planar with the package, while those of the DIP are perpendicular to the body of the package and exit on two sides. This has some implications in terms of mounting to PWBs. In particular, the DIP is ideally suited for insertion mounting onto PWBs via plated through holes (PTHs) by automatic insertion machines and wave soldering, whereas the flatpack has to be mounted using special methods and tools. Consequently, the DIP became the primary package for ICs and, along with through-hole PWBs, has long dominated the electronics assembly market.

Packaging costs also received considerable attention during the 1960s while the industry was deciding which package or packages would become standard. One of the early attempts to develop a low-cost, hermetic package resulted in the CerDIP, which was a DIP constructed of two pieces of sandwiched ceramic with the leads protruding from between the slabs of ceramic as shown in Figure 1.7. The two pieces of ceramic were held together using a low-melting-temperature glass, which also acted as a seal, thereby providing hermeticity. Unfortunately, the glass used originally outgassed moisture, which created reliability problems. The development of vitreous sealing glasses, which do not outgas moisture, coupled with performing the sealing operation in a nitrogen ambient reduced the reliability problem to a tolerable level.

Driven by the need to further reduce packaging costs, the industry pursued fully automated manufacturing of plastic DIPs. The result of this effort was a low-cost plastic package, which was transfer molded around an IC chip that had previously been die and wire bonded to a lead frame. Unfortunately, plastics are not hermetic because of their high permeability to moisture and poor adhesion to the metal leads, which provides a path for water vapor to access the IC. Furthermore, the resins and fillers either initially contained undesirable contaminants (e.g., Cl and Na) or they were polymerization by-products of the plastics, leading to degradation of the IC. These problems were eventually resolved by improving the encapsulant applied to the chip prior to plastic packaging and improvement in the properties of the plastics themselves.

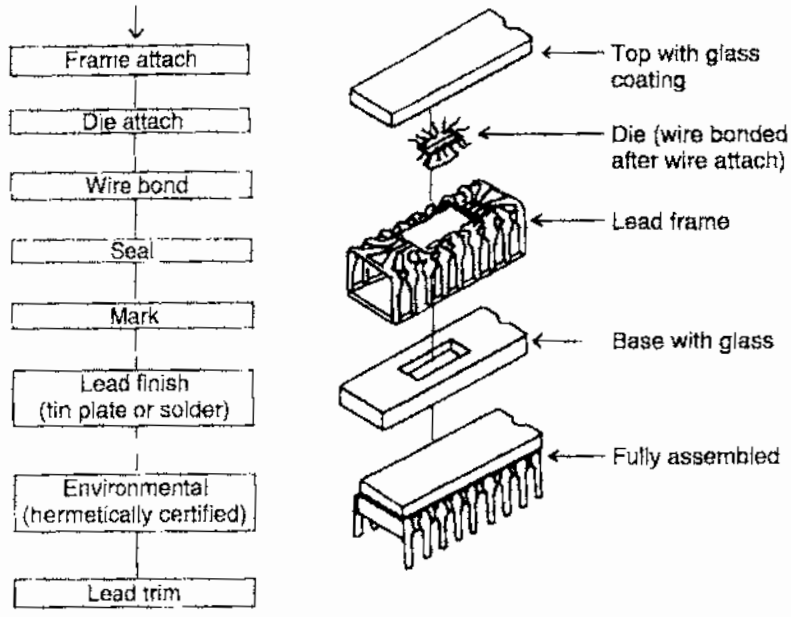

Figure 1.7 Assembly sequence for CERDIP.

The 1970s and 1980s saw the development of several types of IC packages, including surface-mount packages (SMPs), in response to a need for higher density PWBs. When mounted on a PWB, the SMP's leads do not penetrate the PWB like those of through-hole-mounted packages. Thus, they can be mounted on the side of the PWB containing conductor traces. Consequently, SMPs can be mounted on both sides of a PWB. Mounting of SMPs to PWBs is accomplished by reflow solder technology, which gave new life to the flatpack, actually the first surface-mount package. Also, small outline packages (SOPs), which resemble miniature versions of DIPs, as shown in Figure 1.8, were developed for use in surface-mount technology (SMT). The two types of small outline packages are the small outline transistor (SOT) and the small outline IC (SOIC) shown in Figure 1.9. This same period saw the development of chip carriers and quadpacks (or quad flatpacks). The chip carrier is available in both leadless and leaded versions, as well as with plastic and

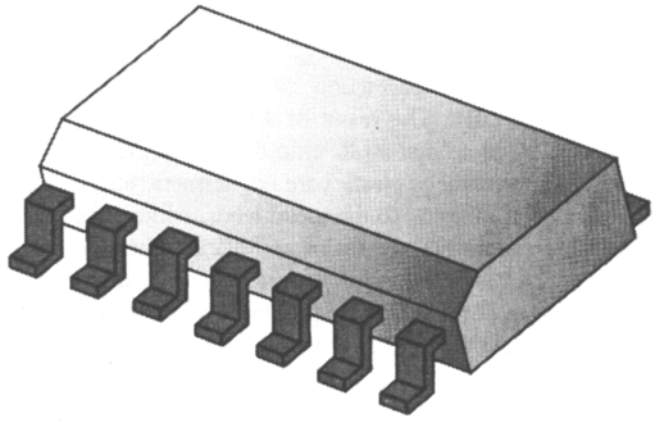

Figure 1.8 Small outline package (SOP).

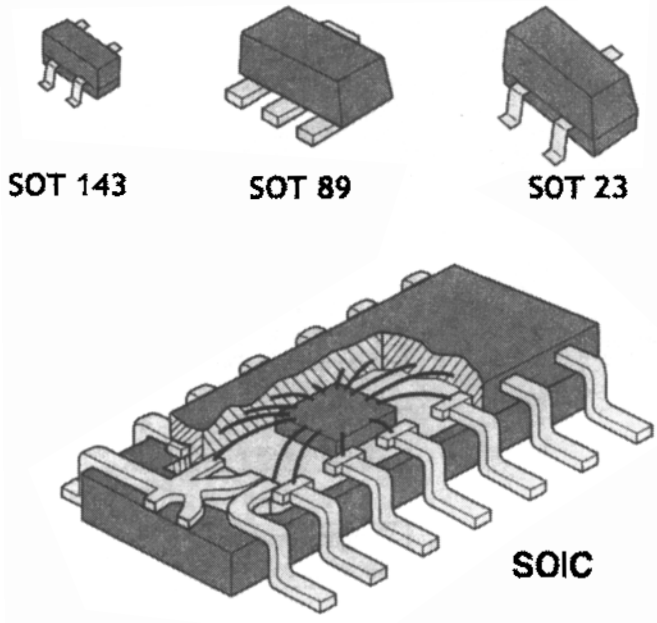

Figure 1.9 Small outline transistor (SOT) and small outline integrated circuit (SOIC) packages.

ceramic bodies (see Fig. 1.10). These type packages conform very closely to the size of the ICs they contain and have leads on all four sides. The quadpack, one of the earliest plastic surface-mount IC packages, comes in a variety of sizes and lead configurations and also has leads on all four sides as shown in Figure 1.11. The terminal pitches vary from 0.3 to 1.0 mm (10 to 50 pins/cm^2). Thus, the quadpack (I/O $\approx$ 300) is generally used when the chip I/O requirements are greater than can be addressed using a DIP (I/O $\approx$ 64 with 10 pins/cm^2).

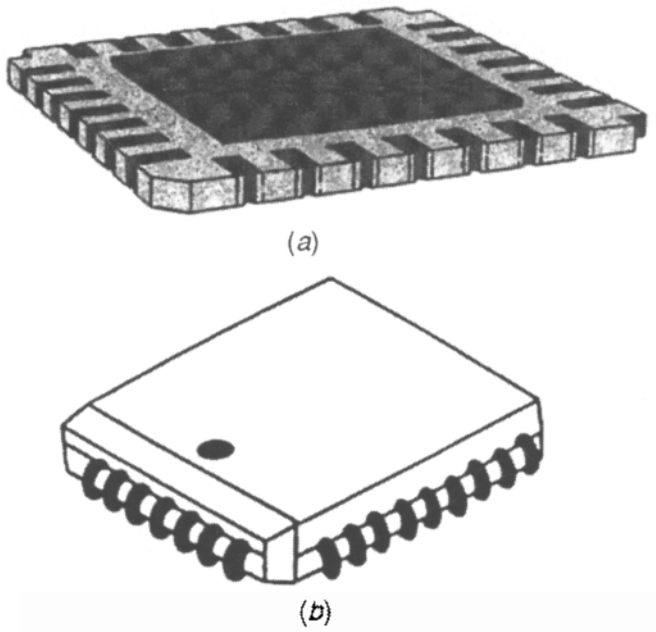

Figure 1.10 (*a*) Ceramic leadless chip carrier and (*b*) plastic leaded chip carrier.

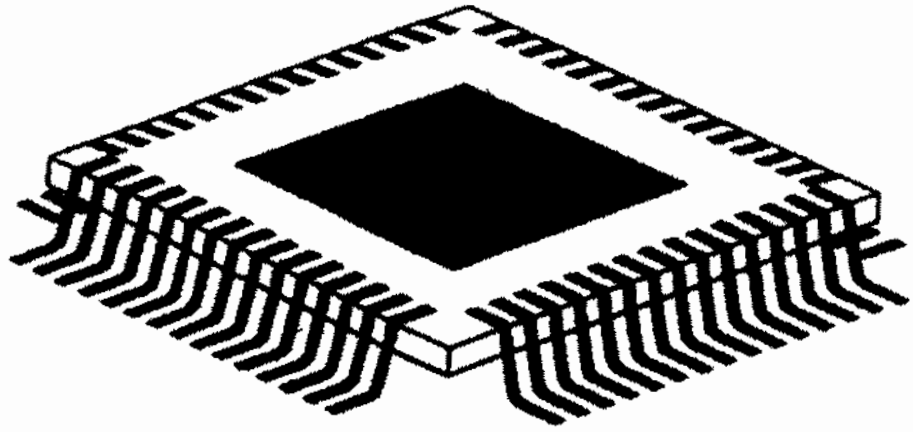

Figure 1.11 Quad flatpack (or quadpack).

The ultimate goal for high-performance electronic systems is generally to pack devices as close together as possible in order to minimize circuit path length. In response to this need, the early 1990s saw the emergence of both pin grid array (PGA) and ball grid array (BGA) packages as a replacement for quad flatpacks (QFPs), primarily because of their high I/O density (the terminals are arrayed on part or all of the bottom of the package), minimum footprint, and shorter electrical paths, which means that they have better electrical performance. For QFPs, lead counts higher than 200 require lead spacings of 0.5 mm, and for 300 leads, the spacing approaches 0.3 mm. Unfortunately, as spacings become tighter, the yield falls exponentially with lead spacing. For I/Os greater than 250, the PGA and BGA have an advantage over the QFP in that they always occupy less space than a QFP. However, PGA and BGA construction is inherently more expensive than that of the QFP because of costs associated with the component carrier substrate. The primary terminal pitches of the BGA are 1.27 and 1.5 mm, yielding a mounting density of 40 to 60 pins/cm^2..

The BGA package evolved from flip-chip technology, also referred to as controlled-collapse chip connect (C4), pioneered by IBM for ICs [6]. Thus, the BGA package can be identified by the solder bumps on the bottom of the package. The solder bumps can be arranged in a uniform full-matrix array (i.e., over the entire bottom surface), a staggered full

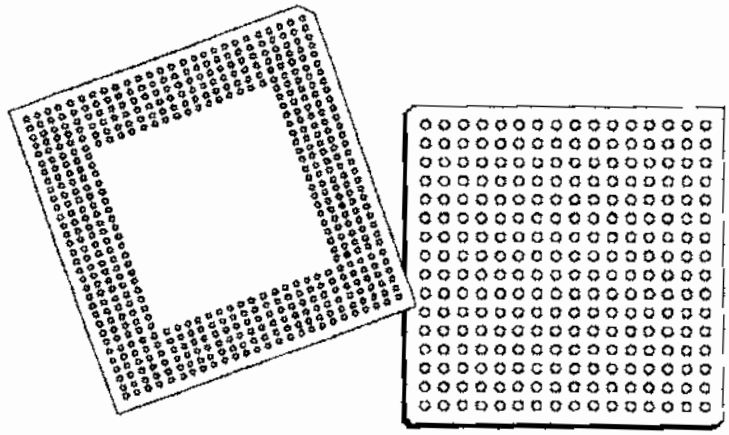

Figure 1.12
Examples of full matrix and perimeter array BGA I/O solder bumps.

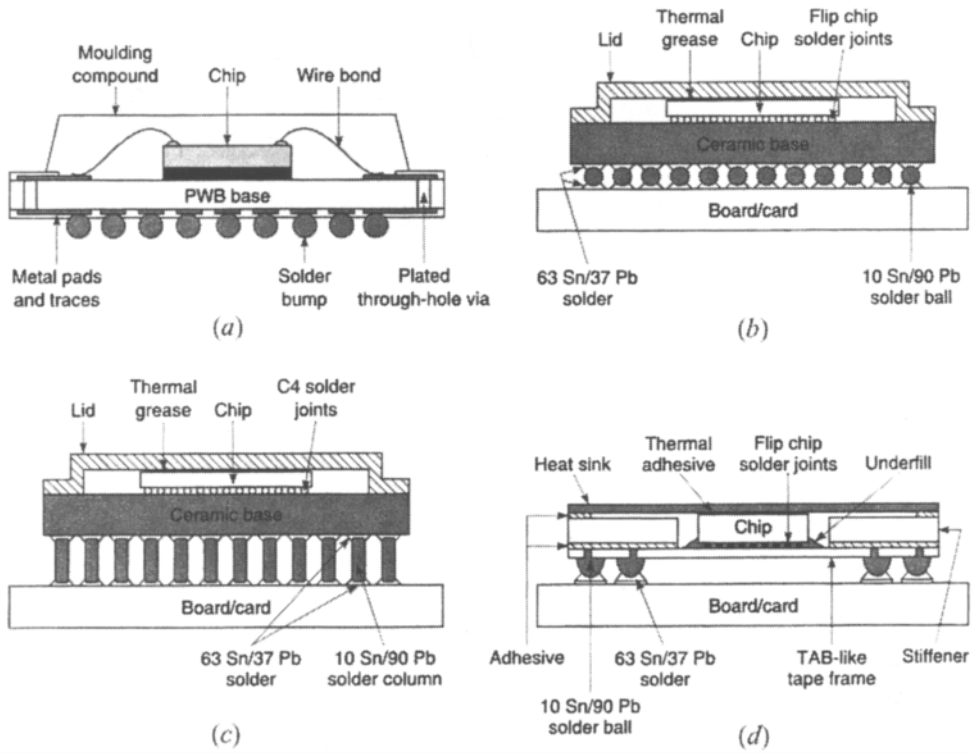

Figure 1.13 Conceptual sketch of (*a*) plastic ball grid array, (*b*) ceramic ball grid array, (*c*) ceramic column grid array, and (*d*) tape ball grid array.

array, or around the perimeter in a multiple number of rows (see Fig. 1.12). No matter how the bumps are arranged, the result is a smaller footprint than that of conventional packages. As noted previously, for a given amount of real estate, the BGA package provides more I/O than QFPs. Thus, the BGA package is considered the package of choice for high-density and high-I/O ICs.

As is the case with other packages, BGAs have been broadly classified according to the type and form of the die carrier substrate material. Thus, the packages have been classified as CBGAs (ceramic), CCGAs (ceramic column), PBGAs (plastic), MBGAs (metal), and TBGAs (tape). These packages, some of which are conceptually illustrated in Figure 1.13, can house either a single chip or multiple chips.

As noted previously, one of the big advantages of BGA packages is that they offer high I/O. Typical I/O for several types of BGAs are 400 I/O PBGAs, 736 I/O TBGAs, and 625 I/O CBGAs, although BGA packages are available with more than 2000 leads. Ceramic column BGAs are available with I/Os greater than 1000. Current and planned designs have solder-bump-array pitches in the range of 40 to 150 μm. The solder bumps are generally of tin–lead or tin–lead–silver composition. Thus, the BGA is a leadless package that is not susceptible to bent or skewed leads, which means that it can be easily handled. However, there are some aspects of BGA packages of concern. In particular, solder joint defects, warpage during reflow, a large variation in solder ball size, the inability to visually inspect the solder joints, reduced resistance to thermal cycling, and problems associated with rework. These can be overcome with good design, process development, and process control

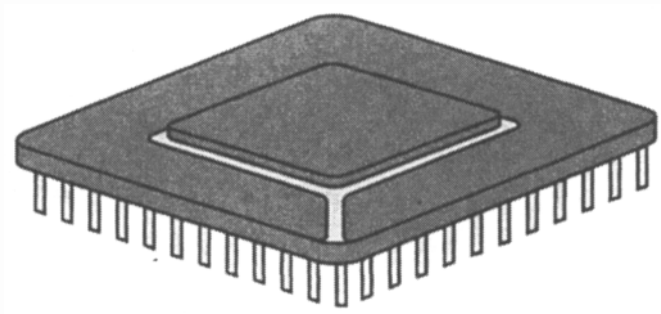

Figure 1.14 Pin grid array package.

so that the resulting yield makes inspection and rework of minor importance. Considering all the pluses and minuses, BGA still appears to be the surface-mount package of the future for both single-chip and multichip packaging. Similarly, the PGA package (I/O $\approx$ 600), illustrated in Figure 1.14, is used when the I/O requirement is higher than that provided by quadpacks.

There always has been and will continue to be motivation to pack more electronic functionality and higher speed performance into a smaller volume of space. Packaging of ICs is one area that offers attractive benefits for reducing size and improving performance by either eliminating the package or reducing the size to the point where it takes up very little more space than the IC. Elimination of the package [i.e., direct chip attach (DCA)] still presents some problems where full functionality and reliability testing are concerned. In other words, the ability to test and burn-in bare die has not yet reached the quality and reliability levels comparable to the same die in a package. Consequently, packaging ICs for testing and burn-in is still very attractive. In the late 1990s, the BGA concept was applied to a packaging technology referred to as chip-scale packaging (CSP) by reducing the terminal pitch to 1.0 mm or less for a mounting density greater than 100 pins/cm^2 [7, 8]. CSP contributed significantly to a reduction in the size, weight, and performance of products such as the cellular phone.

CSPs are essentially "packages" that ruggedize the IC for ease of handling, testing, and assembly. Thus, CSPs are a viable substitute for "known good die" (KGD) if low-cost test and burn-in methods are not available for bare die. CSPs, also referred to as slightly larger than IC carrier (SLICC), are generally defined as packages that are equal to or smaller than 1.2 times the bare die size. Microball grid array, miniball grid array, and micro-SMT packages fit this definition since they are of minimum size and employ direct surface mounting instead of wire bonds. In fact, in excess of 60 different chip-scale package types have been proposed over the years. The primary difference in the various types is the material layers, which serve as compliant members, space transformers, and mechanical protection, between the silicon and the bump array. These material layers serve to categorize the CSPs into tape carrier (flexible laminate), resin mold, ceramic carrier, silicon-based, rigid laminate, lead-on-chip (LOC), and lead frame types.

CSPs are designed to be flip-chip mounted using conventional equipment and solder reflow. Essentially, CSPs take advantage of the attributes of a flip chip in a surface-mountable package. Thus, CSPs offer a method for subjecting ICs to full functional and reliability testing using a packaging technology while essentially maintaining the size and performance of bare die.

The 1980s also marked the turning point in the way electronic engineers viewed IC packaging technology. As noted previously, for many years the electronics industry had been concentrating on increasing the performance of ICs (i.e., more circuitry/silicon area operating at higher speeds) with little consideration of the fact that ICs in an electronic system must communicate with each other through the packages that contain them. As a result of the trend toward higher circuit densities and operating speeds on a chip, the following effects became important considerations for packaging engineers:

- I/O requirements increased sharply.
- Signal transition time between chips became a factor limiting system speed.
- Signal integrity between silicon chips degraded.
- Power requirements per chip increased.
- A problem with heat dissipation was created.

All of these factors forced electronic packaging technology into the spotlight, resulting in a reconsideration of how ICs were being packaged. From this reconsideration evolved multichip packaging, for example, multichip module (MCM) packaging technology [5], examples of which are shown in Figure 1.15. Although the basic concept of a multichip module was not new (hybrid circuits had been around for nearly 50 years), in the late 1980s and throughout the 1990s interest was renewed in mounting a multiple number of ICs in a single package in order to take advantage of inherently shorter interconnection distances between ICs. Thus, the development of MCM technology became an industry effort to push the performance of electronic systems to higher and higher levels.

The simplest definition of an MCM is that of a single electronic package containing more than one IC. The ICs are interconnected through a substrate. Based on this simple definition, an MCM combines high-performance ICs with a custom-designed common substrate structure, which provides mechanical support for the chips and multiple layers of conductors to interconnect them. This arrangement takes better advantage of the performance of the ICs than does interconnecting individually packaged ICs because the interconnect length is much shorter. The really unique feature of MCMs is the complex substrate structure, which is fabricated using multilayer ceramics, polymers, silicon, metals, glass-ceramics, laminates, and the like. Thus, multichip modules are not really new. They have been in existence since the first multichip hybrid circuit was fabricated. Conventional PWBs utilizing chip on board (COB), a technique where ICs are mounted and wire bonded directly to the board (direct chip attach), have also existed for some time. However, if packaging efficiency (also called silicon density), defined as the percentage of area on an interconnecting substrate that is occupied by silicon, is the guideline used to define an MCM, then many hybrid and COB structures with less than 30% silicon density do not qualify as MCMs. The fundamental (or basic) intent of MCM technology is to provide an extremely dense conductor matrix for the interconnection of bare IC chips. Consequently, some companies designated their MCM products as high-density interconnect (HDI) modules and others dropped the MCM designation for multichip packages (MCP).

MCM technology, still a viable technology today, played a major role in the evolution of multichip packaging in the 1990s, which includes three-dimensional (3D) stacking of ICs within a single package [9–13]. Although chips can be stacked physically without connecting them to each other to save board space, present development efforts focus on interconnected, stacked chips. One of the first commercial efforts to stack chips within a single package mated flash memory with static random-access memory (SRAM). However,

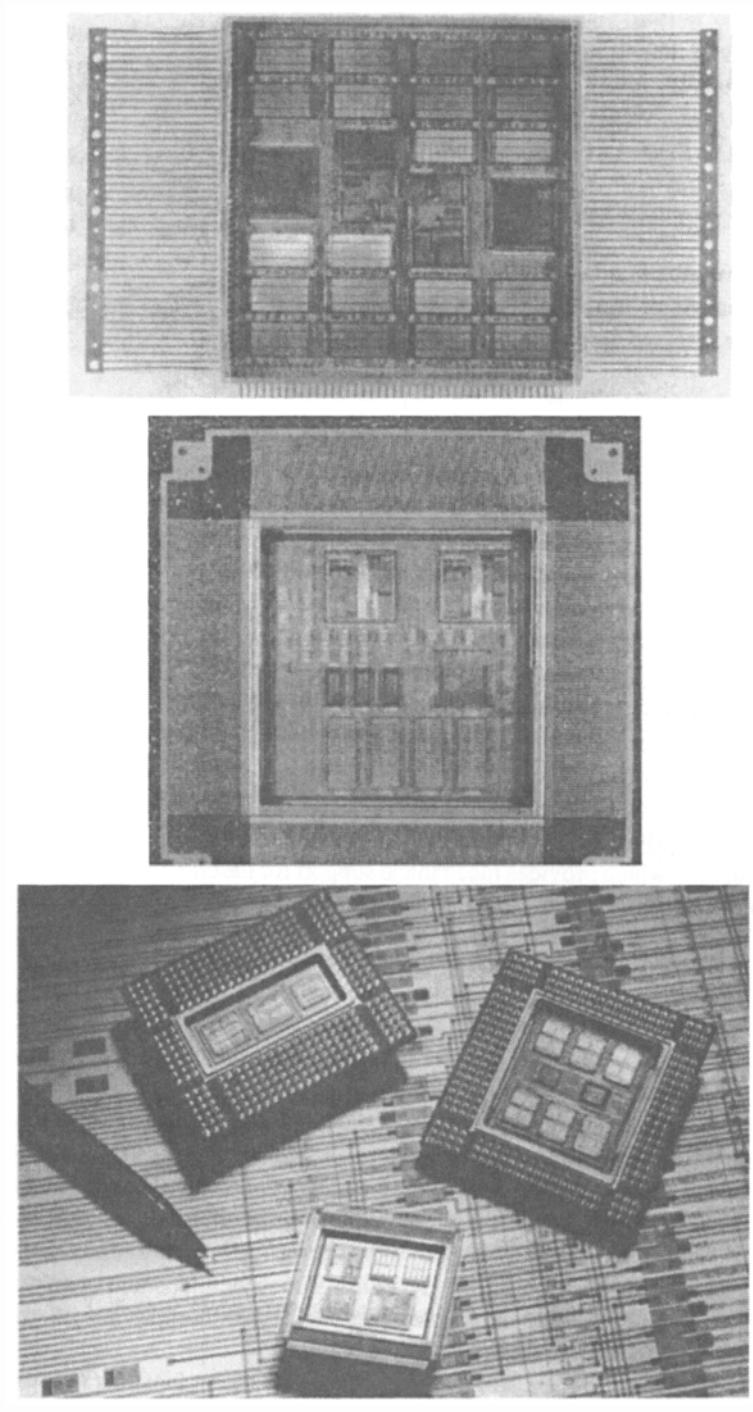

Figure 1.15 Packaged MCMs (courtesy of nCHIP).

several patents issued in the 1980s described and illustrated chip stacking approaches to multichip packaging. As a rule, multichip packaging can take many forms but is simply the packaging of more than one IC in a single package, no matter the details of the IC interconnection or whether or not they are electrically interconnected. In fact, another approach to multichip packaging is referred to as "few-chip packaging" [14]. This generally refers to the placing of 2 to 5 ICs on a laminate substrate in a BGA package that looks very similar to a single-chip package.

The industry desire to reduce product size, weight, and cost [e.g., cell phones, personal digital assistants (PDAs), and other hand-held applications] while providing extra performance (i.e., shorter interconnects that lower capacitance and inductance, reducing crosstalk, and lower power consumption) and increasing functionality, has driven 3D packaging of both chips and packages. Figures 14.16 and 14.17 illustrate some approaches to chip stacking and interconnection, respectively. Chip stacking offers the additional advantage of assembling die of dissimilar geometries and the use of mixed technologies.

Chip stacking may be the proper choice when high-yielding ICs are available in bare die form. However, chip stacking has resulted in the need to thin chips to 100, 75, 50, 20 or even 10 μm and below, so that a multiple number of them can be mounted in a conventional package without increasing the vertical profile [15, 16]. Even so, chip stacking is usually limited to 2 or 3 chips, yielding silicon efficiencies of approximately 140 and 220%, respectively, but as many as 8 chips in a single package has been achieved. The goal appears to be a maximum package height of 1.2 mm for two-die stacks and 1.4 mm for three-die stacks. This packaging approach has been used as an alternative to system on a chip (SOC) [17–20], which has been made possible partly because of the improvement in bare die testing [21–23]. The result is essentially a system on a package (SOP) [24] or a system in a package (SIP) [25]. Interestingly, the success with chip thinning has even spawned an effort to develop thinner packages, referred to as ultrathin or paper-thin packages, for single-chip packaging. The development of such packages also makes package stacking more attractive.

Thinning of chips improves their thermal performance, allows for mounting on irregular surfaces, relieves stress in the chip when mounted, and produces a more mechanically reliable device. However, thinning chips also creates a whole new set of challenges because of the wafer thinning process. These include induced stresses, microcracking, and the creation of defects in the chips. Additionally, dicing and handling of very thin chips during assembly can be problematic. Furthermore, design software, thermal management, and a single chip failure in a stacked system can all contribute to higher cost for a system.

Figure 1.16 shows approaches to package stacking. Any approach to package stacking results in silicon efficiencies in excess of 100%. Package stacking is fairly straightforward and is preferable for lower yielding devices or where chips require burn-in. One merely needs to develop techniques for connecting the packages together mechanically and electrically. This can be accomplished by simply soldering the leads of the packages together (Fig. 1.16*a*) or by the use of an interposer such as a flexible PWB (Fig. 1.16*b*). Package stacking has the advantages of using existing technology, it can have a CSP footprint, and it allows reasonably easy integration of different processes and materials. The biggest disadvantage of package stacking is the height of the resulting unit.

The most recent approach to the packaging of chips is referred to as wafer-level packaging (WLP) or wafer-scale packaging (WSP), which began in the late 1990s [26–30]. In WLP, the die and package are manufactured and tested on the wafer prior to separation of the packaged devices by dicing in the flip-chip fashion. Consequently, the packages are really

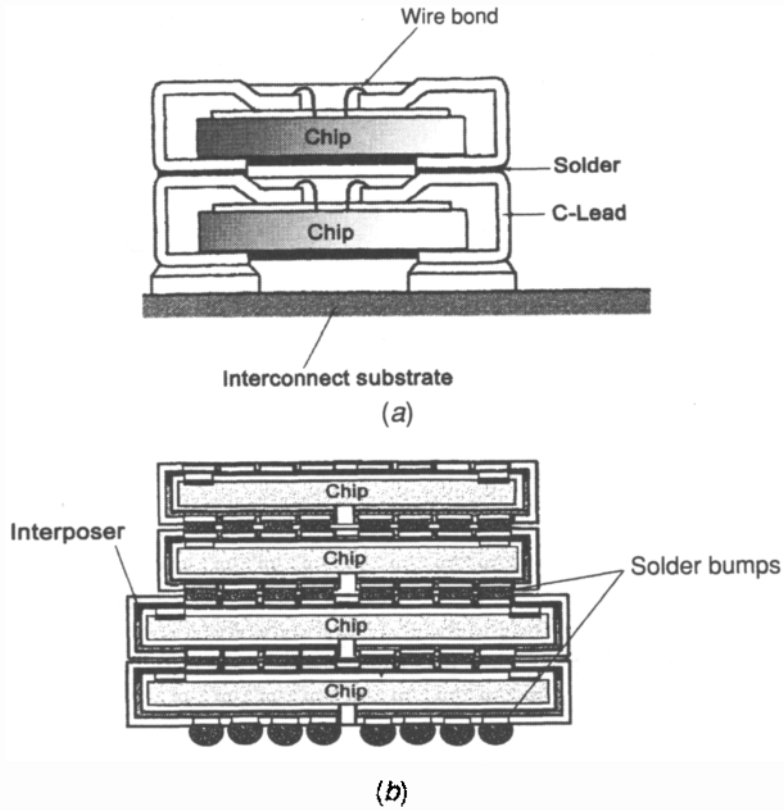

Figure 1.16 Three-dimensional package stacking.

chip size as opposed to chip scale, which has produced the name wafer-scale/chip-scale packages (WS–CSP) or wafer-level/chip-scale packaging (WL–CSP).

The motivation for WLP (WSP) is that peripherally designed die can be transformed, using a thin-film technology, into a standard bump or ball footprint that is compatible with current PCB layout rules, device test practices, and assembly practice. Originally, wafer-level redistribution was intended to physically redistribute perimeter bonding pads to an area array for flip chip technology.

In addition to the package size, some other benefits of WLP are lowest cost per I/O since all interconnections are formed at the wafer level at the same time, lowest testing cost since it can be done at the wafer level, lowest burn-in cost because it is done at the wafer level, elimination of underfilling, and enhanced electrical performance because of the short interconnections.

The next logical step in packaging is presently under development and is referred to as wafer-level stacking (WLS) to yield stacked die that are packaged at the wafer level. Wafers containing ICs are interconnected using a thinly polished wafer (a few tens of microns thick) containing through-wafer vias. Figure 1.17 provides an illustration of wafer-level stacking. An active wafer can be joined to a passive interposer or another active wafer using any convenient joining method. The top wafer is then thinned to expose through-hole contacts. The process is repeated to add more wafers to the stack. Upon completion of the wafer-level packaging process, individual packages containing stacked die are obtained by singulation.

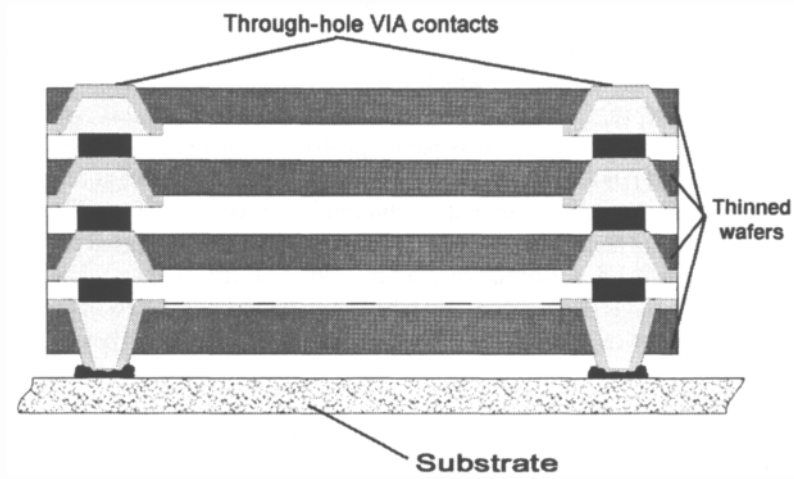

Figure 1.17 Wafer-level stacking to yield wafer-level packaging of stacked die.

There appears to be little doubt that the impact of packaging on future electronic systems will continue to increase with time. In fact, the trend will continue to be toward a more integrated approach to semiconductor packaging and system design. Consequently, the boundary between semiconductor fabrication and packaging will blur, and packaging will, by necessity, become an integral part of system design.

As packaging technology progresses, there are many problems that must be addressed. Some of these are organic materials for substrates that address problems inherent to organic substrates such as moisture absorption, dielectric loss, warpage, limited minimum interconnect dimensions, and so forth. Lower loss dielectrics are also critically important to higher frequency system operation. Given that lead-free soldering probably will be mandated worldwide at some point in time, development of lower cost materials with lower processing temperatures must be developed [31, 32]. Then, for new materials, reliability issues must also be addressed. As minimum chip geometries continue to shrink into the nanometer range, higher pin count, higher wiring density, and passive device integration will provide significant challenges to packaging technology. If these challenges can be and are met, then thermal management will continue to provide challenges for the researcher. Finally, the emerging need for packaging of MEMS, optoelectronics, and nanodevices ensure that packaging technology will remain fertile ground for research and development into the foreseeable future.

1.5 DRIVING FORCES ON PACKAGING TECHNOLOGY

Historically, packaging has always been a substantial fraction of the price of an IC (10 to 50%), and, consequently, reducing packaging costs while maintaining reliability and performance has been the focus of packaging engineers for many years. During this time, IC technology has transitioned from small-scale integration (SSI) in the 1960s to submicron minimum dimension very large scale integration (VLSI) at the present time. Since packaging technology has not enjoyed anywhere near the performance advancement of ICs over the past 30 years, electronic system performance has become increasingly limited by IC packages. Thus, design decisions facing packaging engineers today are becoming increasingly driven by system performance for a market that is still very cost conscious.

Given that cost and performance are the primary concerns in electronic packaging, it is important to examine the factors that relate performance and cost to packaging technology choices. Some factors, which must be considered, are manufacturability, reliability, serviceability, size, weight, signal integrity, mechanical stability, and power consumption with its accompanying heat dissipation problem. In general, packaging costs are driven by materials and fabrication requirements associated with actual manufacturing and by testing and rework associated with manufacturability. In the case of multichip packaging, manufacturing costs include the cost of the IC chips, generally referred to as "known good die." On the other hand, performance is a function of electrical, thermal, and mechanical design constraints, material selection, and fabrication limitations. A few of these cost–performance factors, treated in detail in later chapters, are briefly discussed below.

1.5.1 Manufacturing Costs

As noted previously, manufacturing costs include all the materials and fabrication steps required to produce each packaged IC including the cost of the IC itself. The materials include not only the actual material that goes into the package but also materials such as chemicals required to process the material, which ultimately are part of the package. Manufacturing costs vary widely for packaging and interconnection elements.

1.5.2 Manufacturability Costs

Manufacturability costs, because they are generally associated with how well the product was designed for manufacturability, are incurred as a result of testing, reworking when possible, retesting after rework, and fabrication yield loss. Since testing is, at the present time, the only way to ensure full functionality and high reliability for both single-chip and multichip packaged parts, packaging technology should provide for full testing of the finished product. Furthermore, since the final yield can be increased above initial yield by reworking some of the parts that fail initial testing, it is important that packaging technology also allow for an inexpensive and easy rework process. Although chips usually cannot be repaired, this is not necessarily the case for multichip packaging. Reworking multichip packages, which generally refers to the replacement of a chip or chips within the package is an important cost issue because rework costs are generally high. Consequently, high value chips should be thoroughly tested prior to mounting in a multichip package.

1.5.3 Size and Weight

Because of the many environments in which packaged electronic systems must operate, size and weight are often considered to be performance goals. Restrictions placed on these two physical parameters may be the result of personal preferences or system requirements. For example, weight may be a critical factor if the system is to operate in a satellite or a portable computer. Size (either area or volume or some combination of the two) may be critical in applications such as calculators and cellular phones. Most important, specifying these parameters can impact other design aspects of the electronic package such as material specifications and cooling requirements.

1.5.4 Electrical Design

As noted previously, the on-chip switching speeds of ICs are continuously increasing. Furthermore, noise margins are generally decreasing at the same time. Unfortunately, chip I/O count and interconnection speed have not kept pace so that packaging interconnects now play a dominant and limiting role in determining overall system performance. Each lead from the chip to the package and each package lead to the outside world has some parasitic capacitance, resistance, and inductance that limits switching speed, distorts the shape of signals passing through it, and serves as a source of electrical noise. These leads are also a source of reliability problems. Likewise, the pattern of metal and dielectric that forms the circuitry between chips and from chips to the outside world of an MCP contribute to the degradation of electrical performance. Consequently, some electrical design factors that must be considered include signal lead length (short parallel runs to minimize mutual inductance and crosstalk, and short runs near ground planes to minimize capacitive loading), use of matched impedances to avoid signal reflection, low ground resistance for minimum power supply voltage drop, and power supply spiking caused by signal lines switching simultaneously. All of these factors are functions of geometries and materials.

1.5.5 Thermal Design

The primary objective of thermal design is to remove heat from the junctions of ICs to ensure that they operate properly and to avoid triggering temperature-activated failure mechanisms. This is generally accomplished by conducting the heat away from the chips and into a gas or liquid coolant. Although the power dissipation per gate of ICs has decreased in recent years, the power dissipation per chip has increased during the same time since power per gate scales linearly with feature size, while on-chip circuit power density increases as the square of the feature size reduction ratio. Even complimentary metal–oxide–semiconductor (CMOS) circuit densities and operating frequencies are becoming great enough that thermal design cannot be ignored when packaging these chips. Thermal issues are even more significant in MCP design because the heat density is generally high as a result of closely spaced, high-density, high-performance chips. Consequently, thermal design of MCPs must consider such factors as (1) how heat is to be removed from the IC (through the substrate or directly off the backside of the chip), (2) whether to use forced air or liquid cooling (forced air is generally much cheaper and the system is more likely to survive a fan failure than a pump failure), (3) the use of a high thermal conductivity substrate (high thermal conductivity usually implies a high dielectric constant, diamond being an exception) or thermal vias that can consume a large area of the substrate, thereby reducing interconnect capacity, and (4) stresses induced in the chips and substrate due to mismatches in thermal coefficients of expansion (TCEs). All of these considerations impact performance, cost, and reliability.

1.5.6 Mechanical Design

In the previous section, it was noted that mismatches in thermal coefficients of expansion cause stresses to be induced in ICs, high-density interconnect substrates, and packages of an electronic system as the temperature changes. Such stresses can be very localized, for example, under a small portion of a chip, or universal such as across an entire layer of an MCP substrate. Thus, the mechanical design aspect of electronic packaging technology is, in general, closely related to changes in temperature. Another mechanical property that

may need to be considered is stiffness, characterized by the tensile modulus (E), which is important in areas such as chip attach where three materials (chip, substrate or package, and adhesive) form two interfaces. Thermal stresses increase with increasing E and decreasing thickness of the adhesive layer. Thus, for example, a thin layer of high E adhesive material should only be used with large-area chips if the TCE of the substrate or package closely matches that of the chip.

1.5.7 Manufacturability

No matter how much effort and exactness goes into the design of an electronic package, ultimately high-quality packages must be manufacturable in sufficient quantities to allow for competitive pricing. Successful manufacturing depends on many factors such as the availability of materials, process technologies, and automated fabrication equipment at acceptable costs, cost of piece parts, manufacturing yield, manufacturing cycle time, and repairability. Design specifications must not overly challenge fabrication technology because the limitations of fabrication processes and equipment for any microelectronic technology essentially establish the ultimate capability of the technology. Although zero-defect manufacturing is possible, it is not realistic because of high costs and possible loss of competitive edge due to conservative dimensions, tolerances, materials, and process choices that would all impact performance in a negative way. Thus, the alternative is to balance the above-noted variables against loss of products due to defects, which must be screened out by testing.

Although MCPs offer significant benefits in terms of greater densities, smaller size, and better performance, implementing this technology requires significant changes in design and manufacturing methodologies, fabrication processes, and equipment. Manufacturers have, to some degree, avoided making these changes by "pushing" conventional technologies to achieve higher density/performance levels. MCP technology will continue to offer challenges to manufacturing that are somewhat unique and, thus, will continue to require the development of new materials, new processing technologies, and specialized fabrication equipment.

1.5.8 Testability

A primary motivation for testing is to find and eliminate manufacturing-induced defects. Other reasons for testing include the need to prove a new design, to verify that manufacturing processes are under control, and to predict product performance under normal operating conditions. Generally, testing can be divided into two broad categories: in-process and stress testing. In-process testing is nondestructive and is used to screen for defects that occur as a result of manufacturing and prevent the product from ever operating properly. Such testing can be performed at almost any stage of the fabrication process. At every testing point, factors to consider include testing costs, investment in the product to the point of test, and the scrap and possible repair costs. On the other hand, stress testing, which is often destructive to the product, is most frequently performed on the finished product to evaluate long-term reliability. Thus, stress testing finds product defects that do not initially prevent the product from operating, but do so later. The results of both types of testing are used as feedback to improve both product design and manufacturing.

MCPs must be subjected to the same test requirements as the single-chip packages they replace. However, MCPs present unique challenges in testing compared to single-chip packages because of their unique structure. The usual approach to MCP testing is to perform

separate testing of the substrate on which the chips are to be mounted and interconnected, the ICs prior to mounting on the substrate, and the assembled module prior to sealing in case rework is required. Since the completed MCP is a complex electrical system that must be tested as a single unit, electrical testability must be integrated into the MCP package design. At the present time, not all of the problems associated with assembled MCP testing have been solved.

1.5.9 Reliability

In recent years, highly reliable products have become commonplace in the electronics industry. Consequently, sustained success in this market has depended on a company's ability to provide superior products that are reliable. Reliability assurance is tied very closely to thorough product testing. However, consistently high product reliability requires the interaction of product design, manufacturing, and testing. When properly performed and integrated, these three functions produce a reliable product. At the system level, reliability is highly dependent on the failure rate of its component parts. Thus, in the case of MCPs, reliability of the final substrate is the combined result of the reliabilities of each of its components, pointing out the need to thoroughly in-process test the substrate, ICs, and assembled substrate, followed by stress testing of functional substrates.

1.5.10 Serviceability

Serviceability of a product refers to the demand placed on it by the need to replace failed components. For MCPs containing expensive ICs, this capability may be important when failure of a module is a result of chip failure. Given that rework costs are lower than the price of a new module, the design of the module must allow for chip replacement. Factors that impact this capability are chip spacing, method and material used to attach the die, and method and material used for electrical interconnects. In many cases, the design of this capability into the product may be in complete opposition to the performance criteria, for example, when close spacing of the ICs is extremely important.

1.5.11 Material Selection

Packaging materials play critical roles in the proper functioning of a packaged electronic system [33, 34]. For example, metals provide the means for conducting signals throughout the system via thin-film conductors, wires, contacts, vias, and the like. On the other hand, insulating materials are used to prevent loss of signal currents by confining them to the metal paths. Other materials are used to provide physical and structural support. Finally, there are materials whose primary function is to protect the system from the environment.

The packaging industry is concerned with the electrical, mechanical, thermal, chemical, and physical performance of all materials that are used in electronic packages. Table 1.1 lists some specific material properties in each of these areas that impact the fabrication, performance, and reliability of electronic packages. Because of the wide variation in these properties, material selection for electronic packaging technology is not an easy task. As is generally the case throughout the microelectronics industry, the final choice of a material for a specific application most likely results from a series of compromises or trade-offs aimed at achieving and/or optimizing one or more performance criteria. For interconnect

Table 1.1 Material Properties of Importance in Packaging Technology

Electrical properties	Thermal properties	Mechanical properties	Physical properties	Chemical properties
Dielectric constant	Coefficient of thermal expansion (CTE) (ppm/°C)	Young's modulus (GPa of kpsi)	Microstructure (grain size)	Metal oxidation
Loss tangent ($\tan\delta$)	Decomposition temperature	Poisson's ratio	Flatness and planarization	Metal migration
Resistivity (Ω-cm) volume surface	Melting point	Stress (dyn/cm^2) Shear strength (MPa)	Viscosity (poise)	Reactivity
Dielectric strength (V/cm)	Glass transition temperature (T_g)	Curing temperature	Hermeticity	Adhesion
Temperature coefficient of resistance (Ω-cm/°C)	Thermal conductivity (W/m · K)	Glass transition temperature (T_g)	Melting point	Toxicity
	Shrinkage	Dimensional stability	Eutectic temperature	Environmental
	Curing temperature	Tensile strength (GPa)	Density (g/cm^3)	
	Thermal stability	Flexural strength (GPa)	Glass transition temperature (T_g)	
	Temperature coefficient of resistance (Ω-cm/°C)	Adhesion strength	Hardness (Brinell)	
		Peel strength		
		Ductility		
		Maleability		
		Interface energy		

substrates, the selection of materials can be a particularly challenging task because of their complex multilayered structure.

1.6 SUMMARY

Because of the diversity of opinion on what constitutes an electronic package, an exact date for its origin is not possible. However, the beginning of modern electronic packaging can probably be dated around 1950, shortly after the discovery of the transistor. Since that time, a myriad of electronic packages and packaging materials have evolved. In all cases, the package must provide a structure to physically support the electronic device and protect it from the environment, a means of removing heat generated by the device, and electrical connections to and from the device. Over the years, chip packaging has evolved from simple transistor outline (TO) packages that generally hold a single transistor chip to dual-in-line packages (DIPs) for ICs to quadflatpacks (QFPs) to chip-scale packages (CSPs). The most recent electronic packaging technologies, referred to as multichip packaging (MCP), house an electronic system by interconnecting a multiple number of ICs within a single packaging structure. This can be done either in a planar fashion, such as the case for multichip modules (MCMs), or in the vertical direction by chip stacking. Chip stacking can be accomplished by either stacking single-chip packages or by stacking a multiple number of chips in a single package, or a combination

of the two. More recently, wafer-level packaging, which involves creating the package while chips are still in wafer form and then separating them by dicing, is gaining popularity. Future packaging likely will involve wafer-level packaging of stacked wafers, resulting in stacked chips interconnected by vias formed through the material used to physically separate the wafers. Thus, system packaging at the wafer level will be possible and will permit the mixing of different technologies in a single package.

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EXERCISES

1.1. What do you think is meant by the phrase, "the point has been reached where advancement in integrated circuit performance now drives packaging technology"?

1.2. What are the four basic functions that an electronic package must provide? In addition to these functions, give four other desirable characteristics of an electronic package.

1.3. Define the six levels of packaging hierarchy.

1.4. Which level of the packaging hierarchy is relevant to MCMs and why?

1.5. What are the three primary types of die attach materials?

1.6. What are the three methods used to provide connections between an IC and the package that holds it?

1.7. Lid and pin sealing material must possess five important properties. What are they?

1.8. What three features of the dual-in-line package (DIP) helped it survive the package evolution and become the primary package used today?

1.9. What package feature distinguishes a flatpack from a DIP?

1.10. Describe the construction of a CerDIP.

1.11. What is the most attractive feature of a surface-mount package (SMP) and why is it important?

1.12. From an electrical performance point of view, what three advantages do PGA and BGA packages offer?

1.13. There are five broad classifications of BGA packages according to the form of the die carrier substrate material. What are they?

1.14. The BGA package is not susceptible to bent or skewed leads, but some aspects of BGA packages are of concern. What are they?

1.15. What five effects were created by the trend in the IC industry toward higher circuit densities and operating speeds that gave impetus to the development of MCM technology?

1.16. CSPs are generally defined as packages that are equal to or smaller than _____ times the base die size.

1.17. Thinning of ICs for 3D chip stacking has both positive and negative aspects. What are four positive aspects? What are five negative aspects?

1.18. What are six benefits of WLP?

1.19. What are some of the factors that relate performance and cost to packaging technology choices? Mention at least eight different factors.

1.20. Distinguish between manufacturing costs and manufacturability costs associated with packaging.

1.21. Leads from an IC to a package and from the package to the outside world deleteriously impact electrical signals in three ways. What are they?

1.22. What three electrical design factors must be considered in order to minimize the deleterious effects (from previous exercise) that packaging interconnects have on electrical signals?

1.23. Distinguish between in-process and stress testing of electronics packages. What factors must be considered at every testing point in the fabrication sequence?

1.24. What are some of the problems that must be addressed as packaging technology progresses? Consider at least ten problems.