CHAPTER ONE

Preliminary Concepts and More

In this chapter, some of the basic concepts and techniques used in this book are presented. The chapter is organized as follows:

- Various types of interconnections employed in very large scale integration (VLSI) applications are discussed in Section 1.1.
- Advantages and challenges posed by the copper interconnections and the techniques used for their fabrication are presented in Section 1.2.
- Method of images used to find the Green's function matrix in Chapter 2 is presented in Section 1.3.
- Method of moments used to determine the various interconnection capacitances in Chapter 2 is discussed in Section 1.4.
- Even- and odd-mode capacitances for two and three coupled conductors are discussed in Section 1.5.
- Transmission line equations are derived and coupled transmission lines are discussed in Section 1.6.
- Miller's theorem used to uncouple the coupled interconnections in Chapter 3 is presented in Section 1.7.
- A computer-efficient numerical inverse Laplace transformation technique used at several instances in this book is described in Section 1.8.
- A resistive interconnection has been modeled as a ladder network in Section 1.9.
- Various propagation modes that can exist in a microstrip interconnection are described in Section 1.10.
- A quasi–transverse electromagnetic (TEM) analysis of slow-wave mode propagation in interconnections is presented in Section 1.11.

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- Definitions of propagation delays used in the literature, including delay time and rise time, are presented in Section 1.12.

1.1 INTERCONNECTIONS FOR VLSI APPLICATIONS

Continuous advances in integrated circuit (IC) technology have resulted in smaller device dimensions, larger chip sizes, and increased complexity. There is an increasing demand for circuits with higher speeds and higher component densities. In recent years, growth of GaAs on silicon (Si) substrate has met with a great deal of interest because of its potential application in new hybrid technologies [1–11]. GaAs-on-Si unites the high-speed and optoelectronic capability of GaAs circuits with the low material cost and superior mechanical properties of the Si substrate. The heat sinking of such devices is better since the thermal conductivity of Si is three times more than that of GaAs. This technology is expanding rapidly from research to device and circuit development [12–15].

So far, the various IC technologies have employed metallic interconnections, and there is a possibility of using optical interconnections in the near future. Recently, the possibility of using superconducting interconnections is also being explored. Optical and superconducting interconnections are discussed in Chapter 6.

1.1.1 Metallic Interconnections: Multilevel, Multilayer, and Multipath Configurations

The VLSI chips require millions of closely spaced interconnection lines that integrate the components on a chip. As VLSI technology advanced to meet the needs of customers, it became necessary to use multilayer interconnections in two or more levels to achieve higher packing densities, shorter transit delays, and smaller chips. In this book, the term *level* will be used to describe conductors which are separated by an insulator and the term *layer* to describe different conductors tiered together in one level of interconnection, as shown in Fig. 1.1.1. In most cases, because of its low resistivity and silicon compatibility as shown in Table 1.1.1 [16], aluminum has been used to form metal interconnections. However, as device dimensions are decreased, current density increases, resulting in decreased reliability due to electromigration and hillock formation causing electrical shorts between successive levels of Al [17–20]. Tungsten has also been used for interconnects [21–23] and, sometimes, Al/Cu is used to solve problems characteristic of pure Al [1.24] though this choice has not been without problems [25, 26]. There have been several studies [27–34] aimed at reducing electromigration. All these studies have used layers of two or more metals in the same level of the interconnection. Some of the multilayer structures studied so far have been Al/Ti/Cu [28], Al/Ta/Al [30], Al/Ni [31], Al/Cr [32], Al/Mg [33], and Al/Ti/Si [34]. Coevaporation of Al–Cu–Ti, Al–Cu–Ti, Al–Cu–Co, and Al–Co has also been shown to decrease electromigration [27]. There

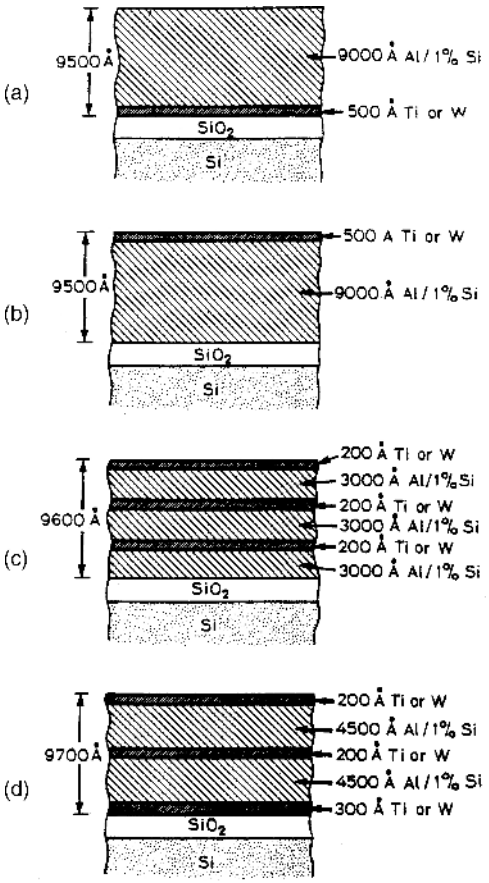


FIGURE 1.1.1 Schematic of layered interconnection structures using (*a*) Ti layer used to match aluminum and silicon expansion coefficients; (*b*) Ti or W layer on top of aluminum to constrain hillocks; (*c*, *d*) multiple layers of Ti or W alternated with aluminum.

have been many studies on the problem of hillock formation as well [16, 35–44]. One method of reducing these hillocks on silicon-based circuits has been to deposit a film of WSi [36] or MoSi between Al and the silicon substrate. Complete elimination of hillocks is reported in studies where the VLSI interconnections were fabricated by layering alternately Al and a refractory metal (Ti or W) [16, 42–44].

Recently, in an attempt to solve the ''interconnect problem,'' that is, the problem of unprecedented high density of interconnections operating at extremely high speeds and carrying high current densities, a modified version of the traditional metallic interconnection called the ''multipath interconnect'' has been proposed [45]. The modified interconnection consists of using the concept of parallel processing by providing two or more paths between the driving gate and the loading

TABLE 1.1.1 Resistivity and Expansion Coefficients

Material	Resistivity ($\mu\Omega \cdot$cm)	Thermal Expansion Coefficient ($^\circ C^{-1}$)	Melting Point ($^\circ$C)
Pure aluminum (bulk)	2.65	25.0×10^{-6}	660
Sputtered Al and Al/Si	2.9–3.4	25.0×10^{-6}	660
Sputtered Al/2% Cu/1% Si	3.9	25.0×10^{-6}	660
LPCVD aluminum	3.4	25.0×10^{-6}	660
Pure tungsten (bulk)	5.65	4.5×10^{-6}	3410
CVD tungsten	7–15	4.5×10^{-6}	3410
Evaporated/sputtered tungsten	14–20	4.5×10^{-6}	3410
Ti (bulk)	42.0	8.5×10^{-6}	1660
$TiAl_3$ (bulk)	17–22	—	1340
$CuAl_2$ (bulk–θ phase)	5–6	—	591
WAl_{12}	—	—	647
Si	—	3.3×10^{-6}	—
SiO_2	—	0.5×10^{-6}	—

Source: From [16]. © 1985, by IEEE.

gate. A schematic of a three-section multipath interconnect (side view) connecting the driver and the load is shown in Fig. 1.1.2. These paths are stacked vertically isolated from one another by insulating layers between any two consecutive paths thereby taking the same area on the chip as a single-path interconnect. Depending on the number of paths, an array of such multipath interconnects could carry much higher currents on the chip. Furthermore, this interconnect structure could be built by an extension of the available microelectronics fabrication techniques.

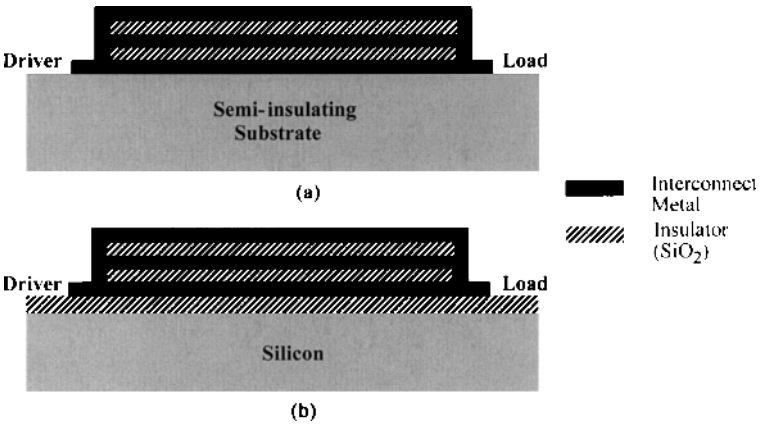


FIGURE 1.1.2 Schematic of three-path multipath interconnection (side view) connecting driver and load on (*a*) semi-insulating substrate such as GaAs and (*b*) silicon substrate.

1.1.2 Optical Interconnections

As an alternative to electrical interconnections, optical interconnections have emerged in recent years which offer fast, reliable, and noise-free data transmission [46–50]. So far, they have been used for computer-to-computer communications and processor-to-processor interconnections. At this time, however, their applicability at lower levels of the packaging hierarchy, such as for module-to-module connections at the board level, chip-to-chip connections at the module level, and gate-to-gate connections at the chip level, is still under investigation. The principal advantages of optical interconnections over electrical connections are higher bandwidth, lower dispersion, and lower attenuation. Some of the problems with optical interconnections under investigation are size incompatibility with ICs, high power consumption, and tight alignment requirements.

1.1.3 Superconducting Interconnections

In recent years, the advent of high-critical-temperature superconductors has opened up the possibility of realizing high-density and very fast interconnections on silicon- as well as GaAs-based high-performance ICs. The major advantages of superconducting interconnections over normal metal interconnections can be summarized as follows: (a) Signal propagation time on a superconducting interconnection will be much smaller as compared to that on a normal metal interconnection, (b) the packing density of the IC can be increased without suffering from the high losses associated with high-density normal metal interconnections, and (c) there is virtually no signal dispersion on superconducting interconnections for frequencies up to several tens of gigahertz.

1.2 COPPER INTERCONNECTIONS

To be able to produce high-speed ICs, it is always desirable to use interconnections that would allow rapid transmission of information, that is, signals among the various components on the chip. For the last 40 years, aluminum has been used almost exclusively to make metallic interconnection lines on ICs. More recently, aluminum–copper alloys have been used because they have been shown to provide better reliability than pure aluminum. In December 1997, in order to lower the resistance of metallic interconnections, IBM announced plans to replace aluminum with copper, a metal with lower resistivity of less than 2 $\mu\Omega \cdot$ cm compared to that of about 3 $\mu\Omega \cdot$ cm for aluminum. It is worth mentioning that while copper interconnections have been a hot topic in the semiconductor industry since the IBM announcement, the race to improve the aluminum interconnect technology has not slowed down. In fact, semiconductor companies are exploring new technologies for aluminum-based interconnections. These include ionized plasma deposition, hot aluminum physical vapor deposition (PVD), and aluminum damascene structures. It is expected that while advanced microprocessors and fast memory circuits may

switch to copper interconnections, aluminum-based interconnections deposited by using the latest techniques will continue to coexist at least in the near future.

While the semiconductor industry has known the potential advantages of using copper interconnects since the 1960s, it took over 30 years for it to overcome the associated challenges until it was announced in a paper on the complementary metal–oxide–semiconductor (CMOS) 7S technology presented at the Institute of Electrical and Electronics Engineers' IEDM conference by IBM in December 1997. Following is a summary of the advantages of copper interconnects and the challenges in implementing this technology:

1.2.1 Advantages of Copper Interconnects

1. An obvious advantage of copper is its lower electrical resistivity compared with aluminum. In fact, copper interconnects offer 40% less resistance to electrical conduction than the corresponding aluminum interconnects, which results in speed advantages of as much as 15% in microprocessor circuits employing copper interconnects.
2. The phenomenon of electromigration that results in the movement of atoms and molecules in the interconnects under high-stress conditions of high temperatures and high current densities causing open- and short-circuit failures of interconnects through the formation of voids and hillocks is known to occur much less frequently in copper interconnects than in aluminum interconnects. That is why aluminum–copper alloys have been preferred over pure aluminum as the interconnect material.
3. Copper interconnects can be fabricated with widths in the range of 0.2 μm while it has been difficult to reduce dimensions below 0.35 μm with aluminum interconnects. This reduction in interconnection dimensions allows much higher packing densities of the order of 200 million transistors per chip.
4. It has been claimed that the deposition of copper interconnects can be achieved with a potential cost saving of up to 30%, which translates into a saving of about 10–15% for the full wafer [51].

1.2.2 Challenges Posed by Copper Interconnects

In the United States, a consortium of 10 leading chip-making semiconductor companies known as SEMATECH (Semiconductor Manufacturing Technology) has worked hard to overcome the challenges posed by the replacement of aluminum interconnects by copper interconnects. Following is a list of technical challenges that must be addressed and met within acceptable standards to fabricate copper-based IC chips [52]:

1. Copper is considered poisonous for silicon-based circuits. It diffuses rapidly into the active source, drain, and gate regions of transistors built on the silicon

substrate and alters their electrical properties affecting the functionality of the transistors.

2. In order to meet the above challenge alone, an entirely new fabrication process is required for implementation of copper interconnects.
3. Fabrication of copper interconnects requires the production and use of a large amount of ultrapure water, which is rather expensive.
4. The release of waste discharges containing copper to the environment must be handled very carefully.

1.2.3 Fabrication Processes for Copper Interconnects

As shown in Fig. 1.2.1, a conventional photolithographic process for depositing aluminum interconnects on the silicon substrate involves the following steps:

1. Deposit a layer of silicon dioxide insulator on the silicon wafer.
2. Deposit a layer of metal on the silicon dioxide layer.
3. Cover the metal layer by depositing a layer of photoresist on it.
4. Project a shadow of the interconnect pattern (drawn on a reticle) on the photoresist layer by using ultraviolet rays and an optical projection system.
5. Develop the photoresist that was exposed to the ultraviolet light.

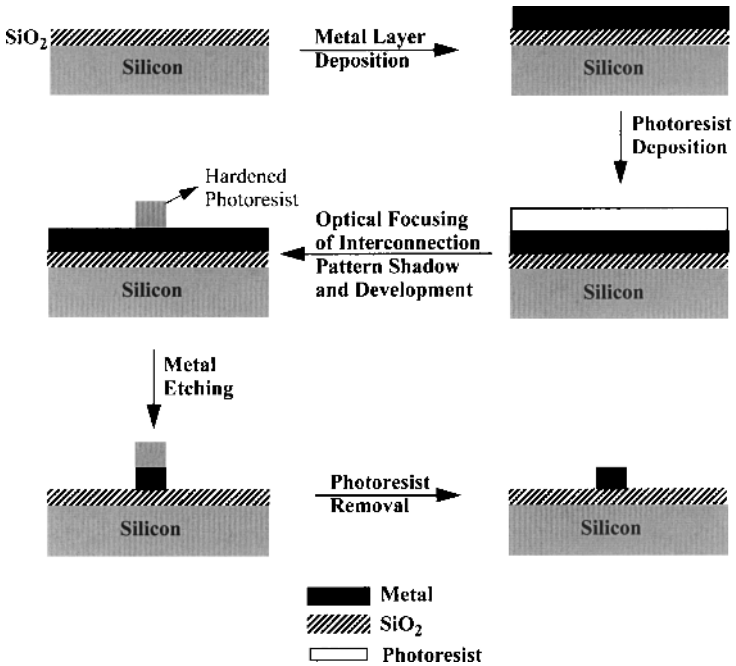


FIGURE 1.2.1 Conventional photolithographic process steps for depositing aluminum metallization on silicon substrate.

6. Using proper chemicals, etch away parts of the metal layer that are not covered by the hardened photoresist.
7. Finally, remove the hardened photoresist, leaving the interconnect metal in the desired pattern on the silicon dioxide layer.

Since copper can contaminate the silicon substrate and the silicon dioxide dielectric layer of an IC resulting in increased junction leakages and threshold voltage instabilities, barrier layers are required to isolate the copper interconnects from the substrate and the dielectric layer. The barrier layer, usually made from tungsten or titanium nitride, should be as thin as possible to minimize the resistance and to maximize the reliability of the copper interconnects. It is applied after the interconnect channels have been etched out in the dielectric layer by photolithography. The barrier layer is covered by a microscopic seed layer of copper to ease further deposition of copper on the entire wafer by electroplating. Finally, the excess copper is removed by a chemical–mechanical polishing process leaving the desired pattern of copper interconnects on the wafer. The various steps are shown in Fig. 1.2.2.

Various techniques have been studied for deposition of copper interconnects on silicon-based circuits. These include chemical vapor deposition (CVD), electroless plating, and electrolytic plating [51]. In each case, the objective was to deposit very thin and even layers of copper interconnects in the horizontal direction and vias in

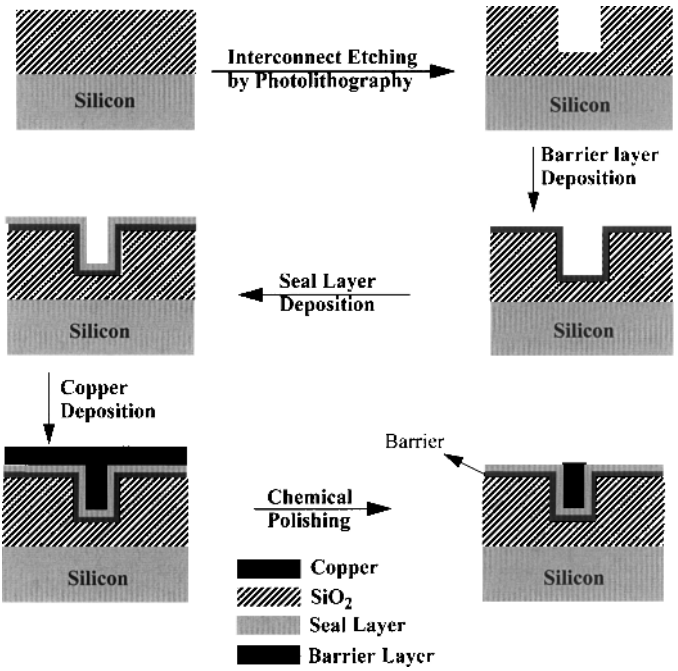


FIGURE 1.2.2 Various steps involved in depositing copper metallizations.

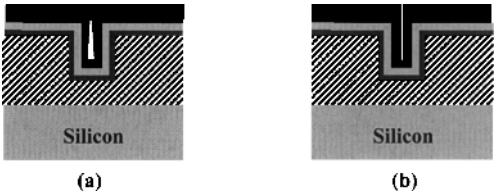


FIGURE 1.2.3 Schematic of (*a*) voids and (*b*) seams that may be formed during late stages of copper deposition.

the vertical direction for connecting interconnects in different levels. It was found that the CVD and electroless plating techniques encountered several problems during fabrication whereas electrolytic plating worked satisfactorily, resulting in even copper films with a faster rate of deposition.

1.2.4 Damascene Processing of Copper Interconnects

At present, the damascene electroplating process is used frequently to make copper on-chip interconnects. The term ''damascene'' originates from the fact that a

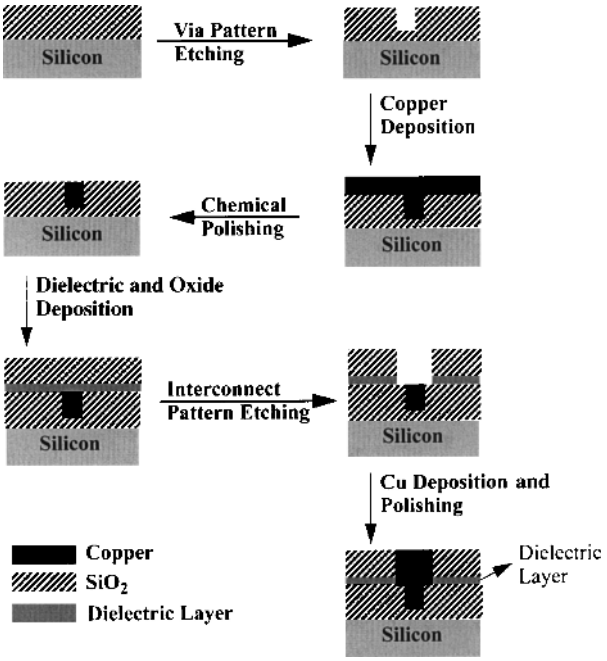


FIGURE 1.2.4 Steps involved in depositing copper interconnections and vias using single-damascene process.

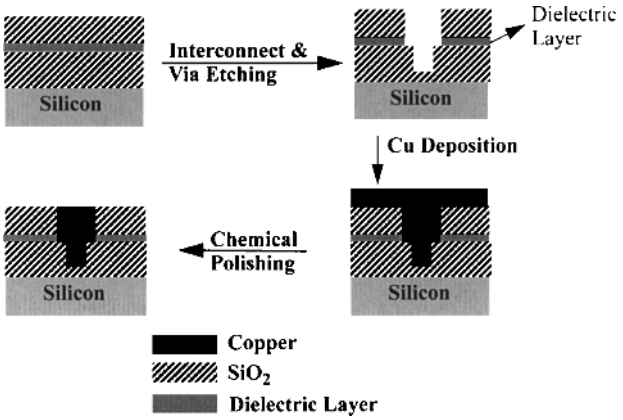


FIGURE 1.2.5 Steps involved in depositing copper interconnections and vias using dual-damascene process.

somewhat similar technique was used by the metallurgists of old Damascus to produce sharpest polished swords in the medieval era. In the world of semiconductor processing, this technique was initially used to form vias that are used to connect interconnects at different levels of an IC.

In damascene processing, the patterns of interconnects or vias are formed first by etching the oxide on the substrate. Then the seed layer is deposited on the patterned substrate/oxide. This is followed by copper electroplating which deposits inside and outside the patterned features. Special care is taken to avoid the formation of voids and seams (shown in Fig. 1.2.3) during the late stages of copper deposition. The excess copper is finally removed by the chemical–mechanical planarization process. The steps involved in making copper interconnects using the damascene process are shown in Fig. 1.2.4. This process is repeated several times to form interconnects and vias for a multilevel interconnect structure required on an IC chip.

The process described above is called the ''single'' damascene process because it differs from the more widely used ''dual'' damascene process in which both the interconnects and the vias are first patterned by etching of the substrate/oxide before the seed layer is formed and copper is deposited. It reduces the number of processing steps by avoiding one copper deposition step and one planarization step for each level of the interconnect structure. The steps involved in making copper interconnects using the dual damascene process are shown in Fig. 1.2.5.

1.3 METHOD OF IMAGES

The method of images can be used to find the potential due to a given electric charge in the presence of conducting planes and dielectric surfaces. To illustrate this

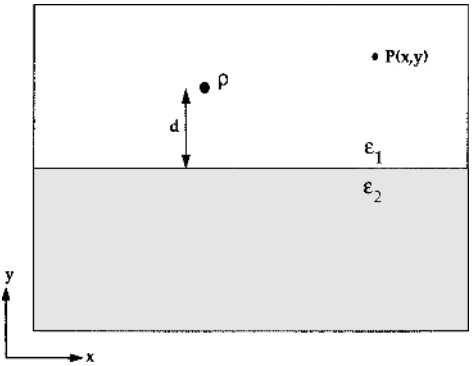


FIGURE 1.3.1 Line charge ρ lying in medium of dielectric constant ε_1 at distance d above second medium of dielectric constant ε_2.

method, let us consider a line charge ρ lying in a medium of dielectric constant ε_1 and at a distance d above a second medium of dielectric constant ε_2, as shown in Fig. 1.3.1. At the interface of the two media, the following two boundary conditions must be satisfied:

1. The normal component of the electric flux density (D_n) is the same on the two sides of the interface.
2. The tangential component of the electric field (E_t) is also the same across the interface.

Using the coordinate system of Fig. 1.3.1, it means that at $y = 0$

$$D_{n1} = D_{n2} \qquad \text{or} \qquad \varepsilon_1 E_{y1} = \varepsilon_2 E_{y2} \tag{1.3.1}$$

and

$$E_{x1} = E_{x2} \tag{1.3.2}$$

The potential V due to an infinite line charge (ρ) in a medium of dielectric constant ε at a distance r is given by

$$V = \frac{-\rho}{4\pi\varepsilon} \ln(r^2) \tag{1.3.3}$$

When a second dielectric is present, the real charge ρ produces image charges across the dielectric interface. If the observation point P is above the interface, that is, on the same side as the real line charge (see Fig. 1.3.2*a*), an image charge ρ_1 will be at a distance d below the interface. With the real line charge at $x = 0$ and $y = d$,

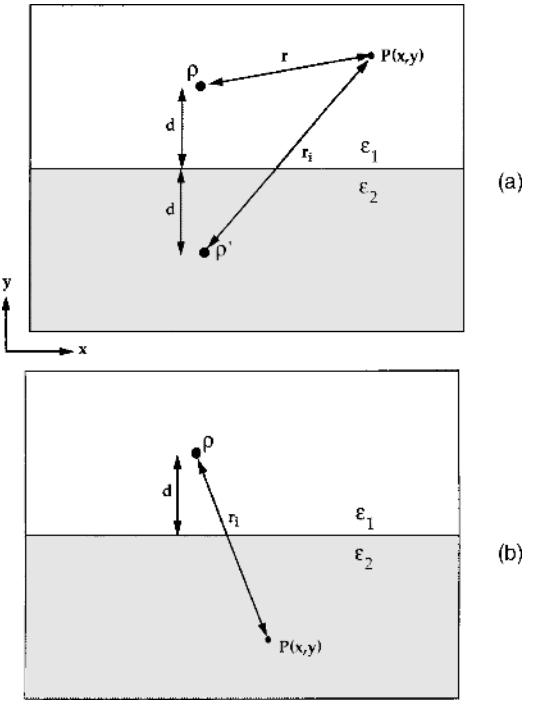


FIGURE 1.3.2 (*a*) Observation point P on same side as real line charge. (*b*) Observation point P below dielectric interface.

the distance between the real charge and the observation point is given by

$$r = \sqrt{x^2 + (y-d)^2}$$

and with the image charge at $x = 0$ and $y = -d$, the distance between the image charge and the observation point is given by

$$r_i = \sqrt{x^2 + (y+d)^2}$$

Using Eq. (1.3.3), the potential at all points above the interface, that is, for $y \geq 0$, will be

$$V_1 = -\frac{1}{4\pi\varepsilon_1}[\rho \ln(r^2) + \rho_1 \ln(r_i^2)]$$

Now since

$$E_{x1} = -\frac{\partial V_1}{\partial x}$$

for $y \geq 0$

$$E_{x1} = \frac{1}{4\pi\varepsilon_1}\frac{\partial}{\partial x}\{\rho \ln[x^2 + (y-d)^2] + \rho_1 \ln[x^2 + (y+d)^2]\}$$

or

$$E_{x1} = \frac{1}{4\pi\varepsilon_1}\left[\rho\frac{2x}{x^2 + (y-d)^2} + \rho_1\frac{2x}{x^2 + (y+d)^2}\right] \tag{1.3.4}$$

Similarly

$$E_{y1} = -\frac{\partial V_1}{\partial y}$$

Therefore, for $y \geq 0$

$$E_{y1} = \frac{1}{4\pi\varepsilon_1}\frac{\partial}{\partial y}\{\rho \ln[x^2 + (y-d)^2] + \rho_1 \ln[x^2 + (y+d)^2]\}$$

or

$$E_{y1} = \frac{1}{4\pi\varepsilon_1}\left[\rho\frac{2(y-d)}{x^2 + (y-d)^2} + \rho_1\frac{2(y+d)}{x^2 + (y+d)^2}\right] \tag{1.3.5}$$

If the observation point P lies below the dielectric interface, that is, in the medium with dielectric constant ε_2 (see Fig. 1.3.2*b*), then the real line charge ρ must be modified to take care of the effect of the dielectric interface. This modified charge, say ρ_2, can be found in terms of ρ as shown below. The distance between the observation point and the charge ρ is again given by

$$r = \sqrt{x^2 + (y-d)^2}$$

The potential V_2 below the interface is then given by

$$V_2 = \frac{-1}{4\pi\varepsilon_2}[\rho_2 \ln(r^2)]$$

Now, since

$$E_{x2} = -\frac{\partial V_2}{\partial x}$$

for $y \leq 0$

$$E_{x2} = \frac{1}{4\pi\varepsilon_2}\frac{\partial}{\partial x}\{\rho_2 \ln[x^2 + (y-d)^2]\}$$

or

$$E_{x2} = \frac{1}{4\pi\varepsilon_2}\left[\rho_2 \frac{2x}{x^2 + (y-d)^2}\right] \tag{1.3.6}$$

Similarly

$$E_{y2} = -\frac{\partial V_2}{\partial y}$$

Therefore, for $y \leq 0$

$$E_{y2} = \frac{1}{4\pi\varepsilon_2}\frac{\partial}{\partial y}\{\rho_2 \ln[x^2 + (y-d)^2]\}$$

or

$$E_{y2} = \frac{1}{4\pi\varepsilon_2}\left[\rho_2 \frac{2(y-d)}{x^2 + (y-d)^2}\right] \tag{1.3.7}$$

Applying the continuity condition (1.3.2) to Eqs. (1.3.4) and (1.3.6), we get

$$\frac{1}{4\pi\varepsilon_1}[\rho + \rho_1]\left[\frac{2x}{x^2 + d^2}\right] = \frac{\rho_2}{4\pi\varepsilon_2}\left[\frac{2x}{x^2 + d^2}\right]$$

From this, it follows that

$$\frac{\rho + \rho_1}{\varepsilon_1} = \frac{\rho_2}{\varepsilon_2} \tag{1.3.8}$$

Applying the continuity condition (1.3.1) to Eqs. (1.3.5) and (1.3.6), we find that

$$\frac{\varepsilon_1}{4\pi\varepsilon_1}(-\rho + \rho_1)\left[\frac{2d}{x^2 + d^2}\right] = \frac{\varepsilon_2\rho_2}{4\pi\varepsilon_2}\left[\frac{-2d}{x^2 + d^2}\right]$$

from which it follows that

$$-\rho + \rho_1 = -\rho_2 \tag{1.3.9}$$

Combining Eqs. (1.3.8) and (1.3.9), we get

$$\frac{\rho + \rho_1}{\varepsilon_1} = \frac{\rho - \rho_1}{\varepsilon_2}$$

from which the image charges ρ_1 and ρ_2 can be found in terms of the real charge ρ and the dielectric constants ε_1 and ε_2 to be

$$\rho_1 = \rho\left(\frac{\varepsilon_1 - \varepsilon_2}{\varepsilon_1 + \varepsilon_2}\right) \tag{1.3.10}$$

$$\rho_2 = \rho\left(\frac{2\varepsilon_2}{\varepsilon_1 + \varepsilon_2}\right) \tag{1.3.11}$$

To find the image of a charge in a grounded conducting plane, it is well known that the image charge has the same magnitude as the real charge but an opposite sign and that it lies as much below the ground plane as the real charge is above it.

1.4 METHOD OF MOMENTS

The method of moments is a basic mathematical technique for reducing functional equations to the matrix equations [53]. Consider the inhomogenous equation

$$L(f) = g \tag{1.4.1}$$

where L is a linear operator, f is a field or response (the unknown function to be determined), and g is a source or excitation (a known function). We assume that the problem is deterministic, that is, there is only one solution function f associated with a given excitation g.

Let us expand the function f in a series of basis functions $f_1, f_2, f_3, \ldots, f_n$ in the domain of L as

$$f = \sum_n \alpha_n f_n \tag{1.4.2}$$

where the α_n are constants. The functions f_n are called expansion functions or the basis functions. For exact solutions, Eq. (1.4.2) is usually an infinite summation and the functions f_n form a complete set of basis functions. For approximate solutions, Eq. (1.4.2) is usually a finite summation. Substituting Eq. (1.4.2) into Eq. (1.4.1) and using the linearity of the operator L, we have

$$\sum_n \alpha_n L(f_n) = g \tag{1.4.3}$$

Now, defining a set of weighting functions or testing functions $w_1, w_2, w_3, \ldots$ in the range of L and taking the inner product with each w_m, the result is

$$\sum_n \alpha_n \langle w_m, Lf_n \rangle = \langle w_m, g \rangle \qquad m = 1, 2, 3, \ldots$$

This set of equations can be written in matrix form as

$$[l_{mn}][\alpha_n] = [g_m]$$

where

$$[l_{mn}] = [\langle wm, Lf_n \rangle]$$

and $[\alpha_n]$ and $[g_m]$ are column vectors. If the matrix $[l_{mn}]$ is nonsingular, then the matrix $[l_{mn}]^{-1}$ exists. The constants α_n are then given by

$$[\alpha_n] = [l_{mn}]^{-1}[g_m]$$

and the solution function f is given by Eq. (1.4.2) as

$$f = \sum_n \alpha_n f_n = [l_{mn}]^{-1}[g_m][f_n]$$

This solution may be exact or approximate depending upon the choice of functions f_n and weighting functions w_n. The particular choice $w_n = f_n$ is known as the Galerkin method. If the matrix $[l_{mn}]$ is of infinite order, it can be solved only in special cases, for example, if it is diagonal. If the sets f_n and w_n are finite, then the matrix $[l_{mn}]$ is of finite order and can be inverted by known methods such as the Gauss–Jordan reduction method.

In most problems of practical interest, the integration involved in evaluating $l_{mn} = \langle w_m, Lf_n \rangle$ is usually difficult to perform. A simple way to obtain approximate solutions is to require that Eq. (1.4.3) be satisfied at certain discrete points in the region of interest. This process is called a point-matching method. In terms of the method of moments, it is equivalent to using Dirac delta functions as the weighting functions. Another approximation useful for practical problems involves dividing the region of interest into several small subsections and requiring that the basis functions f_n are constant over the areas of the subsections. This procedure, called the method of subsections, often simplifies the evaluation of the matrix $[1_{mn}]$. Sometimes, it is more convenient to use the method of subsections in conjunction with the point-matching method.

One of the most important tasks in any particular problem is the proper choice of the functions f_n and w_n. The functions f_n should be linearly independent and chosen so that some superposition (1.4.3) can approximate the function f reasonably accurately. The functions w_n should also be linearly independent and chosen so that

the products $\langle w_n, g \rangle$ depend on the relative independent properties of g. Some additional considerations while choosing the functions f_n and w_n are accuracy of the solution desired, ease of evaluation of the matrix elements, size of the matrix that can be inverted, and realization of a well-conditioned matrix.

1.5 EVEN- AND ODD-MODE CAPACITANCES

In this section, the even- and odd-mode capacitances associated with systems of two or three coupled conductors are discussed.

1.5.1 Two Coupled Conductors

Two coupled conductors of different dimensions lying in the same plane at a distance d above the ground plane are shown in Fig. 1.5.1. We are interested in finding the self and mutual (or coupling) capacitances for this system. In other words, we want to find the capacitances between each conductor and the ground (denoted by C_{11} and C_{22}) and the capacitance between the two conductors (denoted by C_{12}). To simplify the analysis, the problem can be split into the even and odd modes. In the even mode, each conductor is assumed to be at 1 V potential with the same sign for each conductor. In the odd mode, the first conductor is assumed to be at a $+1$ V potential while the second conductor is kept at a -1 V potential. First, we will determine the even- and odd-mode capacitances for each conductor separately.

In the even mode shown in Fig. 1.5.2, there are no electric field lines at the center between the two conductors. Therefore, this plane can be treated as a magnetic wall which represents an open circuit to any mutual capacitance between the two

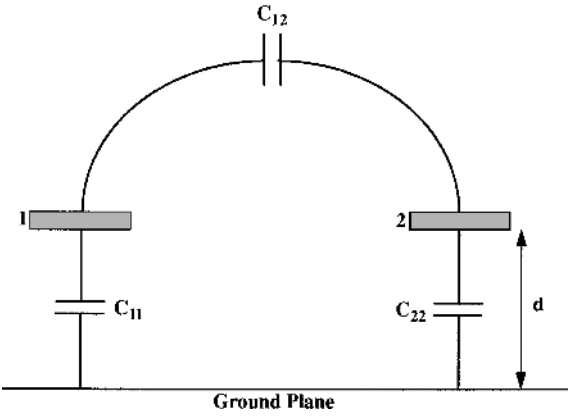


FIGURE 1.5.1 Two coupled conductors of different dimensions lying in same plane at distance d above ground plane.

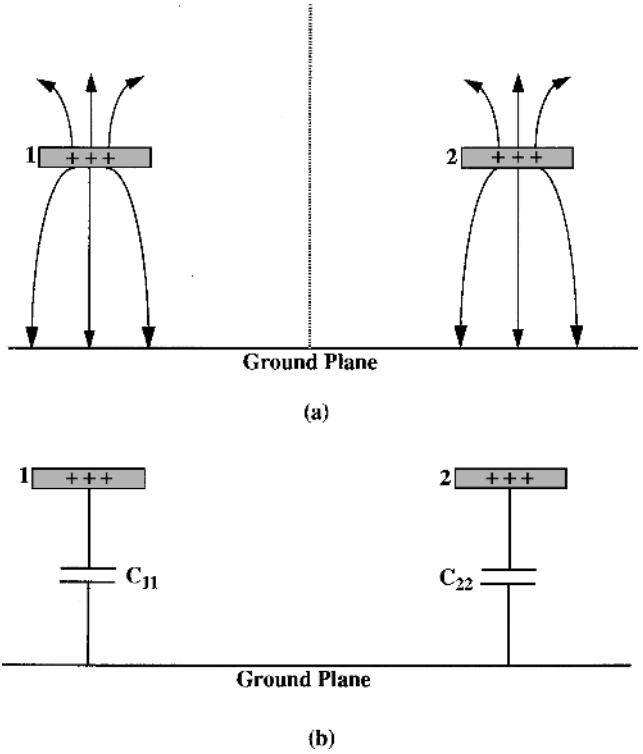


FIGURE 1.5.2 (*a*) Electric field lines for two conductors in even mode. (*b*) Equivalent circuit for two conductors in even mode.

conductors. Therefore, we can say that

$$C_1^{(e)} = C_{11} \tag{1.5.1}$$

$$C_2^{(e)} = C_{22} \tag{1.5.2}$$

where $C_1^{(e)}$ is the even-mode capacitance for the first conductor while $C_2^{(e)}$ is that for the second conductor.

In the odd mode shown in Fig. 1.5.3, the plane of symmetry between the two conductors can be treated as a grounded electric wall. This represents a short circuit to the mutual capacitance C_{12}. Therefore, in this case

$$C_1^{(o)} = C_{11} + 2C_{12} \tag{1.5.3}$$

$$C_2^{(o)} = C_{22} + 2C_{12} \tag{1.5.4}$$

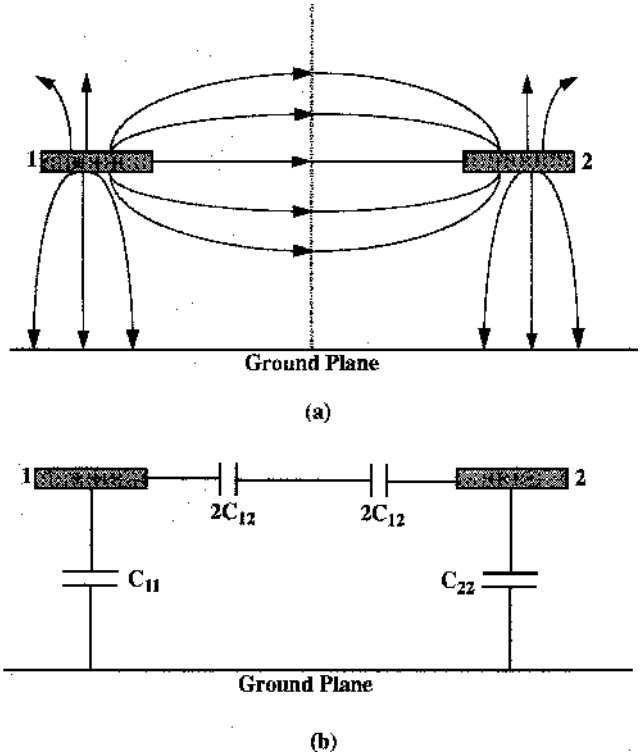


FIGURE 1.5.3 (*a*) Electric field lines for two conductors in odd mode. (*b*) Equivalent circuit for two conductors in odd mode.

where $C_1^{(o)}$ and $C_2^{(o)}$ are the odd-mode capacitances for the first and second conductors, respectively. The mutual capacitance C_{12} can be expressed in terms of $C_1^{(o)}$ and $C_1^{(e)}$ using Eqs. (1.5.1) and (1.5.3) as

$$C_{12} = \tfrac{1}{2}\left[C_1^{(o)} - C_1^{(e)}\right]$$

while the self-capacitances are given by Eqs. (1.5.1) and (1.5.2).

1.5.2 Three Coupled Conductors

As in the case of two conductors, the three-conductor case can also be treated by splitting it into the even and odd modes. In the even mode, each conductor is again assumed to be at a $+1$ V potential. In the odd mode, one conductor is kept at a $+1$ V potential while the other two conductors are assumed to be at -1 V potential. This means that when finding the odd-mode charge on the first conductor, for example, the potentials on the second and third conductors are of the opposite sign to that on

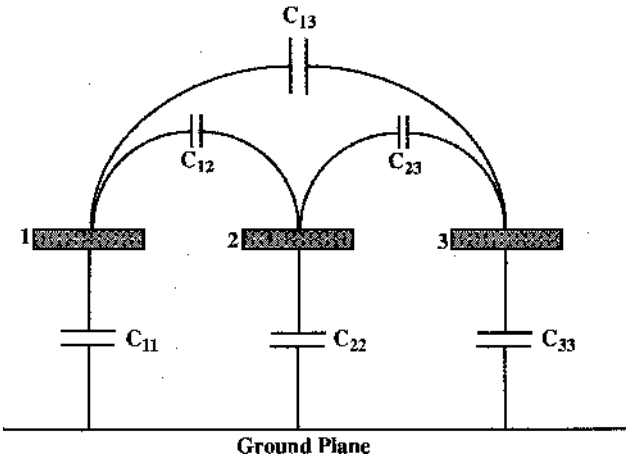


FIGURE 1.5.4 Self- and mutual capacitances for three conductors.

the first conductor. Figure 1.5.4 shows the self and mutual capacitances for the three conductors. These capacitances can be found in terms of the even- and odd-mode capacitances of the three conductors. In the even mode,

$$C_1^{(e)} = C_{11} \qquad C_2^{(e)} = C_{22} \qquad C_3^{(e)} = C_{33} \tag{1.5.5}$$

In the odd mode,

$$\begin{aligned} C_1^{(o)} &= C_{11} + 2C_{12} + 2C_{13} \\ C_2^{(o)} &= C_{22} + 2C_{12} + 2C_{23} \\ C_3^{(o)} &= C_{33} + 2C_{13} + 2C_{23} \end{aligned} \tag{1.5.6}$$

Solving these equations, we can find that the mutual capacitances are given by

$$\begin{aligned} C_{12} &= \tfrac{1}{4}[-C_1^{(e)} - C_2^{(e)} + C_3^{(e)} + C_1^{(o)} + C_2^{(o)} - C_3^{(o)}] \\ C_{13} &= \tfrac{1}{4}[-C_1^{(e)} + C_2^{(e)} - C_3^{(e)} + C_1^{(o)} - C_2^{(o)} + C_3^{(o)}] \\ C_{23} &= \tfrac{1}{4}[C_1^{(e)} - C_2^{(e)} - C_3^{(e)} - C_1^{(o)} + C_2^{(o)} + C_3^{(o)}] \end{aligned} \tag{1.5.7}$$

The self-capacitances are given by Eqs. (1.5.5).

1.6 TRANSMISSION LINE EQUATIONS

A transmission line can be treated as a repeated array of small resistors, inductors, and capacitors. In fact, the transmission line theory can be developed in terms of alternating current (AC) circuit analysis, but the equations become extremely complicated for all but the simple cases [54]. It is more convenient to treat such lines in terms of differential equations which lead naturally to a wave equation which is of fundamental importance to electromagnetic theory in general.

We can develop the differential equations for a uniform transmission line by a simple circuit analysis of its equivalent circuit, shown in Fig. 1.6.1, consisting of several incremental lengths and then taking the limit as the length of the increment approaches zero. The notations of voltage and current at some general points x and $x + \Delta x$ along the line are shown in Fig. 1.6.1. The parameters R, L, G, and C are the resistance, inductance, conductance, and capacitance values per unit length of the line, respectively. As Δx is changed, these values remain the same. We assume that the voltage and current are sinusoidal and that at any point x along the line the time variation of voltage is given by

$$v_x = v_0 e^{j\omega t}$$

Now, if we apply Kirchhoff's voltage law around the first incremental loop in Fig. 1.6.1, we obtain

$$v_x = i_x\, R\, \Delta x + i_x(j\omega L)\, \Delta x + v_{x+\Delta x}$$

or

$$v_{x+\Delta x} - v_x = -i_x(R + j\omega L)\, \Delta x \tag{1.6.1}$$

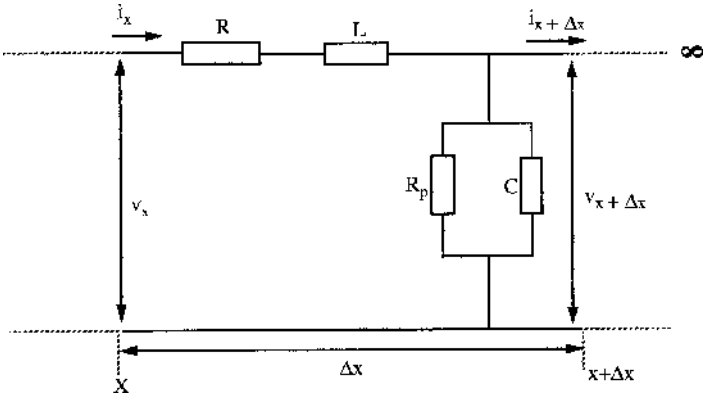


FIGURE 1.6.1 Equivalent circuit for uniform transmission line.

In the above equations, R and L have been multiplied by Δx to get the actual values of resistance and inductance for an incremental section of length Δx. Now, the total current i_x into the first incremental section at x minus the total current $i_{x+\Delta x}$ into the next section at $x + \Delta x$ must be equal to the total current through the shunt capacitance C and the parallel resistance R_p, that is,

$$i_x - i_{x+\Delta x} = \frac{v_x}{R_p/\Delta x} + \frac{v_x}{1/(j\omega C \Delta x)}$$

or, setting $1/R_p = G$, the conductance per unit length, we get

$$i_{x+\Delta x} - i_x = -v_x(G + j\omega C)\ \Delta x \tag{1.6.2}$$

In Eq. (1.6.1), the left-hand side represents the incremental voltage drop along the line denoted by Δv_x. Dividing both sides of Eq. (1.6.1), we get

$$\frac{\Delta v_x}{\Delta x} = -i_x(R + j\omega L)$$

Similarly, Eq. (1.6.2) can be expressed as

$$\frac{\Delta i_x}{\Delta x} = -v_x(G + j\omega C)$$

Now, if Δx is made very very small, then the incremental voltage or current change per incremental distance becomes the corresponding derivative. Thus we get the two fundamental differential equations for a uniform transmission line,

$$\frac{dv_x}{dx} = -(R + j\omega L)i_x \tag{1.6.3}$$

$$\frac{di_x}{dx} = -(G + j\omega C)v_x \tag{1.6.4}$$

where all line parameters are per unit distance. These equations can be solved if they can be written in terms of one unknown (v_x or i_x). An equation in terms of v_x can be written by first taking the derivative of Eq. (1.6.3) with respect to x to yield

$$\frac{d^2v_x}{dx^2} = -(R + j\omega L)\frac{di_x}{dx} \tag{1.6.5}$$

and then substituting Eq. (1.6.4) in Eq. (1.6.5) to get

$$\frac{d^2v_x}{dx^2} = (R + j\omega L)(G + j\omega C)v_x = \gamma^2 v_x \tag{1.6.6}$$

where

$$\gamma^2 = (R + j\omega L)(G + j\omega C) \tag{1.6.7}$$

Similarly, an equation in terms of i_x can be obtained by first differentiating Eq. (1.6.4) and then substituting Eq. (1.6.3) to yield

$$\frac{d^2 i_x}{dx^2} = (R + j\omega L)(G + j\omega C) i_x = \gamma^2 i_x \tag{1.6.8}$$

Equations (1.6.6) and (1.6.8) are the fundamental relationships governing wave propagation along a uniform transmission line.

The symbol γ as defined by Eq. (1.6.7) is known as the propagation constant, that is,

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)}$$

In general, γ is a complex number. The real part of γ gives the reduction in voltage or current along the line. This quantity, when expressed per unit length of the line, is referred to as the attenuation constant α given by

$$\alpha = \mathrm{Re}\sqrt{(R + j\omega L)(G + j\omega C)}$$

For a transmission line with no losses, $\alpha = 0$, that is, a line with no losses has no attenuation. The imaginary part of γ, when expressed per unit length of the line, is known as the phase constant β given by

$$\beta = \mathrm{Im}\sqrt{(R + j\omega L)(G + j\omega C)}$$

For a lossless line where $R = G = 0$, the phase constant becomes

$$\beta = \omega\sqrt{LC}$$

with dimensions of radians per meter in rationalized meter–kilogram–second (RMKS) units. Phase shift per unit length along the line is a measure of the velocity of propagation of a wave along the line, that is,

$$v = \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}}$$

1.7 MILLER'S THEOREM

Miller's theorem is an important theorem which can be used to uncouple nodes in electric circuits. Consider a circuit configuration with N distinct nodes 1, 2, 3,. . ., N

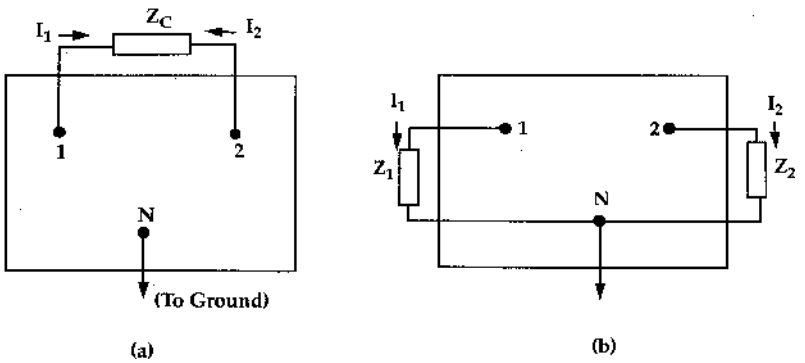


FIGURE 1.7.1 (*a*) Circuit configuration with N distinct nodes. (*b*) Circuit configuration equivalent to that shown in Fig. 1.7.1*a*.

as shown in Fig. 1.7.1*a*. The node voltages can be denoted by V_1, V_2, V_3,. . ., V_N, where V_N is zero because N is the reference node. Nodes 1 and 2 are connected by an impedance Z_c. We assume that the ratio V_2/V_1 is known or can be determined by some means. Let us denote this ratio by K, which, in general, can be a complex number.

It can be shown that the configuration shown in Fig. 1.7.1*a* is equivalent to that shown in Fig. 1.7.1*b* provided Z_1 and Z_2 have certain specific values. These values of Z_1 and Z_2 can be found by equating the currents leaving nodes 1 and 2 in the two configurations. The current I_1 leaving node 1 through impedance Z_c in configuration (*a*) is given by

$$I_1 = \frac{V_1 - V_2}{Z_c} = V_1 \frac{1 - K}{Z_c} = \frac{V_1}{Z_c/(1 - K)}$$

while the current leaving node 1 through impedance Z_1 in configuration (*b*) is given by V_1/Z_1. Therefore, we conclude that

$$Z_1 = \frac{Z_c}{1 - K}$$

In a similar manner, the current I_2 leaving node 2 through impedance Z_c in configuration (*a*) is given by

$$I_2 = \frac{V_2 - V_1}{Z_c} = V_2 \frac{1 - (1/K)}{Z_c} = \frac{V_2}{Z_c/(1 - 1/K)}$$

while the current leaving node 2 in configuration (*b*) is V_2/Z_2. Therefore, the value of impedance Z_2 should be

$$Z_2 = \frac{Z_c}{1 - 1/K} = Z_c \frac{K}{K - 1}$$

Since configurations (*a*) and (*b*) have identical nodal equations, these are identical. However, we note that Miller's theorem is useful only if the value of the ratio K can be determined by some independent means.

1.8 INVERSE LAPLACE TRANSFORMATION

In several cases, it is more convenient to solve the equations in the frequency domain, that is, the s domain, and then obtain the time-domain solution by an inverse Laplace transformation of the s-domain solution. Various techniques for numerical inverse Laplace transformation are available in the literature. The technique presented in this section is simple yet efficient and can be easily incorporated in computer programs. It uses the Padé approximation and does not require the computation of poles and residues [55, 56].

The inverse Laplace transform of $V(s)$ is given by

$$v(t) = \frac{1}{2\pi jt} \int_{c-j\infty}^{c+j\infty} V(s) e^{st}\, ds \tag{1.8.1}$$

The variable t can be removed from e^{st} by the transformation

$$z = st \tag{1.8.2}$$

and then using an approximation for e^z. Substituting Eq. (1.8.2) in Eq. (1.8.1), we obtain

$$v(t) = \frac{1}{2\pi jt} \int_{c'-j\infty}^{c'+j\infty} V(s) e^{z}\, dz \tag{1.8.3}$$

According to the Padé approximation, the function e^z can be approximated by a rational function

$$R_{N,M}(z) = \frac{P_N(z)}{Q_M(z)} \tag{1.8.4}$$

where $P_N(z)$ and $Q_M(z)$ are polynomials of order N and M, respectively. Inserting Eq. (1.8.4) in Eq. (1.8.3), we obtain

$$\hat{v}(t) = \frac{1}{2\pi j} \int_{c'-j\infty}^{c'+j\infty} V\left(\frac{z}{t}\right) R_{N,M}(z)\, dz \tag{1.8.5}$$

where $\hat{v}(t)$ is the approximation for $v(t)$. The integral (1.8.5) can be evaluated by using residue calculus and choosing the path of integration along the infinite arc

either to the left or to the right. To ensure that the path along the infinite arc does not contribute to the integral, M and N are chosen such that the function

$$F(z) = V\left(\frac{z}{t}\right) R_{N,M}(z) \tag{1.8.6}$$

has at least two more poles than zeros. This gives

$$\int_C F(z)\, dz = \pm 2\pi j \sum (\text{residue at poles inside closed path}) \tag{1.8.7}$$

where the positive sign is used when the path C is closed in the left-half plane and the negative sign is applied when C is closed in the right-half plane. For $N < M$, we have

$$R_{N,M}(z) \sum_{i=1}^{M} \frac{K_i}{z - z_i} \tag{1.8.8}$$

where z_i are the poles of $R_{N,M}(z)$ and K_i are the corresponding residues. Closing the path of integration around the poles of $R_{N,M}(z)$ in the right-half plane, we get the basic inversion formula

$$\hat{v}(t) = -\frac{1}{t} \sum_{i=1}^{M} K_i V\left(\frac{z_i}{t}\right) \tag{1.8.9}$$

When M is even, we can write

$$\hat{v}(t) = -\frac{1}{t} \sum_{i=1}^{M'} \text{Re}\left[K_i' V\left(\frac{z_i}{t}\right)\right] \tag{1.8.10}$$

where $M' = M/2$ and $K_i' = 2K_i$. When M is odd, $M' = (M+1)/2$ and $K_i' = K_i$ for the residue corresponding to the real poles. The poles z_i and residues K_i' have been calculated with high precision and are used in the programs in this book.

To summarize, for a given function $V(s)$ in the s domain, the response $v(t)$ at any time t can be obtained by the following steps:

1. Select appropriate values of N and M and take values of z_i and K_i' from the computed tables [55, 56].
2. Divide each z_i by t and substitute (z_i/t) for each s in $V(s)$.
3. Multiply each $V(z_i/t)$ by the corresponding K_i' and add the products.
4. Retain only the real part of the result in step 3 and divide by $-t$.

Note that, because of division by t, the value of $v(t)$ at $t = 0$ cannot be calculated by the above procedure. However, either this value can be obtained by using the initial-value theorem or an approximate value can be found by selecting a very small initial value of t. The technique described above is suitable for the calculation of the system response to a nonperiodic excitation such as a step or an impulse.

1.9 RESISTIVE INTERCONNECTION AS LADDER NETWORK

It is well known that interconnections made of high-resistivity materials such as polycrystalline silicon (poly-Si) result in much higher signal delays than the low-resistivity metallic interconnections. However, in the past, poly-Si has remained a principal material for the second-level interconnections. In order to analyze high-speed signal propagation in resistive interconnections, it is important to understand their transmission characteristics. In this section, it will be shown that resistive interconnections can be modeled as ladder *RC* networks under open-circuit, short-circuit, as well as capacitive loading conditions [57, 58]. Finally, the ladder approximation has been applied to a multipath interconnect to perform a first-order analysis of the dependence of the propagation delays expected in such an interconnect on the number of paths.

1.9.1 Open-Circuit Interconnection

From transmission line theory [59], the open-circuit voltage transfer function of a resistive transmission line is given by

$$\frac{V_2}{V_1} = \frac{1}{\cosh\sqrt{sRC}} \tag{1.9.1}$$

where R is the total line resistance and C is the total line capacitance including the capacitance due to the fringing fields as described by Ruehli and Brennan [60]. Using infinite partial-fraction expansions [61], Eq. (1.9.1) can be written as

$$\frac{V_2}{V_1} = \frac{1}{\cosh\sqrt{sRC}} = \frac{4}{\pi}\sum_{k=1}^{\infty}\left[(-1)^{(k+1)}\frac{2k-1}{(2k-1)^2 + sRC(4/\pi^2)}\right] \tag{1.9.2}$$

If $v_1(t)$ is a Dirac pulse, then the voltage $v_2(t)$ can be found easily by finding the inverse Laplace transforms of the terms on the right side of Eq. (1.9.2). If $v_1(t)$ is a unit step voltage, then $V_1 = V_0/s$ (with $V_0 = 1$) and $v_2(t)$ can be obtained after a simple integration to be

$$v_2(t) = L^{-1}\left[\frac{1/s}{\cosh\sqrt{sRC}}\right] = \sum_{k=1}^{\infty}(-1)^{(k+1)}\frac{4}{\pi(2k-1)}\left[1 - \exp\left(-\frac{(2k-1)^2\pi^2 t}{4RC}\right)\right]$$

or

$$v_2(t) = \frac{4}{\pi}\left(1 - \frac{1}{3} + \frac{1}{5} - \frac{1}{7} + \cdots\right) - \frac{4}{\pi}\left(e^{-\pi^2 t/(4RC)} - \frac{1}{3}e^{-9\pi^2 t/(4RC)} + \cdots\right)$$

$$= 1 - 1.273\, e^{-\pi^2 t/(4RC)} + 0.424\, e^{-9\pi^2 t/(4RC)} - 0.254\, e^{-25\pi^2 t/(4RC)} + \cdots \quad (1.9.3)$$

It should be noted that the expression (1.9.3) differs from the corresponding approximate expression in reference [57],

$$v_{\text{out}}(t) = 1 - 1.172\, e^{-\pi^2 t/(4RC)} + 0.195\, e^{-9\pi^2 t/(4RC)} - 0.023\, e^{-25\pi^2 t/(4RC)} \quad (1.9.4)$$

which was obtained by a finite partial-fraction expansion of an infinite expansion of Eq. (1.9.1). It can be seen that the terms of second and higher orders in Eq. (1.9.4), which are particularly important at low values of time, are far from correct.

A T network and the corresponding n-stage ladder network for an interconnection line are shown in Figs. 1.9.1a and b, respectively. In Fig. 1.9.1b, $r_i = R/(n+1)$ and $c_i = C/n$. Now, we need to determine the number of ladder stages required to generate the output voltage based on the transmission line model given by Eq. (1.9.3). Assuming unit step input, a comparison of the plots of the output voltage versus time for an open-circuited interconnection obtained by using Eq. (1.9.3), obtained by a numerical simulation of the T network and those obtained by

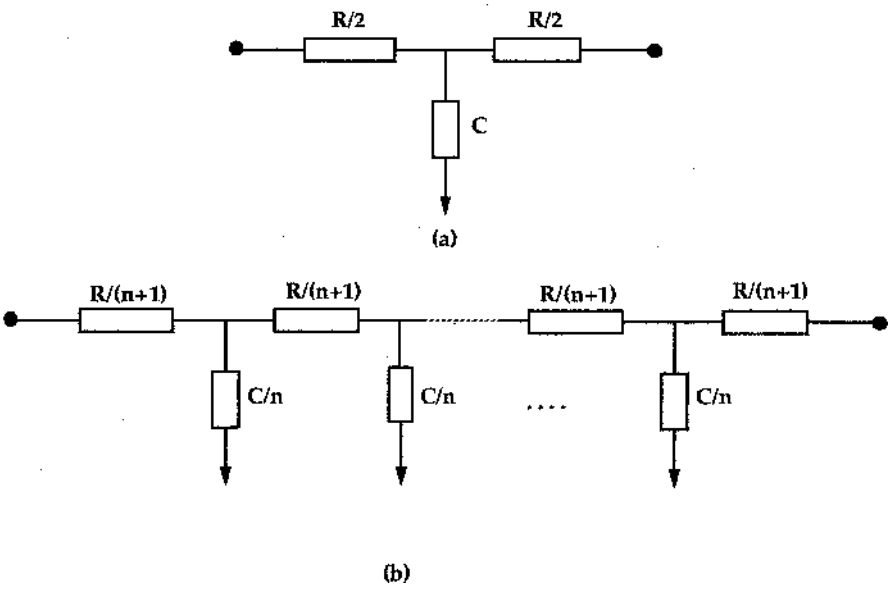


FIGURE 1.9.1 Representation of interconnection line as (a) T network and (b) n-stage ladder network. (From [54]. © 1983 by IEEE.)

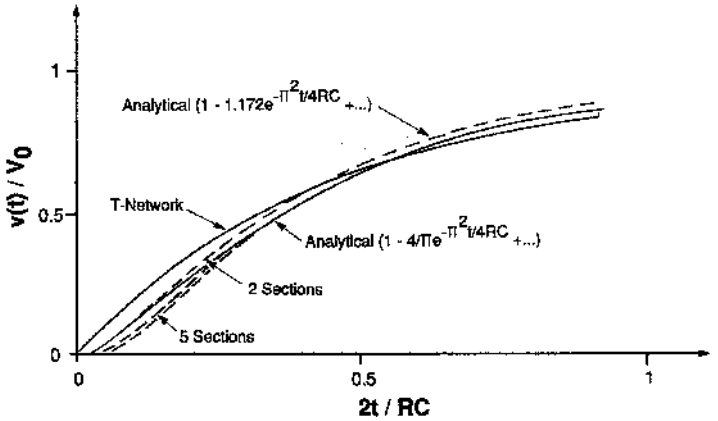


FIGURE 1.9.2 Output voltage versus time for open resistive transmission line for unit step input voltage. (From [55]. © 1983 by IEEE.)

numerical simulations of the ladder network with different number of stages, is shown in Fig. 1.9.2. For the sake of comparison, the output voltage plot obtained by using the approximate expression (1.9.4) is also included in Fig. 1.9.2. It can be seen that the plot obtained by using Eq. (1.9.3) almost coincides with that obtained for the ladder network with 5 stages. In fact, there is negligible difference between the results for the 5- and 10-stage ladder networks.

For an interconnection line loaded with a capacitance C_L, the voltage transfer function can be easily obtained in the s domain, but its analytical inverse Laplace transformation is not possible. Therefore, lumped-circuit approximations have to be used. It can be shown that, for a wide range of C_L/C values, a five-stage ladder network yields sufficient accuracy. Thus, the conclusion for an open-circuit interconnection also holds for a capacitively loaded interconnection.

1.9.2 Short-Circuited Interconnection

For a short-circuited RC transmission line, the output current for a step input voltage V_0/s is given by

$$I = CV_0 \frac{1}{\sqrt{sRC}\sinh\sqrt{sRC}} \tag{1.9.5}$$

Using infinite partial-fraction expansion [61], Eq. (1.9.5) can be written as

$$I = CV_0 \left[\frac{1}{sRC} + \frac{2}{RC} \sum_{k=1}^{\infty} (-1)^k \frac{1}{s + [\pi^2 k^2]/(RC)} \right] \tag{1.9.6}$$

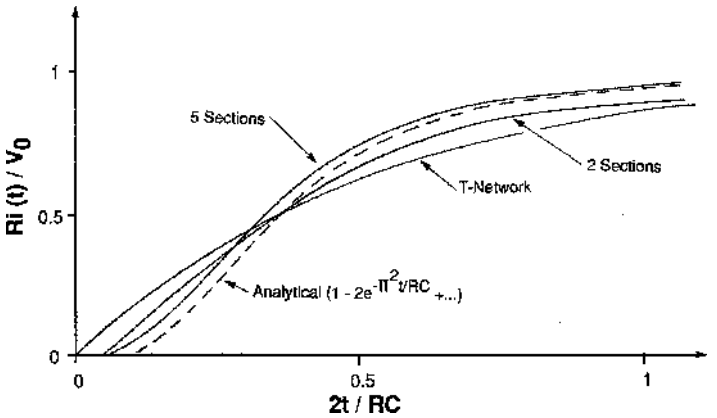


FIGURE 1.9.3 Output current versus time for short-circuited resistive transmission line for unit step input voltage. (From [55]. © 1983 by IEEE.)

The output current in the time domain can then be easily obtained by finding the inverse Laplace transforms of the terms on the right side of Eq. (1.9.6) to be

$$i(t) = \frac{V_0}{R}[1 - 2\,e^{-\pi^2 t/(RC)} + 2\,e^{-\pi^2 4t/(RC)} - 2\,e^{-\pi^2 9t/(RC)} + \cdots] \tag{1.9.7}$$

Assuming unit step input, a comparison of the plots of the output current versus time for a short-circuited interconnection obtained by using Eq. (1.9.7), obtained by a numerical simulation of the T network and those obtained by numerical simulations of the ladder network with different number of stages, is shown in Fig. 1.9.3. It can be seen that, for a short-circuited interconnection, at least 10 stages

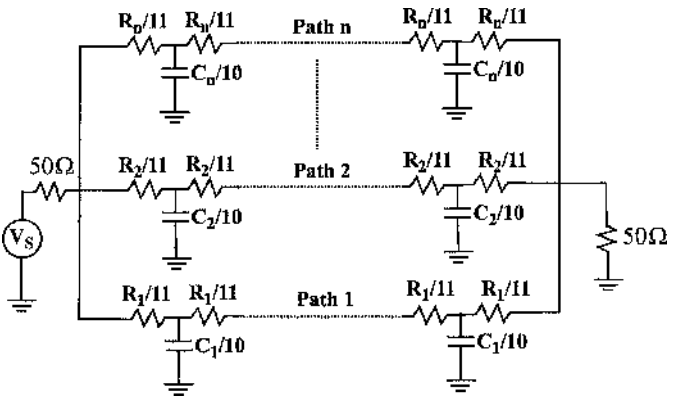


FIGURE 1.9.4 Ten-stage *RC* ladder network approximation applied to each path of multipath interconnection.

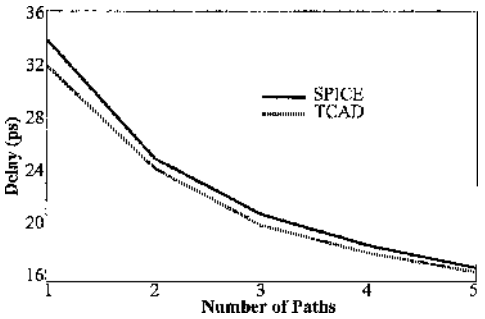


FIGURE 1.9.5 Dependence of propagation delay on number of paths of multipath interconnection included in SPICE model of Fig. 1.9.4. Results obtained by simulation of multipath interconnection by semiconductor TCAD tool also shown.

are required in the ladder network to obtain good agreement with the analytical solution.

1.9.3 Application of Ladder Approximation to Multipath Interconnection

For this analysis, an *n*-path multipath interconnection on the GaAs substrate is considered and the 10-stage ladder network approximation is used for each path of the multipath interconnection. In other words, each path is represented by a ladder of *RC* combinations as shown in Fig. 1.9.4. As shown in this figure, the interconnection is driven by a 50-Ω voltage source and is terminated by a 50-Ω load. The symbols R_1, R_2, and R_n represent the total resistances of the first, second, and *n*th paths of the interconnection whereas C_1, C_2 and C_n represent the total ground capacitances (including the fringing fields) of the first, second, and the *n*th paths. In this analysis, the coupling capacitances between the consecutive paths have been ignored because essentially the same voltage signal is propagating along the different paths of the same interconnection. The dependence of the propagation delay on the number of paths included in the above model using SPICE is shown in Fig. 1.9.5. For the sake of comparison, this figure also includes the results obtained by simulation of the multipath interconnection by a semiconductor technological computer-aided design (TCAD) tool.

1.10 PROPAGATION MODES IN MICROSTRIP INTERCONNECTION

A resistivity–frequency mode chart of the metal–insulator–semiconductor (MIS) microstripline [62] is shown in Fig. 1.10.1, where δ is the skin depth and ρ is the semiconductor resistivity. It can be seen from this figure that the propagation mode

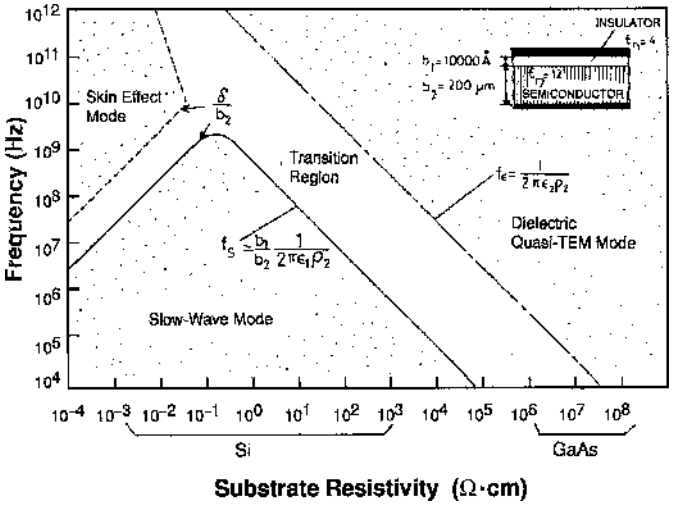


FIGURE 1.10.1 Resistivity-frequency mode chart of MIS microstripline. (From [62]. © 1984 by IEEE.)

in the microstrip depends on the substrate resistivity and the frequency of operation. Figure 1.10.1 shows the following:

1. When the substrate resistivity is low (less than approximately $10^{-3}\,\Omega \cdot \text{cm}$), the substrate acts like an imperfect metal wall having a large skin effect resulting in the skin effect mode.
2. When the substrate resistivity is high (greater than approximately $10^{4}\,\Omega \cdot \text{cm}$) then the substrate acts like an insulator and the dielectric quasi-TEM mode propagates.
3. For an MIS waveguide, the slow-wave mode propagates when the substrate is semiconducting and the frequency is low. The slow-wave mode results because, in the low-frequency limit (note that this frequency limit extends into the gigahertz range at certain substrate resistivities), the electric field lines do not penetrate into the semiconductor whereas the magnetic field lines can fully penetrate into it causing spatially separated storage of electric and magnetic energies.

1.11 SLOW-WAVE MODE PROPAGATION

In this section, a quasi-TEM analysis of slow-wave mode propagation in the micrometer-size coplanar MIS transmission lines on heavily doped semiconductors [63] is presented. The analysis includes metal losses as well as semiconductor losses. The quantities derived from the quasi-TEM analysis are compared with those

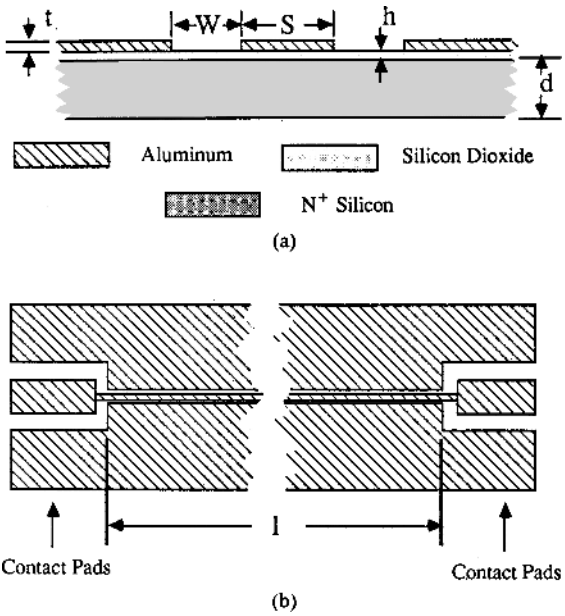


FIGURE 1.11.1 (*a*) Cross-sectional view and (*b*) plan view of micrometer-size coplanar MIS transmission lines. (From [63]. © 1986 by IEEE.)

measured experimentally for a system of four micrometer-size coplanar MIS transmission lines fabricated on N^+ silicon.

1.11.1 Quasi-TEM Analysis

The geometry of the microstructure MIS transmission lines used in this analysis is shown in Fig. 1.11.1. For the experimental results presented below, these structures consist of coplanar aluminum strips (fabricated by evaporating Al on SiO_2) separated from antimony-doped N^+ silicon substrate of doping density $N_d \sim 3 \times 10^{18}\,\text{cm}^{-3}$ and electrical conductivity $80\,(\Omega \cdot \text{cm})^{-1}$ by a thin SiO_2 layer. For the four transmission lines used in the experimental results, the wafer thickness d is 530 μm, the length l is 2500 μm, and the metal thickness t is 1 μm. The values of the other dimensions shown in Fig. 1.11.1 and the capacitance scaling factor used later in this analysis for each of the four lines are listed in Table 1.11.1. Because of the low impedance of the N^+ semiconductor, most of the electrical energy is confined to the insulating layer immediately below the center conductor. However, because the semiconductor is a nonmagnetic material, the magnetic field freely penetrates the N^+ substrate. This separation of the electric and magnetic energies results in the slow-wave mode propagation.

For quasi-TEM propagation of the slow-wave mode of coplanar microstructure MIS transmission line, its equivalent circuit used in this analysis is shown in

TABLE 1.11.1 Dimensions *S*, *W*, and *h* and Capacitance Scaling Factor *K* of Experimental lines

Line	*S*	*W*	*h*	*K*
1	4.2	6.0	0.53	1.3
2	4.2	14.0	0.53	1.3
3	8.7	9.5	0.28	1.1
4	4.7	13.5	0.28	1.2

Source: From [65]. © 1987 by IEEE.

Note: All dimensions are in micrometers.

Fig. 1.11.2. The inductance per unit length, L, is given by

$$L = \frac{1}{c^2 C_{\text{air}}} \tag{1.11.1}$$

where c is the phase velocity in vacuum and C_{air} is the capacitance per unit length of an equivalent air-filled transmission line. Here, C_{air} can be determined by conformal mapping [64] leading to the following expression for L:

$$L = \frac{1}{4c^2 \varepsilon_0 F} \tag{1.11.2}$$

where ε_0 is the permittivity of free space and F is a geometric factor given approximately by [64]

$$F = \begin{cases} \dfrac{\ln[2(1+\sqrt{k})/(1-\sqrt{k})]}{\pi} & 0.707 \le k \le 1 \\ \dfrac{\pi}{\ln[2(1+\sqrt{k'})/(1-\sqrt{k'})]} & 0 \le k \le 0.707 \end{cases} \tag{1.11.3}$$

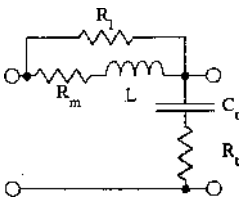


FIGURE 1.11.2 "Slow-wave" mode equivalent circuit of micrometer-size coplanar MIS transmission line used in quasi-TEM analysis. (From [63]. © 1986 by IEEE.)

with

$$k = \frac{S}{S + 2W} \tag{1.11.4}$$

$$k' = \sqrt{1 - k^2} \tag{1.11.5}$$

In Fig. 1.11.2, the resistance R_m in series with L represents the correction due to the metal conductive losses. Its value in ohms per unit length is approximately equal to the effective resistance of the center conductor given by

$$R_m = \begin{cases} \dfrac{1}{\sigma_m t S} & \text{for } t \leq \delta_m \\ \dfrac{1}{\sigma_m \delta_m S} & \text{for } t \geq \delta_m \end{cases} \tag{1.11.6}$$

where σ_m and δ_m are the conductivity and skin depth of aluminum, respectively. The ground-plane contribution to R_m can be ignored because the current densities in it are much smaller than those in the center conductor.

The resistance R_L is inserted in the equivalent circuit of Fig. 1.11.2 to account for the loss caused by the longitudinal current flowing in the N^+ semiconductor parallel to the current in the center conductor. Since the longitudinal semiconductor current flows in addition to the longitudinal current in the metal, a parallel connection has been used. The value of R_L is given by

$$R_L = \frac{1}{\sigma_S \delta_S S} \tag{1.11.7}$$

where σ_S and δ_S are the conductivity and skin depth of the N^+ semiconductor, respectively. Equation (1.11.7) is based on the assumption that the longitudinal electric field under the center conductor decays exponentially in the vertical direction with decay constant δ_S.

To account for the energy storage and loss associated with the transverse electric field and current, the transverse capacitance C_t and transverse resistance R_t have been included in Fig. 1.11.2. The transverse capacitance per unit length is given approximately by

$$C_t = \frac{\varepsilon_i \varepsilon_0 S K}{h} \tag{1.11.8}$$

where ε_i is the dielectric constant of SiO_2 and K is a geometric factor listed in Table 1.11.1 introduced to account for the capacitance associated with the fringing fields. Equation (1.11.8) is based on the assumption that most of the electric energy is stored in the dielectric layer under the center conductor. The value of the transverse resistance is given approximately by

$$R_t = \frac{1}{2\sigma_S F} \tag{1.11.9}$$

where F is the geometric factor given by Eq. (1.11.3). In this analysis, we have ignored the finite transverse capacitance through the air because its susceptance is very small compared with that of C_t and R_t in series.

For a transmission line consisting of the circuit elements of Fig. 1.11.2, the complex propagation constant γ and the complex characteristic impedance Z_0 are given by

$$\gamma = \alpha + j\beta = \sqrt{ZY} \tag{1.11.10}$$

$$Z_0 = Z_0' + jZ_0'' = \sqrt{\frac{Z}{Y}} \tag{1.11.11}$$

where

$$Z = \frac{1}{1/R_L + 1/(R_m + j\omega L)} \tag{1.11.12}$$

$$Y = \frac{1}{R_t + 1/(j\omega C_t)} \tag{1.11.13}$$

and the quality factor Q and the "slowing factor" λ_0/λ_g are given by

$$Q = \frac{\beta}{2\alpha} \tag{1.11.14}$$

$$\frac{\lambda_0}{\lambda_g} = \frac{\beta}{\omega\sqrt{\mu_0\varepsilon_0}} \tag{1.11.15}$$

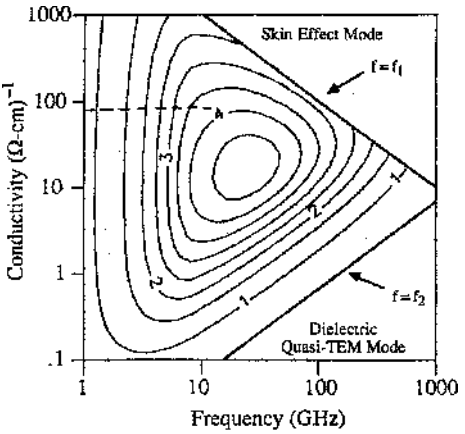


FIGURE 1.11.3 Contours of constant Q for transmission line 2. Dashed line corresponds to experiment parameters. (From [63]. © 1986 by IEEE.)

The quasi-TEM mode analysis presented above is valid only at frequencies which satisfy both $f \ll f_1$ and $f \ll f_2$, where

$$f_1 = \frac{1}{\pi\sigma_S\mu_0(W + S/2)^2} \tag{1.11.16}$$

$$f_2 = \frac{\sigma_S}{2\pi\varepsilon_0\varepsilon_S} \tag{1.11.17}$$

The contours of constant Q for the transmission line 2 are shown in Fig. 1.11.3. This figure shows that, at frequencies satisfying $f \ll f_1$ and $f \ll f_2$, the mode of propagation is the ''slow-wave'' mode because, in this region, the magnetic field freely penetrates the substrate while the electric field does not. When $f_2 < f < f_1$, both transverse electric and magnetic fields freely penetrate the semiconductor substrate and the ''dielectric quasi-TEM'' is the mode of propagation. On the other hand, when $f_1 < f < f_2$, neither field penetrates the substrate and the mode of propagation is the ''skin effect mode.'' Using worst-case parameters for the four transmissions lines studied in this section, we can determine that $f_1 = 120\,\text{GHz}$ and $f_2 = 12,000\,\text{GHz}$. Therefore, all four lines satisfy the criteria for the slow-wave mode propagation and for validity of the quasi-TEM analysis.

1.11.2 Comparison with Experimental Results

The experimental results presented below are obtained by measuring the S parameters over the frequency range 1.0–12.4 GHz [63]. The attenuations of the

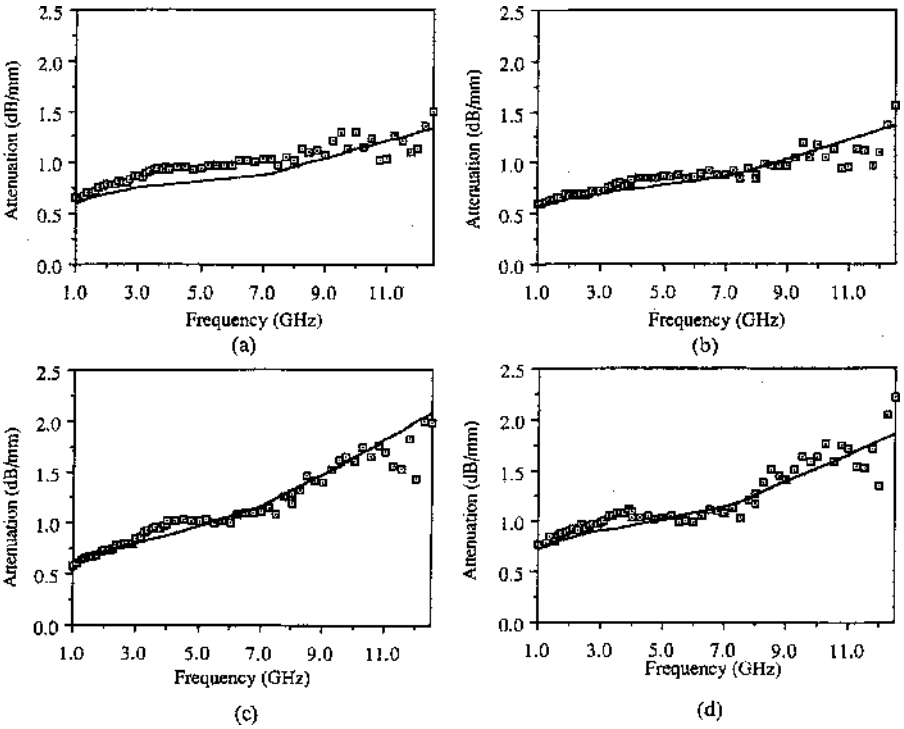


FIGURE 1.11.4 Dependence of attenuation on frequency for (*a*) line 1, (*b*) line 2, (*c*) line 3, and (*d*) line 4. Solid lines represent theoretical values obtained from quasi-TEM analysis. Symbols are experimental values. [63]. © 1986 by IEEE.)

four lines versus frequency are shown in Figs. 1.11.4*a–d*. Solid lines represent theoretical values obtained from the quasi-TEM analysis presented above. The real (Z_0') and imaginary (Z_0'') parts of the characteristic impedance as functions of frequency for the four lines are shown in Figs. 1.11.5*a–d*. It can be seen that the characteristic impedances of all four lines are nearly real, of the order of 50 Ω, and almost independent of frequency. The dependences of the ''slowing factors'' (λ_0/λ_g) on frequency for the four lines are shown in Figs. 1.11.6*a–d*, which also display the quality factor Q versus frequency. It can be seen that each of the four quality factors increases with frequency, reaching values in the range 3.6–4.3 at 12.4 GHz.

It is obvious that there is excellent agreement between theory and experiments over the full frequency range from 1.0 to 12.4 GHz for all four transmission lines. It can be concluded from this close agreement that the slow-wave mode propagating on these micrometer-size MIS transmission lines is, in fact, a quasi-TEM mode and can therefore be analyzed by elementary techniques.

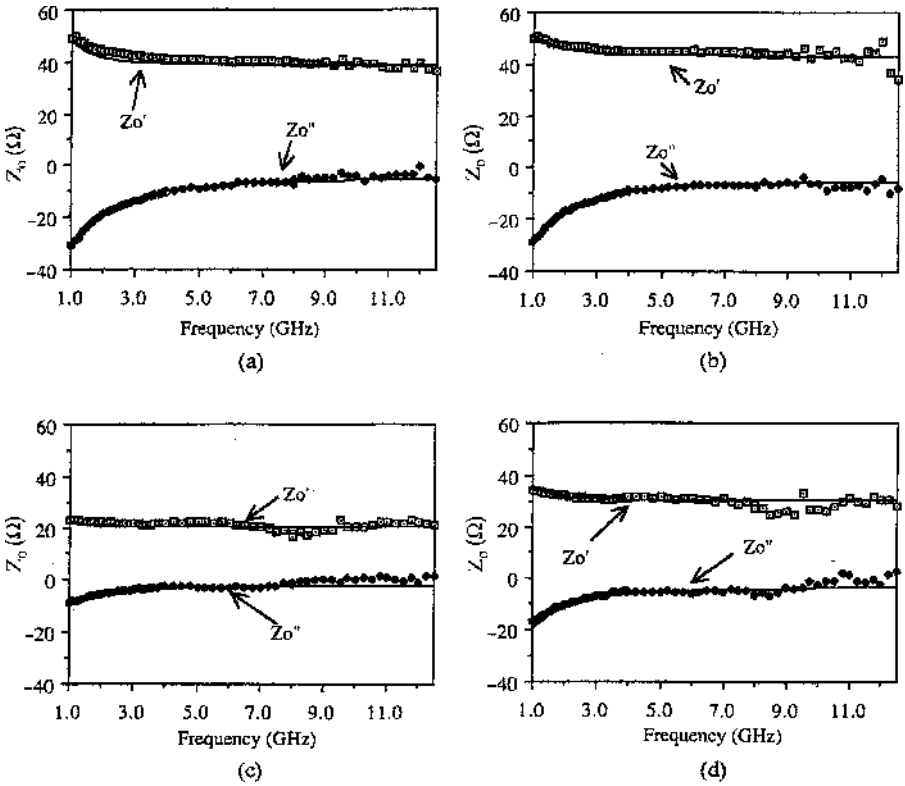


FIGURE 1.11.5 Dependence of real and imaginary parts of characteristic impedance on frequency for (*a*) line 1, (*b*) line 2, (*c*) line 3, and (*d*) line 4. Solid lines represent theoretical values obtained from quasi-TEM analysis. Symbols are experimental values. (From [63]. © by 1986 IEEE.)

In this analysis, we have included three loss mechanisms, namely metal loss, longitudinal semiconductor loss, and transverse semiconductor loss. It can be shown that the relative contribution of each loss mechanism in the above model can be approximately (within 1%) calculated by keeping the corresponding resistance in the circuit of Fig. 1.11.2 while setting the other two resistances to zero. The results for transmission line 2 are shown in Fig. 1.11.7. It can be seen that the metal loss contribution is dominant at frequencies below 25 GHz and decreases with increasing frequency though, even at 100 GHz, it accounts for nearly 20% of the total loss. It can also be noted that both the transverse and the longitudinal semiconductor losses increase with frequency though the transverse loss component is very small.

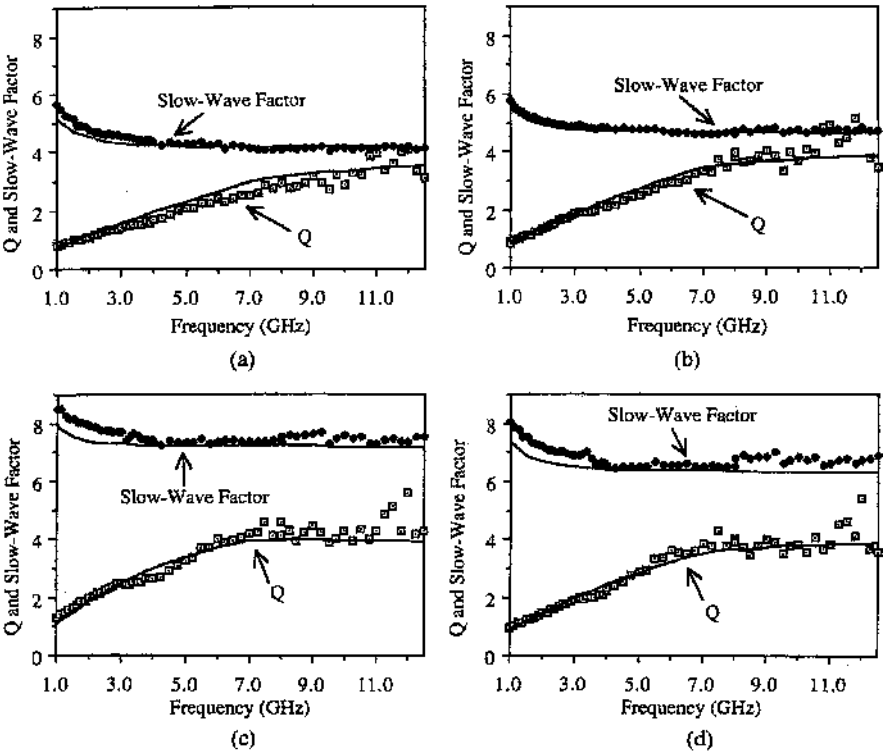


FIGURE 1.11.6 Dependence of quality and slow-wave factors on frequency for (*a*) line 1, (*b*) line 2, (*c*) line 3, and (*d*) line 4. Solid lines represent theoretical values obtained from quasi-TEM analysis. Symbols are experimental values. (From [63]. © 1986 by IEEE.)

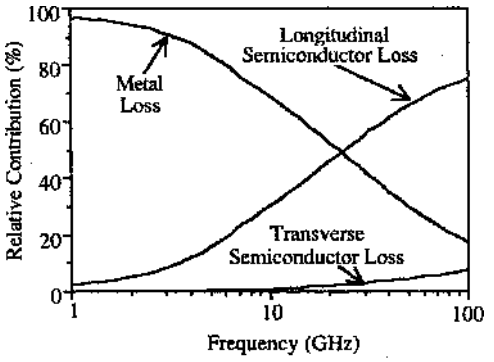


FIGURE 1.11.7 Relative contributions of three loss mechanisms for transmission line 2. (From [63]. © 1986 by IEEE.)

1.12 PROPAGATION DELAYS

In the literature, three measures of propagation delays in an electric circuit are defined [65]:

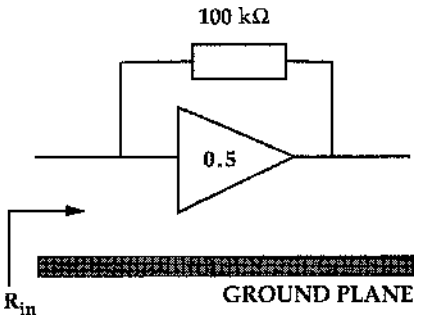
Delay Time. The time required by the output signal (current or voltage) to reach 50% of its steady-state value.

Rise Time. The time required by the output signal (current or voltage) to rise from 10 to 90% of its steady state value.

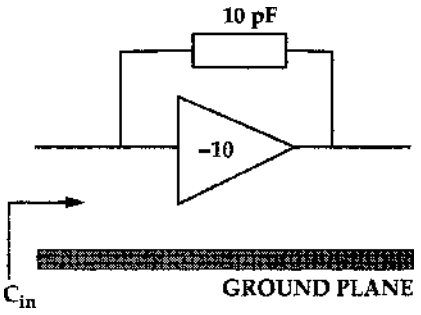
Propagation Time. The time required by the output signal (current or voltage) to reach 90% of its steady-state value.

EXERCISES

E1.1 In the circuit shown below using an ideal voltage amplifier of gain 0.5, determine the input resistance R_{in}.



E1.2 In the circuit shown below using an ideal voltage amplifier of gain -10, determine the input capacitance C_{in}.



E1.3 Following the steps in Section 1.5, write the expressions for the even- and odd-mode capacitances for a system of four coupled conductors and solve them for the self and mutual capacitances for the four conductors. Comment on the accuracy of your results.

E1.4 Following the steps in Section 1.5, write the expressions for the even- and odd-mode capacitances for a system of five coupled conductors and solve them for the self and mutual capacitances for the five conductors. Comment on the accuracy of your results.

E1.5 Suggest situations where it will be preferable to model an interconnection as a lumped circuit or as a transmission line.

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