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ONE-DIMENSIONAL SEMICONDUCTOR NANOSTRUCTURE GROWTH WITH TEMPLATES

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1.1 INTRODUCTION

In this introductory section, we will provide a brief background for the development of technology based on epitaxial growth of semiconductor nanowires. Since the 1950s, low-dimensional structures have dominated semiconductor technology. The rapid developments of their products drive the dramatic downscaling of electronics, a miniaturization that the industry expects to continue for at least another two decades. Since the 1970s, the field-effect transistor (FET) became the fundamental logic element in semiconductor chips.[1] Moore's law states that the number of transistors on a given chip area doubles roughly every 18 months. The design of most functional semiconductor nanostructures is based on the Si platform at present. Although group III–V compound semiconductors have been considered as building blocks for high-speed and high-frequency electronic devices,[2,3] more recently, Si/Ge and Si/SiGe heteroepitaxial nanostructures have attracted much attention.[4,5] One-dimensional (1D) nanostructures are promising as new emerging semiconductor devices. In this chapter, several aspects of the controlled growth of 1D semiconductor nanostructures with the assistance of several templates are illuminated.

A semiconductor nanowire is generally a solid rod with a diameter of <100 nm, which is composed of one or several semiconductor materials. A lower limit of a few nanometers (nm) in diameter was defined from a technological perspective.[6] Experimentally, many techniques for the control of composition, doping, and the interface definition along the 1D nanostructure have been developed, such as molecular beam epitaxy (MBE), chemical beam epitaxy (CBE), chemical vapor deposition (CVD), and vapor-phase epitaxy (VPE).[7] The term *growth* here means that the semiconductor nanowires are nucleated from precursors, regardless of whether it is in vapor or liquid phase. In particular, growth is catalyzed by a metal particle, which strongly accelerates the growth rate and determines the diameter. Wagner and Ellis presented a model on the growth of silicon whiskers, which is generally described as the vapor–liquid–solid (VLS) growth mechanism.[8] With several metal catalysts, most of the semiconductor nanowires (Si, Ge, group III–V compounds) have been synthesized via VLS growth.[9] The target semiconductor materials should exhibit a binary-phase eutectic alloy with the catalyst at the growth temperature. The related crystal growth rate, in one dimension confined by the catalytic particle, is greatly enhanced resulting in the one-dimensional (1D) structure. If the catalyst particle is a solid at growth temperature, the mechanism is then called (*vapor–solid–solid*) (VSS).[10] In general, there are two kinds of solid catalysts, compounds or metals. For Si this can be a silicide[11] or a metal with high eutectic temperature.[12] Otherwise, semiconductor nanowires can

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be grown catalyst-free, that is, without any metallic catalyst involved, such as the Si and Ge nanowire growth with the decomposition of the corresponding oxide,[13] or the selective III–V nanowire growth by masking a substrate.[14]

Semiconductor nanowires are explicitly mentioned as realistic additions to complementary metal oxide semiconductor (CMOS) devices. Among the potential feasibilities, researchers have focused on studies of nanowire-based vertical surround-gate field-effect transistors (VS-FET).[15] The generic process for fabrication of a wrap-gated VS-FET could also be based on epitaxially grown Si nanowires[16] and InAs nanowires.[17] The advancement of doping techniques and high-quality heterostructures, together with studies on the simulation of bandgap engineering to tuning the properties of FETs, are quite promising.[18,19] Si nanowire-based solutions have been proposed for optoelectronic devices,[20] biosensors,[21] and energy sources,[22] as well as other functional semiconductor materials.

At the time of writing, devices based on semiconductor nanowires are, however, still in an embryonic stage from an industrial perspective. Their introduction as new technologies would require a long-term research-and-development (R&D) process in the electronics industry. Whether they will really have an impact on future post-CMOS technology, which requires nanostructures <10 nm, depends on other factors such as the intensive exploration of alternative materials, such as GaAs or InAs instead of Si. Controllable size and crystallographic orientation of semiconductor nanowires with high reproducibility are, therefore, two key issues in potential applications. In this chapter, the template-assisted growth of semiconductor nanowires will be demonstrated as one promising solution, which could provide size-controlled nanostructures while also enabling selective crystallization within limited space.

Epitaxial growth refers to a method of crystal formation on an underlying crystalline substrate. Semiconductor epitaxy can be realized from gaseous or liquid precursors. With the substrate surface intrinsically serving as a seed crystal, or by a surface modification, the deposited material crystallizes in a lattice structure and orientation identical to those of the substrate. Ideally, a two-dimensional 2D film epitaxial structure is formed after several atomic layer depositions onto a substrate. If the material is deposited on a substrate of the same composition, the process is called *homoepitaxy*. Otherwise, it is called heteroepitaxy.

Without introducing additional forces, the morphology at the initial stage of homoepitaxial growth is, based on the thermodynamic "wetting" model, determined by the minimum of interfacial free energies.[23] Briefly, the smaller one of the total free energy of epilayer/vacuum interface plus the epilayer/substrate interface ($f_e + f_i$) and the free energy of the substrate/vacuum interface (f_s), determines the wetting behavior of the epilayers. The epilayers supposedly cover the substrate homogeneously with a decrease in free energy, when $f_e + f_i < f_s$. In case of $f_e + f_i > f_s$, a three-dimensional (3D) island morphology is formed preferentially. The partial uncovering of the substrate decreases the total free energy.

For a system with lattice mismatch, we should factor in the strain from the lattice mismatch in the growth model. The buildup of strain energy at the interface increases with the initial wetting growth of the epilayer, and the increased f_i leads to 3D island formation. For different systems, a competition between different strain relaxation mechanisms was experimentally found, resulting in the formation of either 3D island without dislocations (coherent islands) or dislocations.[24] A significant amount of work has focused on fabrication of heteroepitaxial nanostructures that could restrict carriers to 1D quantum wires or to zero-dimensional (0D) quantum dots, following since the first observation of confinement in a quantum well.[25] Axial heterostructure nanowires were first demonstrated in 1994 for the GaAs-InAs system.[26] Further development of axial InAs/InP superlattices with atomically perfect interfaces was realized, and a conduction band offset of 0.6 eV was deduced from the electrical current measurement, due to thermal excitation of electrons over an InP barrier.[27] For a lateral heterostructure, spatial separation of subband energies leads to a carrier confinement and a reduced carrier scattering, due to confinement of carriers in the radial direction. For example, Lieber's group used bandstructure design and controlled epitaxial growth to create a 1D hole gas system in Ge/Si core/shell nanowire heterostructures, with ballistic transport through individual 1D subbands and long carrier mean free paths at room temperature.[28,29] Furthermore, most of the interesting physical behaviors are only observed from true quantum heterostructures, whose lateral dimension should be on the scale of ≤ 10 nm, to be comparable to the de Broglie wavelength of charge carriers. Geyer et al. have demonstrated that, using a top–down method, the diameter of Si nanowire arrays containing Si/SiGe superlattices could be scaled down to <20 nm.[30]

The application of the 1D semiconductor nanomaterials necessitates, for convenient device integration and processing, large-scale control of position and orientation. Table 1.1

TABLE 1.1 Methods Used to Realize 1D Semiconductor Nanostructures at Defined Locations, with Corresponding Size Scale

Method	Size (nm)	Reference(s)
Catalyst lithography	50–100	35,36
Masked neutral beam etching	<10	37
Patterned metal-assisted etching	<10	33
Surface-programmed assembly	<10	34,38
Surface template	1–2	32
Porous template-assisted	<10	39,40

shows a collection of various methods that have been reported thus far to realize 1D semiconductor nanowires at defined locations, with the corresponding scaling range and the literature references. The most common process for position control is based on electron or ion lithographic processing. For semiconductor nanowire growth, catalyst lithography has proved to be the most popular technique for position control. The substrate is patterned by electron beam lithography, a processing with exposure of a resist layer, metal evaporation, and a lift off step. Thus far, large-area lithographic technologies have been limited to scales >22 nm. The growth direction of nanowire is influenced by many factors, and positioning of catalysts at well-defined locations will not effectively ensure control of nanowires position and direction. For these reasons, alternative means of down scaling to small diameters (≤10 nm) are utilized. The surface template method was derived from the selective-area growth on a lateral patterned surface. A quantum wire structure was produced on a GaAs(100) substrate with an etched pattern of parallel V-shaped grooves.[31] The epitaxial nanowires had a crescent shape, and with a core thickness in the 10 nm scale. Using the scanning tunneling microscopy (STM) approach with atomic resolution, ultrathin Cu_3N nanowires with a width down to 1 nm were demonstrated to grow laterally on a single crystalline Cu(110) reconstructed surface.[32] To realize vertically aligned nanowire arrays, reactive-ion etching (RIE) and patterned metal-assisted etching methods were used, through a self-organized porous mask, decreasing the mean size of nanowire arrays down to the <10 nm scale.[33] However, some top–down techniques produce surfaces of nanowires with a high density of defects, via the high-energy ion bombardment at the bulk material. Although the crystallographic orientation could be confined vertically to the substrate, the nanowires were found to taper with increase in length/diameter ratio. The surface programed assembly method[34] does not impose stringent demands on the growth process; only proper selective alignment is crucial for well-controlled structures. Nanowires and nanotubes are initially, without position control, grown with a fixed growth direction and size. Afterward, they are collected by a liftoff process and placed on a prepatterned substrate. A precise single-unit alignment is, however, not easily achieved.

The criteria periodicity, small diameter, and vertical alignment of the nanowires can be satisfied by the assistance of self-organized porous templates. Either a liquid or a gaseous precursor can be used for the growth. A supercritical fluid (SCF) inclusion technique combined with a mesoporous silica film was developed, which produced ordered semiconductor nanowire arrays with several nanometers in diameter.[41,42] The high diffusivity of the fluid enables a rapid transport of the precursor into the mesopores of the silica film. However, rigorous safety precautions should be considered in these experiments, because of the high pressures and temperatures used to allow nucleation and growth.[43] The ideal growth of semiconductor nanowires is assumed to be bottom–up epitaxial growth. Selective bottom–up filling in the vertical 1D direction can be realized by a combination of VLS growth and porous template with catalysts at the nanowire tips. This means that no template sidewall deposition occurs or at least that slow the rate of parasitic growth on the sidewall is lower than that for the nanowire. Otherwise, cracks or voids affecting conductive properties of products would be inevitable. At this point, not only is high diffusivity of the source gas required at the growth temperature; the templates must also satisfy the following conditions: (1) ordered pores attaining the desired degree of nanowire growth, (2) chemical stability against source gas and by-products during CVD at the growth temperature, and (3) selective deposition of catalyst metal at the pore bottom to enable the epitaxy. Satisfying these conditions, the molecules of source gas can smoothly enter into the pore, being cracked only at the surface of the catalyst with direct contact with the substrate surface.

To realize the integration of Si-based 1D nanoelectronics, the most promising approach is the epitaxial growth of Si nanowires directly on Si substrate with desired crystallographic orientation and doping. Technically, the most widely used method for the high-quality epitaxy is based on a VLS growth mechanism.[44] In particular, with the CVD growth technique, the essential concept is a metal/silicon alloy in the liquid phase working as a medium to transform Si atoms from components of gaseous molecules into a solid crystal. The Si epitaxy is a continuous extension of Si lattice planes from the surface plane of a hydrogen-terminated single-crystal Si substrate.

A typical VLS growth model using gold as catalyst is shown in Figure 1.1a. Gaseous molecules with Si

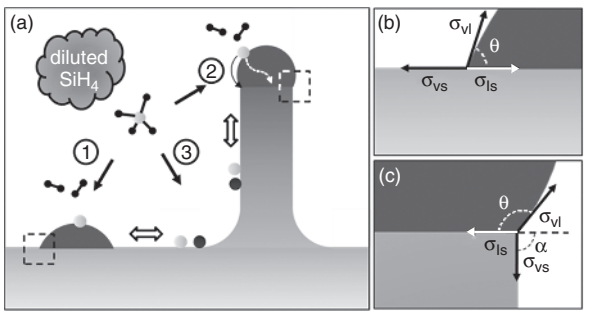

Figure 1.1 (a) Schematic of VLS growth mechanism with AuSi droplet formation and Si nanowire epitaxy: (1) SiH_4 decomposed on AuSi eutectic droplet; (2) Si atoms precipitate at liquid–solid interface or at edge of the three-phase line through bulk or surface diffusion, respectively; (3) Si atoms deposited from SiH_4 directly onto the Si surface. Expanded views of selected three-phase line junction areas are presented for initial droplet (b) and nanowire (c) growth.

components (e.g., diluted SiH_4, Si_2H_6, $SiCl_4$) are introduced into a vacuum chamber, where an H-terminated Si substrate covered by a deposited thin Au film is heated above the Au-Si eutectic temperature of 363°C.[45] We should first mention that, during the dewetting process, bigger Au-Si droplets always grow at the expense of smaller ones in their neighborhood (Ostwald ripening) through a surface diffusion process. Meanwhile, traces of Au saturating the Si dangling bonds as a submonolayer film are distributed over the Si surface in between. Although studies of the wetting behavior observed a depression of Si surface where the droplets once stood,[46] we assume in the schematic that the liquid Au-Si alloy droplets are formed on a flat Si surface, namely, the initial positions of Si epitaxy. With SiH_4 decomposed on both surfaces of the catalysts and the Si crystal, Si atoms can diffuse into the catalyst particle. At the same time, the byproduct H_2 is removed by the gas flow. In order to provide sufficient Si atoms to freeze out at the solid–liquid interface from a supersaturated Au-Si alloy droplet, the precursor species must decompose to some extent at the growth temperature. The nucleation model suggests that Si atoms nucleate at the edge at the three-phase boundary with propagation toward the center by the Burton–Cabrera–Frank mechanism.[47] Experimentally confirmed,[48] the Si nanowire base during the initial phase of growth has an expanded shape as shown in Figure 1.1a. Surface thermodynamics was adopted to explain the interplay between droplet and nanowire in the VLS epitaxy.[49] They presented a model of stable growth that predicts a limited range of possible contacting angles. Depicted in the expanded view of Figure 1.1b, forces at the three-phase line have mainly three components corresponding to the vapor–solid, liquid–solid, and vapor–liquid interfacial tensions, namely, σ_{vs}, σ_{ls}, and σ_{vl}, respectively. It was pointed out that an additional line tension contribution should be considered if the contact radius is on the order of a few nanometers.[50] In equilibrium, the lateral driving forces for a three-phase boundary movement are balanced. Si atoms are nucleated at the growth interface by bulk or surface diffusion. In a typical VLS growth, the liquid diffusion pathways in the droplet dominate the transportation. Surface diffusion along the nanowire and on the Si substrate should be considered as well, since nanowire growth was experimentally found to be in an unsteady state.[51] For example, faceting and tapering of Au-catalyzed Si nanowires were observed at elevated growth temperatures due to surface migration of Si and Au. The competition between these two Si transportation processes, surface diffusion and bulk diffusion in the liquid, leads to a characteristic profile of the supersaturation as a function of the radius. The supersaturation at the rim has the highest value, and thus the nucleation probability is highest at the three-phase line. If high supersaturations are used, nucleation will also occur with high probability at other positions at the interface of liquid and solid. This can result in a rough interface by polycentric nucleation. During the nanowire growth, depicted in the enlarged view of Figure 1.1c, the vapor–solid interface is inclined to the nanowire surface with an angle α, satisfying the force balance in the lateral direction as well.

One issue that is intimately connected with the Si nanowire epitaxy is the question of the relation between diameter and growth directions. In free space, metal-catalyzed Si whiskers grown by CVD prefer to grow in <111> directions.[52] Additionally, other growth directions such as <110>,[53] <112>,[54] and <100>,[55] were also experimentally found. A transition between different preferred growth directions was observed for epitaxial Si nanowires.[56] The preferred growth directions were <111> for large-diameter (>40 nm) nanowires, a mixture including <112> for intermediate diameters, and <110> for small diameters (<20 nm). The influence of supersaturation on the growth direction using other conditions, such as plasma excitation[57] and pressure change,[58] were investigated to some extent. However, using the VLS growth mechanism, mainly three epitaxial growth directions on bare silicon substrates were obtained, which do not include the <100> growth directions.

1.2 ANODIC ALUMINUM OXIDE (AAO) AS TEMPLATES

Considering that conventional Si micro/nanoelectronics is based on Si(100) wafers, it is meaningful to realize high-density epitaxial Si[100] nanowire arrays vertically grown on Si(100) wafers, especially for devices requiring vertical nanowire alignment. Compared with the growth in free space, it is possible to obtain controllable growth directions of embedded 1D nanostructures with the assistance of porous templates. Lew et al. demonstrated successfully the use of AAO membranes as template for Si nanowire growth.[59] The Si nanowires grown by this method had two gold tips at each ends, and the single-grain Si nanowires were found with two growth directions, parallel to <100> and <211>. Shimizu et al. anodized an AAO membrane directly on a Si(100) substrate in order to realize the homoepitaxy of Si.[60] After selective removal of the barrier layer and silicon dioxide, Au catalysts were electrolessly deposited on Si confined at the bottom of AAO pores, leading to an epitaxial growth of Si[100] nanowires perpendicular to the Si surface.

1.2.1 Synthesis of Self-Organized AAO Membrane

Porous AAO synthesized by electrochemical oxidization of aluminium has been studied and used in numerous fields for more than half a century.[61,62] Based on a two-step anodization process, in 1995, a self-ordered porous AAO

membrane with 100 nm interpore distance was first reported by Masuda and Fukuda.[63] The long-term first anodization results in an equilibrium morphology at the oxide/metal interface, which shows a textured aluminum surface after removal of the first oxide layer. The textured aluminum surface results in highly ordered hexagonal pore arrays in the second anodization step. Since this discovery, AAO can be used to provide ordered honeycomb nanopore arrays, perpendicular to the surface. Most importantly, the diameter of AAO pores can be controlled from a few nanometers to several hundreds of nanometers depending on the anodic voltage and acid species used for anodic oxidation. To date, the most popular model for the self-adjustment of ordering in AAO is based on the mechanical stress, which is associated with the expansion between neighboring pores during the oxidation process.[64] Under conventional *mild anodization* (MA) conditions, AAO formation is described by a 10% porosity rule, corresponding to a volume expansion ratio of 1.2 between aluminum and alumina.[65] Lee et al. reported that, using the *hard anodization* (HA) process, well-ordered hexagonal pore arrays in AAO can be produced with a growth rate 25–35 times larger than with MA but a smaller porosity rate of only 3%.[66]

Anodization can be carried out under constant-voltage mode (potentiostatic) or constant-current mode (galvanostatic). In general, a two-step constant voltage anodization is recommended. The experimental setup is quite simple, as shown on the illustration of Figure 1.2. In order to ensure homogeneous reactions, the electrolyte is stirred. The structure of pore arrangement after the second anodization is characterized as a close-packed hexagonal pore array (top-view SEM image), and columnar cells containing elongated cylindrical nanopores are normal to the Al surface. Each nanopore ends in a thin barrier oxide layer with approximately hemispherical shape (side-view SEM image, white insert). Typically, AAO films with different pore diameters and interpore distances ranging from 20 to 200 nm can be prepared, using three major inorganic acid electrolytes: H_2SO_4, $H_2C_2O_4$, and H_3PO_4. The respective electrochemical parameters and dimensional measurements obtained by *ex situ* SEM characterization are shown in Table 1.2. We can conclude that, without further pore widening after the second anodization, the pore diameter after ordering in sulfuric acid is the smallest down to the 20 nm range. The pore density is increased with decreasing of constant voltage, similar to the reported

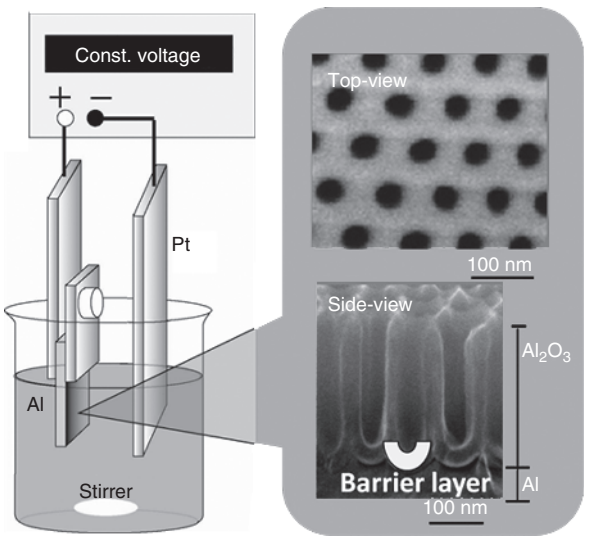

Figure 1.2 Simplified illustration of the experimental setup of a two-step constant-voltage anodization. The structure of the AAO film was characterized by top-view and side-view SEM images.

approximately 2.5 nm/V linear relationship. On the other hand, the pore diameter and shape are influenced by the electrolyte temperature and the anodization time because of the chemical etching on the pore wall. For example, the sulfuric acid anodization at 25 V results in a minimum pore diameter of 20 nm at 1°C rather than the 25 nm at 8°C.

1.2.2 Synthesis of Polycrystalline Si Nanotubes

Using the confinement effects of the sidewalls, AAO template-assisted synthesis of polycrystalline Si nanotubes have been reported, such as the catalyst-assisted CVD method,[67] the molecular beam epitaxy (MBE) method,[68] and the chemical reductive deposition method.[69] Smaller diameters and controllable structures still remain challenges. An ultra-high-vacuum (UHV) CVD method combined with a transition metal as catalyst was used to fabricate Si nanotubes with cobalt silicide ends. The growth length, diameter, and thickness of tube walls can be well controlled by the high-quality AAO templates.[70]

TABLE 1.2 Recommended Electrochemical Parameters for Ordered AAO Preparation

Electrolyte	Concentration	Voltage (V)	Temperature (°C)	First Anodization Time (h)	Oxide Etching T(°C)/t(h)	Pore Diameter (nm)/ Interpore Distance (nm)
H_2SO_4	0.3 M	25	1–8	20–40	60/16	20/65
$H_2C_2O_4$	0.3 M	40	1–8	20–40	60/20	40/100
H_3PO_4	1.0 wt%	195	1–2	16–20	45/24	180/500

1.2.2.1 Growth Mechanism Figure 1.3 schematically illustrates the proposed growth mechanism by sketching three main procedures. In step 1, a gold film was sputtered onto one side of the AAO membrane as a contacting electrode. Cobalt nanowires with a defined length were electrodeposited into the pores. The overall cross-sectional structure is shown in the SEM image of Figure 1.3, step 4. The average pore diameter and thickness of the as-prepared AAO templates were 45 nm and 40 μm, respectively. The electrodeposition of cobalt was performed in a galvanostatic mode with a current density of 1.5 mA/cm^2 with an electrolyte consisting of 200 g/L $CoSO_4 \cdot 7H_2O$ and 20 g/L H_2SO_4. A thin gold film ~300 nm in thickness covered one top surface of the AAO template as the cathode and a platinum mesh was employed as the anode. The different contrasts in the SEM image of Figure 1.3, step 4 correspond to the Co nanowires and the remaining pore spaces with Si nanotubes. Subsequently, in step 2, the AAO template with embedded Co nanowires was transferred into the UHV system. The annealing was performed at 600°C for 2 h, resulting in a homogeneous decoration of Co nanoclusters on the sidewalls and the other top surface of the AAO template. It is well known that the sidewalls of AAO templates contain electrolyte anions after anodization. These anions would attract the positively charged metallic ions on the sidewalls during the exposure to the Co sulfate solution. During the UHV annealing process, the linked OH^- anions could reduce Co^{2+} to the metallic nanoclusters:

$$2Co^{2+} + 4OH^- \rightarrow 2Co + 2H_2O + O_2 \qquad (1.1)$$

Simultaneously the byproducts (H_2O and O_2) are pumped away with a vacuum pressure under 1×10^{-9} mbar.

An indirect proof of a homogeneous Co decoration on the surfaces of AAO is the homogeneous Si growth. A flow rate of 20 sccm (standard cubic centimeters per minute) of 5% SiH_4 gas was fluxed into the UHV chamber with controlled partial pressures, from 0.1 to 0.75 Torr and a fixed growth temperature of 500°C, the growth lasted for 30 min. The transmission electron microscopic (TEM) image in Figure 1.3, step 5 was taken from a sample grown at 0.1 Torr partial pressure. It confirms the Si growth with a homogeneous thickness, even at the pore opening. The AAO was selectively etched by a 5% H_3PO_4 solution. The lower inset indicates that the nanotubes can grow up to several micrometers long with a homogeneous thickness inside the pore. This can be understood if Co nanoclusters formed with a high density/uniformity and then functioned as catalytic nuclei for the Si growth during step 3. The Si grains grown at each nucleus were progressively connected and thickened with the continuous SiH_4 decomposition. Finally, a polycrystalline Si nanotube attached tightly to the sidewalls. Meanwhile, SiH_4 reached the top surface

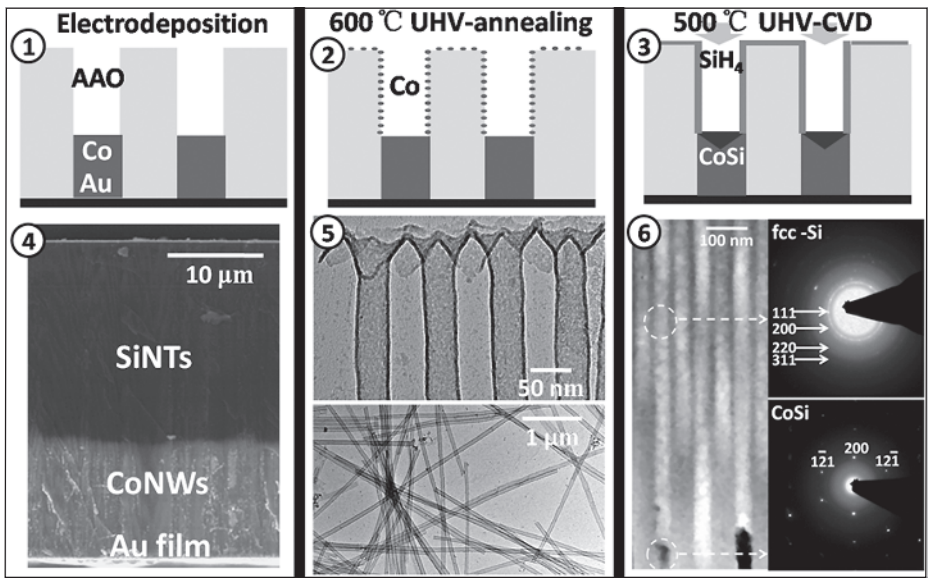

Figure 1.3 Schematic illustration of the growth mechanism of Si nanotubes by three main procedures: (1) electrodeposition of Co nanowires into AAO pores with a Au film as counterelectrode; (2) UHV annealing produces Co nanoclusters decorating AAO surface; (3) growth at 500°C with SiH_4; (4) cross-sectional SEM image of a sample after CVD process; (5) TEM images of the Si nanotubes after removal of AAO template; (6) cross-sectional TEM image of as-prepared heterostructures within AAO and its selective-area diffraction patterns with indexing. (Reproduced from *Nanotechnology* 2010, 21, 055603 (6 pp), Copyright © 2010, IOP Publishing Ltd.[70])

of the Co nanowires, resulting in the formation of cobalt silicides connected to the end of the Si nanotubes. The silicides are shown in the cross-sectional TEM image (Figure 1.3, step 6) of the structures embedded in the AAO template. The selected-area energy dispersive (SAED) patterns that were taken from one tube body and the end of this tube were indexed as polycrystalline Si and CoSi, respectively.

1.2.2.2 Characterizations of Crystallographic Structure and Compositions Selected-area energy-dispersive X-ray spectroscopy (EDS) was used to determine the compositions, at five different positions (spot 1–spot 5 in Figure 1.4), along one nanotube of 10 μm length, as shown in Figure 1.4a. Si, Co, and Au are all found in the EDS spectrum taken from these five spots (Figure 1.4b). An enlarged view near 6.93 keV shows the Co Ka1 peaks with higher sensitivity (Figure 1.4c). The histograms of the atomic ratio of Co and Si (Figure 1.4d) confirm that the tip consisted of Co and Si with a stoichiometric ratio of ~1 : 1, whereas the Co concentration was almost constant in the tube body. It was also revealed that the observed Au was from background contamination, which is shown to be constant in Figure 1.4d, and spot 2 was interferred by the nearby silicide with a higher Co atomic ratio. The crystallographic structure at the end of the tube was further investigated by a high-resolution (HR) TEM image. Figure 1.4e reveals a crystalline cone at the end of the nanotube, the shoulder edge of which is connected with the Si nanotube (indicated by the black arrows). Insets are the enlarged views of the selected dashed squares: (1) the tip consists of a single-phase CoSi with CsCl structure (ICSD database, space group *pm 3m* with a lattice constant $a =$ 2.816 Å), whose calculated interplanar spacing of 0.20 nm is very close to that of the CoSi(110) plane (1.99 Å); (2) the nanotube with a wall thickness of ~6 nm consists of 1–2-nm-thick amorphous oxide layers and polycrystalline core, where the (220) lattice planes ($d = 0.19$ nm) of the crystallized silicon regions are still observed. As we know, several Co-Si alloy phases are expected to appear in sequence according to the thermal equilibrium phase diagram of Co-Si. In such a case, Co_2Si, CoSi, and $CoSi_2$ will be formed with increasing temperature.[71] It was reported that for a thin-film Co/Si couple, the phase appearing first at the Co/Si interface will be Co_2Si when the annealing temperature is >350°C. With longer time and higher temperature, CoSi will form when additional Si is available. When the temperature is increased up to 500°C, the $CoSi_2$ phase can be observed.[72] In our experiment, the CoSi phase should be

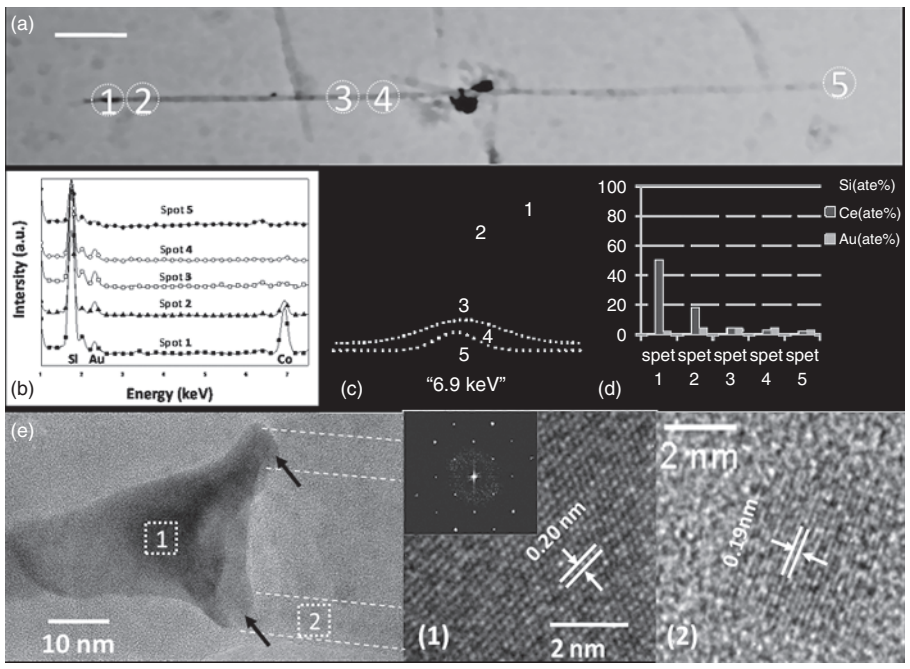

Figure 1.4 (a) TEM image of a single nanotube with one end sealed, characterized by compositional measurements (circled numbers highlight the areas on which the electron beam was focused); (b) EDS spectra taken from the five positions; (c) enlarged view of Co peak at ~6.93 keV; (d) histograms of atomic ratios of Co, Si, and Au; (e) HRTEM image of solid end and tube wall with enlarged inserts from selected regions, respectively (dashed lines represent the Si tube wall). (Reproduced from *Nanotechnology* 2010, 21, 066503 (6 pp), Copyright © 2010, IOP Publishing Ltd.[70])

the dominant compound since it is more stable in thin films than is Co_2Si or $CoSi_2$ at 500°C.

1.2.2.3 Control of Wall Thickness of Si Nanotube Control of wall thickness of polycrystalline Si nanotubes was achieved experimentally in 45 nm pore diameter AAO by adjusting the partial pressure of SiH_4 at a given temperature (500°C) and using a fixed growth period (30 min). Obviously, there is an increase in wall thickness with increasing pressure, shown as the measured curve and corresponding TEM images of each measured sample in Figure 1.5. With the other conditions unchanged, an increase of the SiH_4 partial pressure increases the growth rate. With the highest partial pressure of 0.75 Torr, the thickness of the Si approached 10 nm. The growth might be explained analogically to the experiments by Kamins et al., who used a silicide forming metal as catalyst for nanowire growth.[11] Initially, the metal (Ti or Co) reacts to form a silicide. With the Si supply continued, the Co nanoparticles are consumed with a higher Si supersaturation required. It is possibly related to the limited diffusion rate of Co into the Si at a given temperature with the Co/Si system as well. No further Si could be catalyzed from the precursor when the wall of Si nanotube approached its maximum thickness. The wall thickness was found to be homogeneous, although the thickness of the self-catalyzed Si growth was confirmed to be a function of distance to the AAO surface.

1.2.3 AAO as Template for Si Nanowire Epitaxy

Thermal and chemical stabilities of AAO are high enough for VLS growth of Si nanowires (NWs), since the main component is a stable material. Early experiments using AAO as templates to grow semiconductor nanowires have been undertaken with freestanding membrane without epitaxy.[73,74] Ordered vertical nanowires would allow a higher packing density than the presently used lateral structures. If nanowires are grown epitaxially on the substrate from defined catalyst locations, for integration convenience, the wires can be left in place, and the contacts can be postprocessed to the exposed top of the wires. One approach utilized a thin aluminum film on a conductive substrate:[75] the electrochemical formation of aluminum oxide stops as soon as all Al metal is consumed, and the thinner AAO barrier layer formed on the conductive material can be removed by chemical etching. In this case, the AAO membranes are fitting and connected to the substrate. If the thin Al film is deposited on the Si substrate and anodized, the ordering of AAO is difficult to achieve because of the complicated surface roughness and nonuniform crystallite size. The surface condition of the Al film will directly affect the ordering of the grown nanopore arrays. However, with pore formation guided by lithographic or imprinted surface patterns, controlled pore ordering and independently controlled pore spacing can be realized.[76] Another big advantage of a fixed AAO membrane on a substrate is that the AAO nanopores can be used as templates to control the epitaxial growth direction of semiconductor nanowires perpendicular to the substrate surface, even if the direction is not a preferred orientation of nanowire growth in free space.

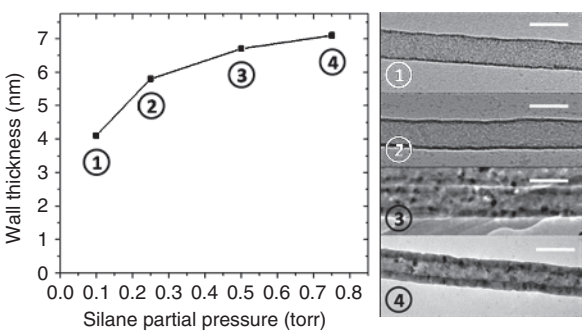

Figure 1.5 Variation in wall thickness of SiNTs versus silane partial pressure at 500°C; TEM images of Si nanotubes grown at pressures from 0.1 to 0.75 Torr (scale bars = 50 nm).

1.2.3.1 AAO Anodization on Si Substrate Figure 1.6a is a schematic illustration of Al anodization on Si substrate, the barrier layer formation, and the morphology of the AAO/Si interface after removal of the barriers. First, a thin Al layer (thickness <1 μm) was sputtered onto the H-terminated *n*-type Si(100) substrate. A standard anodization for the fabrication of AAO with 40 nm pore diameter was performed. The pore formation process proceeds with a thick barrier layer underneath as shown in Figure 1.6b. Normal anodization ceases as soon as the Al below the center of the pore is oxidized. The anodization can be continued until it consumes all of the aluminum beneath the barriers. When this process is continued, the resulting oxide barrier layer structure at the bottom of the pores is, as shown in Figure 1.6c, quite different from the morphology in the bulk aluminum. A void structure is observed beneath a thin arch-shape barrier layer bended upward at the end of each pore. Forces on preexisting oxide by newly formed oxide combined with geometric conditions produce the upward bending. In conclusion, anodization of an Al film on a conducting Si substrate has two main peculiarities: (1) the void beneath the insulating arch-shape barrier alumina layer is easy to remove without obvious widening of the pore diameter and (2) the Si surface reacts electrochemically in a controllable manner, and its oxide thickness can be selected by monitoring the anodization current–time (I–t) curve after the anodization of Al is complete. In this process, proper switchoff time is crucial in order to avoid the detachment of the AAO from the Si substrate after removing the SiO_2 layer. Inhomogeneities of Al metal film

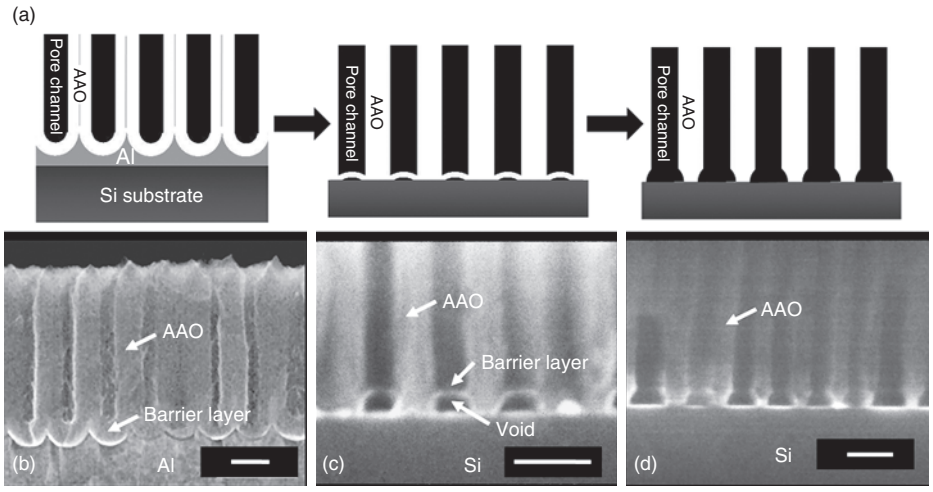

Figure 1.6 (a) Schematic illustration of AAO anodization on Si substrate, barrier layer formation, and pore opening by etching off the barriers; (b–d) side-view SEM images corresponding to each single process illustrated in (a), respectively (all scale bars = 100 nm).

thickness and of current density during anodization result in different optimum anodization times required at different positions of the sample.

1.2.3.2 Epitaxial Growth with Controllable Growth Direction One specific target is the realization of epitaxial Si nanowire growth on Si substrate with controllable growth direction. Moreover, the diameter of the nanowires has to be as small as possible, in particular <25 nm. Generally, it is difficult to obtain epitaxial growth of embedded material in the AAO nanopores, since an amorphous layer called the *barrier layer* exists at each nanopore bottom. There are two basic approaches to removal of the AAO barrier layer:

1. Separating the AAO membrane from the Al bulk by selective chemical etching of Al. After this separation process, the end of the AAO membrane with the barrier layer is etched away, and continuous pores are prepared as shown in Figure 1.7a. Putting this AAO membrane on a substrate, it can be used as shadow mask for evaporation to form nanodot arrays directly on the substrate. Lombardi et al. prepared gold (Au) nanodot arrays on a Si(111) substrate by this method.[77] They utilized the Au dots as catalyst for VLS growth of Si after removal of the AAO membrane from the substrate. They succeeded in preparation of a vertically grown epitaxial Si[111] on a Si(111) substrate as illustrated in Figure 1.7b. AAO membrane grown by this method usually have micrometer-scale gradual roughness. Therefore, the membrane is not suitable for template growth of epitaxial nanowires, because only small areas are connected to the AAO membrane.

2. Using a thin aluminum film on a conductive substrate. The electrochemical formation of aluminum oxide ceases as soon as all Al metal is consumed. The thinner AAO barrier formed on the conductive material is removed by selective chemical etching. In this case, the AAO membranes are fitted and connected to the substrate. Shimizu et al. prepared AAO membrane directly on two types of substrate, in particular Si(100) and Au films as catalyst on Si(100).[60,78]

The processes are schematically shown in Figure 1.7c and 1.7d, respectively. In the electroless Au plating cases as illustrated in Figure 1.7d, catalyst Au for VLS growth was selectively deposited on Si surface at the bottom of the AAO pore, and formed Au particles directly on Si(100) substrate. Epitaxial growth of Si(100) nanowires were observed in both cases. The HF acid contained in the electroless Au plating solution facilitates direct contact between Au and Si. One problem that should be mentioned here is that, when this anodization process is done with a thin evaporated film of Al on *p*-type Si(100) wafer with a doping level of $\leq$0.001 Ω·cm, the pore formation process proceeds until it consumes all of the Al and stops at the Al-Si interface. Afterward, both oxalic and sulfuric acid solutions will react unfavorably with such *p*-type Si at any anodization voltage, and anodic silicon oxide is produced unless an intermediate layer was used to protect the substrate before the Al deposition. However, such a protective layer needs to be thin and homogeneous, which is technically difficult to achieve.

1.2.3.3 AAO Bonding As mentioned previously, the approach of anodizing an Al layer on the Si substrate has two main drawbacks: (1) a good ordering of AAO pores requires a long-term etching and a thick and smooth Al film, which could not be obtained with available equipment; and (2) the undesired anodization of Si leads to a rough Si

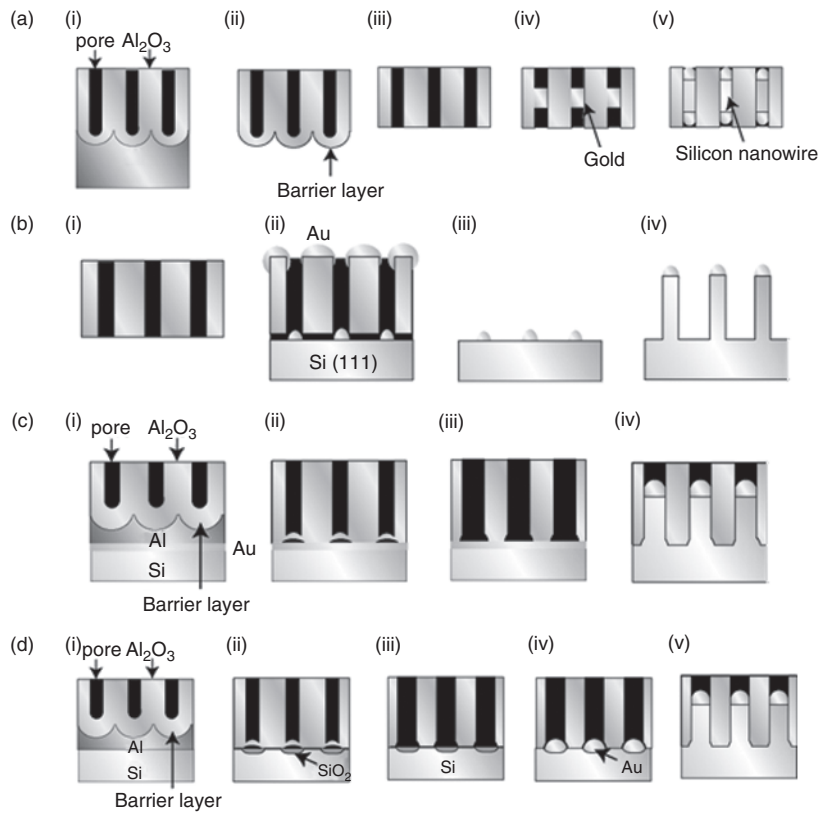

Figure 1.7 Schematic drawings of (a) freestanding AAO as template for Au-catalyzed Si nanowire growth; (b) AAO membrane as shadow mask for Au evaporation to form nanodot arrays for nanowire growth; (c) AAO directly grown on Au/Si substrate for Si nanowire epitaxy; (d) Au electroless plating and Si nanowire epitaxial growth in an AAO template.

surface with dimples beneath each pore bottom. A new method was invented, based on the idea of processing a freestanding AAO membrane and bonding the thin membrane onto a Si wafer. Instead of filling the pores with an etching solution and simultaneously etching pore walls and the barrier at the pore bottom, a freestanding AAO membrane can be floated on an etching solution, and only the barrier layer contacts the chemicals.

In order to realize a freestanding continuously open AAO membrane bonded onto Si substrate, a polymer-assisted method was used as illustrated in Figure 1.8a. First, a thin AAO film was synthesized by the standard two-step anodization process as step 1. Here we show one sample as an example, because different electrochemical parameters correspond to different pore diameters and interpore distances. Following application of a constant voltage of 25 V in 0.3 M H_2SO_4 acid (3°C), the first anodization lasted for 24 h. Then, the oxide layer was completely removed by wet etching (a mixture of 1.8 wt% chromic acid and 6 wt% phosphoric acid) at 45°C to obtain a textured surface on Al. The second anodization was conducted with the same parameters as the first one, and lasted for only 180 s for an oxide thickness of ~100 nm. A spin coating process (step 2) was used to fill into the pores a thin layer of polystyrene (PS), which attached homogeneously to AAO after spinning at 3000 rpm (rev/min) for 60 s using 1.5 wt% PS/$CHCl_3$ solution, followed by a 90°C solidification heating. The protection layer of PS enhances the buoyancy of AAO, and its hydrophobic nature enables the remaining Al substrate to be etched completely by floating on a mixture of $CuCl_2$ and HCl solutions. It should be pointed out that the thin PS film prevents the thin ceramic membrane from mechanical deformation. The integral structure can be retained during handling and transfer. After removal of Al, the barrier layer was selectively etched by changing the etching solution to 5% H_3PO_4 at 30°C for 15 min (step 3). Since the whole pores were filled by PS, the side effect of pore widening was avoided. The whole PS/AAO membrane still floating on the surface of deionized water was transferred to a desired substrate such as Si (step 4). One sample is shown in Figure 1.8b, a tilted side-view SEM image. The AAO has a thickness of around 100 nm with a homogeneous 30-nm-thick PS film covering the surface. The pores are

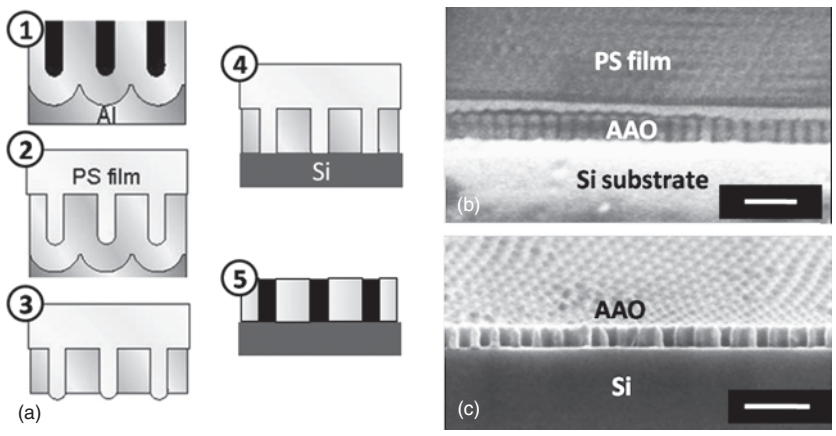

Figure 1.8 Thin AAO membrane bonded onto Si substrate: (a) Fabrication scheme: (1) thin AAO film on Al with high ordering, (2) spin coating of PS film, (3) selective etching of Al substrate and barrier layer, (4) transfer of AAO membrane onto Si substrate, (5) removal of PS; (b) tilted side-view SEM image of AAO/PS bonded on Si as in step 4 (scale bar = 100 nm.); (c) tilted side-view SEM image of sample; (b) after step 5, scale bar = 150 nm.

sealed and attached to the Si surface. The exterior PS film can be removed by a $CHCl_3$ washing, and the PS inside the pores can be further dissolved with an immersion into $CHCl_3$ or vacuum pyrolysis. This process (step 5) not only eliminates the PS but also enables the conformal contact of the AAO bottom side with the flat Si surface (shown in Figure 1.8c). The pores are oriented along the normal of the substrate.

The van der Waals forces at the interface exhibit an excellent contact that can even survive evacuation. The thickness of an AAO film produced with sulfuric acid anodization should not exceed 250 nm, which corresponds to a pore length/diameter ratio of 10. The same ratio limitation was found in the case of oxalic acid, with a 40 nm pore diameter. Beyond this ratio, the PS always filled the pores only incompletely, and conformal contact was impossible because of surface roughness after selective etching. The analysis of pore morphologies of the two AAO/Si integration methods, as shown in Figure 1.9, demonstrates the advantages of the new method. Using the direct growth of Al on Si substrate method (Figure 1.9a) with a short first (initial) anodization, the self-ordering is quite limited, and the pore diameters have a distribution factor (i.e., the full-width at half-maximum (FWHM)/mean diameter ratio) of >40%. Partial pores are branched, and are not perpendicular to the substrate. The new method of thin AAO film bonded onto Si inherits the highly self-ordered pore arrangement caused by a long first anodization (Figure 1.9b). While keeping the mean diameter with the same potentiostatic voltage, the pore diameter has a narrow size distribution of ∼10%. Judged from the top-view SEM image, the pores are all perpendicular to the substrate and they form close-packed hexagonal array.

1.2.3.4 Bottom Imprint Method The central idea of our approach is to bond a AAO thin film directly onto the Si substrate with a predeposited catalyst film, forming tight and conformal contact. Under proper temperature and load, it is possible to imprint the bottom structure of the AAO template into the metal film to form homogeneously separated nanoparticle arrays. Finally, with a UHV-CVD process, Si nanowires grow epitaxially inside the pores with the same ordering and size distribution as the template.

The bottom imprint (BI) method used to synthesize ordered Si[100] nanowire arrays is schematically depicted in Figure 1.10. In step (i), an H-terminated Si substrate was covered with a homogeneous catalyst film through UHV thermal evaporation. The thickness of this metallic deposit was adjusted according to different pore sizes of AAO templates. Au and Al films with ∼10 nm thickness were realized with negligible surface roughness at room temperature. Thus, the Si beneath the catalyst layer was protected against the oxidization when it was removed from the UHV chamber temporarily. In step (ii), an AAO template with a PS protective layer was bonded onto the desired substrate as described previously. The pores are filled with PS completely in order to prevent pore widening during the selective etching of the barrier layer. To obtain an adequate imprint, the fragile AAO thin film must be partially elastic to enable conformal contact on the substrate surface, which means that it must adapt flexibly without leaving voids created by the natural roughness of the substrate and itself. A polymer material can play such a role to increase the conformal contacting area. In step (iii) the difference in hardness between AAO and plastic metals (e.g., Au, Al, Ag) allows AAO to be used as an imprint stamp. Both Young's modulus and hardness of the

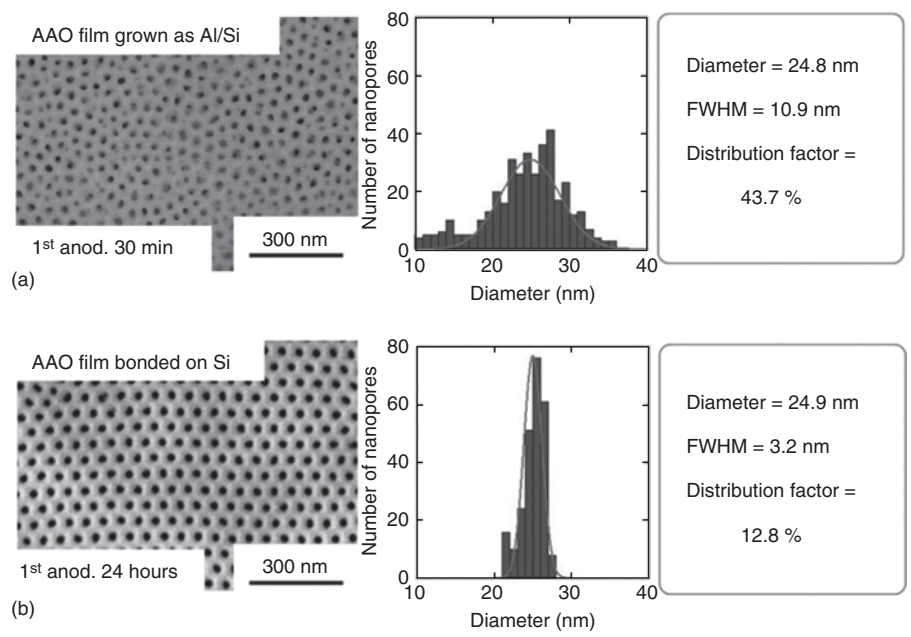

Figure 1.9 Comparison of two methods for AAO/Si integration: (a) anodization of Al film deposited directly on Si substrate; (b) thin film of AAO bonded on Si substrate. *Left*—top-view SEM images of pore morphologies with first anodization of 30 min and 24 h; *right*—size distribution diagrams together with key parameters.

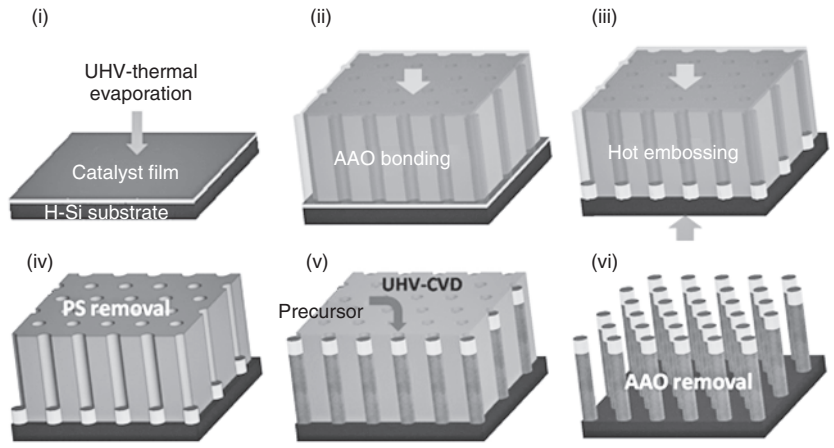

Figure 1.10 Schematic diagram of the bottom imprint method workflow: (i) covering the H-terminated single-crystal Si substrate with catalyst film by UHV thermal evaporation; (ii) bonding PS-filled AAO membrane onto catalyst film; (iii) hot embossing of catalyst film into separated nanoparticle array by imprinting with bottom pattern of AAO; (iv) removal of PS inside pores by organic solution; (v) epitaxial growth of semiconductor nanowire arrays inside template with catalyst tips; (vi) removal of AAO template by selective chemical etching. (Reproduced from *Adv. Mater*. 2009, *21*, 4701. Copyright © 2009, Wiley-VCH.[81])

metals decrease as the temperature and indentation load increase, and the process shown in step (iii) was optimized by slightly heating the press.[79] During the hot-embossing process, only the bottom side of the press was heated, and the temperature of the sample was slightly lower than the melting point of PS (240°C). Thus, the metal could enter and occupy the space inside the pores by deforming the softened PS at the base. With the help of the polymer filling, the extruded metallic catalysts were isolated from each other by the alumina. The polymer prevented oxidization of the Si surface beneath the metal layer during the whole process. Finally, the surrounding alumina wall was

connected with the silicon substrate tightly, and the metal film was patterned exactly into the hexagonally ordered porous structure of the AAO template. In step (iv) (of Figure 1.10), the PS was removed by organic solvents, and then the sample was inserted into the UHV system. Specific care should be taken in removal of PS. High-purity (99.9%) chloroform was used to prevent oxidation at the metal/Si interface, and the sample was transferred into the load-lock chamber immediately after the chloroform dipping. In step (v), the metal nanoparticles sitting at the bottom of the pores acted as catalyst to crack the precursor gas, which finally formed the epitaxial semiconductor nanowire arrays along the pores with catalyst tips. In step (vi), AAO could be removed with selective chemical etching; thus we finally get the vertically-aligned epitaxial nanowire arrays directly on Si substrate with the same ordering and size distribution as the template.

1.2.3.5 Au as a Catalyst with BI Figure 1.11a shows a cross-sectional structure of a bonded AAO template on Si(100) substrate before the imprint. The PS has been removed from the side surface by O_2 plasma etching to enhance the contrast of the pore structure of AAO with SEM characterization. From the distinct contrast difference, we identify that a 300-nm-thick, 40-nm-pore-diameter AAO film tightly bonds with a homogeneous 30-nm-thick Au film on Si substrate. No voids or remaining barrier layers were observed in between these two bonded surfaces. After imprinting and removing of the PS from the surface, part of the AAO was detached by an adhesive tape to reveal the Au morphology underneath (Figure 1.11b). Caused by the force applied during liftoff of the adhesive tape, some PS pillars are left over from the pores, remaining on the substrate as milky areas. The insert is an enlarged top-view image, the bright contrast of which corresponds to the Au catalysts formed inside the base of AAO pores, and the dark contrast in between represents the bare surface of the Si substrate. It was confirmed that, working as a stamp, the AAO imprints on the Au film in its hexagonally close-packed pattern, and the Au nanoparticles were separated from each other since the AAO was connected with Si directly by the indentation.

In a steady VLS process, the small AuSi liquid droplet moves upward from the Si surface along the vertically aligned pore of AAO. For a 40-nm-pore-diameter, 300-nm-thick AAO template, the growth rate of Si was 10–12 nm/min at a growth temperature of 400°C and a total pressure of 1.0 Torr which contained a gas mixture of 5% SiH_4 and 95% Ar.[80] The tight and conformal connection of the bottom side of AAO with the Si surface prevents the agglomeration of Au-Si droplets during the heating process, which caused some problems in an earlier experiment.[78] Figure 1.12a shows a cross-sectional TEM image of the Si nanowire array after removal of the AAO. The horizontal dashed line indicates the surface of the original Si(100) substrate. From the contrast difference between Si and SiO_2 which was deposited as a protection layer during the focused ion beam (FIB) sample preparation, the two parallel dashed lines indicate the sidewalls of one single Si nanowire with Au cap. All the nanowires revealed in this image have similar growth height of ~220 nm, and all are connected to Au caps in dark contrast at the top side. Moreover, some small Au nanoparticles were observed on the substrate, under the bottom surface of AAO, but no obvious Au was visible in the Si nanowires. The interfacial region is revealed by a HRTEM image in Figure 1.12b. The fast Fourier transform (FFT) patterns from three representative regions along the wire are shown as inserts, respectively. It was confirmed that the Si nanowires grew epitaxially on the Si(100) substrate, and the growth direction was parallel to the [100] direction, since the FFT in each insert is exactly the same viewed along a [011] zone axis. A deformation observed at the bottom part of the nanowire was caused by the indentation of the AAO on Si. Thus, there is a smaller diameter at the base of the nanowire,

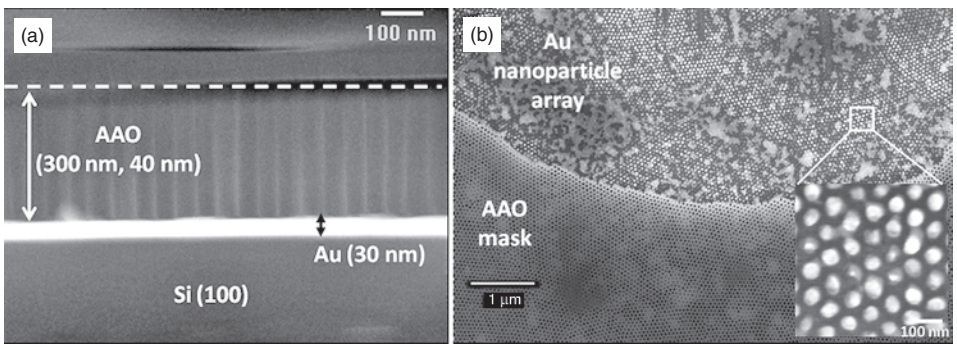

Figure 1.11 (a) Cross-sectional SEM image of bonded AAO thin film on Au/Si(100) substrate before BI, where dashed line indicates top side of AAO sealed by PS layer; (b) top-view SEM image of Au nanoparticle array with AAO film partially detached by an adhesive tape; inset is an enlarged view of the selected area.

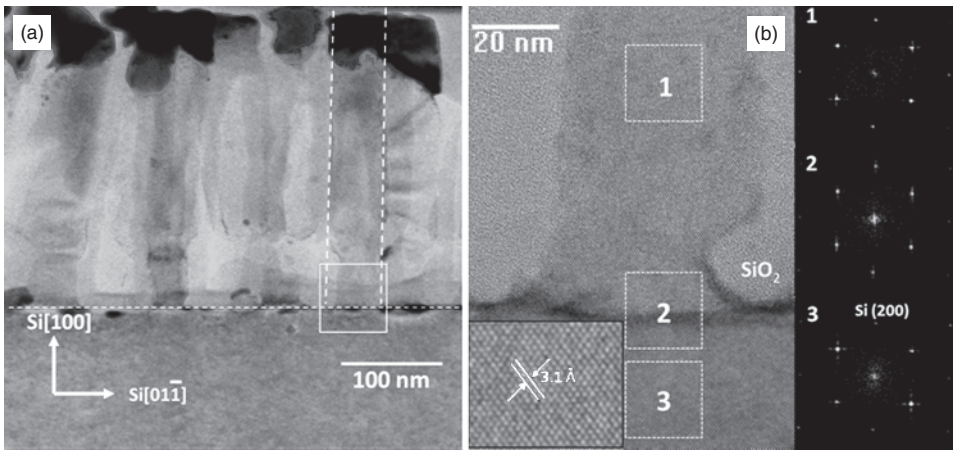

Figure 1.12 (a) Cross-sectional TEM image of the Si nanowire array after removal of the AAO template. The horizontal dashed line indicates the surface of the Si(100), and the two parallel lines outline an integral nanowire. (b) The HRTEM image shows the bottom side connected to the Si substrate, with insets 1–3 showing fast Fourier transforms of the numerically corresponding square regions. (Reproduced from *Adv. Mater*. 2009, *21*, 2824. Copyright © 2009, Wiley-VCH.[80])

which is opposite to the scenario observed in AAO grown directly on Si substrate. At 20 nm above the interface, the nanowire grows with constant diameter during the whole VLS process with the Au tip moving up along the pore. The insert is an enlarged HRTEM from the interface, in which the Si{111} lattice planes are continuous with a measured lattice distance of 3.1 Å, and no dislocations were observed.

1.2.3.6 Al as a Catalyst with BI Aluminum creates an impurity level only close to the valence band of Si with better compatibility to the standard CMOS process lines, although it is accompanied by *p*-type doping. Whether the *p*-type doping introduced into the Al-catalyzed Si nanowire growth is an advantage or disadvantage depends on specific applications; however, further experimentation to control the shape and crystallographic structure of these nanowires is highly essential since the electrical and optical properties strongly depend on these parameters. Vertically oriented, well-ordered nanowire arrays with Al as catalyst grown at low temperature by the bottom imprint (BI) method can be potentially useful in ultra-high-density nanoscale devices compatible with CMOS processing. The BI method uses a highly ordered AAO membrane as an imprint stamp and, in principle, can be combined with other plastic metal catalysts such as Al. With the BI method, any crystallographic orientation of Si substrate can be used, and the epitaxial Si nanowire arrays are perpendicular to the substrate in a good ordering.[81] The surface of the metal Al film is covered by a thin native oxide layer after exposure to air, beneath which the Al and Si are protected from further oxidization after temporary removal from the UHV chamber temporarily. Figure 1.13a shows a homogeneous Al film of 20 nm thickness that was deposited onto an H-terminated Si substrate by MBE under a vacuum of 5×10^{-10} mbar. The AAO membrane with a pore diameter of 20 nm was bonded tightly onto the Al film. With the BI, the bottom surface of AAO is pressed into the Al layer on Si surface, and the Al film is transformed into

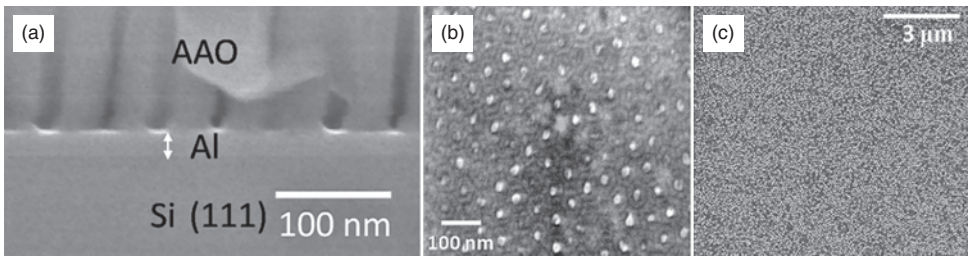

Figure 1.13 (a) Cross-sectional SEM image of sample before BI, with a homogeneous Al film sandwiched between AAO with 20 nm pore diameter and Si(111) substrate; (b) top-view image with AAO partially removed by adhesive tape after BI; (c) low-magnification view of Al nanoparticle array imprinted by 45 nm pore diameter AAO with a homogeneous imprint area of $10 \times 10\ \mu m^2$.

an array of Al islands. As shown in Figure 1.13b, the AAO was removed by a gluing tape in order to reveal more morphologic details. The hexagonal imprint mark on Si is a copy pattern of the AAO bottom surface with sharp edges by the indentation. The low-magnification view shows that the homogeneous imprint area can reach up to a $10 \times 10\ \mu m^2$ (Figure 1.13c).

Deep levels can be caused not only by impurities but also by point defects or spatially extended defects. Examples for extended defects are dislocations and nanowire surfaces. The crystallographic structure of Al-catalyzed Si nanowires using the BI method was substantiated by using HRTEM microscopy. The wire substrate and the wire-catalyst interfaces from individual wires on both (111) and (100) substrates were investigated, and are shown in Figure 1.14a–d, respectively. Distinguished from the surrounding SiO_2 amorphous layer, the tips are outlined in Figure 1.14a,c. The FFT pattern close to the tip in Figure 1.14a reveals that a twin defect exists. Comparing with wires grown in free space,[82] we believe that the defects are on the top side of the wires, due to the final cooling procedure. If we assume that the defects were caused by the stress difference between Al and Si due to the VSS process, such defects should be found along the whole wire, not only on the top side. In contrast, in Figure 1.14c, two planar twin defects with a cross angle of 71° are observed, identical with the angle between two {111} planes in the [011] viewing direction. These two defects extend from the tip to the surface of the wire body, which are $(11\bar{1})$ and $(1\bar{1}1)$ twin planes marked with the arrows. We checked other wires on the TEM samples, and more twin defects were observed in the [100]-oriented Si nanowires compared with the [111]-oriented ones. Without the template confinement, these defects cause the wormlike freestanding epitaxial growth of Si nanowire on Si(100) substrate. Stresses are caused by the lateral forces on the solid Al catalyst extruding through the inner walls of AAO while moving up along the pore. However, in the Au-catalyzed VLS growth on Si(100) using BI, as shown in Figure 1.14e, as long as the liquid Au/Si tip is inside the template, the shape of the catalyst is confined to the diameter of the pore. In this wire, the interface of Au and Si has a 22° tilt parallel to the substrate, which is perpendicular to the [110] direction of the Au crystal estimated by the FFT patterns from Au tip in the selected region. The stresses accumulated by the confinement of AAO could be released through the deformation of liquid Au/Si alloy without introducing further structural defects into the Si growth. The surface depletion region can compensate for shallow dopants and, as a consequence, reduce the conductivity. Recombination occurring on the nanowire surface can drastically degrade the performance of minority-carrier devices such as light emitting diodes, lasers, and bipolar transistors.

The BI method has several advantages: (1) a well-arranged positioning and control of the crystallographic

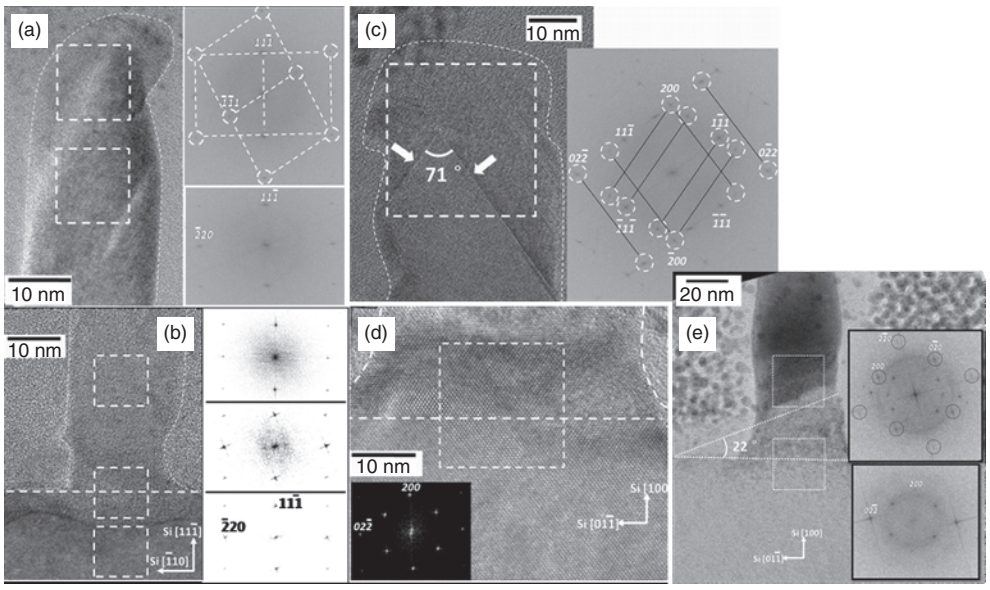

Figure 1.14 Cross-sectional HRTEM images taken with the electron beam parallel to the [112] and [011] directions of Si(111) (a,b) and Si(100) (c–e) substrates, respectively. Insets of FFT patterns in all these figures are from the selected dashed square regions, respectively. The outlines of wires are profiled by the dashed curves; the horizontal dashed lines at the base of wires indicate the surface position of Si substrates. (Reproduced from *Adv. Mater*. 2009, *21*, 4701. Copyright © 2009, Wiley-VCH.[81])

orientation of the vertically standing epitaxial semiconductor nanowire arrays on Si, thus avoiding any annealing process of the AAO >900°C; (2) adjustable diameter of nanowires from 20 nm to 45 nm with a narrow size distribution (<10%) according to specific pore diameter in the AAO template; and (3) low-temperature growth (400°C) of Si nanowire arrays via a solid-phase Al catalyst with diameter and crystallographic orientation control.

1.3 CONCLUSION AND OUTLOOK

As a multifunctional porous template, the synthesis of ultrathin AAO membranes directly and indirectly combined with Si substrates was studied. Specifically for AAO directly grown on Si substrate, the growth mechanism with upward bending of the barrier layer and the effect of subsequent HF treatment was studied. The drawbacks of this approach, widening of the pores and anodizing the surface of Si, stimulated the development of a polymer-assisted method of bonding a freestanding AAO membrane onto the Si substrate. Integration of semiconductor nanowires on the Si platform is one of the essential issues for device applications. Therefore, control of growth direction, positioning, diameter, and catalytic material of semiconductor nanowire arrays were discussed in this chapter. A new method was presented. Highly ordered AAO thin films were used as both porous pattered mold and growth template. This improved the controllable growth of ordered epitaxial semiconductor nanowire arrays. Most importantly, it was successfully extended to the growth of Al-catalyzed Si nanowires in the low-temperature vapor–solid–solid (VSS) growth mode.

Still, our understanding of 1D semiconductor nanostructure growth mechanisms, as well as the effective characterization of their physical properties, is incomplete. The state-of-the-art growth techniques offer limited control of structural and crystallographic properties, especially at doping. Efforts to improve synthesis techniques have stimulated 1D nanomaterial research, and the need for sufficient understanding of their unique properties is the driving force behind the semiconductor nanowire-based device applications.

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