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SILICON PHOTONICS

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1.1 INTRODUCTION

Since the beginning of the century, silicon photonics has grown from a niche research field to a field with strong industrial interest and several near-future applications [1, 2]. This rapid growth can be attributed to several unique characteristics of silicon photonics. First of all, the use of silicon makes it possible to make photonic integrated circuits (PICs) with much smaller building blocks than in other material systems [3]. This enables smaller chips, but also more complex photonic circuits. Also, silicon is the base material for electronic circuits, and huge investments in manufacturing technology can be put to work to make photonic circuits. This offers a route to high volume, low cost photonic circuits that could be applied in many applications in sensing [4, 5] and optical communication [6, 7].

In this chapter, we will discuss current state of the art in silicon photonics. We will look a bit closer in the applications, and from that we derive the functions needed on the chip. Finally, we discuss the technology implementations.

1.2 APPLICATIONS

1.2.1 Interconnects

Integrated photonics has been mainly used for applications in optical communication, especially in telecom backbone and metro networks. The advent of silicon photonics

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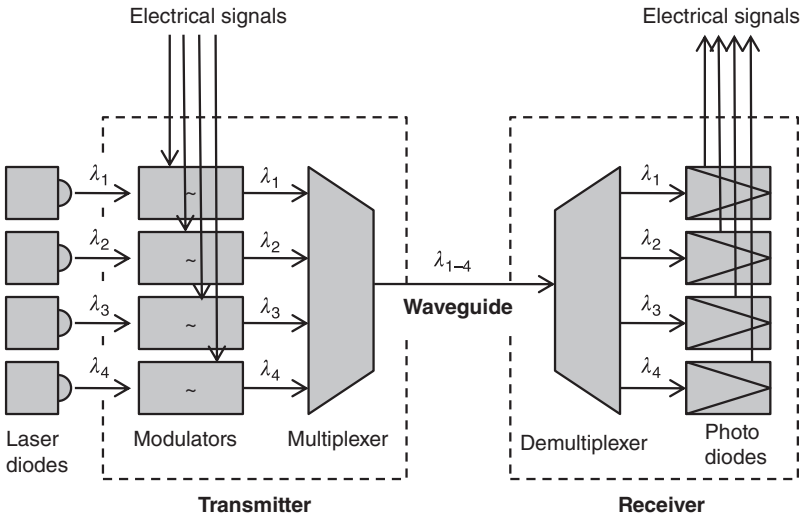

FIGURE 1.1 A WDM optical interconnection.

and its potential for low cost and low power transceiver chips has opened up new, shorter-range interconnect applications in high-performance computing and datacenters [8,9]. Silicon photonic chips might turn out to be a game-changer in interconnects on an even smaller scale: it is the first technology that can offer an attractive solution to solve the off-chip bandwidth bottleneck [10].

Typical optical links involve light sources, signal modulators, a waveguide medium, and a photodetector. These individual functions are described in Section 1.3. In the case of wavelength-division multiplexing (WDM), signals are encoded onto different carrier wavelengths, which are multiplexed into the same waveguide. This technique, illustrated in Figure 1.1, is widely used to increase the bandwidth of optical links. As we will see in Section 1.3.2, silicon photonics can implement WDM filters with a very small footprint.

1.2.2 Sensors and Spectroscopy

Another application field where silicon photonics can enable unique capabilities is that of sensing. As we will see later in this chapter, silicon waveguides can be extremely sensitive to different effects, such as temperature, cladding index [11], strain [12] and deposition of layers [13]. Especially the latter is important, as proper surface chemistry enables selective response to specific effects or molecules, enabling biosensors [5] or specific gas sensors [14]. In addition to high sensitivity, the technology offers integration of many sensor functions on a single chip, potentially with the inclusion of the read-out circuitry. Some examples of photonic sensors that could be integrated on a silicon chip are shown in Figure 1.2: A ring resonator could be

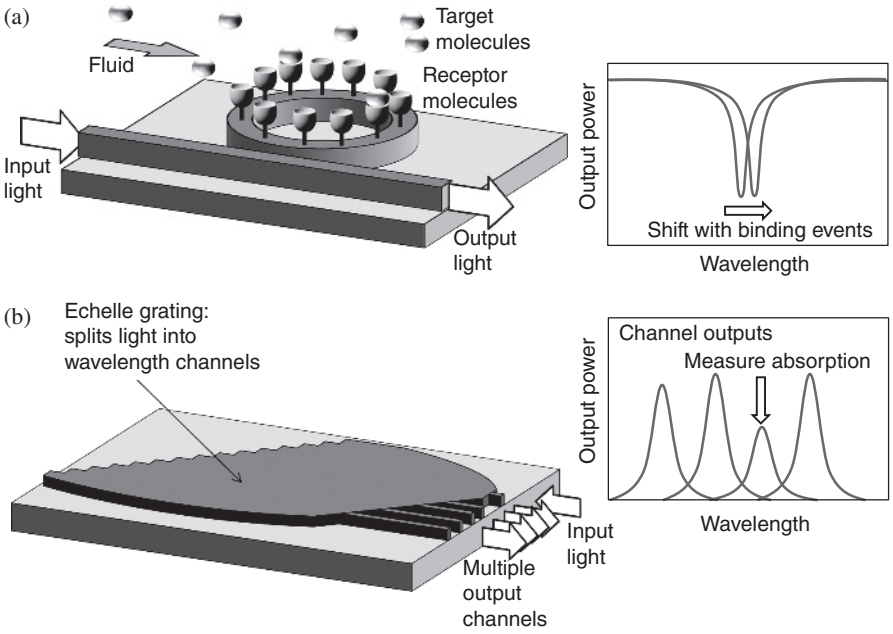

FIGURE 1.2 Two examples of silicon-photonics-based sensor systems. (a) A ring-resonator-based biosensor [4] and (b) an on-chip spectrometer [15].

used to capture selective molecular binding events and thus measure concentrations of specific (bio)molecules in a medium. Or, wavelength filters of multiplexers could be used to make a spectrometer that could be used for a variety of spectroscopic measurement systems [15].

1.3 OPTICAL FUNCTIONS

A PIC can accommodate many different optical functions. The most common functions have to do with transport of light, wavelength filtering and coupling to off-chip elements and fibers. These are called passive functions, as light is typically not altered in the process. Active functions involve electro-optic elements such as light sources, signal modulators, and photodetectors. We will discuss these functions and the state of the art in terms of performance that has been demonstrated in silicon photonics. The actual technology is discussed in Section 1.4

1.3.1 Waveguides and Routing

The key optical function on a PIC is guiding light between parts on a chip. An optical waveguide consists of a high-index core surrounded by a lower-index cladding. The

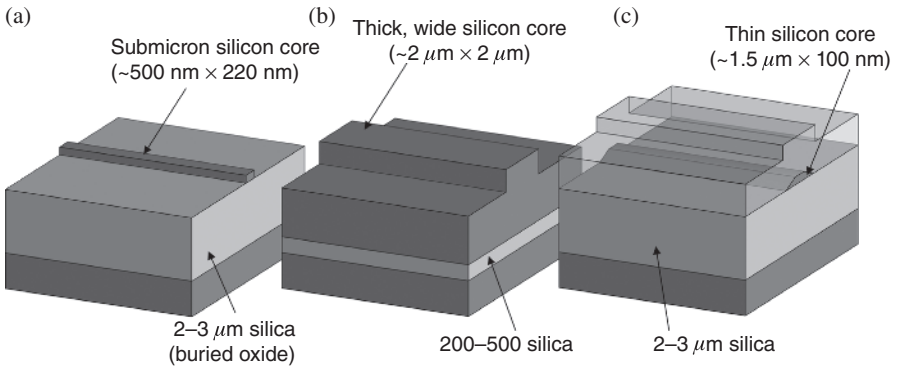

FIGURE 1.3 Silicon waveguides: (a) small-core photonic wires [17], (b) large-core rib waveguides [20], and (c) oxidized waveguide [23].

higher the index contrast, the more compact you can make the waveguide core. As it is, silicon has a very high refractive index in the regime where it is transparent (wavelength $> 1.2\,\mu$m). This way, it is possible to make high contrast waveguides with core dimensions down to 200–500 nm, using a cladding oxide ($n = 1.45$) or air ($n = 1.0$) [3, 16]. Such waveguides, often called photonic wires, can have bend radii of only a few micrometers with low loss [17].

Apart from photonic wires, it is also possible to use silicon for large-core waveguides. Such waveguides are defined in silicon of several micrometers thick [18–20], and to obtain single-mode condition, they are only partially etched. Such waveguide is shown, together with a photonic wire waveguide, in Figure 1.3. Because the index contrast between the unetched core and the etched cladding is relatively low, such waveguides still require a large bend radius.

The key performance metic for optical waveguides is the propagation loss. Typical photonic wires have a loss of 1–2 dB/cm [16, 17, 21]. Large-core waveguides have a lower loss, on the order of 0.1 dB/cm [20]. To obtain lower loss in the small-code waveguide system, one can also use a shallow-etched rib waveguide geometry, which can reduce the losses with a factor of 3–4, but again with a penalty of larger bend radius [22].

Because waveguide losses are largely caused by scattering at etched sidewalls, alternative definition techniques can reduce the losses. For instance, waveguides can be defined by oxidation, which provides a smooth sidewall surface [23].

The high contrast and submicron dimensions of silicon photonic wire waveguides give them a rather strong dispersion. While the effective index of a 450 nm × 220 nm wire is around 2.4 (at 1550 nm wavelength), its group index is around 4.3. The tight confinement also makes these waveguides very susceptible to small variations, both in geometry and material parameters. A very small deviation of the width or height will have a significant effect on the effective index, to the extent that for some functions, nanometer-scale precision is required. Large-core waveguides, on the other hand, are much less sensitive to geometrical variations.

Small-core photonic wires are very birefringent. The TE and TM polarization have a very different effective index. While it is in theory possible to make a non-birefringent waveguide [24], the tolerances on the waveguide dimensions is extremely stringent. Therefore, photonic wire waveguide circuits are typically optimized to function at a single polarization only.

1.3.2 Wavelength Filtering

Wavelength filtering is one of the more common functions in photonic circuit. It is important for multiplexing and demultiplexing WDM channels, but wavelength filters are also often used for sensing applications. Wavelength filters can be implemented in various ways, but their operation is always based on interferometry. Different types of wavelength filters are shown in Figure 1.4.

Mach–Zehnder interferometers (MZIs) are by far the simplest filter in concept, and as any other waveguide component, they can benefit from small bends to obtain a reduced footprint. Also, the large group index of silicon wires will help, as the optical delay in an MZI will scale with the inverse of the group index.

Ring resonators are a very widely used structure in silicon photonics, because the rings can again be very compact [27]. In a ring, the light self-interferes to build up a resonance, so a much sharper filter characteristic can be obtained, compared to an MZI. The sharpness of the resonance is largely determined by the ring's losses, so the quality of the waveguide is important. Rings and Mach–Zehnders can actually be cascaded into more complex spectral filter structures to obtain sharper filter characteristics or flat transmission bands [26].

Instead of a single delay path, it is possible to use multiple delays. An arrayed waveguide grating (AWG) distributes light over many waveguides with a different delay, and by recombining the light in spherical phase front, the refocusing can be directed as a function of wavelength: this way, different wavelengths are routed to different output waveguides [28]. The same device can of course be used to combine wavelength channels into a single waveguide. Similarly, an echelle grating introduces multiple delays by etching a set of reflective facets in an unpatterned region of the silicon [25].

All these different filter types can be implemented in both small-core and large-core silicon waveguides, but of course the performance will differ. In large-core waveguides, the devices will have a much larger footprint, because both the waveguides and the bends are much larger. On the other hand, large-core waveguides will make it easier to have wavelength filters fabricated to match the design specifications. This is because these waveguides are much less sensitive to small geometric variations, and the effective index of the waveguides can be better controlled.

Photonic-wire-based wavelength filters can suffer easily from variability in the manufacturing process, where geometric changes of the order of 1 nm can already induce a wavelength shift of the same magnitude [29]. This makes it difficult to make absolute wavelength filters without some tuning or active feedback mechanisms, such as integrated heaters [30–32].

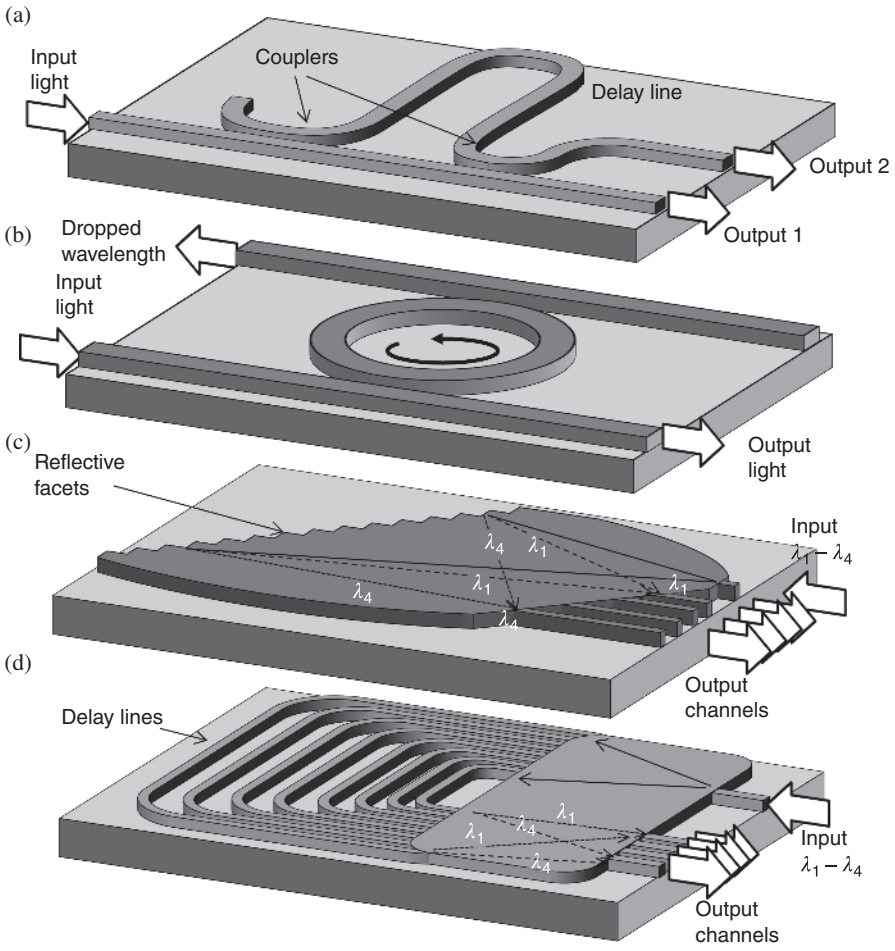

FIGURE 1.4 Wavelength filters implemented in silicon: (a) Mach–Zehnder interferometer, (b) ring resonator, (c) Echelle grating or planar concave grating [25], and (d) arrayed waveguide grating [26].

1.3.3 Coupling to Fiber

An essential function for many applications is efficient coupling to and from optical fibers. As single-mode fibers are still the standard transport medium for light, this means the optical mode in the silicon waveguide should be converted to a fiber mode. Several mechanisms are possible and the most common are illustrated in Figure 1.5.

For large-core silicon waveguides, the mismatch in mode profile is relatively small, and often a simple taper structure suffices to have an efficient butt-coupling between waveguides and fiber [33]. Instead of full-size single-mode fibers, the use of ultrahigh NA fibers, with a mode field diameter of about 3 μm, can relax the requirements for

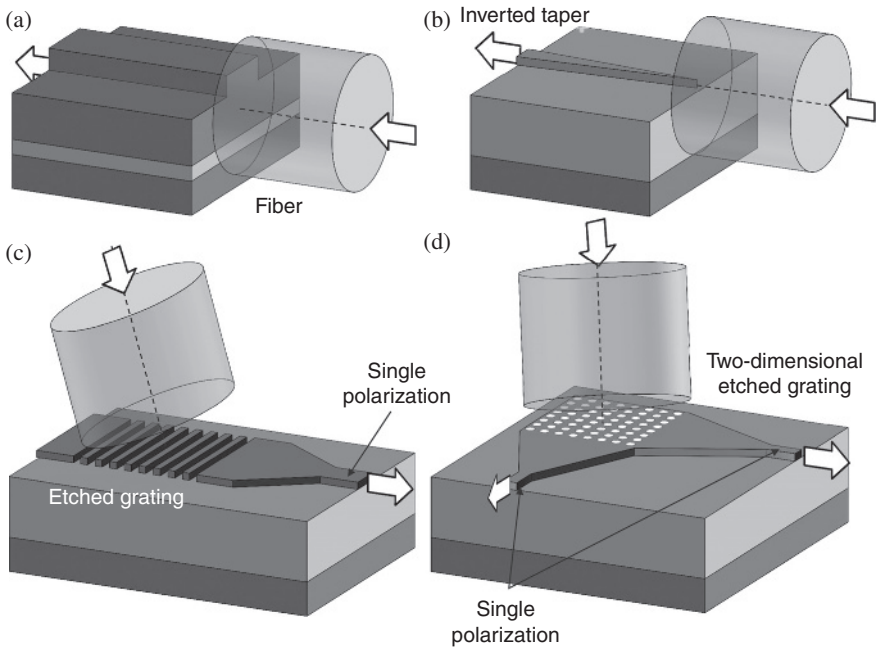

FIGURE 1.5 Coupling schemes for silicon photonic chips to and from optical fiber. (a) Edge coupling for large-core waveguides, (b) an inverted taper for edge coupling of photonic wires, (c) 1D grating coupler [34], and (d) a 2D grating coupler with polarization splitting [35].

the taper. The fibers can be mounted on the same substrate by etching V-grooves, which control the horizontal and vertical alignment.

For small-core silicon photonic wires, the mode mismatch is very large. Direct butt coupling would result in a coupling efficiency of only 0.1%. Expanding the mode of the wire waveguide in the lateral direction can be accomplished by defining a taper. However, the challenge is expanding the waveguide mode in the vertical direction. This can be accomplished by tapering the waveguide to a very narrow width, effectively pushing the mode towards cutoff and expelling it from the waveguide core. Such an inverted taper structure in the silicon can then be accompanied by a larger-core waveguide in a lower-index material (e.g., silicon oxynitride [24] or polymer [36] with a cross section that is matched to an ultra-high numerical aperture (UHNA) fiber). Such coupling structures have been demonstrated to achieve 95% coupling efficiency.

An important drawback of edge coupling mechanisms is that this can only be done after the wafer processing is complete and the devices have been diced, and if needed, facet-polished. This means that wafer-scale testing of devices is not possible.

The alternative to edge coupling is vertical coupling. For this, the most used component is a grating coupler [34]. A grating coupler is a diffraction grating that diffracts light from a fiber into an on-chip waveguide, or vice versa. Depending on the fabrication process, such gratings can have efficiencies upward of 50% [37, 38].

However, because of the birefringence of the silicon waveguides, such a grating coupler couples only to one fiber polarization. To couple both polarizations, a 2D grating can be used, which performs the same function for both fiber polarizations at the same time [35].

By diffracting the light immediately in a thin silicon waveguide, the grating coupler already performs a mode compression in the vertical direction. In the lateral direction, a taper can be used, or the grating coupler can be designed to have a focusing function [37,39]. This can even be done in two dimensions [37,40]. This way, a very compact footprint coupling structure is possible that allows for wafer-scale optical probing of a photonic chip.

The main drawback of grating couplers is that they have a limited wavelength bandwidth, as the operating principle is based on a diffractive grating. Typical 3 dB bandwidth is of the order of 60–80 nm.

1.3.4 Electro-Optic and Opto-Electronic Conversion

For active photonic circuits, efficient conversion of electrical signals to optical signals is needed. For electro-optic modulation, silicon is actually a poor material: it has no intrinsic electro-optic effects. Instead, indirect effects are needed to obtain a modulation of the optical properties. Such mechanisms include mechanical structures based on MEMS [41], thermal tuning using heaters [30, 42, 43], and electro-optic cladding materials such as liquid crystals [44]. These mechanisms are typically limited in operation speed and are used for tuning and switching rather than for signal modulation.

For high speed modulation, the most-adopted mechanism is carrier manipulation. The refractive index of silicon depends on the concentration of free electrons and holes [45]. The density of carriers can be electrically influenced by incorporating a junction or capacitor in the core of the waveguide [46]. The larger the spatial overlap of the carrier accumulation or depletion region with the optical mode of the waveguide, the stronger the modulation effect. The junction or capacitor can bet either horizontally or vertically oriented and are electrically connected to the metal interconnect layers, as illustrated in Figure 1.6.

The modulation of the carrier density will modulate the absorption in the waveguide, but the stronger effect is the modulation of the real part of the effective index [45]. Carrier-based silicon modulators are therefore more effective as a phase modulator rather than an amplitude modulator. To obtain amplitude modulation from a phase modulator, the phase shifter section should be embedded inside an interferometer or a resonator [46].

Carrier-based silicon modulators have now been demonstrated with quite good efficiency [46] and modulation speeds over 40 Gbps. Modulators can be implemented both in ring resonator configuration [47,48] and Mach–Zehnder configuration [49–51].

For the conversion of optical signals back into electrical signals, the common solution is the use of photodetectors. As silicon is transparent at the wavelengths used for telecommunication, another material should be introduced. This can be III-V semiconductor, which can be bonded onto the silicon [52], but the commonly accepted

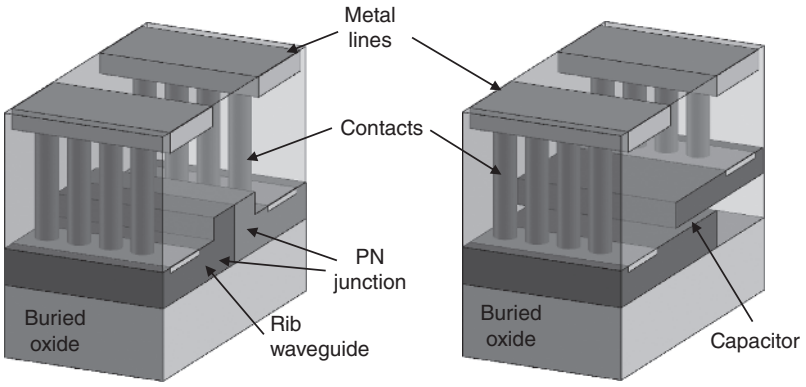

FIGURE 1.6 Different modulators in silicon. (a) P–N junction geometry and (b) capacitor geometry.

material for photodetectors in silicon photonic circuits is germanium, as this can be epitaxially grown on silicon [53]. Germanium photodetectors have been demonstrated with good high speed performance (over 40 Gbps [54]), but typically suffer from higher dark currents that their III-V counterparts. Also, avalanche photodiodes have also been made in this technology, with very good bandwidth-gain products [55]. while Germanium detectors are more compact when integrated with thin-silicon waveguides, it is also possible to integrate them with thick silicon rib waveguides [56].

1.3.5 Lasers

The most challenging function to integrate in a silicon photonic circuit is obviously the light source. Silicon has an indirect bandgap, so light emission is not very efficient compared to nonradiative recombination mechanisms. Therefore, alternative ways to integrate a light source are needed.

The most obvious integration method for a light source is to just use an external laser (or multiple lasers) and connect them to the silicon chip either through flip-chip-like integration [37] or using a fiber connection. The advantage of this approach is that the laser simply acts as an external optical power supply, and that it can be electrically and thermally decoupled from the silicon chip.

In large-core silicon waveguides, it is possible to integrate lasers into the same waveguide substrate using flip-chip assembly techniques. By defining proper alignment structures, the laser mode can be aligned with the silicon waveguide core [57]. The mode size of the silicon waveguide can be adapted to match that of the laser, to obtain a good coupling efficiency.

To integrate laser directly into small-core silicon waveguide circuits, a suitable laser material needs to be integrated. This can be accomplished by incorporating suitable material (mainly III–V semiconductor stacks of quantum wells) on the chip. Direct epitaxy is not trivial, so the most promising approach at the moment is bonding [58]. Using various variations of this technique, lasers with outputs of several milliwatts have been demonstrated [59], including DBR lasers [60], ring lasers [61], and

widely tunable lasers. Also, microlasers with output power of the order of 100 μW have been demonstrated using disk geometries [62] or photonic crystals.

While bonding has already shown promising results and is the likely technology to provide short-term availability of on-chip lasers in silicon waveguides, the longer-term objective is to have epitaxially grown lasers monolithically integrated into the chip. III–V epitaxy on silicon is not yet sufficiently advanced to realize this objective, but lasers have been demonstrated in epitaxially grown germanium on silicon. This did require extensive bandgap engineering to favor recombination in the direct bandgap [63], but it offers a future route for integrated lasers on silicon.

1.4 SILICON PHOTONICS TECHNOLOGY

In this section, we go deeper into the technology that is used to make silicon photonic components and circuits, and the impact that technology has on the functionality of the devices discussed in the previous section.

1.4.1 Passive Circuits

Passive silicon waveguide circuits, which include waveguides, wavelength filters, and coupling structures, are usually fabricated with a simple lithographic process, both in large-core platforms as small-core photonic wire-based platforms. A schematic process flow is depicted in Figure 1.7 [17]. The base substrate material is silicon-on insulator (SOI), which consists of a silicon substrate, and oxide buffer layer, and a single-crystal top layer in which the waveguide circuit will be defined. The thickness of the layer stack depends on the requirements of small-core or large-core silicon waveguides. Small-core waveguides have a top layer of 200–500 nm, and require a buried oxide of 2 μm or more to decouple the waveguide from the substrate. Large-core waveguides have a thicker waveguide layer, and because the confinement is larger in the thicker silicon, they can have a thinner buffer oxide layer, on the order of 400–100 nm.

The pattern of the waveguide circuit is defined in a photosensitive resist using a lithography step (optical or e-beam lithography). After development, the pattern is transferred into the silicon layer. This is typically done using reactive ion etching or a

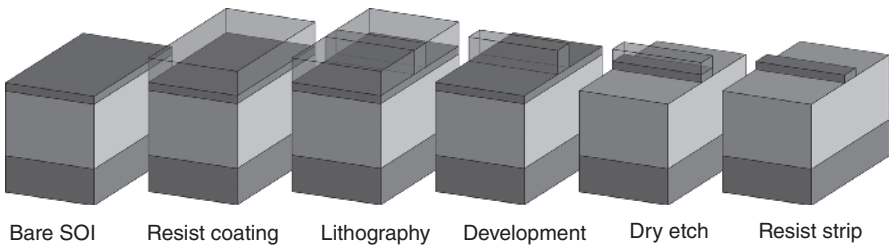

FIGURE 1.7 Fabrication process for passive waveguides. From Reference 17.

similar plasma-based etch. The etch can be either completely through the silicon (for strip waveguides) or partially in the silicon (for rib waveguides). After patterning, the resist layer and hard masks can be stripped. Multiple patterns with different etch depths can be applied subsequently, for instance, to implement shallow-etched grating couplers in deep-etched strip waveguides [26].

The details of such a fabrication process have a significant effect on the performance of the devices. As already mentioned, small geometry variations will induce a change in the effective index of the waveguides. While the linewidth and the thickness of the silicon waveguide have the largest impact, secondary factors such as sidewall angle after the etch can impact bend losses or unwanted polarization conversion [64]. The patterning itself also introduces imperfections. The lithography process should have sufficiently high resolution. While for large-core waveguides contact lithography or i-line lithography is sufficient, small-core waveguides require deep UV lithography at 248 nm [3, 65] or 193 nm [17]. E-beam lithography is also used, but it has limited scalability with respect to circuit size and industrial deployment.

Even with high-end lithography, the pattern definition can induce unwanted effects. For example, (optical) proximity effects will affect feature dimensions if neighboring features are present. In some cases, corrections can be applied, but it is difficult to guarantee uniform dimensions. For example, a waveguide might get a different linewidth in a directional coupler because of the presence of a second waveguide [3]. Also, the etch process might be influenced by the local and global density of patterns.

Controlling uniformity in silicon photonic waveguide circuits is especially challenging in small-core waveguides. Uniformity needs to be managed within a single chip, between chips on a wafer and between wafers and lots. High-end lithography tools already enable nanometer-level control of the linewidth [29]. However, a more difficult problem is the control of the thickness of the silicon layer. While SOI wafers can be manufactured with precision of a few percent, this still means variations on the order of 10 nm. To correct this, it is possible to use local processing of the wafer to make the top layer more uniform [66].

SOI is not the only material to make silicon waveguides. It is also possible to manufacture high quality waveguides in deposited layers, such as amorphous silicon. The advantage of such materials is that they can be used to add waveguides to substrates that have already active structures on them, such as electronics. While amorphous silicon has a somewhat higher optical absorption than crystalline silicon, good waveguides have been demonstrated [67, 68]. Polycrystalline waveguides have a higher propagation loss due to scattering and absorption at grain boundaries [69].

Deposited silicon (amorphous or poly) can also be used in combination with the crystalline waveguide circuits to provide special functions, or add a degree of freedom in defining local geometry where higher absorption losses have a lower impact [38].

1.4.2 Modulators

To implement carrier-based modulators, a junction or capacitor needs to be incorporated in the waveguide core. The most common way to define a junction is by

ion implantation, where P-doping and N-doping are subsequently implanted after a patterning step [46]. Of course, the alignment of the P and N patterns is crucial to obtain good electrical properties as well as a good overlap with the optical mode [70]. Multiple junctions can be used to enhance this overlap [51], or the junctions can be arranged in a finger pattern [70]. However, larger junction area might improve the modulation efficiency (larger phase shift for the same bias voltage) but it will also increase the electrical capacitance of the modulator, and thus limit the modulation bandwidth. Higher implantation doses will also improve the modulation efficiency, but at the expense of a higher optical loss.

Similar to a junction, a capacitor can be embedded into the waveguide. This is not straightforward to implement in a horizontal geometry, but the capacitor can be created with a vertical silicon-oxide-silicon stack [71, 72]. With a thin oxide layer, a capacitor can accumulate more charge than a reverse-biased p–n junction, and it can have a higher modulation efficiency. Again, this can come at the expense of RC-limited modulation bandwidth.

Both in the junction as the capacitor it is required to activate the implanted dopants. This can be done by applying a short high temperature anneal (1000C). Depending on the doping profile, this anneal will also induce some diffusion, so a good trade-off between anneal conditions and performance is needed [73].

Electrically contacting the modulators requires the use of a compatible metallization process. While different materials can be used, the preferred solution is to use Complementary Metal Oxide Semiconductor (CMOS)-compatible contacting. This usually involves a high dose implantation step, followed by a local silicidation. CMOS-compatible contacts to silicide are typically implemented in a tungsten (W) damascene process, involving etching, deposition and a chemical-mechanical polishing step. Metal wiring is done using aluminium or copper.

1.4.3 Active Tuning

While carrier modulators can reach operational speeds up to 40 Gbps, they are not the most effective method for slow tuning or switching. The effect is not that strong, and the implants and carriers induce excess optical loss.

To implement active tuning, the most straightforward technique is to incorporate heaters close to the waveguide structures. Heaters consist of an electrically contacted resistor, and they can be implemented in the metal layers of the modulator metallization, but also in dedicated resistive layers of tungsten [42] or titanium [74]. It is also possible to use the silicon or silicide layers as a resistor, positioned next to the optical waveguide instead of above it [75]. While often having different electrical properties, most heater mechanisms have similar efficiency, expressed in induced phase shift per dissipated power, on the order of 30 mW/π.

The main influence on tuning power is the thermal environment, rather than the electrical or optical properties of the device. The tuning power can be reduced dramatically by thermally insulating the optical element together with its heater from the surroundings. This can be done by etching deep trenches around the device [74].

1.4.4 Photodetectors

Photodetectors often have the most extensive processing, as they require the introduction of Germanium onto the chip. Germanium can be grown epitaxially on silicon, but it takes care to avoid the emergence of dislocations in positions where photocarriers are generated or collected, as recombination or trapping of carriers could reduce the efficiency of the detector.

Dislocations can be avoided or trapped by growing the germanium in a confined area. This way, dislocations are diverted to the sidewalls of the confined area where they cause no harm to the device. The epitaxy imposes a thermal budget on the rest of the processing, such as the anneal step for the modulator implants. This needs to be executed in advance.

Alternatively, amorphous germanium can be deposited and crystallized at a later stage using solid or liquid phase epitaxy [63]. This is an alternative way of avoiding dislocations. It does require a high temperature step to perform the regrowth.

1.4.5 Lasers

For lasers, we already discussed that bonding is the most likely solution for the short-term implementation of lasers on silicon [58]. The technique consists of bonding III–V epitaxial stacks onto the processed silicon photonic wafers, after which the bonded material is thinned down to a film of 100–2000 nm thick, depending on the applications. Multiple dies, or even entire III–V wafers, can be bonded on silicon photonics wafer. After bonding and thinning, the thin films of III–V material can be processed with wafer-scale processes similar to those used for the silicon processes. A schematic process is shown in Figure 1.8.

The bonding itself can be done in different ways. Molecular bonding uses Van Der Waals forces between two surfaces to attach the III–V material to the silicon circuit. For this, it is required that both surfaces are close to atomically flat. This technique has been used to demonstrate Fabry–Perot lasers [76], DFB-lasers [59], ring lasers [61] as well as small microdisk lasers [77]. An advantage of molecular bonding is that there is a close contact between the silicon layer and the III–V material, which provides a decent thermal contact to sink the dissipated power in the laser. Still, careful thermal design is needed.

An alternative to molecular bonding is adhesive bonding, which uses a glue layer to attach the III–V material to silicon [78]. Because of the intermediate spin-coated glue layer, this technique is more tolerant toward surface flatness. Bonding layers of 30 nm up to 1000 nm can be used, by tuning the viscosity of the adhesive, which is typically Dynamic Vapour Sorption-Benzocyclobutene (DVS-BCB). Similar to molecular bonding, different types of lasers have been demonstrated [62].

While epitaxial III–V materials are not yet sufficiently mature, germanium can be grown onto silicon substrates. Germanium has an indirect bandgap, but also a direct conduction band valley with a slightly higher energy than the indirect valley. By applying strain in the germanium layer during the epitaxial growth, the difference in energy can be partially compensated [63]. Subsequently, strong N-type doping

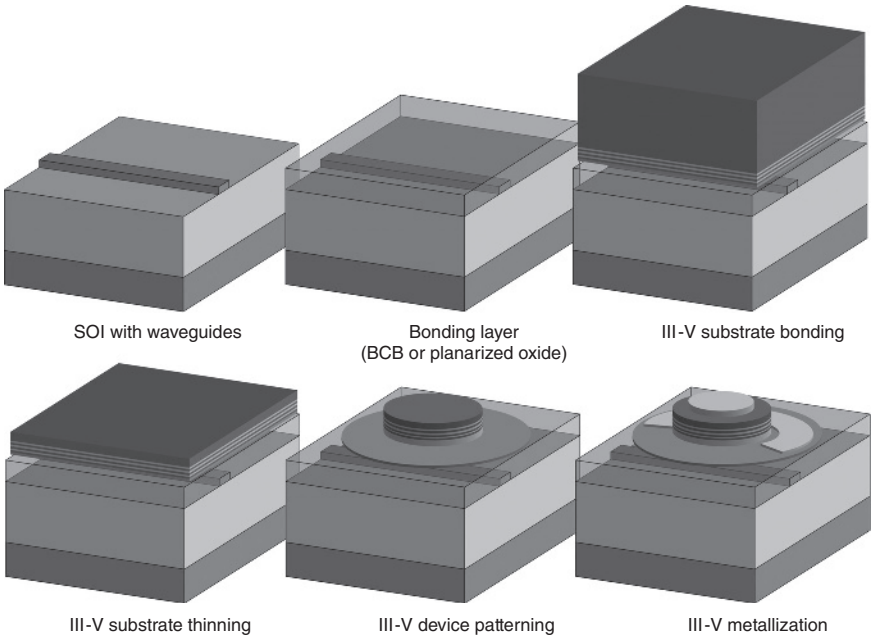

FIGURE 1.8 Fabrication of bonded lasers. From Reference 58.

can saturate the indirect conduction band valley, favoring recombination of injected electron–hole pairs via the direct conduction band valley [63]. A germanium laser based on this principle has been demonstrated [79].

Processing an efficient laser on silicon will still require significant effort. While it would definitely increase the flexibility of silicon photonic circuits, the currently most relevant technique is still the use of an outside discrete source, flipchipped on or fiber-pigtailed to the silicon chip.

1.4.6 Photonic–Electronic Integration

While silicon photonics can provide most optical functions on a chip, many of these functions require electronic control (e.g., modulators, photodetectors, and tuning elements). As circuits will become more complex, more electronics is needed. Depending on the applications, the electronics is needed to control the optical functions of the silicon chip, but in many cases, especially interconnect, the photonics is introduced to augment the performance of the electronics (e.g., high speed interconnects). The requirements of the photonic–electronic integration might be very different depending on this relation.

Different mechanisms exist for photonic–electronic cointegration. When no dense integration is needed, the simplest solution can be wirebonding, or simple flipchipping. When dense interconnects are needed, and especially operating at high speed, flipchipping with microbumps is an option.

Even denser integration is possible using through-silicon vias (TSV). 3D stacking using TSVs can enable very dense vertical interconnects with very little electrical

parasitics. However, such dense integration can introduce problems with thermal crosstalk. TSVs can be implemented in different metals, but typically the standard CMOS materials such as W and Cu are used [80].

As SOI is not only a suitable material for photonics, but also for electronics, it is possible to integrate photonics and electronics side by side in the silicon layer [37]. This has the advantage that there can be a very tight integration between electronics and photonics, but on the other hand, it means that there is competition for floor space between both technologies, which might in the end result in a much larger chip. Also, process requirements can be very different for both technologies, so it is not always possible to reconciliate the two technologies.

Instead of using crystalline silicon, it is also possible to use deposited silicon, which can be amorphous or polycrystalline. Layers of this material can be deposited on top of electronics layers, or anywhere in the stack of such wafers. This way, it is possible to implement photonic circuits together with the metal interconnect layers, without having a competition of floor space. The main issue is that amorphous silicon has a poorer performance than crystalline silicon, and that it is difficult to implement electro-optic modulators in it.

To use a crystalline silicon substrate for both electronics and photonics without having a competition for floor space, it is possible to use both sides of the wafer, one for photonics and one for electronics, and use TSVs to connect both layers. This approach introduces difficulties in processing, as the patterned backside needs to be protected during the processing of the front side. Also, TSVs need to pass through the entire wafer, which requires large and deep holes.

1.5 CONCLUSION

In this chapter, we tried to sketch an overview of the field of silicon photonics. We structured the technology from the applications downward, looking at the optical functions that are needed and the technologies that can implement them. In this approach, we mainly stuck to what is considered to be the mainstream silicon photonics, which is being developed by silicon fabs in various places in the world [37, 65, 80].

Still, the field of silicon photonics is much richer than this, with a lot of research exploring the introduction of new materials, design of waveguide structures, and novel applications.

Given the potential of silicon photonics, we can expect to see it deployed in actual products and industry in the coming years.

REFERENCES

[1] R. Soref, "The past, present, and future of silicon photonics," *J. Sel. Top. Quantum Electron.* **12**(6), 1678–1687 (2006).

[2] G. T. Reed and A. P. Knights, *Silicon Photonics: The State of the Art* (Wiley Online Library, 2008).

[3] W. Bogaerts, R. Baets, P. Dumon, V. Wiaux, S. Beckx, D. Taillaert, B. Luyssaert, J. Van Campenhout, P. Bienstman, and D. Van Thourhout, "Nanophotonic waveguides

in silicon-on-insulator fabricated with CMOS technology," *J. Lightwave Technol.* **23**(1), 401–412 (2005).

[4] K. De Vos, J. Girones, T. Claes, Y. De Koninck, S. Popelka, E. Schacht, R. Baets, and P. Bienstman, "Multiplexed antibody detection with an array of silicon-on-insulator microring resonators," *IEEE Photonics J.* **1**(4), 225–235 (2009).

[5] M. Iqbal, M. Gleeson, B. Spaugh, F. Tybor, W. Gunn, M. Hochberg, T. Baehr-Jones, R. Bailey, and L. Gunn, "Label-free biosensor arrays based on silicon ring resonators and high-speed optical scanning instrumentation," *J. Sel. Top. Quantum Electron.* **16**(3), 654–661 (2010).

[6] A. Mekis, S. Abdalla, P. De Dobbelaere, D. Foltz, S. Gloeckner, S. Hovey, S. Jackson, Y. Liang, M. Mack, G. Masini, et al., "SPIE. Scaling CMOS photonics transceivers beyond 100 Gb/s," in *Proc SPIE*, Conference on Optoelectronic Integrated Circuits XIV, San Francisco, CA, January 25–26, 2012, p. 8265.

[7] T. Pinguet, B. Analui, E. Balmater, D. Guckenberger, M. Harrison, R. Koumans, D. Kucharski, Y. Liang, G. Masini, A. Mekis, et al., "Monolithically integrated high-speed CMOS photonic transceivers," Group IV Photonics 2008, pp. 362–364.

[8] J. Shah, "High performance Silicon Photonics technology for ubiquitous communications: intrachip to data warehouses," Optical Interconnects Conference 2012, (2012), p. 112.

[9] Y. A. Vlasov, "Silicon CMOS-integrated nano-photonics for computer and data communications beyond 100G," *Commun. Mag. IEEE* **50**(2), s67–s72 (2012).

[10] S. Beamer, C. Sun, Y. Kwon, A. Joshi, C. Batten, V. Stojanović, and K. Asanović, "Re-architecting DRAM memory systems with monolithically integrated silicon photonics," in *ACM SIGARCH Computer Architecture News*, (ACM, 2010), Vol. 38(3), pp. 129–140.

[11] K. De Vos, I. Bartolozzi, E. Schacht, P. Bienstman, and R. Baets, "Silicon-on-insulator microring resonator for sensitive and label-free biosensing," *Opt. Express* **15**(12), 7610–7615 (2007).

[12] D. Taillaert, W. Van Paepegem, J. Vlekken, and R. Baets, "A thin foil optical strain gage based on silicon-on-insulator microresonators," in *Proc. SPIE.*, Vol. 6619 of Third European Workshop on Optical Fibre Sensors (EWOFS), 2007, p. 661914.

[13] M. S. Luchansky, A. L. Washburn, T. A. Martin, M. Iqbal, L. C. Gunn, and R. C. Bailey, "Characterization of the evanescent field profile and bound mass sensitivity of a label-free silicon photonic microring resonator biosensing platform," *Biosens. Bioelectron.* **26**(4), 1283–1291 (2010).

[14] N. A. Yebo, P. Lommens, Z. Hens, and R. Baets, "An integrated optic ethanol vapor sensor based on a silicon-on-insulator microring resonator coated with a porous ZnO film," *Opt. Express* **18**(11), 11859–11866 (2010).

[15] E. Ryckeboer, A. Gassenq, N. Hattasan, K. Kuyken, L. Cerutti, J.-B. Rodriguez, E. Tournie, G. Roelkens, W. Bogaerts, and R. Baets, "Integrated spectrometer and integrated detectors on silicon-on-insulator for short-wave infrared applications," in *CLEO: Science and Innovations* (Optical Society of America, 2012), p. CTu1A.3.

[16] Y. A. Vlasov, and S. J. McNab, "Losses in single-mode silicon-on-insulator strip waveguides and bends," *Opt. Express* **12**(8), 1622–1631 (2004).

[17] S. K. Selvaraja, P. Jaenen, W. Bogaerts, D. Van Thourhout, P. Dumon, and R. Baets, "Fabrication of photonic wire and crystal circuits in silicon-on-insulator using 193 nm optical lithography," *J. Lightwave Technol.* **27**(18), 4076–4083 (2009).

[18] A. G. Rickman and G. T. Reed, "Silicon-on-insulator optical rib waveguides: loss, mode characteristics, bends and y-junctions," IEE *Proc. : Optoelectron.* **141**(6), 391–393 (1994).

[19] S. Bidnyk, D. Feng, A. Balakrishnan, M. Pearson, G. M., H. Liang, W. Qian, C.-C. Kung, J. Fong, J. Yin, and M. Asghari, "Silicon-on-insulator-based planar circuit for passive optical network applications," *IEEE Photonics Technol. Lett.* **18**(22), 2392–2394 (2006).

[20] U. Fischer, T. Zinke, J. R. Kropp, F. Arndt, and K. Petermann, "0.1 dB/cm waveguide losses in single-mode SOI rib waveguides," *IEEE Photonics Technol. Lett.* **8**(5), 647–648 (1996).

[21] M. Gnan, S. Thoms, D. S. Macintyre, R. M. De La Rue, and M. Sorel, "Fabrication of low-loss photonic wires in silicon-on-insulator using hydrogen silsesquioxane electron-beam resist," *Electron. Lett.* **44**(2), 115–116 (2008).

[22] W. Bogaerts and S. K. Selvaraja, "Compact single-mode silicon hybrid rib/strip waveguide with adiabatic bends," *IEEE Photon J.* **3**(3), 422–432 (2011).

[23] M. A. Webster, R. M. Pafchek, G. Sukumaran, and T. L. Koch, "Low-loss quasi-planar ridge waveguides formed on thin silicon-on-insulator," *Appl. Phys. Lett.* **87**, 231108 (2005).

[24] T. Shoji, T. Tsuchizawa, T. Watanabe, K. Yamada, and H. Morita, "Low loss mode size converter from 0.3 μm square Si waveguides to singlemode fibres," *Electron. Lett.* **38**(25), 1669–1700 (2002).

[25] J. Brouckaert, W. Bogaerts, S. Selvaraja, P. Dumon, R. Baets, and D. Van Thourhout, "Planar concave grating demultiplexer with high reflective bragg reflector facets," *IEEE Photonics Technol. Lett.* **20**(4), 309–311 (2008).

[26] W. Bogaerts, S. Selvaraja, P. Dumon, J. Brouckaert, K. De Vos, D. Van Thourhout, and R. Baets, "Silicon-on-insulator spectral filters fabricated with CMOS technology," *J. Sel. Top. Quantum Electron.* **16**(1), 33–44 (2010).

[27] W. Bogaerts, P. De Heyn, T. Van Vaerenbergh, K. De Vos, S. Kumar Selvaraja, T. Claes, P. Dumon, P. Bienstman, D. Van Thourhout, and R. Baets, "Silicon microring resonators," *Laser Photon Rev.* **6**(1), 47–73 (2012).

[28] C. Dragone, "An NxN optical multiplexer using a planar arrangement of two star couplers," *IEEE Photonics Technol. Lett.* **3**(9), 812–814 (1991).

[29] S. K. Selvaraja, W. Bogaerts, P. Dumon, D. Van Thourhout, and R. Baets, "Subnanometer linewidth uniformity in silicon nanophotonic waveguide devices using CMOS fabrication technology," *J. Sel. Top. Quantum Electron.* **16**(1), 316–324 (2010).

[30] F. Gan, T. Barwicz, M. A. Popovic, M. S. Dahlem, C. W. Holzwarth, P. T. Rakich, H. I. Smith, E. P. Ippen, and F. X. Kartner, "Maximizing the thermo-optic tuning range of silicon photonic structures," in *Photonics in Switching 2007*, pp. 67–68.

[31] D. Dai, L. Yang, and S. He, "Ultrasmall thermally tunable microring resonator with a submicrometer heater on Si nanowires," *J. Lightwave Technol.* **26**(5–8), 704–709 (2008).

[32] I. Kiyat, A. Aydinli, and N. Dagli, "Low-power thermooptical tuning of SOI resonator switch," *IEEE Photonics Technol. Lett.* **18**(1–4), 364–366 (2006).

[33] C. Kopp, S. Bernabe, B. Bakir, J. Fedeli, R. Orobtchouk, F. Schrank, H. Porte, L. Zimmermann, and T. Tekin, "Silicon photonic circuits: on-CMOS integration, fiber optical coupling, and packaging," *IEEE J. Sel. Top. Quantum Electron.* **17**(3), 498–509 (2011).

[34] D. Taillaert, W. Bogaerts, P. Bienstman, T. Krauss, P. Van Daele, I. Moerman, S. Verstuyft, K. De Mesel, and R. Baets, "An out-of-plane grating coupler for efficient butt-coupling between compact planar waveguides and single-mode fibers," *J. Quantum Electron.* **38**(7), 949–955 (2002).

[35] D. Taillaert, H. Chong, P. Borel, L. Frandsen, R. De La Rue, and R. Baets, "A compact two-dimensional grating coupler used as a polarization splitter," *IEEE Photonics Technol. Lett.* **15**(9), 1249–1251 (2003).

[36] S. J. McNab, N. Moll, and Y. A. Vlasov, "Ultra-low loss photonic integrated circuit with membrane-type photonic crystal waveguides," *Opt. Express* **11**(22), 2927–2939 (2003).

[37] A. Mekis, S. Gloeckner, G. Masini, A. Narasimha, T. Pinguet, S. Sahni, and P. De Dobbe-laere, "A grating-coupler-enabled CMOS photonics platform," *IEEE J. Sel. Top. Quantum Electron.* **17**(3), 597–608 (2011).

[38] D. Vermeulen, S. Selvaraja, P. Verheyen, G. Lepage, W. Bogaerts, P. Absil, D. Van Thourhout, and G. Roelkens, "High-efficiency fiber-to-chip grating couplers realized using an advanced CMOS-compatible silicon-on-insulator platform," *Opt. Express* **18**(17), 18278–18283 (2010).

[39] F. Van Laere, T. Claes, J. Schrauwen, S. Scheerlinck, W. Bogaerts, D. Taillaert, L. O'Faolain, D. Van Thourhout, and R. Baets, "Compact focusing grating couplers for silicon-on-insulator integrated circuits," *Photonics Technol. Lett.* **19**(23), 1919–1921 (2007).

[40] F. van Laere, W. Bogaerts, P. Dumon, G. Roelkens, D. Van Thourhout, and R. Baets, "Focusing polarization diversity grating couplers in silicon-on-insulator," *J. Lightwave Technol.* **27**(5), 612–618 (2009).

[41] K. Van Acoleyen, J. Roels, P. Mechet, T. Claes, D. Van Thourhout, and R. Baets, "Ultra-compact phase modulator based on a cascade of NEMS-operated slot waveguides fabricated in silicon-on-insulator," *IEEE Photonics J.* **4**(3), 779–788 (2012).

[42] A. Masood, M. Pantouvaki, D. Goossens, G. Lepage, P. Verheyen, D. Van Thourhout, P. Absil, and W. Bogaerts, "CMOS-compatible Tungsten heaters for silicon photonic waveguides," Group IV Photonics 2012, pp. 234–236.

[43] T. Barwicz, M. A. Popovic, F. Gan, M. S. Dahlem, C. W. Holzwarth, P. T. Rakich, E. P. Ippen, F. X. Kartner, and H. I. Smith, "Reconfigurable silicon photonic circuits for telecommunication applications," *Proc. SPIE* **6872**, 68720Z–68720Z–12 (2008).

[44] W. De Cort, J. Beeckman, T. Claes, K. Neyts, and R. Baets, "Wide tuning of silicon-on-insulator ring resonators with a liquid crystal cladding," *Opt. Lett.* **36**(19), 3876–3878 (2011).

[45] R. Soref and B. Bennett, "Electrooptical effects in silicon," *J. Quantum Electron.* **23**(1), 123–129 (1987).

[46] G. T. Reed, G. Mashanovich, F. Y. Gardes, and D. J. Thomson, "Silicon optical modulators [Review]," *Nature Photonics* **4**(8), 518–526 (2010).

[47] M. R. Watts, D. C. Trotter, R. W. Young, and A. L. Lentine, "Ultralow power silicon microdisk modulators and switches," Group IV Photonics 2008, pp. 4–6.

[48] Q. Xu, S. Manipatruni, B. Schmidt, J. Shakya, and M. Lipson, "12.5 Gbit/s carrier-injection-based silicon micro-ring silicon modulators," *Opt. Express* **15**(2), 430–436 (2007).

[49] W. M. J. Green, M. J. Rooks, L. Sekaric, and Y. A. Vlasov, "Ultra-compact, low RF power, 10 Gb/s silicon Mach-Zehnder modulator," *Opt. Express* **15**(25), 17106–17113 (2007).

[50] L. Liao, A. Liu, J. Basak, H. Nguyen, M. Paniccia, D. Rubin, Y. Chetrit, R. Cohen, and N. Izhaky, "40 Gbit/s silicon optical modulator for highspeed applications," *Electron. Lett.* **43**(22) (2007).

[51] D. Marris-Morini, L. Vivien, J. M. Fédéli, E. Cassan, P. Lyan, and S. Laval, "Low loss

and high speed silicon optical modulator based on a lateral carrier depletion structure," *Opt. Express* **16**(1), 334–339 (2008).

[52] J. Brouckaert, G. Roelkens, D. Van Thourhout, and R. Baets, "Compact InAlAs/InGaAs metal-semiconductor-metal photodetectors integrated on silicon-on-insulator waveguides," *IEEE Photon Technol. Lett.* **19**(19), 1484–1486 (2007).

[53] L. Colace, M. Balbi, G. Masini, G. Assanto, H. C. Luan, and L. C. Kimerling, "Ge on Si p-i-n photodiodes operating at 10 Gbit/s ," *Appl. Phys. Lett.* **88**(10) (2006).

[54] L. Vivien, J. Osmond, J.-M. Fédéli, D. Marris-Morini, P. Crozat, J.-F. Damlencourt, E. Cassan, Y. Lecunff, and S. Laval, "42 GHz p.i.n Germanium photodetector integrated in a silicon-on-insulator waveguide," *Opt. Express* **17**(8), 6252–6257 (2009).

[55] Y. Kang, H.-D. Liu, M. Morse, M. Paniccia, M. Zadka, S. Litski, G. Sarid, A. Pauchard, Y.-H. Kuo, H.-W. Chen, et al., "Monolithic germanium/silicon avalanche photodiodes with 340 GHz gain-bandwidth product," *Nat. Photonics* **3**(1), 59–63 (2009).

[56] D. Feng, S. Liao, P. Dong, H. Feng, N.-N. Liang, D. Zheng, C.-C. Kung, J. Fong, R. Shafliha, J. Cunningham, et al., "High-speed Ge photodetector monolithically integrated with large cross-section silicon-on-insulator waveguide," *Appl. Phys. Lett.* **95**(26), 261105–261105–3 (2009).

[57] J. Bruns, T. Mitze, M. Schnarrenberger, L. Zimmermann, K. Voigt, M. Krieg, J. Kreil, K. Janiak, T. Hartwich, and K. Petermann, "SOI-based optical board technology," *AEU Int. J. Electron. Commun.* **61**(3), 158–162 (2007).

[58] G. Roelkens, L. Liu, D. Liang, R. Jones, A. Fang, B. Koch, and J. Bowers, "III-V/silicon photonics for on-chip and inter-chip optical interconnects," *Laser Photon Rev.* **4**(6), 751–779 (2010).

[59] B. Koch, A. Fang, E. Lively, R. Jones, O. Cohen, D. Blumenthal, and J. Bowers, "Mode locked and distributed feedback silicon evanescent lasers," *Laser Photon Rev.* **3**(4), 355–369 (2009).

[60] A. Fang, B. Koch, R. Jones, E. Lively, D. Liang, Y.-H. Kuo, and J. Bowers, "A distributed bragg reflector silicon evanescent laser," *IEEE PhotonicsTechnol. Lett.* **20**(20), 1667–1669 (2008).

[61] A. Fang, B. Koch, K.-G. Gan, H. Park, R. Jones, O. Cohen, M. Paniccia, D. Blumenthal, and J. Bowers, "A racetrack mode-locked silicon evanescent laser," *Opt. Express* **16**(2), 1393–1398 (2008).

[62] J. Van Campenhout, P. Rojo Romeo, P. Regreny, C. Seassal, D. Van Thourhout, S. Verstruyft, L. Di Ciocco, J.-M. Fedeli, C. Lagahe, and R. Baets, "Electrically pumped InP-based microdisk lasers integrated with a nanophotonic silicon-on-insulator waveguide circuit," *Opt. Express* **15**(11), 6744–6749 (2007).

[63] J. Liu, X. Sun, D. Pan, X. Wang, L. Kimerling, T. Koch, and J. Michel, "Tensile-strained, n-type Ge as a gain medium for monolithic laser integration on Si," *Opt. Express* **15**(18), 11272–11277 (2007).

[64] S. K. Selvaraja, W. Bogaerts, and D. Van Thourhout, "Loss reduction in silicon nanophotonic waveguide micro-bends through etch profile improvement," *Opt. Comm.* **284**(8), 2141–2144 (2011).

[65] K.-W. Ang, T.-Y. Liow, Q. Fang, M. Yu, F. Ren, S. Zhu, J. Zhang, J. Ng, J. Song, Y. Xiong, et al., "Silicon photonics technologies for monolithic electronic-photonic integrated circuit (EPIC) applications: current progress and future outlook," in *Electron Devices Meeting (IEDM)*, 2009 IEEE International, pp. 1–4.

[66] S. Selvaraja, L. Fernandez, M. Vanslembrouck, J.-L. Everaert, P. Dumon, J. Van Campenhout, W. Bogaerts, and P. Absil, "Si photonic device uniformity improvement using

wafer-scale location specific processing," Photonics Conference (IPC), 2012 IEEE, pp. 725–726.

[67] D. Sparacin, R. Sun, A. Agarwal, M. Beals, J. Michel, L. Kimerling, T. Conway, A. Pomerene, D. Carothers, M. Grove, et al., "Low-loss amorphous silicon channel waveguides for integrated photonics," Group IV Photonics 2006, pp. 255–257.

[68] S. Selvaraja, E. Sleeckx, M. Schaekers, W. Bogaerts, D. Van Thourhout, P. Dumon, and R. Baets, "Low-loss amorphous silicon-on-insulator technology for photonic integrated circuitry," *Opt. Comm.* **282**(9), 1767–1770 (2009).

[69] S. Zhu, Q. Fang, M. B. Yu, G. Q. Lo, and D. L. Kwong, "Propagation losses in undoped and n-doped polycrystalline silicon wire waveguides," *Opt. Express* **17**(23), 20891–20899 (2009).

[70] Y Hui, M. Pantouvaki, J. Van Campenhout, D. Korn, K. Komorowska, P. Dumon, Y. Li, P. Verheyen, P. Absil, L. Alloatti, et al., "Performance tradeoff between lateral and interdigitated doping patterns for high speed carrier-depletion based silicon modulators," *Opt. Express* **20**(12), 12926–12938 (2012).

[71] J. C. Rosenberg, W. M. J. Green, S. Assefa, D. M. Gill, T. Barwicz, M. Yang, S. M. Shank, and Y A. Vlasov, "A 25 Gbps silicon microring modulator based on an interleaved junction," *Opt. Express* **20**(24), 26411–26423 (2012).

[72] J. Van Campenhout, M. Pantouvaki, P. Verheyen, S. Selvaraja, G. Lepage, H. Yu, W. Lee, J. Wouters, D. Goossens, M. Moelants, et al., "Low-voltage, low-loss, multi-Gb/s silicon micro-ring modulator based on a MOS capacitor," in *Optical Fiber Communication Conference* (Optical Society of America, 2012), p. OM2E.4.

[73] H. Yu, W. Bogaerts, and A. De Keersgieter, "Optimization of ion implantation condition for depletion-type silicon optical modulators," *J. Quentum. Electron.* **46**(12), 1763–1768 (2010).

[74] P. Dong, W. Qian, H. Liang, R. Shafiiha, D. Feng, G. Li, J. Cunningham, A. Krishnamoorthy, and M. Asghari, "Thermally tunable silicon racetrack resonators with ultralow tuning power," *Opt. Express* **18**(19), 20298–20304 (2010).

[75] J. Van Campenhout, W. M. J. Green, S. Assefa, and Y. A. Vlasov, "Integrated NiSi waveguide heaters for CMOS-compatible silicon thermooptic devices," *Opt. Lett.* **35**(7), 1013–1015 (2010).

[76] M. Lamponi, S. Keyvaninia, F. Pommereau, R. Brenot, G. de Valicourt, F. Lelarge, G. Roelkens, D. Van Thourhout, S. Messaoudene, J.-M. Fedeli, et al., "Heterogeneously integrated InP/SOI laser using double tapered single-mode waveguides through adhesive die to wafer bonding," Group IV Photonics 2010, pp. 22–24.

[77] T. Spuesens, F. Mandorlo, P. Rojo-Romeo, P. R6greny, N. Olivier, J.-M. Fédil, and D. Van Thourhout, "Compact integration of optical sources and detectors on SOI for optical interconnects fabricated in a 200 mm CMOS pilot line," *J. Lightwave Technol.* **30**(11), 1764–1770 (2012).

[78] G. Roelkens, J. Brouckaert, D. Van Thourhout, R. Baets, R. Notzel, and M. Smit, "Adhesive bonding of InP/InGaAsP dies to processed silicon-on-insulator wafers using DVS-bis-benzocyclobutene," *J. Electrochem. Soc.* **153**(12), G1015–G1019 (2006).

[79] R. Camacho-Aguilera, Y. Cai, N. Patel, J. Bessette, M. Romagnoli, L. Kimerling, and J. Michel, "An electrically pumped germanium laser," *Opt. Express* **20**(10), 11316–11320 (2012).

[80] J. Fedeli, E. Augendre, J. Hartmann, L. Vivien, P. Grosse, V. Mazzocchi, W. Bogaerts, D. Van Thourhout, and F. Schrank, "Photonics and electronics integration in the HELIOS project," Group IV Photonics 2010, pp. 356–358.