1 Fundamentals of Electrical Overstress

FUSE-BLOCK

"*To all whom it may concern:*

Be it known that I, THOMAS A. EDISON, of Menlo Park, in the county of Middlesex and State of New Jersey, have invented a certain new and useful Improvement in Lightning Arresters (Case No. 644,) of which the following is a specification.

My invention relates to fusible safety-catches or lightning-protections for telephones, telegraph, and similar circuits in which the fusible wire is placed in an inclosing shell or chamber of insulating material; and my object is to prevent or diminish the liability to surface creeping of lightning or other powerful current . . ."

United States Patent Office
Patent No. 438,305
14 October 1890

Electrical overstress (EOS) has been an issue with the coming of the electrical age, when electricity and electrical product were first introduced into the mainstream of society. With the introduction of electrical power systems, the telephone, and electronics, inventions such as circuit breakers and fuses became the first type of electrical overstress protection concepts to avoid over-load of electronic systems.

In this text, electrical overstress (EOS) will be addressed for the modern age of new devices, components, and systems. We will first visit the 1970s where the interest in EOS arose due to a growing interest in the reliability and quality of components and systems. In the end of the text, we will arrive at the future of "Nano-EOS" – EOS in nanotechnologies.

Electrical Overstress (EOS) : Devices, Circuits and Systems, First Edition. Steven H. Voldman.

1.1 ELECTRICAL OVERSTRESS

Electrical overstress (EOS) has been an issue in devices, circuit and systems for electronics for many decades, as early as the 1970s [1–12], and continues to be an issue today [13–83]. Market segments from consumer, industrial, aerospace, military, and medical are all influenced by this issue. The experience of EOS failures occurs at the device manufacturer, supplier, assembly, and the field. In the electronic industry, many products and applications are returned from the field due to "EOS" failure. To make progress in addressing the EOS issue, it is important to provide a framework for the evaluation and analysis of EOS phenomena. As part of this framework, it is important to apply a vocabulary and definitions. It is key to apply both physical and mathematical definitions to quantify the EOS conditions. It is equally important to establish a methodology of failure analysis and testing. It is also critical to establish an awareness of the origins and sources of EOS concerns. In the end, to provide better EOS robust products, it is important to define design practices and procedures, as well as EOS control programs for manufacturing and production areas.

1.1.1 The Cost of Electrical Overstress

One of the key concerns of EOS is the cost. There are different types of costs associated with EOS. In this section, the cost associated with field returns will be discussed. In order to quantify the cost of EOS events on products, it is critical to categorize what percentage of field returns are in fact EOS related.

1.1.2 Product Field Returns – The Percentage that is Electrical Overstress

Product field returns occur in all electronic components independent of the technology generation and period of time of evaluation. One of the key difficulties in the semiconductor industry is the ability to track, record, and maintain a database of these field failures.

A key question in the electronic industry is what is the percentage of the field returns that is due to electrical overstress (EOS)?

In the mid-1980s, the military established an in-house program to track, record, and categorize field failures to answer this question [49]. The United States military and the Reliability Analysis Center (RAC) in Rome, N.Y., jointly established the Field Failure Return Program (FFRP), with the objective of providing feedback to the semiconductor industry, and determine the root cause of failure. With establishing the root cause of failure, the corrective action can be initiated. The FFRP goals were as follows [49]:

- Identify high failure rate, or component problems.
- Identify their root causes of failure from failure analysis
- Feedback the information to the supplier, industry, or government organization for corrective action.

Table 1.1 Field failure categories and percentages

Field failure category	Field Failures (%)
Electrical overstress (EOS)	46
IC design, fabrication, and assembly	25
Retested without observed failure	17
Electrostatic discharge (ESD)	6
EOS or ESD	6

In this early reliability study, data from 24 different systems was collected and reviewed. In this review, 1650 parts were evaluated, of which the part numbers were from actual field failures that were operational from two to 10 years. Table 1.1 shows the results of the field failure categories [49].

From this study, 46% of the field returns were associated with electrical overstress (EOS). It was regarded from this study that a number of EOS issues were associated with poor system design, improper maintenance procedures, and improper operational procedures. In the second category, it was regarded that these failures were from inherent flaws and latent defects. Of the field returns, only a small percentage was related to electrostatic discharge (ESD). Note that in some cases it was decided that it was not possible to determine if the failures were EOS or ESD (Figure 1.1).

The results of this study are not significantly distinct from other future studies. It is typically quoted that EOS is a high percentage of field failures, and a certain percentage cannot distinguish EOS from ESD.

In more recent studies, C. Thienel's study for the automotive industry called "Avoiding electrical overstress for automotive semiconductors by new connecting concepts," attributed 6% of the failures to ESD and 94% were associated with EOS [77,79,80]. A large percentage of the fails were "no defect found" and approximately 32% were EOS/ESD failures.

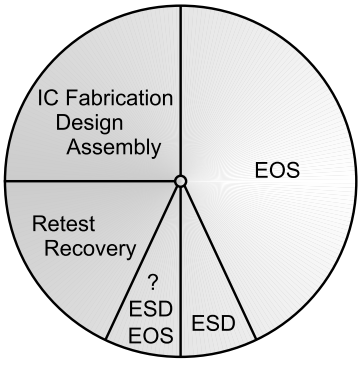

Figure 1.1 Failure categories pie chart

1.1.3 Product Field Returns – No Defect Found versus Electrical Overstress

In practice, product field returns are sent from the customers back to the source of production. These "field returns" come back to the quality organization, where the root cause of the field failure is diagnosed. A large percentage of the field returns are labeled "no defect found" (NDF) when the root cause cannot be observed. It is well known that many of the field returns are electrical overstress (EOS) related.

1.1.4 Product Failures – Failures in Integrated Circuits

Failures occur in the production of integrated circuits (IC) impacting yield. Studies have shown that the impact to IC productions from electrical overstress (EOS) and electrostatic discharge (ESD) can be up to 37% of the product failures (Table 1.2) [49]. In this study, it was found that 25% of the product failures were associated with fabrication. For the assembly process, it was found that the magnitude of yield loss was on the order of 12%, and another 12% was unknown. These percentages are dependent on the technology and controls in the foundry, but provide use with a view of the impacts of the various issues that accompanies yield loss.

In this chapter, some fundamental definitions will be introduced and concepts to open the discussion of (EOS). In future chapters, the text will proceed with the aforementioned topics of EOS.

1.1.5 Classification of Electrical Overstress Events

Electrical overstress (EOS) is such a broad spectrum of phenomena, it is important to establish classifications of EOS. The definition of EOS includes electrical response to current, voltage, and power.

Electrical phenomena is categorized into different definitions, which will be discussed in depth in future sections. Common categorization include electrostatic discharge (ESD), electromagnetic interference (EMI), electromagnetic compatibility (EMC), and latchup issues (Figure 1.2) [84–89]. At times, all of these are included in the definition of EOS; yet others separate these categories as separate items to distinguish them for the purpose of determining cause–effect relationships, as well as root cause. For example, although ESD is a form of EOS, it is established in the semiconductor industry to distinguish them. One of the reasons this is done is due to determining the root cause of failure.

Table 1.2 Failures in IC production

Cause of yield loss	Percentage (%)
Electrostatic discharge/electrical overstress	37
Fabrication	25
Assembly	12
Unknown	12

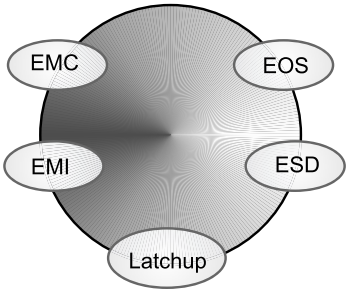

Figure 1.2 EOS, ESD, EMI, EMC, and latchup

Electrical overstress (EOS) cause and effect for integrated circuits can be the following [80]:

- Electrostatic discharge (ESD)
- Latchup
- Electromagnetic interference (EMI)
- Electromagnetic compatibility (EMC)
- Misapplication.

For ESD phenomena, there exists event models for the component and system levels. For component-level ESD, failures can be associated with human body model (HBM), machine model (MM), charged device model (CDM), and human metal model (HMM) [84–86,88–91]. For system-level ESD, failures can be associated with charged board model (CBM) and cable discharge event (CDE) [84–86,88–90].

For latchup, there exists causes associated with direct current (d.c.) and transient phenomena [87]. Direct current latchup events can be in the form of "internal latchup" and "external latchup." Transient latchup is also the initiation of latchup from a transient voltage event.

For electromagnetic interference, EOS events can occur from the following [80]:

- Noise
- Surge currents
- Slow voltage transients
- Fast voltage transients
- Radio frequency (RF) signals.

For the EMI events, there are causes for noise, surge currents, transients, and RF interference. Noise can be a result of lack of proper filters and switching events. Surge currents can occur due to poor electrical isolation and switching of capacitors. Voltage transients can occur due to the power-up and power-down of printed circuit boards and integrated circuits (ICs). Inductive switching is also a transient voltage concern. Radio frequency (RF)

interference can be a concern from lack of filters, lack of shielding, shielding openings, and the printed circuit board (PCB) design quality [73,80].

Human error and misapplication is a large cause of EOS events. This can happen in the following forms:

- System design
- Improper testing
- Improper assembly
- Specification violation.

EOS can be a result of poor system design [73,80]. System design can be both hardware or software. Improper or inadequate design of both the electrical and thermal properties can lead to electrical overstress.

EOS events can be the result of improper testing [73,80]. Human error from incomplete tests, hot swapping, switching of components, to over-voltage or over-current application to components, to inadequate margins can lead to overstress. Over-voltage can also occur in the test equipment sources themselves due to noise, transient spikes, and other poor quality test environments.

Improper assembly and human error can also be the cause of EOS issues. In the assembly process, mis-orientation, mis-insertion, reverse insertion, and assembly of powered or un-powered states can lead to electrical overstress.

In addition, electrical specifications can be violated due to defective hardware (e.g., opens and shorts), poor electrical contacts, poor ground connections, and overheating.

Throughout the text, these issues will be re-emphasized, repeated, and addressed in detail. To continue with our discussion, more definitions will be established in this chapter.

1.1.6 Electrical Over-Current

There are different forms of electrical overstress (EOS). In electrical conditions that are in excess of the intended or application current, devices, components, or systems can undergo latent or permanent damage; this condition can be defined as electrical over-current (EOC).

When EOC occurs, electronic components can have excessive Joule heating, material property changes, melting, or fire. Electrical over-current (EOC) is one classification of EOS. Electrical over-current (EOC) can be prevented by electrical fuses, temperature sensing circuitry, and current-limiting EOS protection devices.

1.1.7 Electrical Over-Voltage

In electrical conditions that are in excess of the intended or application voltage, devices, components, or systems can undergo latent or permanent damage; this condition can be defined as electrical over-voltage (EOV). When EOV occurs, electronic components can undergo different conditions. Electrical overvoltage (EOV) can lead to electrical breakdown of dielectrics, semiconductors, and conductors. Electrical over-voltage (EOV) is a second classification of EOS.

Electrical over-voltage (EOV) can be prevented by voltage-limiting EOS protection devices, and electrostatic discharge (ESD) protection circuits.

1.1.8 Electrical Over-Power

In electrical conditions that are in excess of the intended or application current, voltage or power, devices, components, or systems can undergo latent or permanent damage; this condition can be defined as electrical over-power (EOP). Electrical over-power (EOP) is a concern when the power exceeds the power-to-failure, P_f. Electrical over-power (EOP) is a third classification of EOS. Electrical over-power (EOP) can be prevented by utilizing over-voltage voltage-limiting EOS protection circuits, current-limiting EOS protection devices, fuses, and other circuit solutions.

1.2 DE-MYSTIFYING ELECTRICAL OVERSTRESS

Electrical overstress (EOS) is regarded as a difficult issue to define. This belief has led to a slow growth of the EOS discipline definition and quantification. This was also true for the electrostatic discharge (ESD) discipline; in early days, it was regarded as "black magic" and a subject that could not be quantified. After three decades of development and research, the ESD discipline has been quantified and understood. This has led to a number of standards in industry for the qualification of semiconductor components.

Likewise, the EOS field requires "de-mystification" to establish continued understanding, quantification, and establishment. The steps for quantification will require an increased understanding of the following:

- Failure mechanisms understanding and categorization
- Physical models
- Circuit and system circuit models
- EOS test methods and standards
- EOS protection devices
- EOS design procedures
- EOS design rule checking (DRC)
- EOS layout versus schematic (LVS) verification
- EOS electrical rule checking (ERC) development
- EOS qualification release process
- EOS certification of EOS protected areas (EOS-PA)
- EOS program management and auditing.

1.2.1 Electrical Overstress Events

Electrical overstress (EOS) can occur within manufacturing environments, production areas, and in the field [73]. EOS events can occur internal or external of electronic systems. External sources can be associated with voltage sources, current sources, and phenomena associated with inductive, capacitance, or resistive components. The phenomena can be direct current (d.c.), alternating current (a.c.), or transient phenomena.

Examples of different external sources of EOS events can include the following:

- *Inductance:* Inductive loads
- *Capacitive:* Cable capacitance charge
- *Resistive:* Ground resistance.

Electronic noise in different forms is also a key cause of EOS events. Noise events, both internal and external, can create component failures. Example of noise events include the following:

- *External Switching Noise:* Switching noise on antennas
- *External Ground Plane Noise:* Noise on ground plane or current return
- *External electromagnetic interference (EMI):* EMI noise due to poor shielding
- *Internal Switching I/O Noise:* Sequential switching of digital I/O off-chip driver circuitry
- *Internal Switching Clock Noise:* Switching of timing clocks
- *Internal I/O Transients:* Overshoot and undershoot.

Electrical overstress (EOS) phenomena also comes in different categorizes. For example, CMOS latchup is particular form of an EOS event associated with parasitic devices within a chip leading to thermal runaway and destruction.

1.3 SOURCES OF ELECTRICAL OVERSTRESS

Electrical overstress (EOS) can occur in many different environments. EOS can occur in manufacturing, production, and assembly environments.

1.3.1 Sources of Electrical Overstress in Manufacturing Environment

Electrical overstress (EOS) is a concern in the manufacturing environment. A key source of electrical overstress is the power line (e.g., also known as grid power, or mains). Power-line EOS from the power grid is due to the following reasons (Figure 1.3) [73]:

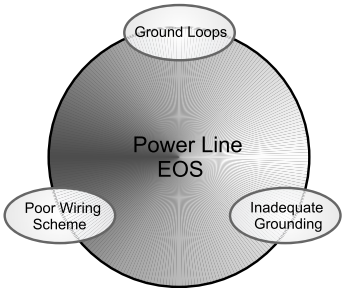

Figure 1.3 Power line EOS

- Poor wiring schemes
- Lack of adequate grounding
- Ground loops.

Mains-caused alternating current (a.c.) EOS events can occur to both voltage induction and current induction. In addition, there is direct current (d.c.) caused electrical overstress in manufacturing environments [73].

1.3.1.1 Alternating Current Electrical Overstress

For alternating current (a.c.) voltage induction, it has been shown that a.c. signals exists on power lines up to 2.3 V. A strong relationship exists between the ground impedance and in voltage induced a.c. voltage inside the manufacturing tooling. One example of how manufacturing environments can lead to this voltage-induction concern is when the neutral and ground wires are reversed.

For alternating current (a.c.) current induction, motors and high transient currents within a tool generate magnetic fields. The magnetic fields can induce both voltages and currents within adjacent wiring and wiring loops.

1.3.1.2 Direct Current Electrical Overstress

In a manufacturing environment, there are direct current (d.c.) motors in equipment. Low voltage d.c. motors have the negative terminal connected to a chassis, which establishes the return path for the current through the d.c. motor. The resistance drop through the chassis of the tool can lead to a differential voltage between the chassis and the true ground of the motor. This differential voltage between the chassis and the ground can lead to a low voltage EOS event.

1.3.1.3 High Frequency Noise

Switches, solenoids, relays, variable frequency motors, and other tools can generate electromagnetic interference (EMI) [73]. EMI events can induce a voltage on components,

leading to EOS. EMI-induced EOS events can occur in the magnetic recording industry and future nano-structures.

1.3.2 Sources of Electrical Overstress in Production Environments

Electrical overstress (EOS) is a concern in the manufacturing area, as well as the production environment. In production environments, sources of EOS events are soldering irons, power tools, and power supply commutation [73].

In soldering irons, EOS events can occur due to the following:

- Loss of ground connection
- Noise on the ground line
- Noise on the power line
- Transient switching spikes
- Solder iron tip oxidation.

In power tools, EOS events can occur due to improper grounding. For example, power tools used in production environment that can cause EOS events are screwdrivers. Screwdrivers tips have both oxidizing films and insulating barriers between the ground line and the screwdriver tip. Lack of good connections to the true ground can lead to EOS events.

A third source of EOS events is power supply commutation. Power supply commutation is the process of transferring current from one connection to another within an electric circuit; this is achieved typically by an electronic "switch." In power converter circuits, there is a significant number of EOS spikes that occur in the production environment during power commutation.

1.4 MISCONCEPTIONS OF ELECTRICAL OVERSTRESS

In the field of electrical overstress (EOS), there are many misconceptions [80]. This was also true for the field of electrostatic discharge (ESD) between 1970 to the mid-1990s. In the field of ESD protection, examples of some of the typical misconceptions were as follows:

- *Current Path Misconception:* All the ESD current will flow into the ESD protection device and no current flows into the input/output (I/O) circuitry.
- *ESD Failure:* During an ESD event, the failing structure is always the ESD protection circuit.
- *ESD Circuitry Placement:* The ESD network must be placed next to the bond pad.
- *Charged Device Model:* All CDM failures are on receiver gate structures.

In the field of EOS, equivalently, there are also many similar misconceptions. Here are a few examples of misconceptions about EOS phenomena [80]:

- *EOS Current Path:* The current path for all types of EOS events is the same within a printed circuit board and an integrated circuit component.
- *EOS Failure Location:* The failure damage location for all types of EOS events is the same.
- *EOS Equal Response:* Specific parts of an integrated circuit responds equally to different types of EOS events.
- *EOS IC Response:* EOS response is independent of its operational mode.
- *EOS Response Proportionality:* The response of an integrated circuit to an EOS event is linearly proportional to the EOS event magnitude.

1.5 MINIMIZATION OF ELECTRICAL OVERSTRESS SOURCES

A solution to addressing electrical overstress (EOS) is to minimize both the sources of EOS. The EOS cause and effect for integrated circuits can be the following:

- Electrostatic discharge (ESD) [84–90]
- Latchup [87]
- Electromagnetic interference (EMI) [93–115]
- Electromagnetic compatibility (EMC) [93–115]
- Misapplication.

With a focus on the minimizing the impact of ESD, latchup, EMI, EMC, and misapplication, EOS failure can be reduced. This can be achieved through semiconductor technology robustness, circuit design, printed circuit board design, electrical isolation, transient minimization, shielding, filters, test procedures, handling, and auditing controls.

1.6 MITIGATION OF ELECTRICAL OVERSTRESS

A solution to mitigate electrical overstress (EOS) failure is to have an EOS Mitigation Strategy [80]. An EOS Mitigation Strategy can include independent design of integrated circuits, or a co-design strategy that plans the printed circuit board design, placement of the components, and integrated circuit design jointly.

An EOS Mitigation Strategy for the system is as follows [80]:

- ESD discharge control
- Current loop reduction for noise minimization

- Shielding
- Noise filters
- Connector design
- EOS on-board voltage-limiting devices
- EOS on-board current-limiting devices
- Decoupling capacitors
- Low effective series resistance (ESR) capacitors
- Low effective series inductor (ESL) capacitors
- Printed circuit board (PCB) EMC compliant design.

An EOS Mitigation Strategy for the components are as follows [80]:

- Increased voltage tolerance
- Voltage clamps
- Decoupling capacitors
- De-coupling of cross-component parasitic
- EOS on-chip voltage-limiting devices
- EOS on-chip current-limiting devices
- Integrated circuit (IC) EMC compliant design.

1.7 SIGNS OF ELECTRICAL OVERSTRESS DAMAGE

After an electrical overstress (EOS) event, there are different means of verification [92]. One way to determine that there was an EOS event is the electrical signature. A second sign is the visual signature.

1.7.1 Signs of Electrical Overstress Damage – The Electrical Signature

After an electrical overstress (EOS) event, there are different means of verification. One way to determine that there was an EOS event is the electrical signature [92]. Evaluation of the electrical characteristics can be an indicator of an EOS event. Some of the EOS event electrical characteristics are as follows (Figure 1.4):

- Electrical open (open connections)
- Electrical short of signal pin to power rail (V_{DD})

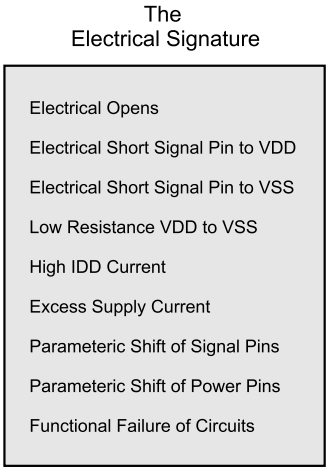

Figure 1.4 Signs of EOS damage – the electrical signature

- Electrical short of signal pin to ground power rail (V_{SS})
- Low resistance between power supply rail (V_{DD}) and ground rail (V_{SS})
- High I_{DD} current
- Excess supply current
- Parametric shift of signal or power pins
- Functional failure of circuits.

All of the above are indications that the product either has an open, short, or degradation that leads to either functional failure, increased leakage, or latent mechanisms.

1.7.2 Signs of Electrical Overstress Damage – The Visual Signature

After an electrical overstress (EOS), a second way to determine that there was an EOS event is the visual signature [92]. In the case of visual EOS damage signature, this can be either external visual damage, or internal visual damage. External visual damage is typically associated with the package, whereas internal visual damage is contained within the package. Some of the EOS event visual external damage characteristics are as follows (Figure 1.5):

- External package power or signal pin melting
- External cracking in the package
- External displacement of the package (e.g., top removed)
- Melting of the package material

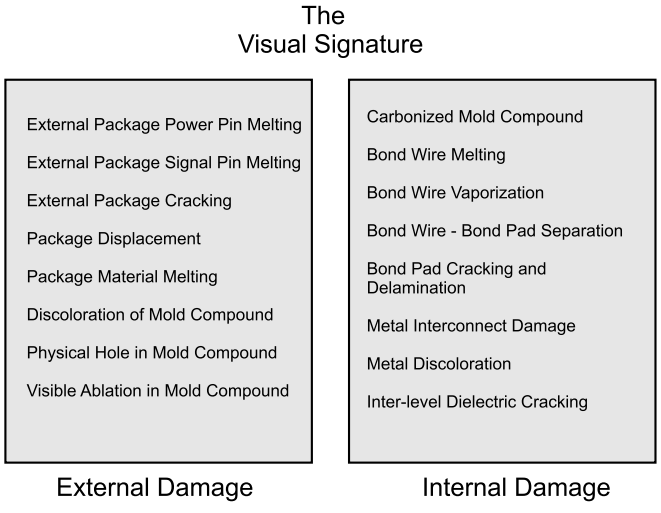

Figure 1.5 Signs of EOS damage – the visual signature

- Discoloration of the mold compound
- Physical hole in the mold compound
- Visible bulge or ablation in the mold compound.

Internal EOS visual damage may be the following:

- Carbonized mold compound
- Bond wire melting
- Bond wire vaporization
- Bond wire–bond pad separation
- Bond pad cracking and de-lamination
- Metal interconnect damage – blistering, agglomeration, or displacement
- Metal discoloration
- Inter-level dielectric (ILD) cracking
- Dielectric breakdown.

1.8 ELECTRICAL OVERSTRESS AND ELECTROSTATIC DISCHARGE

A key issue in determining the root cause is distinguishing between an electrical overstress (EOS) event and an electrostatic discharge (ESD) event [73]. As discussed in the prior

sections, ESD events are part of the EOS spectrum, as a sub-classification, but historically there is a desire to distinguish between the two, to hone in on the root cause of the failure. To follow suit with this thinking, let us make a distinction between the two classifications. In the following sections, let us draw a distinction between these classifications in more depth.

1.8.1 Comparison of High and Low Current EOS versus ESD Events

Electrical overstress (EOS) and electrostatic discharge (ESD) can be grouped into three general areas based on the event characteristics. Electrical overstress phenomena into three groups: (1) ESD, (2) Low current EOS, and (3) high current and high power EOS. The first two groups affect consumer products, automotive, military, and medical applications, whereas the third group (e.g., lightning) is associated with automobiles, airplanes, buildings, and electronics. This third group is associated with lightning and power.

1.8.2 Electrical Overstress and Electrostatic Discharge Differences

Although there are similarities between electrical overstress (EOS) and electrostatic discharge (ESD), there are a greater number of differences. The differences can be broken into the following categories [73]:

- Nature and source of the charge and current
- Characteristic time response
- Waveform definition
- Periodicity
- Repeatability
- Failure mechanisms.

1.8.2.1 Nature and Source of the Charge and Current

Electrostatic discharge (ESD) events are typically associated with tribo-electric charging and accumulation of charge; this process is followed by a rapid discharge of the event through electrical contact or arc discharge. The ESD current is associated with the discharge process of the accumulated charge.

In contrast, EOS events are associated with voltage or currents associated with power sources, power generating equipment, machinery, and tooling.

1.8.2.2 Characteristic Time Response

The electrostatic discharge (ESD) event characteristic time response is associated with a specific process of charge accumulation and discharge. Hence, the characteristic time

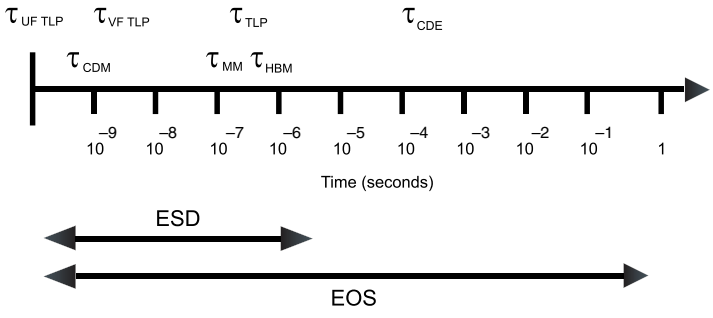

Figure 1.6 EOS and ESD event time constant spectrum

response is definable enough to establish an ESD standard associated with the specific process. Second, the time response of ESD events are fast processes. The time constant for ESD events range from sub-nanoseconds to hundreds of nanoseconds.

In contrast, EOS events do not have a characteristic time response. They can have short time response or long (note: today, it is popular to separate the "ESD events" as distinct from "EOS events", which is what will be followed in this text). EOS processes are typically slower and distinguishable from ESD events by having longer characteristic times. The time constant for EOS events range from sub-microseconds to seconds (Figure 1.6).

1.8.2.3 Waveform Definition

For electrostatic discharge (ESD) events, the waveform is well defined for given events. The ESD pulse waveform is codified within the ESD standards. The different ESD events, such as human body model (HBM), machine model (MM), charged device model (CDM), human metal model (HMM), IEC 61000-4-2, and transmission line pulse (TLP) are well defined waveforms [84–90].

In contrast, for EOS events, the waveforms are not well defined [73]; EOS has no specific waveform. Historically, this has made the quantification of EOS events less tractable and definable; this has limited EOS standard development and a requirement for the shipping of components and systems. Today, the standard IEC 61000-4-5 for transients and surges is gaining interest as a standard for the quantification of EOS phenomena.

1.8.2.4 Periodicity

Electrostatic discharge (ESD) events are typically aperiodic [73]. Charge is accumulated, and current transfer occurs as the result of a switch or electrical breakdown. The events are typically a single pulse. The pulse can be single polarity or bi-directional.

EOS events can be periodic, aperiodic, and can be single polarity or bi-directional. EOS events can be oscillatory signals on the power grid or incoming power source.

1.8.2.5 Repeatability

Electrostatic discharge (ESD) events are not repeatable events, whereas EOS events can be repeatable [73]. EOS events associated with motors, actuators, machinery, and power sources can be repeatable events.

1.8.2.6 Failure Mechanisms

Electrostatic discharge (ESD) event failure damage is typically localized and a small area in one device in a semiconductor chip. ESD events can be larger areas when the current magnitude or voltage is significant.

It is commonly viewed that EOS events cause larger failure sites. One misconception is that if it is large, it must be an EOS event (note: this is not always true). EOS event failure damage can be the same as ESD events, but the key distinction is that there exists additional failures not observed from ESD events. EOS event failure damage can include the following:

- Bond pads
- Wirebond delamination
- Wirebond bending
- Wirebond melting
- Package seal materials
- Package molding materials
- Package paddle
- Package delamination
- Package discoloration
- Package pin damage
- Package melting
- Solder joint failure
- Printed circuit board (PCB) trace failure
- Discrete component (e.g., capacitors, diodes)
- EOS protection device failures.

1.8.3 Electrical Overstress and Electrostatic Discharge Similarities

Electrical overstress (EOS) and electrostatic discharge (ESD) events are both processes that can cause semiconductor device failure and system failures. These processes have both differences and similarities. In this section, the similarities between EOS and ESD events will be discussed.

EOS and ESD events lead to electrical over-voltage (EOV), electrical over-current (EOC), and electrical over-power (EOP) failures.

A second similarity is both EOS and ESD events can occur in manufacturing and production environments and in the field.

A third similarity is EOS and ESD can lead to failure of semiconductor component failures. In both events, the current and voltage levels are significant enough to lead to dielectric breakdown, second breakdown (It2), and melting of the semiconductor devices. EOS and ESD events can damage the following components:

- Active semiconductor devices
- Passive semiconductor devices
- Wire interconnects (e.g., wiring layers, vias, and contacts)
- Interconnect power bus
- Interconnect ground bus
- Inter-level dielectrics (ILD).

Because both EOS and ESD events can cause damage to semiconductor components, at times, it is hard to distinguish whether the event is EOS or ESD; this interferes with the ability to determine the root cause for some events.

1.8.4 Comparison of EOS versus ESD Waveforms

Figure 1.7 contains examples of both electrostatic discharge (ESD) and electrical overstress (EOS) waveforms. In the plot, ESD waveforms for the human body model (HBM), machine

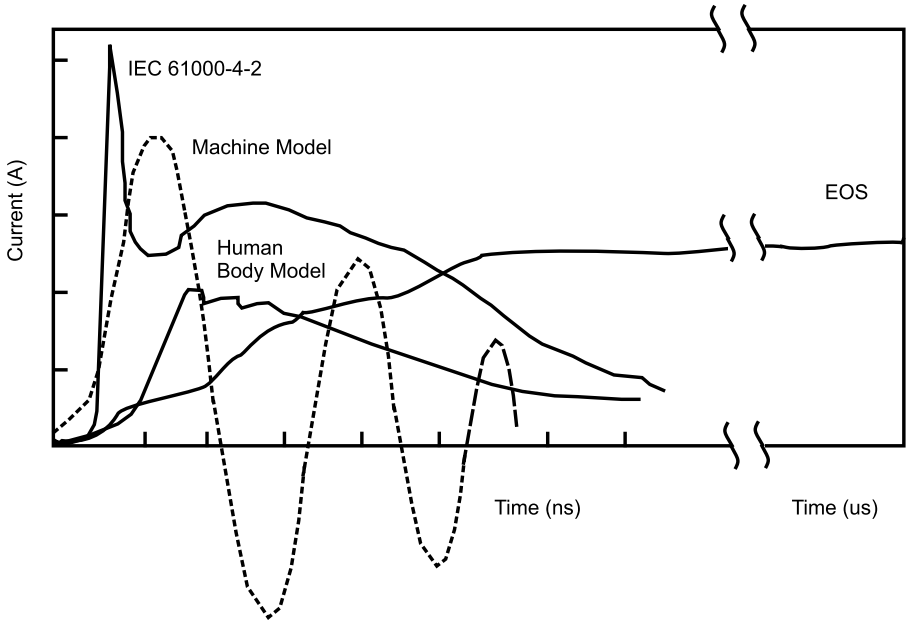

Figure 1.7 EOS and ESD event waveform comparison

model (MM), and IEC 61000-4-2 are shown. In comparison, an EOS waveform is highlighted. The key point is that the ESD event waveforms are significantly shorter than EOS events.

1.8.5 Comparison of EOS versus ESD Event Failure Damage

It is a common practice to judge the root cause based on the signature of electrical overstress (EOS) or electrostatic discharge (ESD).

For the electrical signature, both EOS and ESD events produce the following:

- Electrical open (open connections)
- Electrical short of signal pin to power rail (V_{DD})
- Electrical short of signal pin to ground power rail (V_{SS})
- Low resistance between power supply rail (V_{DD}) and ground rail (V_{SS})
- High I_{DD} current
- Excess supply current
- Parametric shift of signal or power pins
- Functional failure of circuits.

From these items, one cannot distinguish if the event was an EOS or ESD. These electrical signatures can occur due to printed circuit board failures, component package failures, interconnect failures, component signal pin ESD network failures, I/O failures, component ESD power clamp failures, or internal chip failures.

From the visual signature, whereas EOS events cause these type of failures, ESD events do not cause the following failures:

- External package power or signal pin melting
- External cracking in the package
- External displacement of the package (e.g., top removed)
- Melting of the package material
- Discoloration of the mold compound
- Physical hole in the mold compound
- Visible bulge or ablation in the mold compound
- Carbonized mold compound
- Bond wire melting
- Bond wire vaporization

- Bond wire–bond pad separation
- Bond pad cracking and de-lamination
- Electro-migration.

Both EOS and ESD events lead to the following signatures:

- Metal interconnect damage – blistering, agglomeration, or displacement
- Metal discoloration
- Metal film crystalline structure change
- Inter-level dielectric (ILD) cracking
- MOSFET source–drain silicon melt damage
- Diode emitter–base metallurgical junction damage
- Silicide film discoloration
- Silicide film phase change and crystal structure change
- Silicide metallurgical junction spiking
- Tungsten metal contact surface spiking.

It is commonly believed that EOS events are larger damage patterns than ESD events. This can lead to misdiagnosis of the root cause of events. Charged board events (CBE) and even charged device model (CDM) failures can be large areas when involving charge transfer from a substrate or a power grid (e.g., V_{DD}).

What is true is some ESD events may be isolated spatially to one or two devices within a I/O circuit. EOS events can be related to multiple currents, and multiple devices. Typically, in an ESD event, it is related to one current path, and a few devices in that given current path.

1.9 ELECTROMAGNETIC INTERFERENCE

Electromagnetic interference (EMI) is interference, or noise, generated from an electromagnetic field [94–115]. Electromagnetic interference is electric and magnetic fields that interfere with electrical components, magnetic components, and electrical or magnetic systems. EMI can lead to both component level or system level failure of electronic systems. EMI can lead to failure of electronic components, without physical contact to the electronic system. In the industry, there are a significant number of standards and tests to address both EMC and EMI concerns [94–115].

1.9.1 Electrical Overstress Induced Electromagnetic Interference

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1.10 ELECTROMAGNETIC COMPATIBILITY

Electromagnetic compatibility (EMC) is the ability of an electronic system to function properly in its intended electromagnetic environment and not be a source of electronic emissions to that electromagnetic environment [94–115]. EMC has two features. The first feature is a source of emission of an electromagnetic field. A second feature is the collector of electromagnetic energy. The first aspect is the emission of an electromagnetic field which may lead to electromagnetic interference of other components or systems. The second aspect has to do with the susceptibility of a component or system to the undesired electromagnetic field. Today, there are many standards and tests on the subject of EMC [99–111].

1.11 THERMAL OVER-STRESS

When electrical over-current occurs, electronic components can have excessive Joule heating, material property changes, melting, or fire. This state can be referred to as thermal over-stress (TOS). Thermal over-stress can be a result of an electrical over-current, or electrical over-power [118]. TOS can occur when a component undergoes thermal breakdown, thermal instability, or thermal run-away. Failure signatures from thermal overstress can be as follows:

- External package power or signal pin melting
- External cracking in the package
- External displacement of the package (e.g., top removed)
- Melting of the package material
- Discoloration of the mold compound
- Visible bulge or ablation in the mold compound
- Carbonized mold compound
- Bond wire melting
- Bond wire vaporization
- Bond wire–bond pad separation

- Bond pad cracking and de-lamination
- Electro-migration
- Dielectric breakdown.

1.11.1 Electrical Overstress and Thermal Overstress

Electrical overstress (EOS) can lead to thermal overstress (TOS). For example, electrical overvoltage of semiconductor bipolar junction transistors, MOSFETs, or LDMOS transistors undergoes electrical breakdown, followed by thermal instability, and then thermal runaway. But, not all forms of EOS lead to thermal failure.

In some cases, electrical over-voltage (EOV) does not lead to thermal overstress. For example, electrical breakdown of dielectric materials can lead to damage to the dielectric and impact device, circuit, or system operability. Electrical overstress can lead to changes in the material properties, which are non-destructive. In this case, thermal overstress may not be present and there is no concern for melting or fire. Thermal overstress can also occur from internal heating from functional operation, burn-in, and functional voltage stresses.

1.11.2 Temperature Dependent Electrical Overstress

Electrical overstress (EOS) is temperature dependent because the materials on the printed circuit board and components have electrical properties which are temperature dependent [118].

Metal conductors, such as aluminum and copper, have a resistance which increases with temperature. Joule heating occurs in conductors, leading to heating of the conductors. As the metal conductors increase in temperature, the resistance increases, leading to a higher internal Joule heating; this process can lead to thermal runaway.

Junction breakdown is also temperature dependent. As will be discussed in Chapter 2, the power-to-failure of a material is dependent on a critical temperature; this critical temperature can be the melting temperature. Melting temperatures are discussed in the next section.

Dielectric breakdown also involves a thermal process. Time dependent dielectric breakdown (TDDB) can occur from electrical over-voltage (EOV). Different competing models of dielectric breakdown have been developed which involve both electrical and thermal processes [113–118].

It is believed, for short pulse events, that the dielectric breakdown is an intrinsic breakdown, driven by electric processes [118]. For longer pulse events, such as EOS events, thermal processes take place. The two-stage process incorporates a first stage which is associated with localized hole and electron trapping in the bulk and interactions at the interface. When the density of carriers forms a conduction path, known as a percolation path, current flows through the dielectric. Since the heat transfer within the dielectric is low, the Joule heating is local to the percolation path. A thermo-chemical process occurs, which involves both heating and bond breakage. The temperature dependency of the dielectric is a function of the physical thickness of the dielectric [118].

Table 1.3 Materials and melting temperatures

Material	Melting temperature
Aluminum	660 °C
Germanium	938.25 °C
Gold	1064 °C
Copper	1200 °C
Silicon	1312 °C
Silicon dioxide	1600 °C
Titanium	1668 °C
Tantalum	2400 °C
Tungsten	3422 °C

1.11.3 Electrical Overstress and Melting Temperature

During electrical overstress (EOS), high currents can lead to melting of the materials in the semiconductor chip, packaging, printed circuit boards, and system. Semiconductor components are made of dielectrics, semi-conductors, and conductors. Table 1.3 shows examples of materials used in semiconductors and melting temperatures. From EOS failures, molten material can be observed. Given that the material has melted, this teaches us the minimum temperature at the location of failure. Semiconductor interconnects consist of metal film, such as aluminum or copper, and refractory metals as liners. The refractory metals typically have very high melting temperatures.

1.12 RELIABILITY TECHNOLOGY SCALING

The scaling of semiconductor components and systems has influenced both reliability and electrical overstress (EOS) robustness. This issue will be a concern as technologies migrate to 10 nm technology.

1.12.1 Reliability Technology Scaling and the Reliability Bathtub Curve

As technology is scaled, the reliability of semiconductor devices becomes affected. This can be observed from the reliability "bathtub" curve. The reliability bathtub curve has three regimes to predict failure rate on a logarithm–logarithm plot of FITs versus time. The FIT rate is the number of fails in one billion hours. The first region is known as the infant mortality regime, followed by a second time regime, known as the use or useful life regime, followed by the end-of-life regime. The infant mortality is a decreasing linear regime on a log FIT versus log time plot. The second useful life regime is time independent and a low flat FIT rate. As one approaches the end-of-life (EOL) regime, reliability "wear-out" begins, leading to a linear increase in the FIT rate (Figure 1.8).

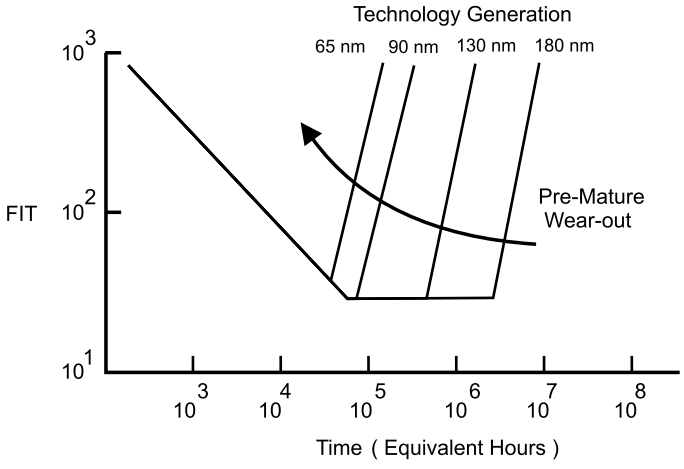

Figure 1.8 Reliability bath tub curve and technology scaling

As technologies are scaled, pre-mature wear-out occurs with a continued decrease in the length of the useful life regime. As technologies are scaled from 180 nm to below 65 nm, the length of useful life decreases and wear-out will be a larger issue.

This indicates that the fundamental devices within a semiconductor chip are becoming weaker with technology scaling; it will be important to improve the reliability of components by improving EOS robust circuits through layout, design, topology, and other means to counter the decreasing reliability of semiconductor devices.

1.12.2 The Shrinking Reliability Design Box

With technology scaling, the reliability design box is decreasing. Figure 1.9 shows an example of the scaling of the technology reliability design box. With each successive generation, technologies are getting less robust from a reliability perspective. To compensate

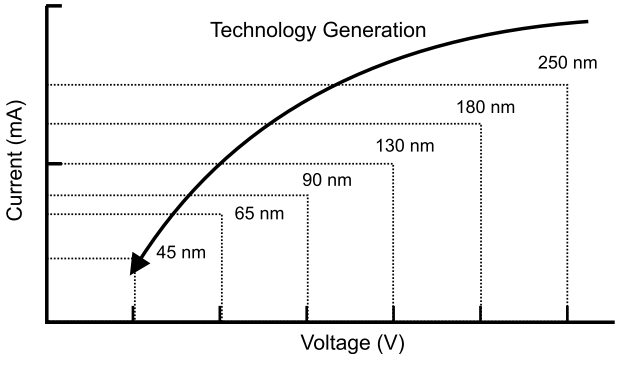

Figure 1.9 Shrinking technology design box

for the degradation in technology device reliability, the solution to provide future EOS robust technology is by providing more EOS robust circuits. EOS robust circuits will be achieved through design layout and circuit topology solutions.

1.12.3 The Shrinking Electrostatic Discharge Design Box

With technology scaling, the electrostatic discharge (ESD) design box has also been decreasing. The ESD design box decreases both in current and voltage magnitudes. The solution to address the decreasing ESD design box is through ESD layout design techniques, new innovations of ESD protection devices, and circuit topology.

1.12.4 Application Voltage, Trigger Voltage, and Absolute Maximum Voltage

One of the challenges in the development of an electrical overstress (EOS) solution is to develop EOS protection networks whose turn-on voltage is initiated above the application voltage, but below the failure voltage of the device or circuit. On the voltage axis, there is an application voltage, a trigger-voltage (e.g., clamp voltage) of the EOS protection device, and the absolute maximum (e.g., ABS MAX) voltage allowable on the device or circuit. Hence, there is a desired "window" on the voltage axis where the EOS protection network should operate, as illustrated in Figure 1.10. If the EOS protection voltage turn-on is below the application voltage, the EOS element is "on" during the voltage application range. If the EOS protection voltage turn-on is above the absolute maximum voltage (ABS MAX) then the circuit fails prior to initiation of the EOS protection solution.

Where the difficulty arises is that the application voltage must address variations in the power supply, V_{DD}, with a maximum application voltage of $V_{DD} + \Delta V_{DD}$. This reduces the triggering window for the EOS solution. In addition, there are temperature variations that also broaden the application space. As a result, the EOS trigger window also is reduced.

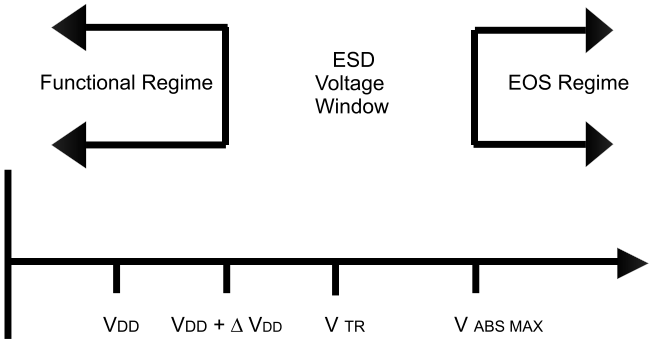

Figure 1.10 Voltage axis highlighting application voltage, EOS protection trigger voltage, and the ABS MAX voltage

Hence, the EOS protection element must remain "off" during the worse case voltage and worst case temperature conditions of the application.

For EOS solutions, another challenge is that there most likely are ESD elements in series with the EOS protection solution, which may also remain off during the application voltage and must also turn-on below the absolute maximum voltage condition of the circuit or device. For power electronics and smart power applications, one of the challenges is to provide a solution for both EOS and ESD protection.

1.13 SAFE OPERATING AREA

Electrical devices, either in integrated electronics or discrete elements, have a region which is regarded as the safe operating area (SOA) in current–voltage (I-V) space. Current–voltage (I,V) points in the interior of the safe operating I-V space are regarded as states where the device is safe to operate, and (I,V) points outside of this (SOA) are regarded as a domain where it is regarded as unsafe.

The SOA can be defined from an electrical or thermal perspective. Additionally, one can define a d.c. SOA or a transient SOA.

Figure 1.11 provides an example of an SOA in the I-V space for a given device.

1.13.1 Electrical Safe Operating Area

Figure 1.12 shows an example of a safe operating area which includes a thermal limit. The power contours form hyperbolas on an I-V plot. In components and systems, the voltage and current specifications for a rectangle in the I-V space. But, due to power limitations, the upper right corner is limited by both power and thermal limits.

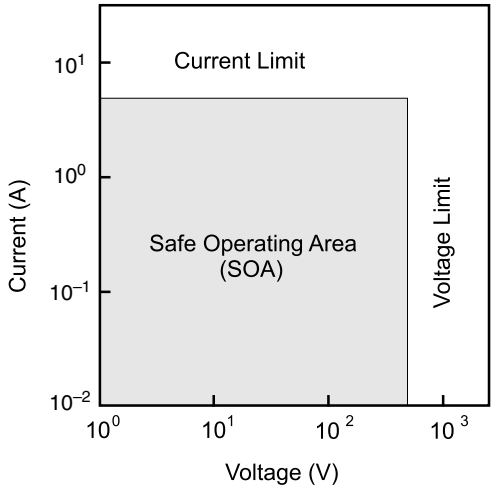

Figure 1.11 Safe operating area (SOA)

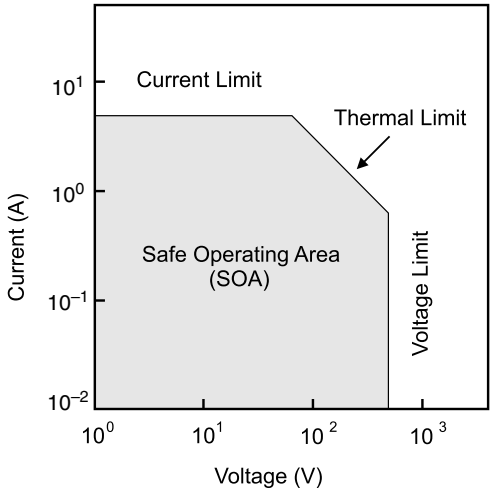

Figure 1.12 SOA with thermal limit

1.13.2 Thermal Safe Operating Area

With electronic components, there is a region for current and voltage conditions between the electrical safe operating area (E-SOA) and thermal runaway (e.g., thermal breakdown). This region can be referred to as the thermal safe operating area (T-SOA). Figure 1.13 shows the safe operating area with a thermal limit and second breakdown limitations. Thermal breakdown leads to failure and destruction of a component.

In the T-SOA, permanent degradation of electrical components can occur due to excessive heating. In this regime, Joule heating can occur.

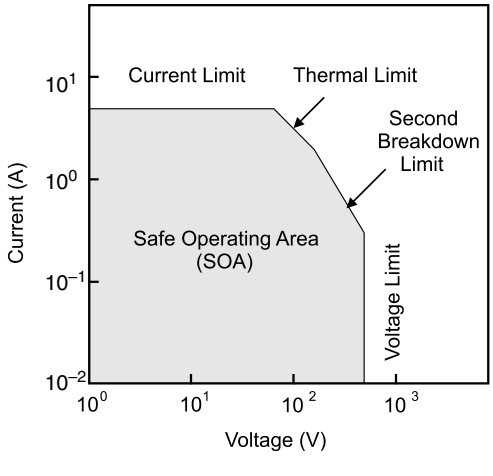

Figure 1.13 SOA with thermal limit and second breakdown limit

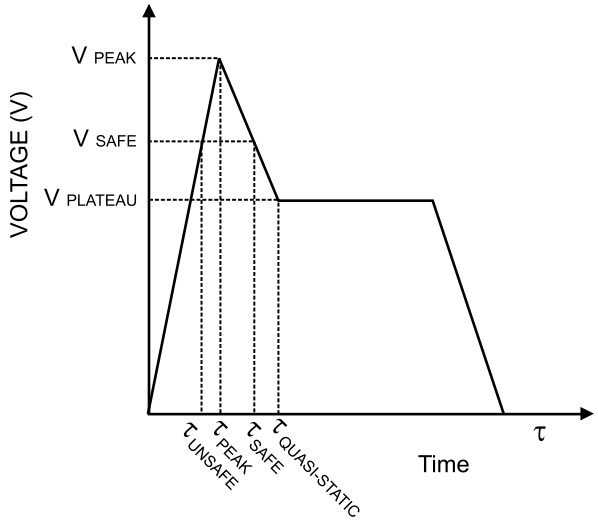

Figure 1.14 Transient safe operating area voltage–time waveform

1.13.3 Transient Safe Operating Area

For electrical overstress (EOS), transient phenomena can influence the failure level of a device or component. The quantification of the transient response can be defined by identifying and defining a "transient safe operating area." To define the transient pulse, it can be quantified as a trapezoidal pulse as defined in the transmission line pulse event. The trapezoidal pulse is defined with a rise time, a plateau, and a fall time. As shown in Figure 1.14, voltage states and affiliated time constants can be defined. The voltage can be defined as a plateau voltage, a peak voltage, and a "safe" voltage. For the time constants, corresponding times can be quantified, such as the unsafe transient time constant (time to the safe voltage), the peak voltage time, the safe voltage time, the quasi-static time (time to the plateau state), as well as the pulse time and the fall time.

1.14 SUMMARY AND CLOSING COMMENTS

In Chapter 1, the foundation for discussion of electrical overstress (EOS) was established. Chapter 1 opened the dialog for defining electrical overstress (EOS) and its relationship to other phenomena, such as electrostatic discharge (ESD), electromagnetic interference (EMI), electromagnetic compatibility (EMC), and latchup. EOS was defined as well in terms of electrical over-current, electrical over-power, and other concepts. In our discussion, there was an emphasis on distinguishing EOS from ESD. As a result, we drew distinctions through the text on differences of failure analysis, time constants, and other means of identification and classification. A plan to define a safe operating area (SOA) and its role in EOS was also emphasized.

In Chapter 2, the goal is to demonstrate the mathematics and physical models associated with power to failure, time constants, and materials. This chapter will provide the tools necessary to understand the equations and physical limits of the electro-thermal models derived in the past. A key distinction in this chapter is that the ESD time regime from the EOS time regime will be identified to draw attention to the different power-to-failure solutions for these processes. In Chapter 2, the physical and mathematical basis for understanding EOS is provided.

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