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Introduction to Modular Multilevel Converters

1.1 Introduction

The purpose of this chapter is to explain the circuit topology and the operation of modular multilevel converters (MMCs), and put them into their context. To this end the chapter begins with a review of other voltage source converter (VSC) topologies, starting with the two-level converter. This review also includes other multilevel converters. This serves as a basis for a description and analysis of the MMC. Finally, a number of similar topologies are reviewed and compared to the MMC.

Until the 1970s, power electronics for conversion between alternating current (ac) and direct current (dc) was dominated by current source converters (CSCs) operating by natural commutation. The main application was rectification, to provide direct voltage for dc motors and industrial processes. Also, high-voltage direct current (HVDC) power transmission originally made use of CSCs. The available current valves, first thyratrons and mercury arc valves and later thyristors, lacked turn-off capability, and were therefore only suited for naturally commutated converters.

The advent of power semiconductors with turn-off capability, allowing for forced current commutation, paved the way for VSCs which can operate independently from the ac grid. These converters offer increased controllability and improved harmonic performance, which radically expanded the field of application.

At the same time several new challenges in terms of electric power conversion emerged. Concerns about the negative environmental impact of traditional energy sources, such as the burning of fossil fuels, have led to a desire to use renewable energy sources (RES), such as wind power and solar power. None of these uses the kind of large synchronous generators operating at constant speed traditionally employed for electricity generation. Therefore, there is a need for a power electronic interface, which in most cases is best implemented by VSC.

Similar concerns have also led to demands for energy savings. Within electrical drive systems very significant savings can be achieved by a transition to variable-speed operation.

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In the past, pumps and fans, for instance, were usually operated at fixed speed with the fluid flow being controlled by throttling, which caused efficiency to be very poor at low flow rates. If the speed of the electric machine can be controlled overall power losses can be significantly reduced. Additionally, variable speed operation allows for improved control and precision in many industrial processes, contributing to increased automation and the improved quality of the product. The VSC fits these demands very well since it allows for convenient torque and speed control of synchronous machines and induction machines. The speed of dc motors could be controlled by CSCs, but such motors are less attractive because of the high maintenance cost of their brushes and commutators.

Also in transmission grid applications such as HVDC and FACTS (flexible alternating current transmission systems), the VSC has made inroads at the expense of thyristor-based naturally commutated converters. Several of the features of VSCs are attractive and sometimes also necessary in this field. The ability to impose a voltage on the ac side and thus control active and reactive power independently from each other is required in several applications. To these belong, for instance, HVDC connection of offshore wind farms as discussed earlier in this book.

From the beginning the prevailing VSC topology was the two-level converter and it is still the preferred solution for low-voltage applications. For systems operating at voltages beyond a couple of kilovolts, however, it is less useful since there are no available power semiconductors able to block voltages above this level. An option is to directly connect semiconductor elements in a series to create valves capable of withstanding higher voltages. Such concepts have been developed, but they tend to be complex since several problems need to be solved in order to ensure the operation and fault tolerance of such a valve. Also, this technology is not widely available, making it costly.

Instead, a transition to multilevel converter topologies offers better prospects for providing cost-effective power conversion at higher voltages. These topologies do not require direct series connection for increasing the operating voltage. Furthermore, the harmonic properties are much improved, so that the requirements on voltage and current distortion can be met without excessive switching losses.

The first multilevel topology to be used on a large scale was the three-level neutral point clamped (NPC) converter. It is still in frequent use for high-power motor drives. However, it cannot easily be extended to additional levels, which limits the field of application to the medium voltage range, at least if the series connection of semiconductors is not used to boost the voltage capability.

For operation at high voltage, using cascaded topologies that are based on series connection of converter *submodules* rather than semiconductors is a much more feasible alternative.

This chapter seeks to explain the development of cascaded converter topologies with a strong focus on MMCs for ac/dc conversion, since these are the main focus of this book. First, as a background, the two-level VSC is described. This is vital also to understand MMCs, since its basic building block, the two-level phase leg, is also used in the submodules of MMCs. The rest of the chapter is devoted to multilevel converters, starting with a general discussion of the consequences of the transition to multilevel operation. A brief treatment of diode-clamped converters is also given, focussing on the three-level variety, the NPC, since it is one of the most commercially viable multilevel converters. Thereafter, to introduce cascaded multilevel topologies, the concepts of converter submodules and submodule strings are presented and their operation is explained. This forms a basis for the treatment of the half-bridge MMC.

This topology and its operation and limitations are described in detail. Finally, a number of other cascaded converter topologies are reviewed and their properties are discussed in relation to those of the MMC.

1.2 The Two-Level Voltage Source Converter

The two-level converter is by far the most frequently used VSC for all applications with dc-side voltages up to approximately 1800 V. It is found in industrial drives, home appliances, automotive drive systems, as well as in low-voltage grid-connected converters (e.g. for integrating solar power into the power distribution grid). Furthermore, the two-level phase leg forms the basic building block also for the cascaded converter structures that are the main object of study in this book. For these reasons a thorough description of the two-level converter and its operation is given below.

1.2.1 Topology and Basic Function

Figure 1.1 shows the schematic diagrams of different two-level converters, only differing in terms of the number of phase legs. Like all VSCs, they are equipped with short-term energy storage, in the form of a dc capacitor, which will maintain the dc-side voltage approximately constant for a fraction of a fundamental cycle, regardless of the ac-side currents. The terminals of this capacitor form the dc terminals of the converter. To these terminals a number of phase

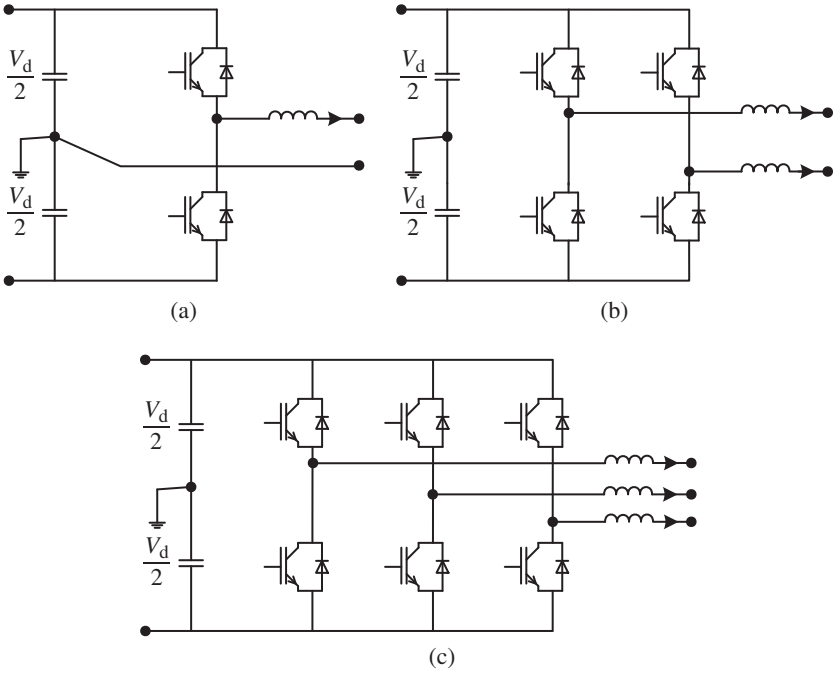


Figure 1.1 Two-level voltage source converters with different numbers of phase legs.

legs are connected in parallel. Each of these is equipped with two series-connected semiconductor valves capable of conducting current in both directions and blocking voltage in one direction by gate control. These are commonly implemented by a unidirectional controllable switch and an anti-parallel diode, although the switch and diode functions may be physically integrated, as is the case for metal-oxide-semiconductor field-effect transistors (MOSFETs) with a body diode. For a poly-phase converter, simply more phase legs are connected in parallel, as shown in the figure. The ac terminal is formed between the midpoints of the phase legs. Generally, an inductance is connected in series with the ac terminals, which will maintain the ac-side currents fairly constant in the short timeframe between commutations of a phase leg. Depending on the application, this inductance may be realized by a physical device, as in the case of a grid-connected converter with phase reactors. It may also be implemented indirectly, which is the case when an electric machine (generator or motor) or a transformer is connected to the converter ac terminal. Under such circumstances, the inductance results from the magnetic leakage fluxes of this device.

In Figure 1.2 the basic operation of the phase leg is explained in detail. The figure displays the different steps of a commutation cycle, which during operation is repeated at a frequency considerably higher than the ac-side fundamental frequency. Throughout the cycle, it is assumed that the ac-side current is directed out of the terminal as indicated by the arrow. Initially, in stage (a), the upper switch is conducting and the ac-terminal potential v_s equals that of the positive dc rail, $+V_\mathrm{d}/2$. In stage (b), the upper switch is gated *off* and the current is forced to instead start flowing through the lower diode since this is the only available path for a current in the given direction. When the current has fully commutated to the lower diode, stage (c), the potential at the ac terminal instead coincides with that of the negative dc terminal $-V_\mathrm{d}/2$. When this state has been achieved, normally the lower switch is also turned *on* so that a reversal of the direction of the phase current is possible. This is made after a certain delay, normally referred to as the *blanking time*. By inserting this delay, a situation where both switches are in the on-state and the dc link is shorted, albeit temporarily, can be avoided. Such a short-circuit can otherwise lead to a current surge which may damage the switches.

To make the ac outlet potential return to the positive dc rail the lower switch is first gated *off*. After the blanking time has passed the upper switch is again gated *on*, stage (d), whereby there will be a free current path from the dc-bus capacitor through this switch and the lower diode. This path only holds a low stray inductance, meaning that the current through it will increase rapidly, driven by the dc voltage. This rise implies that the current through the upper switch will increase, whereas that of the lower diode will decrease at the same rate. This becomes obvious by applying Kirchhoff's current law to the phase leg and keeping in mind that the ac-terminal current stays fairly constant during the commutation process. Finally, the lower diode turns off whereby the upper switch has replaced it as the path for the ac-side current. Thereby, the phase leg is back in the initial state and the sequence can be repeated.

The commutation sequence for the case where the ac-side current is instead flowing in the opposite direction (into the phase leg midpoint) is entirely analogous, but the current will instead be commutating between the upper diode and the lower switch.

It is often convenient to introduce a variable s to denote the switching state of a phase leg. It assumes the value $+1$ when the phase leg connects the ac outlet to the positive dc rail and -1 when instead the negative dc rail is connected, i.e.

$$v_\mathrm{s} = s\frac{V_\mathrm{d}}{2}. \tag{1.1}$$

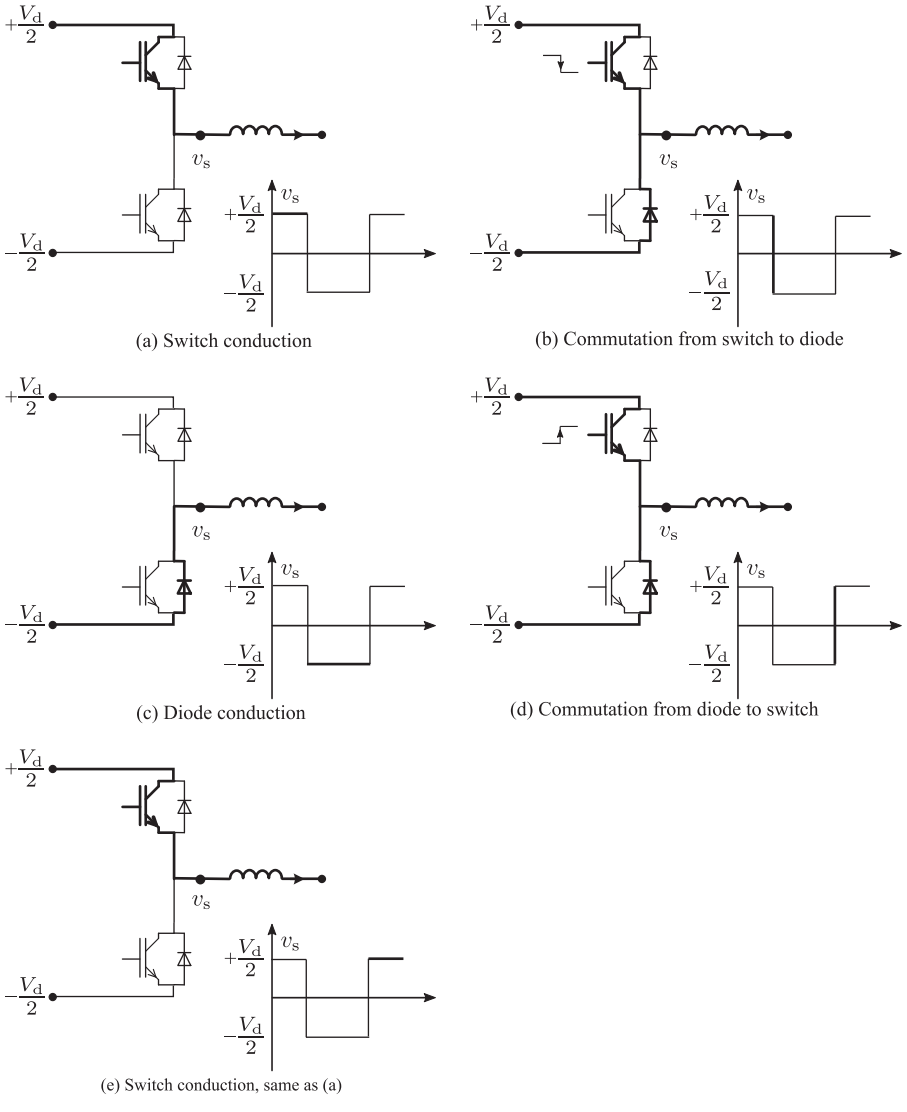


Figure 1.2 Stages in the operation of a two-level converter phase leg.

The switching states described above are used in the normal operation of the phase leg. It is obviously also possible to leave both switches in the *off*-state. Then the phase leg will behave like a diode bridge and the ac potential will be determined by the direction of the alternating current.

By employing the switching sequence described above the potential at the ac terminal, v_s, can be switched from one of the dc rails to the other at any desired instant and the converter can thus be made to behave as a controllable voltage source. Using repetitive switching and

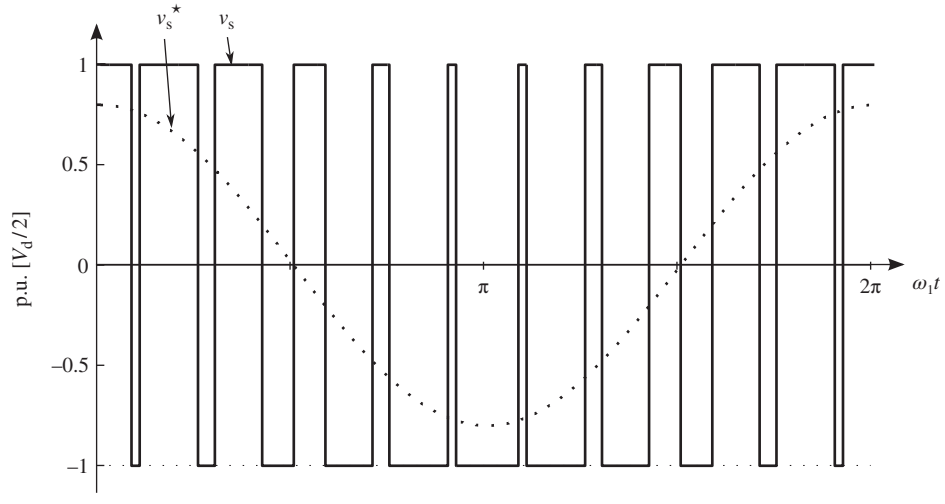


Figure 1.3 PWM of one phase leg.

appropriately timing the switching instances, a desired ac-side voltage can be achieved. This methodology is referred to as *pulse-width modulation* (PWM) since the outcome is that the width of the voltage pulses is varied. In Figure 1.3 it is explained how a desired reference voltage $v_s^\star$ can be realized by a converter employing PWM. In this figure the reference for the phase potential is assumed to be a sinusoid of frequency ω_1. Notably, the pulse width is varied so that the average of the switched phase voltage, taken over one cycle of the switching frequency, coincides with the reference voltage. Thus, when the reference curve assumes values close to $+V_d/2$, the ac terminal voltage will mostly be connected to the positive dc rail and, conversely, when the reference lies far below zero, it will instead be mostly connected to the negative rail. This way, the fundamental frequency component of the switched waveform will approach that of the reference. Because the output voltage is switched between discrete levels rather than varying continuously, the voltage will also contain a significant amount of higher-order harmonic components. However, owing to the high frequency, these will in most cases not cause significant currents or magnetic fluxes in equipment connected at the ac terminal. Therefore, in the first approximation they will not have any major impact on the system and can often be neglected. The issue of determining the switching instances is treated in more detail in Chapter 5, which covers modulation.

1.2.2 Steady-State Operation

The relationship between ac- and dc-side quantities will now be analyzed, with special emphasis on a converter with three phase legs that consequently can provide a three-phase alternating voltage; see Figure 1.4. As discussed above, the converter can be assumed to act as a controllable voltage source.

A key figure to be introduced at this stage is the *modulation index*, also sometimes referred to as the amplitude modulation ratio. It links the dc-side voltage to the fundamental component

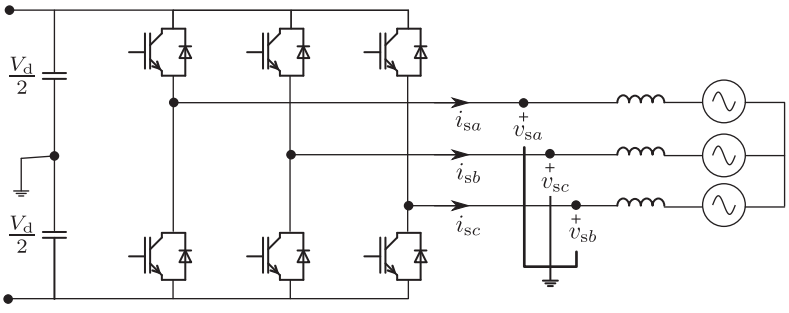


Figure 1.4 Three-phase two-level voltage source converter connected to symmetric load or source.

of the modulated voltage:

$$\hat{v}_s = m_a \frac{V_d}{2}. \tag{1.2}$$

Any static power converter needs to balance the active power flow on the dc and ac sides. This power balance can be formulated as

$$\frac{3}{2}\hat{v}_s\hat{i}_s \cos(\varphi) = V_d I_d. \tag{1.3}$$

Substituting Equation (1.2) into this expression gives an equation relating the currents on both sides of the converter:

$$3m_a\hat{i}_s \cos(\varphi) = 2I_d. \tag{1.4}$$

To allow for a simple analysis the phase voltages are assumed to be balanced and sinusoidal. Accordingly,

$$\begin{aligned} v_{sa} &= m_a \frac{V_d}{2} \cos(\omega_1 t) \\ v_{sb} &= m_a \frac{V_d}{2} \cos(\omega_1 t - 2\pi/3) \\ v_{sn} &= m_a \frac{V_d}{2} \cos(\omega_1 t + 2\pi/3). \end{aligned} \tag{1.5}$$

As already mentioned, the voltages of the converter will also contain high-order harmonics owing to their origin in PWM, but their impact can often be neglected.

Also the currents are assumed to be sinusoidal and balanced. This is, in most cases, a fair assumption given that the inductance, which is always connected at the ac terminal, will filter out higher-order harmonic components, leaving mainly the fundamental. Furthermore, they are lagging the voltage by an arbitrary power angle of φ.

$$\begin{aligned} i_{sa} &= \hat{i}_s \cos(\omega_1 t - \varphi) \\ i_{sb} &= \hat{i}_s \cos(\omega_1 t - \varphi - 2\pi/3) \\ i_{sc} &= \hat{i}_s \cos(\omega_1 t - \varphi + 2\pi/3). \end{aligned} \tag{1.6}$$

When φ is positive the converter will generate reactive power, whereas a negative value corresponds to the consumption of reactive power (assuming that $|\varphi| < \pi$ in both cases). The instantaneous power flow associated with one of the phases will amount to

$$p_{\mathrm{sa}} = v_{\mathrm{sa}} i_{\mathrm{sa}} = m_{\mathrm{a}} \frac{V_{\mathrm{d}}}{2} \cos(\omega_1 t) \hat{i}_{\mathrm{s}} \cos(\omega_1 t - \varphi) = m_{\mathrm{a}} V_{\mathrm{d}} \hat{i}_{\mathrm{s}} \frac{1}{4} [\cos(\varphi) + \cos(2\omega_1 t - \varphi)]. \quad (1.7)$$

There is a constant term whose magnitude depends on the power angle between voltage and current. This term corresponds to the active power being exchanged between dc and ac sides. Also, there is a fluctuating term oscillating at twice the ac-side fundamental frequency. The presence of this term is not surprising, considering that both the current and the voltage show zero crossings with a frequency of twice the fundamental. At these zero crossings the instantaneous power will obviously be zero.

The presence of a phase shift that is common to both the phase current and the phase voltage will naturally result in the same phase shift in the instantaneous power as it amounts to the product of these quantities. Thus, if the phase voltages and currents are symmetrically phase shifted, as in Equation (1.5) and (1.6) this will also be the case with the three powers of the phases

$$p_{sa}(\omega_1 t) = p_{sb}(\omega_1 t - 2\pi/3) = p_{sc}(\omega_1 t + 2\pi/3). \quad (1.8)$$

Therefore, the power flow related to the other two phase legs can be written as

$$\begin{aligned} p_{sb} &= m_{\mathrm{a}} V_{\mathrm{d}} \hat{i}_{\mathrm{s}} \frac{1}{4} [\cos(\varphi) + \cos(2\omega_1 t - \varphi - 2\pi/3)] \\ p_{sc} &= m_{\mathrm{a}} V_{\mathrm{d}} \hat{i}_{\mathrm{s}} \frac{1}{4} [\cos(\varphi) + \cos(2\omega_1 t - \varphi - 4\pi/3)]. \end{aligned} \quad (1.9)$$

The second-harmonic power fluctuation present in the phase quantities will thus cancel out in the total instantaneous power, which is obtained by summing p_{sa}, p_{sb}, and p_{sc}, and thus will be constant:

$$p_{\mathrm{s}} = p_{sa} + p_{sb} + p_{sc} = \frac{3}{4} m_{\mathrm{a}} V_{\mathrm{d}} \hat{i}_{\mathrm{s}} \cos(\varphi). \quad (1.10)$$

This result is also not really surprising considering that power remains constant in any balanced three-phase system and that there is no energy storage in the converter apart from the dc link capacitor. Hence, the only currents flowing into this capacitor will be higher-order harmonics resulting from the PWM. When either the phase currents or phase voltages are unbalanced, however, there will generally be second-harmonic pulsations in the capacitor.

Since only high-frequency harmonics will normally be present in the current fed into the capacitor, it can be small in size. The nominal energy storage capacity of the capacitor, which determines its size and cost, is computed as

$$E = \frac{C V_{\mathrm{d}}^2}{2}. \quad (1.11)$$

Thus, it is proportional to the capacitance. Typical values for many grid-connected converters are 2–4 J of stored energy per kilowatt of rated converter power. This means that the energy stored in the dc link capacitor corresponds to the power converted during 2–4 ms of nominal operation. Thus, the total energy stored could only sustain the rated power during a fraction of a fundamental cycle even if the capacitor was entirely discharged. Such low values of energy

storage are possible because only the higher-frequency current components are present in the current fed into the capacitor. These do not cause significant ripple in the voltage, bearing in mind that the reactance of the capacitor amounts to $1/\omega C$.

As will be evident in subsequent sections, in MMCs the dc capacitors need to absorb significant low-frequency harmonic current components. Therefore, these converters have greater demands in terms of stored energy in the capacitors.

1.3 Benefits of Multilevel Converters

Two-level VSCs are generally the most economical solution for low power ratings and low voltage, up to approximately 1 MVA. They have a simple structure with few components. For applications such as large industrial drives, FACTS, and HVDC transmission, where medium or high voltage needs to be handled, a number of shortcomings become evident, however.

- The ac-side voltages will contain significant harmonic components around multiples of the switching frequency. In converters using low-voltage power semiconductors high switching frequency can be used which mitigates this issue since only high-order harmonics will appear in the spectrum. However, for a converter in power transmission applications there is normally a desire to employ devices (typically insulated gate bipolar transistors (IGBTs) or integrated gate commutated thyristors (IGCTs)) with several kilovolts of blocking voltage. Each switching of such devices normally incurs high losses, implying that a switching frequency higher than approximately 1 kHz will cause excessive power losses. At low switching frequency more costly filters will be required to prevent the harmonics from causing negative effects in the equipment or the grid that is connected to the converter.
- The maximum blocking voltage of currently available power semiconductors applicable in VSCs (switches with turn-off capability and fast diodes) fall into the range of a couple of kilovolts. Thus, to realize a high-voltage converter for grid applications, a series connection of semiconductors has to be employed. This is related to a number of difficulties and no widely available technical solutions to achieve such series connection exist.
- In a two-level converter the phase voltage is always switched between the dc rails. In order to keep switching losses to feasible levels the switchings have to be fast, usually within a microsecond. At high direct voltages this implies that the voltage slope will be high, which imposes very significant stress on the insulation of any equipment connected to the ac terminal.

A transition to multilevel converter topologies can offer significant improvements of all these issues. Multilevel converters have more than one dc link capacitor, which means that several separate dc levels can be created inside the converter. The blocking capability requirements of the semiconductor valves is determined by the individual capacitor voltages rather than by the full dc link voltage. Therefore, the voltage rating and thereby the power rating of the converter can be increased without direct series connection of semiconductor elements.

The positive impact on the relation between the harmonic properties of the output voltage on the one hand and the switching frequency of the semiconductor valves on the other can be split into two largely independent parts. First, the output voltage waveform has more than two discrete levels. This is vital, since it implies that the amplitude of the harmonics can be reduced. Second, every semiconductor valve is not involved in every transition of the output

voltage. This implies that the frequency at which the output voltage is changed can be increased without increasing the switching frequency. Thereby, the first harmonics in the spectrum will appear at higher frequency where they can be more easily filtered out.

In Figure 1.5 the impact of a transition from the use of two-level to multilevel converter topologies is illustrated in the time and frequency domains. In this figure the switching frequency of the semiconductor valves has been kept constant at 15 times the fundamental as the number of levels is increased from two to seven. In the first approximation the switching losses would thus remain constant in all cases. Both the phase voltage and the amplitude spectra of this signal are displayed for each number of levels. As discussed, the pulse frequency is also

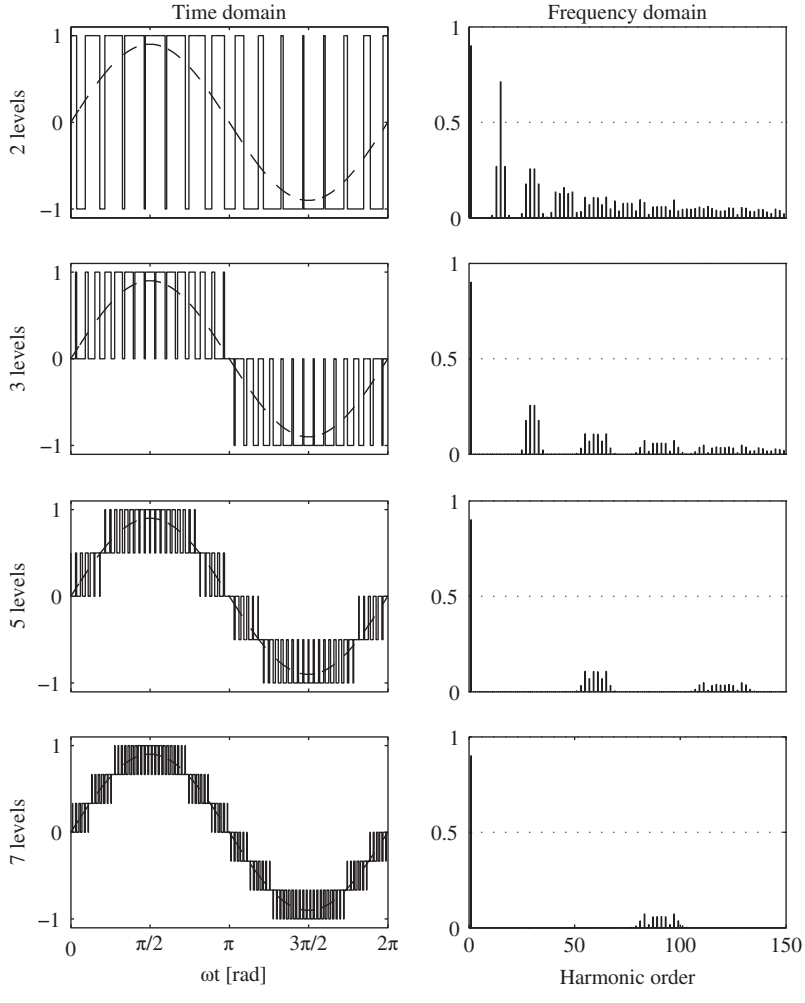


Figure 1.5 Impact of a transition to multilevel converters. The charts show the phase voltage of converters with two to seven levels in the time domain (left) and the frequency domain (right). In all cases the switching frequency is maintained constant at 15 times the fundamental frequency. The voltages are normalized by half of the pole-to-pole dc link voltage, i.e. the unit is p.u. $[V_d/2]$.

increased when a converter with a higher number of levels is used. The two-level waveform does not at all resemble a sinusoid, and its sole justification is that the use of PWM allows for a separation in the frequency domain between the desired fundamental and the undesired harmonics. However, with more levels the switched waveform will increasingly resemble the reference. In the frequency domain it is evident that more levels cause the harmonics to both appear at higher frequency and be of less magnitude. Both of these effects contribute to reducing the amount of filtering needed to achieve acceptable harmonic distortion. If the number of levels were to be increased further, an arbitrarily accurate approximation of the reference curve would result.

1.4 Early Multilevel Converters

This section will briefly describe a couple of multilevel VSCs that were introduced and developed before the MMC and other cascaded topologies, namely the *diode clamped topologies* and *flying capacitor topologies*. These have been extensively used for medium voltage applications such as high-power motor drives in industry, but also in some cases as high-voltage converters for power transmission applications. However, the number of levels generally cannot easily be extended beyond a few, which means that a direct series connection of power semiconductors is required for handling transmission-level voltages. As is the case for the two-level converter, they all have in common that a single dc-link capacitor, or a series connection of several capacitors, takes up the full pole-to-pole dc-side voltage.

1.4.1 Diode Clamped Converters

Diode clamped converters were first introduced by Nabae, Takahashi and Akagi in 1981 [1]; see Figure 1.6 showing three- and four-level variants. The dc link is split by series-connected capacitors creating additional dc levels. These topologies are also characterized by having diodes (called *clamping diodes*) providing additional paths for the current so that the ac terminal can be temporarily connected to these dc levels during operation. Thus, the creation of additional ac voltage levels is made possible.

The three-level variant is referred to as a *neutral point clamped* (NPC) converter since the clamping diodes in this case can link the ac terminal to the midpoint (which may be of neutral potential) of the dc link. This was also the name used in [1] which did not cover the extension to more than three levels. The NPC converter is the only diode clamped converter that has met significant commercial success. Although the concept is extendable to four or more levels, as shown in the figure, this has in most cases not been feasible in terms of cost. As the number of levels is increased the number of clamping diodes rises and, more importantly, the number of interconnects between the different valve elements goes up. This makes the mechanical design of the converter more complex. For a high-voltage converter this is particularly undesirable since in this case large mechanical clearances have to be observed, owing to the insulation requirements present. The three-level NPC converter, on the other hand, is being used extensively in medium-voltage applications, mainly high-power motor drives for industry. They are also used in railway traction converters and for the grid integration of wind turbines.

The different switching states of one phase leg of the three-level NPC converter are illustrated in Figure 1.7. States (a) through (c) are relevant to the case where the ac-side current is

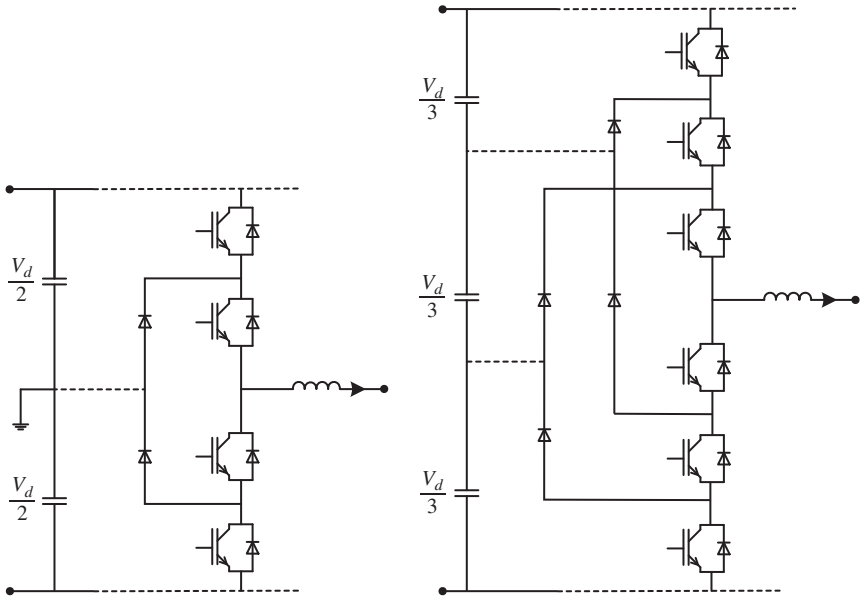


Figure 1.6 Diode clamped converter topologies. One phase leg shown of (a) a three-level (NPC) converter and (b) a four-level converter.

directed out of the phase terminal, whereas the states with opposite current direction are (d) through (f). The states where the phase outlet should be connected to either of the dc poles [(a), (c), (d) and (f)] are principally the same as in the two-level converter. Either both upper switches (for $v_s = +V_d/2$) or both lower switches (for $v_s = -V_d/2$) are gated on to achieve these states. To enter states (b) and (e) that connect the ac terminal of the phase leg to the dc link midpoint ($v_s = 0$) both inner valves S_2 and S_3 are gated on, whereas the outer switches are kept in the off-state.

During a fundamental cycle the phase potential should generally alternate between zero and $+V_d/2$ during the half-cycle when the reference is positive, and between zero and $-V_d/2$ during the other half-cycle (see also the graph corresponding to three-level modulation in Figure 1.5). From Figure 1.7 it is, for instance, evident that alternation between zero voltage and $+V_d/2$ is achieved by switching between states (a) and (b) when the direction of the alternating current is out of the phase leg, and between states (d) and (e) otherwise. As is the case for the two-level converter, there is no need to know the current direction to decide the switching pattern, as long as a blanking time delay is provided between the turn-off and turn-on of switches during a transition. For instance, states (b) and (e) are both achieved by having the inner switches conducting and the outer switches blocking, and the ac-side current direction determines which of these states is assumed.

Notably, as long as the dc link capacitors are well balanced, in none of the switching states does any valve need to block more than $V_d/2$ (i.e. half of the dc-link voltage). Thus, using semiconductor switches and diodes with a given blocking voltage and current rating, the three-level

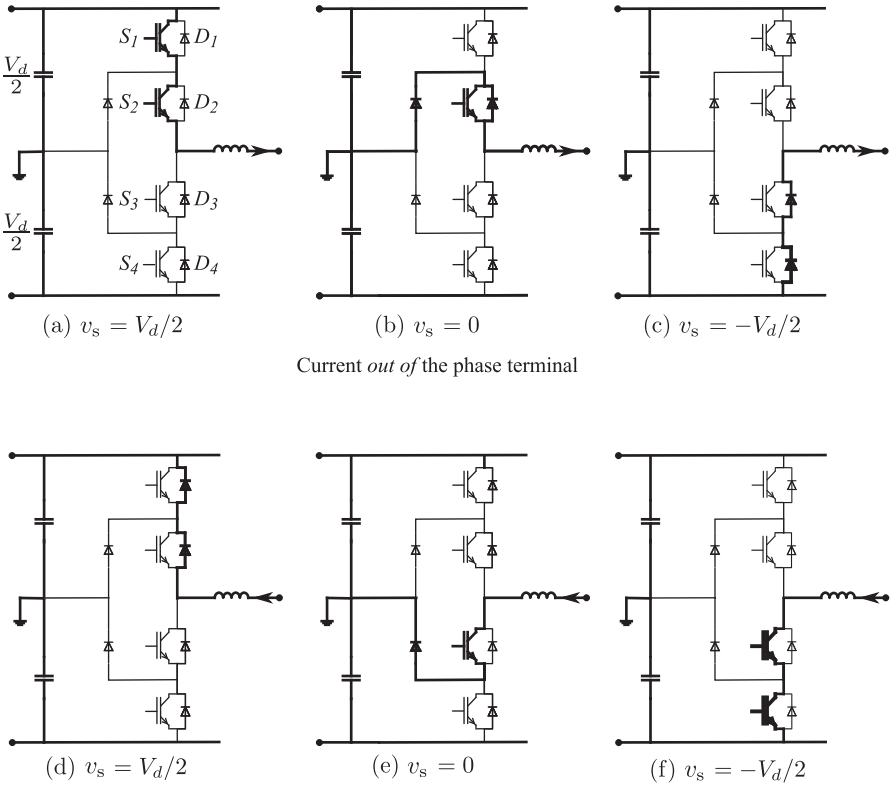


Figure 1.7 Switching states of the three-level neutral point clamped converter.

NPC converter can handle twice the direct voltage and hence twice the power of a two-level converter.

A weakness of the three-level NPC converter in HVDC applications is that in operation at high modulation index and with mainly active power flow ($\cos\varphi = 1$ or $\cos\varphi = -1$) the losses dissipated in the power semiconductors will be unevenly distributed. The outer switches S_1 and S_4 will experience both high switching losses and high conduction losses. The inner switches, on the other hand, will see mainly conduction losses since they stay in the conducting mode when transitions between states (a) and (b) and between states (e) and (f) take place. Hence, in an operating point that is typical for an HVDC converter the outer valves may see significantly higher losses than the inner valves. For this reason the valves need to be overrated, or otherwise semiconductors with a different rating would need to be used for the inner and outer valves respectively. Neither of these alternatives is attractive from a cost point of view.

To mitigate these issues another topology, labeled the *active neutral point clamped* (ANPC), converter has been introduced [2]. It differs from the normal NPC converter in that the clamping diodes have been replaced by valves of the same kind as the main valves (i.e. with a switch and an anti-parallel diode); see Figure 1.8. This opens up a few more possibilities in terms

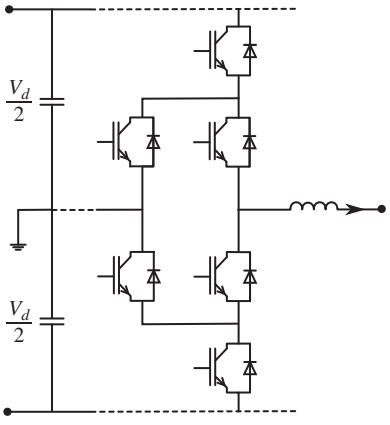


Figure 1.8 Three-level active neutral point clamped converter. One phase leg shown.

of control. More specifically, a three-phase ANPC phase leg offers more ways of implementing the zero-voltage state. This allows for a more even distribution of the losses among the semiconductors.

The ANPC converter has been used in two significant VSC HVDC projects, the *Cross-Sound Cable* and the *Murray link* [3, 4].

1.4.2 Flying Capacitor Converters

A further multilevel converter topology is the so-called *flying capacitor converter*, first presented in 1992 [5]. The topology is shown in Figure 1.9, which displays schematics of a generic phase leg with N levels (a) as well as a complete three-phase three-level converter (b). Like other multilevel topologies, it is based on using extra capacitors holding controlled direct voltages to provide the additional voltage levels. In this case the capacitors have no connection to a common dc link, and are therefore referred to as *flying capacitors*.

Figure 1.10 shows the different switching states of a three-level phase leg for the case where the ac-side current is directed out of the ac terminal at the midpoint of the phase leg. The voltage of the flying capacitor should be maintained at half of the pole-to-pole dc-side voltage (which is V_d). As evident from the figure, two of the states are again identical to the switching states of the ordinary two-level phase leg. These are labeled (a) and (d) and connect the ac terminal to either of the dc rails, whereby the terminal voltage becomes $+V_\mathrm{d}/2$ or $-V_\mathrm{d}/2$. By using other combinations of switches in the off- and on-states it is possible to instead force the current through the ac terminal to also flow through the flying capacitor. Thereby, the terminal voltage is zero and a third level is achieved. This becomes possible since in this case the flying capacitor voltage is added to, or subtracted from, the dc pole potentials. These states, labeled (b) and (c), are redundant in the sense that they produce the same null ac potential. However, the current direction through the flying capacitor is different in the two states. This makes it possible to balance the capacitor voltage by choosing the appropriate state whenever zero voltage should be imposed. With the direction of the ac-side current as indicated in the figure, state (b) will be chosen when the capacitor voltage is below the desired value, and state (c)

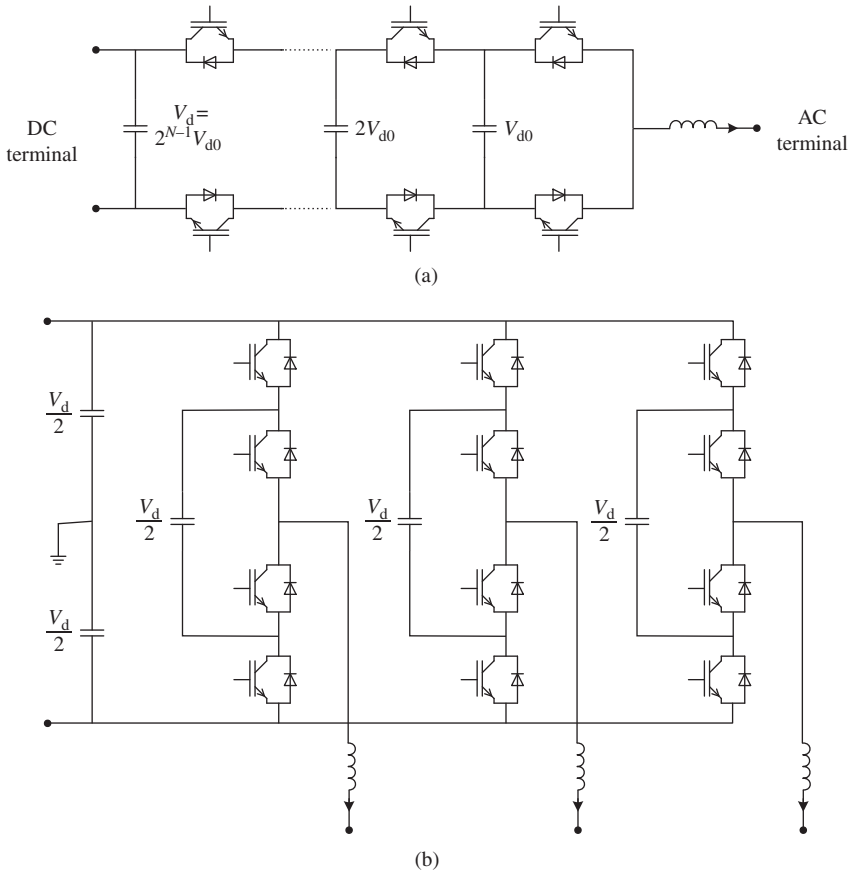


Figure 1.9 Flying capacitor converters, (a) one phase leg (generic schematic for an arbitrary number N levels), (b) three-phase three-level converter.

otherwise. At opposite direction of the ac-side current the states are interchanged. Thus, it is always possible to correct a deviation in the flying capacitor voltage in the next switching cycle. It should therefore generally only contain harmonics from the switching frequency and upwards. These are low in amplitude, owing to the low impedance of the capacitor at these frequencies. Thus, the existence of redundant zero-voltage states allows for maintaining the stored energy in the flying capacitor essentially constant over time.

As mentioned, Figure 1.10 shows the current paths during the possible switching states during the half-cycle when the ac-side current is directed out of the terminal. For the opposite case (into the terminal), the current paths in the phase leg are the same, but the current flows through diodes in the valves where it flew through switches in this figure, and vice versa.

In terms of voltage rating requirements, each valve in the three-level flying capacitor converter has to block half of the dc-bus voltage. Therefore, the required voltage blocking capability of each semiconductor device is the same as in the three-level NPC converter, and thus half of that of a two-level converter with the same rating.

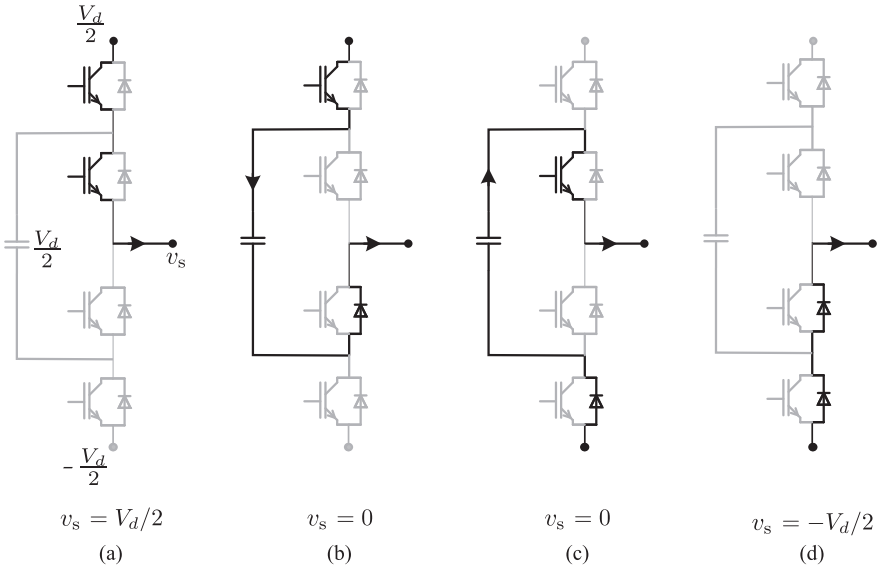


Figure 1.10 Switching states of a three-level flying capacitor converter phase leg. AC current directed out of the phase leg midpoint.

As seen in Figure 1.9(a), this topology can be extended to an arbitrary number of levels, and a correspondingly increased voltage handling capability, by adding more capacitors and semiconductor valves. Thus, it would be possible, at least in theory, to design a high-voltage converter (e.g. for hundreds of kilovolts) without the need for direct series-connection of power semiconductors. This would be the case if the number of levels were extended to the point where the voltage a single valve needed to block in the off-state were lower than the feasible blocking capability of available devices (i.e. a couple of kilovolts). However, such a circuit would be very complex, owing to the many flying capacitors that would connect valves at different points, creating many meshes. This would result in difficulties for the mechanical design of the converter, not least because the insulation requirements which stipulate that parts at different electrical potential need to be physically separated to avoid flashovers. Furthermore, it would require a large number of capacitors rated for different voltages, which would add significant cost. Notably, the total amount of stored energy in the capacitors would increase with the number of levels implemented. The capacitor cost, which is driven by the energy that can be stored, would therefore be higher for a converter with many levels. Therefore, a high-voltage converter, (e.g. for HVDC applications) would likely need to be implemented using a relatively limited number of levels and thereby would require valves capable of blocking high voltage. Thus, the valves would be implemented by series-connecting power semiconductor elements, although fewer devices would be in series compared to the case of a two-level converter of the same voltage rating.

Commercially, the flying capacitor converter appears to have met limited success compared to the NPC converter. It was marketed by the manufacturer Alstom for MV motor drive applications under the trade mark *Symphony*. Adoption by other vendors may have been impeded by certain patents, held by Alstom, that cover this topology.

1.5 Cascaded Multilevel Converters

The previous section treats two classes of multilevel topologies: diode clamped and flying capacitor converters. These are suitable for medium voltage applications (i.e. where the output voltage is a couple of kilovolts). The voltage can to a certain extent be increased without series connection of semiconductors, and the additional voltage levels improve the balance between harmonic performance and switching losses. For high-voltage applications they exhibit significant shortcomings, however. The number of levels cannot easily be extended, since this leads to very complex circuits where the commutation paths, where the current is switched to alter the output voltage, involve large parts of each phase leg.

This section introduces a further possibility, namely *cascaded multilevel converters*. These are based on the series-connection of converter elements, *submodules*, which each contain both of the core components of any VSC–dc capacitors and unidirectional semiconductor valves. They therefore represent a more truly modular approach where the commutation circuits are internal to the submodules. In general, no other effort than adding more submodules is required to increase the number of levels.

First, different kinds of submodules are discussed, and how these can be connected into strings to achieve more voltage levels and handle higher voltage. Later, the MMC with half-bridge submodules is discussed in detail. This converter permits ac/dc conversion with any number of levels in the voltages and it is the main topic of study in this book. Finally, a couple of other cascaded converters will be described and their operation explained.

1.5.1 Submodules and Submodule Strings

The fundamental building blocks of all cascaded multilevel converters are switching submodules (also referred to as *cells* or *chain links*), derived from the basic two-level phase leg described in Section 1.2. In Figure 1.11 schematics of the two basic alternatives are shown: half-bridge and full-bridge submodules. The half-bridge submodule consists of one two-level phase leg parallel to a dc capacitor that will maintain a direct voltage. The external terminals of the submodule are formed by the phase leg midpoint on the one hand and one of the dc capacitor terminals on the other hand. Two possible switching states are possible. In the first, called *bypass*, the switch in the valve parallel to the external terminal is conducting and the terminal voltage is zero. In the other state, labeled *insertion*, the valve in series with the submodule capacitor is conducting, implying that the voltage at the terminal equals the capacitor voltage. The output voltage of the submodule can be described in terms of a switching function s as

$$v = sV_c. \tag{1.12}$$

The switching function assumes the value 0 in the bypass state and 1 when the submodule is inserted. An additional state, labeled *blocking*, can be archived by leaving both switches in the non-conducting state. In this state the voltage at the terminals will depend on the direction of the current since only the diodes may conduct. In one direction the voltage will be zero and in the other the capacitor voltage will be present. This state is not used in normal operation, only during start-up and certain emergency conditions.

The full-bridge submodule has two phase legs connected in parallel to the same capacitor, and the external terminals are formed by the midpoints of the two legs. The normal switching

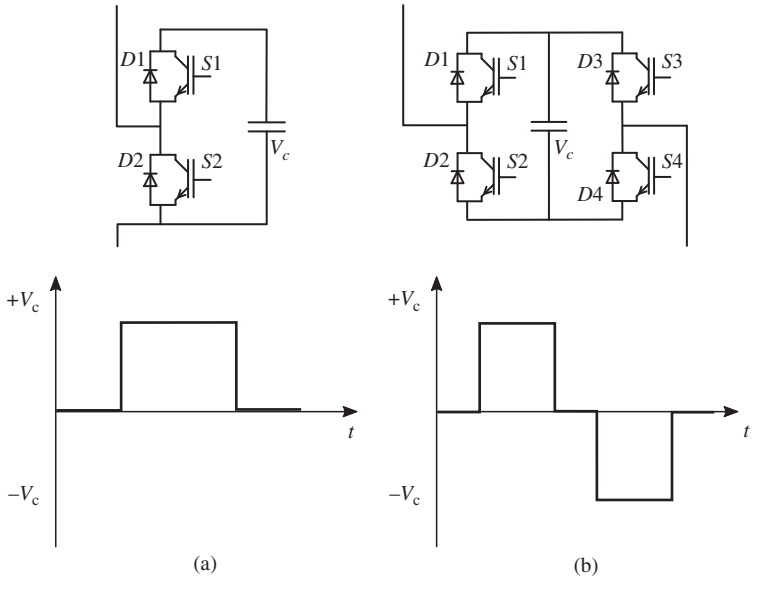


Figure 1.11 Converter submodules: half-bridge submodule (a) and full-bridge submodule (b).

states of the legs give rise to four different switching states for the entire submodule. Using the switching functions for the two legs the submodule voltage can be written as

$$v = (s_1 - s_2)V_c. \tag{1.13}$$

The switching functions again assume the values 0 or 1. With $s_1 = 1$ and $s_2 = 0$

$$v = +V_c$$

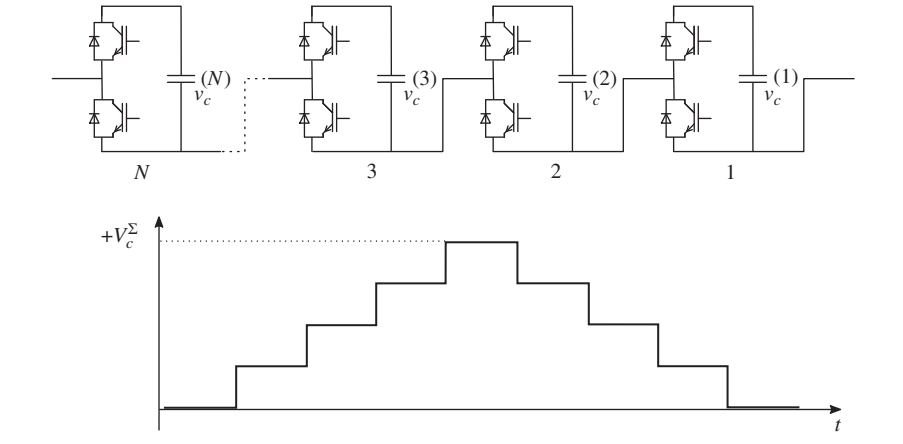
and with $s_1 = 0$ and $s_2 = 1$

$$v = -V_c.$$

Unlike the half-bridge, the full-bridge is thus able to provide a bipolar voltage. The two states $s_1 = s_2 = 0$ and $s_1 = s_2 = 1$ will both bypass the submodule and thus result in zero output voltage. However, the current through the submodule will follow different paths in these states. Either through the same node as the positive or the negative capacitor terminal. Therefore, in practical operation, both of these states will normally be used alternately in order to achieve even loading of the semiconductor valves and symmetric distribution of power losses.

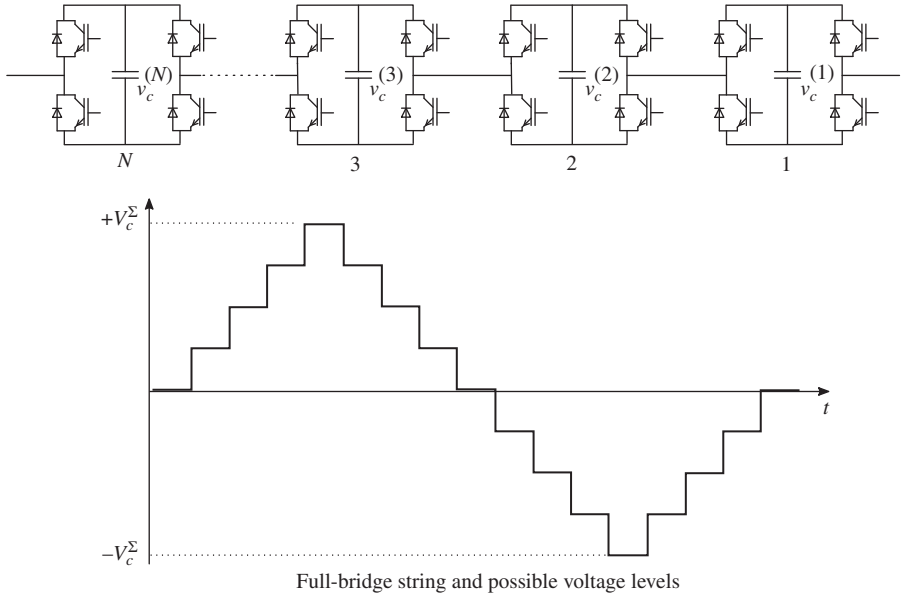
Also the full-bridge submodule may be blocked (i.e. all of the switches are gated off). In this case it will behave as a diode bridge, and the terminal voltage will equal the capacitor voltage ($+V_c$) regardless of the current direction.

In conclusion, the converter submodules described can behave as controllable voltage sources, as long as the voltage of the submodule capacitor is maintained sufficiently constant. The half-bridge submodule can only provide a unipolar voltage and is therefore only suited to producing a voltage with a dc component. The full-bridge, on the other hand, is bipolar and can deliver a pure alternating voltage or a combination of ac and dc components.



Half-bridge string and possible voltage levels

(a)



Full-bridge string and possible voltage levels

(b)

Figure 1.12 Submodule strings and their possible voltage levels: (a) half-bridge string and (b) full-bridge string.

In both of the discussed submodule types the capacitor has to be of significant size as it should maintain an approximately constant direct voltage while carrying significant currents at low harmonic order, usually fundamental and second.

Series connection of the submodules discussed above into *submodule strings* allows for extending the voltage that can be handled; see Figure 1.12. Also, the number of levels the terminal voltage can assume obviously increases with the number of series-connected

submodules. A string of N half-bridge submodules can take values between zero and NV_c (i.e. a total of $N + 1$ levels). A full-bridge string with the same number of submodules can provide all voltage levels between $-NV_c$ and $+NV_c$, including zero, which implies a total of $2N + 1$ levels. In a converter intended for high voltage, strings of hundreds of submodules may be required to handle the voltage. Under such circumstances the voltage provided may be seen as approximately continuous since the size of one voltage level (i.e. the submodule capacitor voltage) is very small in comparison to the total voltage provided by the submodule string. As is further elaborated in Chapter 5, using more submodules also enables significantly reduced harmonic content.

For the operation of any submodule or submodule string it is mandatory that the power flow is balanced over time (i.e. that there are no constant terms in the power transferred at the terminals). Such a constant term would result in an uncontrolled increase or decrease in the capacitor energy, and thus also in the capacitor voltage. Accordingly,

$$\int_{t}^{t+T} vid\tau = 0, \tag{1.14}$$

where T is the duration of a fundamental frequency period. In the frequency domain this expression translates into

$$V_{\mathrm{d}} I_{\mathrm{d}} + \frac{1}{2} \sum_{h=1}^{\infty} \hat{v}_h \hat{i}_h \cos \varphi_h \equiv 0, \tag{1.15}$$

where V_{d} and I_{d} are the dc components of the voltage and current, respectively, whereas $\hat{v}_h$ and $\hat{i}_h$ are the magnitudes of the voltage and current harmonic components of order h and φ_h represents the phase angle difference between them.

An exception to these rules occurs if the submodule is equipped with some sort of energy storage significantly larger than the submodule capacitor. There has, for instance, been proposals put forth in the literature for connecting batteries in parallel to the submodule capacitors. This would be a way of creating a variable energy storage with an ac terminal. In such a case there can be a nonzero term in the power flow to or from the string, amounting to the power exchange with the battery.

Fulfilling Equations (1.14) and (1.15) will ensure that the stored energy of the submodule string does not change over a fundamental cycle. Generally, different forms of closed-loop control are required to maintain this balance.

For a converter based on submodule strings it is usually convenient to split the power balancing problem into two parts, which are addressed separately. The first relates to the overall energy exchange with the string and thus with maintaining constant total energy in it. This is equivalent to keeping the sum of the capacitor voltages V_c^{Σ} at a desired set point. There will generally be a certain inevitable variation during a fundamental cycle, owing to low-frequency alternating currents injected into the capacitors. This control feature is, therefore, aimed at regulating the average voltage over a cycle.

The second part concerns the balancing of the capacitor voltages of the individual submodules *within* the string. Owing to the fact that the submodules are not all inserted or bypassed at the same time, the capacitor voltages will differ slightly between the submodules. This control is local to each string and its purpose is generally to maintain the individual capacitor voltages, v_c^k, at equal fractions of the total capacitor voltage, v_c^{Σ}, i.e.

$$v_c^k = \frac{v_c^{\Sigma}}{N}. \tag{1.16}$$

As long as the power balance is maintained, a submodule string can behave as a fairly ideal voltage source within boundaries defined by the total capacitor voltage. Appropriate modulation of the switching pattern can implement the desired low-frequency and direct voltage components at the terminals of a string. The total capacitor voltage is a key factor in determining the cost of the string. It will determine the rating and thus the cost of the power semiconductors as well as the submodule capacitors. In an MMC, generally a direct voltage component as well as an alternating voltage component need to be provided simultaneously by each string. It is, therefore, of interest to understand how limits in terms of the ability to generate these voltage components are related to each other, and to the capacitor voltage. Or stated otherwise: what total submodule capacitor voltage V_c^{Σ} is required to produce the voltages required for a certain conversion task? This is the case particularly since the capabilities of full-bridge and half-bridge strings differ considerably in this regard.

It can easily be understood that to produce a voltage waveform containing certain low-frequency and dc components the submodule string has to be able to provide a short-time average voltage (over a carrier cycle) coinciding with this desired waveform. This is evident from Figure 1.5. The submodule string voltage must be able to assume values spanning the waveform to be reproduced at all times. Thus, it follows that a half-bridge string can produce a short-time-average voltage in the range $[0, V_c^{\Sigma}]$. With a dc component of V_{d} the half-bridge string can produce a peak alternating voltage with maximum amplitude

$$\hat{v}_1 = \frac{1}{2}\{V_c^{\Sigma} - |2V_{\mathrm{d}} - V_c^{\Sigma}|\}. \tag{1.17}$$

This relation is visualized in Figure 1.13(a). Evidently, the ac component can never exceed the dc level in the output. That is, without a direct voltage no alternating voltage is possible. Furthermore, from Equation (1.17) it can be understood that it is uneconomical to design the submodule string for operation with $V_{\mathrm{d}} < V_c^{\Sigma}/2$ since a lower total capacitor voltage can allow for the same ac and dc components to be produced.

On the other hand, the instantaneous voltage of a full-bridge string has to fall in the range $[-V_c^{\Sigma}, V_c^{\Sigma}]$. Therefore, in this case, the maximum ac voltage will instead relate to the dc component as

$$\hat{v}_1 = V_c^{\Sigma} - |V_{\mathrm{d}}| \tag{1.18}$$

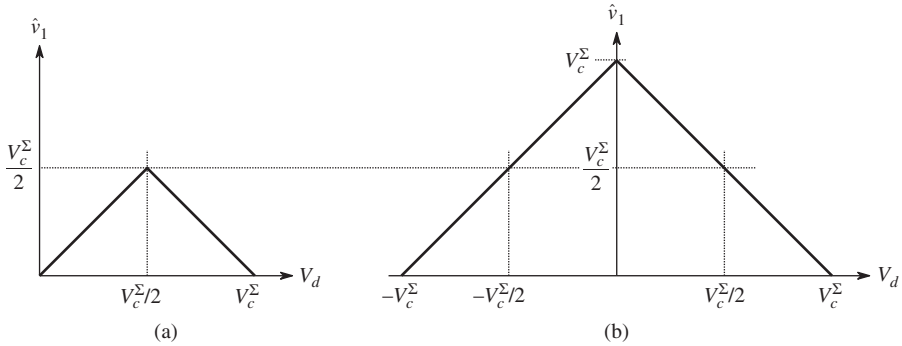


Figure 1.13 Capability of submodule strings to provide ac and dc voltage components given the same total submodule capacitor voltage V_c^{Σ}: (a) half-bridge string and (b) full-bridge string.

which is shown in Figure 1.13(b). Evidently, the capabilities either coincide with, or exceed, those of the half-bridge string. Only full-bridges can produce a pure ac component or a dc component with negative polarity. In case only an ac component is to be provided its magnitude can equal the full capacitor voltage, which is twice the maximum level possible with a half-bridge string. However, if the task is to produce a unipolar direct voltage with an ac component whose magnitude does not exceed the dc level, the two alternatives are equivalent. This can be understood by comparing the rightmost parts of the two charts in Figure 1.13.

The above reasoning assumes that the capacitor voltages are constant. Owing to the presence of harmonic currents fed into the submodule capacitors, there will generally be a certain fluctuation in the sum capacitor voltage (V_c^{Σ}) of a string during operation. This fluctuation may affect the capability to deliver a certain desired voltage. Depending on whether the peaks of the sum capacitor voltage coincide with the peaks of the reference voltage or not, the fluctuation may either reduce or increase the voltage capability, as explained in, for example, reference [6].

1.5.2 Modular Multilevel Converter with Half-Bridge Submodules

Until the year 2000 no pure cascaded converter topologies for ac/dc conversion were available. High-voltage VSCs (e.g. for HVDC applications), were implemented using direct series-connection of the semiconductor devices in order to withstand the voltage. Converters for reactive power compensation using full-bridge submodules were in use [7], but these lacked a dc terminal and were therefore not suited for ac/dc conversion, see also Section 1.5.3. There existed cascaded converters for ac/dc conversion, but these required individual isolated feeding of the submodules by transformers, and were not truly modular [8].

A major breakthrough was made by the introduction of the MMC with half-bridge submodules by Prof. Marquardt in 2002 [9]. It puts submodule strings to use in an ingenious way so that ac/dc conversion is made possible while maintaining the important benefits of cascaded converters in terms of voltage scalability and harmonic performance. These features have in a relatively short time made it one of the most used cascaded converter topologies.

Also, very intense research and development efforts, both in academia and in industry, have taken place. A search of the scientific database IEEE Xplore® made in the year 2015 using the exact search string "modular multilevel" yielded more than one thousand results. Notably, all of those results were published after the mentioned initial publications from 2002 so they have all been created within a time span of approximately 13 years. Also, the adoption within industry of this technology has been rapid. The manufacturer Siemens AG first employed the MMC for HVDC transmission, and the first major application was the Trans Bay Cable link installed in the US in 2010 [10]. Currently, all major vendors of HVDC systems offer solutions based on the modular multilevel topology.

1.5.2.1 Topology and Basic Function

In the previous section converter submodules and submodule strings were discussed. It was concluded that they can be made to behave as controllable voltage sources, as long as there is no net power exchange with a string over time, and as long as the energy balance between the submodules is maintained.

Figure 1.14 shows the schematic of an MMC for ac/dc conversion. The overall circuit structure resembles that of a three-phase two-level converter in that there are three phase legs with

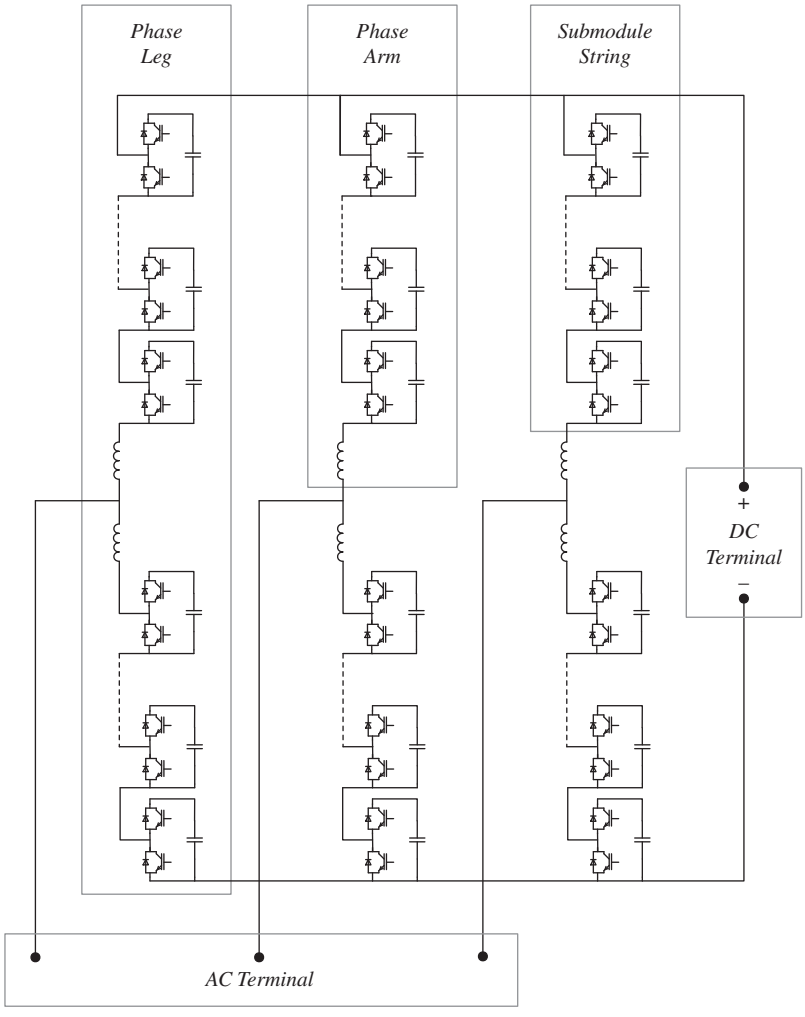


Figure 1.14 Three-phase MMC with half-bridge submodules.

a midpoint connection each. Together, these midpoints form the ac terminal of the converter. However, instead of the valves found in the phase arms of the two-level converter, the MMC has submodule strings. Therefore, the mode of operation is also fundamentally different. The circuit also has small inductors in each phase arm, which also implies an important difference from the two-level converter, where the inductance of the phase legs should be kept low to allow for rapid current changes during the commutations of the phase legs. In the MMC this is not needed since the commutations are internal to the submodules and there should be no such rapid changes of the phase arm currents. Instead, reactors are necessary in the phase arms since direct parallel connection of the voltage sources implemented by the submodule strings should be avoided. Without them, potentially high transient currents could occur between the phase legs. However, given that the voltages of the submodule strings can be controlled with

great precision, particularly if the number of submodules is high, these inductors generally do not need to be large.

Notably, numbers of phase legs other than three are also possible, which allows for connection to ac networks with other numbers of phases. For a converter connected to a single-phase network (e.g. a catenary network for railway power supply), two phase legs can be used instead. In such a case, the single-phase ac terminal is obtained between the midpoints of these phase legs.

In short, the operation of the converter is based on controlling the six submodule strings in such a fashion that the combination of voltages they provide results in the desired voltages being imposed on the dc and ac sides of the converter. Figure 1.15 explains how this is possible. The figure shows how the upper and lower submodule string voltages of a phase leg change during the course of one fundamental cycle. The *sum* of these voltages is maintained approximately equal to the desired pole-to-pole dc-side voltage V_d. Simultaneously, the *difference* in voltage between the upper and lower strings is varied. This way the potential at the ac outlet can be set to any point between the dc rails, neglecting the voltage drop across the relatively small arm inductors. In particular, an alternating voltage can be imposed at the outlet. It is also obvious that in a converter with several phase legs a symmetric set of alternating voltages can be provided while all legs maintain the same direct voltage. Thus, the converter can behave as a controllable voltage source not only with respect to the ac side but also as seen from the dc side. This differs considerably from the two-level converter and the other multilevel converters described thus far, which function as current sources behind a capacitor as seen from the dc terminal. Given that any number of submodules can be used, both ac-side and dc-side voltages of the MMC can be controlled with great precision.

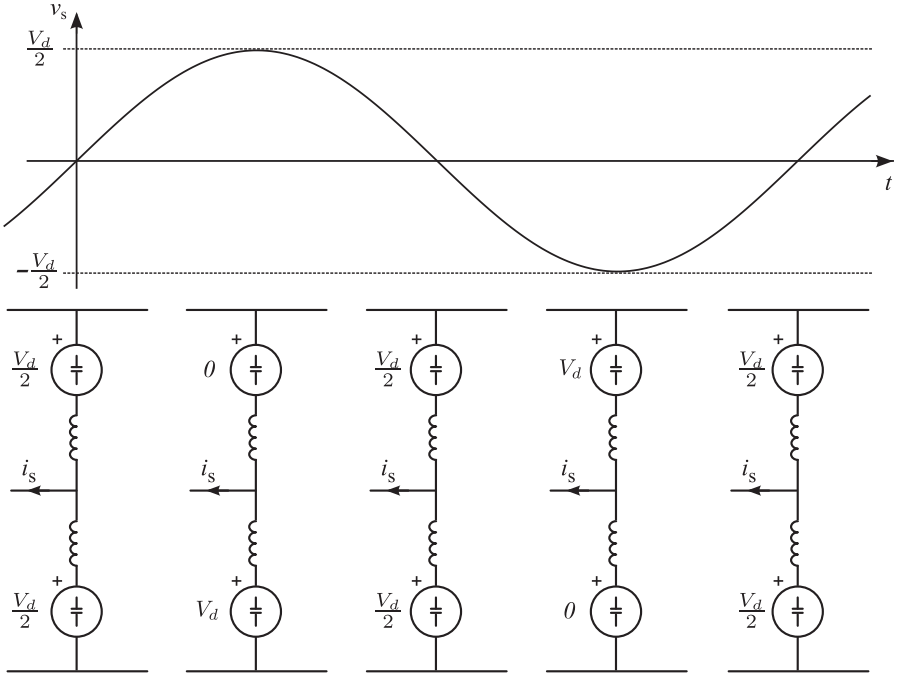


Figure 1.15 Voltages in a phase leg of an MMC.

Since the converter imposes voltages at both its terminals, the corresponding currents will depend on these voltages, and on the ac and dc networks connected. On the dc side it is a fair assumption that a relatively constant direct current can be maintained since the converter can provide a constant direct voltage. Likewise, if the converter is connected to a symmetric ac network and imposes symmetric voltages on it, symmetric ac-side currents will result. In Figure 1.16 the typical paths of these currents inside the converter are shown. It is seen how the dc-side currents split between the phase legs, and that the same current passes through both upper and lower arms. Also, the ac-side currents split between upper and lower phase arms. Since they are symmetric, they will sum to zero in the positive and negative dc poles and thus no ac components will appear on the dc side. It is obvious that the submodule strings of each phase arm need to provide direct as well as alternating voltage components while both direct and alternating currents flow through them.

The switching processes inside the MMC normally only involve one submodule at a time. Compared to the two-level converter, which switches the full pole-to-pole voltage at once, this implies a great improvement. In addition to the many benefits in terms of harmonic performance obtained by multilevel operation, the fact that only a small fraction of the direct voltage is switched simplifies the design of the converter. The steepness of the voltage flanks (dv/dt) during switchings is considerably reduced. Therefore, the impact of stray capacitances becomes much smaller, simplifying the mechanical design of the converter. Also the requirements on the insulation of equipment connected to the converter, such as transformers, can be significantly relaxed thanks to the lowered dv/dt.

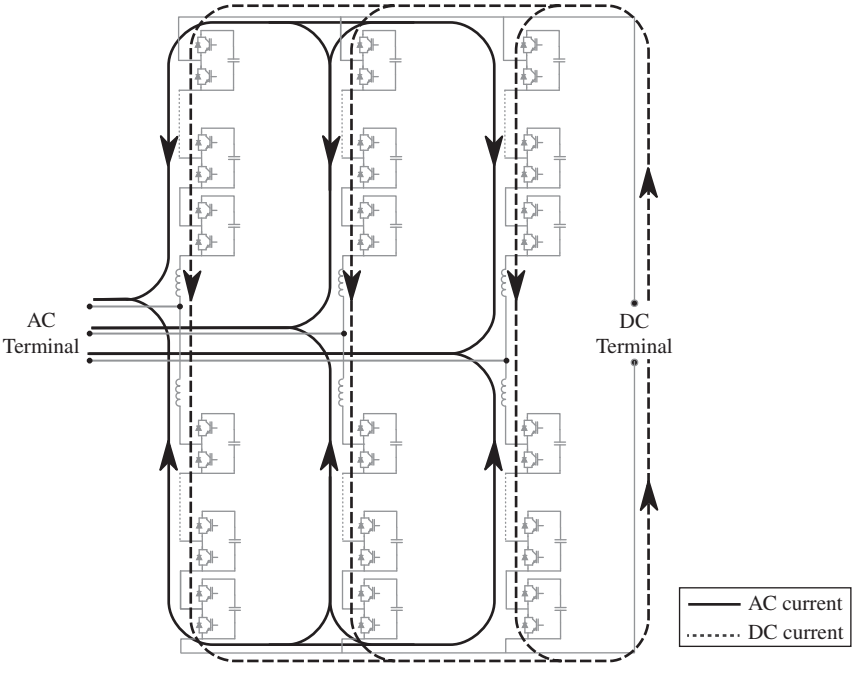


Figure 1.16 Paths for ac and dc current components within an MMC.

Furthermore, having the paths for the commutating currents internal to the submodules rather than involving large parts of the converter implies very significant benefits. The shortened commutation paths make it easier to keep the stray inductances low enough to avoid overvoltages during switchings. Also, reduced stray elements mean that faster switchings can be permitted, implying that the switching losses are reduced.

In terms of electromagnetic interference (EMI), the fact that the commutation loops are shortened and that the voltage steepness is reduced also has a very positive impact. Generally, less effort is required for limiting radiated EMI emissions in the design of an MMC than with a two-level converter of a similar rating.

1.5.2.2 Decoupling of AC and DC Sides

In this section a general framework for analysing the operation of the MMC is described. The circuit equations governing the converter are decoupled by using a linear variable transformation linking the currents and voltages of the phase arms to quantities that are more convenient for describing the operation. At this stage the submodule strings in each phase arm are treated as controllable voltage sources, as discussed in Section 1.5.1.

In Figure 1.17 an equivalent circuit of the converter is displayed. The voltages provided by the submodule strings of the phase arms are labeled $v_{l\phi}$ (lower arm, phase leg ϕ) and $v_{u\phi}$ (upper arm, phase leg ϕ), where index ϕ is substituted with any of the phase symbols a, b, or c. The corresponding currents flowing through the phase arms are labeled $i_{l\phi}$ and $i_{u\phi}$. The external circuits on the ac and dc sides are modeled in such a way so as to allow for common-mode as well as differential-mode voltages and currents on both sides.

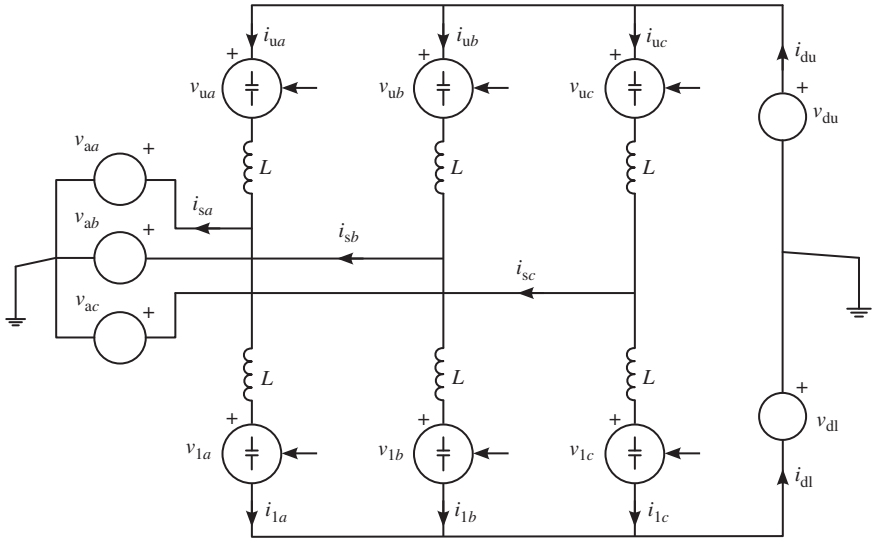


Figure 1.17 Simplified equivalent schematic of an MMC. Submodule strings depicted as controllable voltage sources.

The mentioned linear transformation is defined as

$$\begin{aligned} v_{s\phi} &= \frac{v_{l\phi} - v_{u\phi}}{2} \\ v_{c\phi} &= \frac{v_{l\phi} + v_{u\phi}}{2} \\ i_{s\phi} &= i_{u\phi} - i_{l\phi} \\ i_{c\phi} &= \frac{i_{u\phi} + i_{l\phi}}{2}. \end{aligned} \tag{1.19}$$

A physical interpretation of these quantities is that $i_{s\phi}$ are the ac-side phase currents and $v_{s\phi}$ the inner emf (electromotive force) of each phase leg driving these currents. Correspondingly, $i_{c\phi}$ are the average currents of each phase leg, whereas $v_{c\phi}$ are the voltages driving these currents. The main part of these latter voltages and currents is the dc component, accounting for the active power flow through the converter. However, $i_{c\phi}$ also contains any currents circulating between the phase legs and $v_{c\phi}$ any voltages driving these circulating currents. The inverse of the transformation is obtained simply by solving for the phase-arm quantities:

$$\begin{aligned} v_{u\phi} &= v_{c\phi} - v_{s\phi} \\ v_{l\phi} &= v_{c\phi} + v_{s\phi} \\ i_{u\phi} &= i_{c\phi} + \frac{i_{s\phi}}{2} \\ i_{l\phi} &= i_{c\phi} - \frac{i_{s\phi}}{2}. \end{aligned} \tag{1.20}$$

The voltage equation for a loop comprising an arbitrary phase leg and the dc link can be written as

$$v_{u\phi} + v_{l\phi} + L\frac{di_{u\phi}}{dt} + L\frac{di_{l\phi}}{dt} - v_{du} - v_{dl} = 0. \tag{1.21}$$

Substituting the inverse of the transformation (1.20) into this equation, and simplifying, yields

$$v_{c\phi} + L\frac{di_{c\phi}}{dt} - v_{dc} = 0, \tag{1.22}$$

with v_{dc} representing the average of the upper and lower dc-link voltages (i.e. $v_{dc} = (v_{du} - v_{dl})/2$). Correspondingly, the voltage equations for a loop going from the midpoint of the dc link to the midpoint of the ac side reads

$$v_{du} - v_{u\phi} - L\frac{di_{u\phi}}{dt} - v_{a\phi} = 0 \tag{1.23}$$

and

$$-v_{dl} + v_{l\phi} + L\frac{di_{l\phi}}{dt} - v_{a\phi} = 0. \tag{1.24}$$

By summing these two equations, and again substituting the inverse of the employed linear transformation (1.20) into the resulting equation the following is obtained:

$$v_{s\phi} - \frac{L}{2}\frac{di_{s\phi}}{dt} - v_{a\phi} - v_{ds} = 0. \tag{1.25}$$

The symbol v_{ds} represents any imbalance between the upper and lower dc-side voltages. It will be close to zero in most cases. Finally, applying Kirchhoff's current law to the positive and negative dc rails, respectively, of the circuit in Figure 1.17 we obtain

$$\begin{aligned} i_{\mathrm{d}u} &= i_{\mathrm{u}a} + i_{\mathrm{u}b} + i_{\mathrm{u}c} \\ i_{\mathrm{d}l} &= i_{\mathrm{l}a} + i_{\mathrm{l}b} + i_{\mathrm{l}c}. \end{aligned} \tag{1.26}$$

Summing and subtracting these equations, respectively, and yet again employing the definitions given by (1.20) we get

$$i_{\mathrm{dc}} = i_{ca} + i_{cb} + i_{cc} \tag{1.27}$$

and

$$i_{\mathrm{ds}} = i_{sa} + i_{sb} + i_{sc}. \tag{1.28}$$

In most practical cases there is no connection from the dc link midpoint, implying that the latter current, i_{ds}, is zero.

Equations (1.25) and (1.28), on the one hand, correspond to an equivalent schematic diagram governing all ac-side currents and the common-mode dc-side current, shown in Figure 1.18(a). Equations (1.22) and (1.27), on the other hand, correspond to an equivalent schematic diagram governing the circulating currents and the differential-mode dc-side current; see Figure 1.18(b). The dominant part of the latter current is generally the dc component, which accounts for the active power flow between the dc and ac sides.

1.5.2.3 Steady-State Operation

The circuit behavior of the MMC as seen from the ac and dc terminals has been explained by the circuit decoupling described above. The insights gained will now be put to use to explain the basic operation of the converter. In particular, ac/dc conversion under stationary and symmetric conditions will be discussed. Furthermore, the implications for the internal energy fluctuations

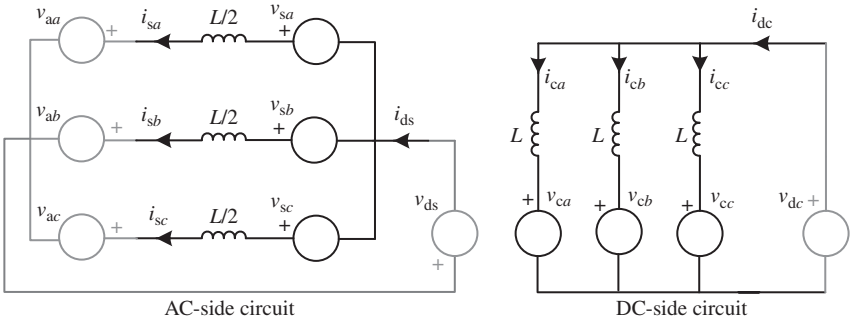


Figure 1.18 Decoupled equivalent circuits of the converter for the ac and dc sides. Parts related to the converter highlighted.

inside the converter phase arms will be analyzed. Since symmetry is assumed, the operation of the different phase legs will be identical apart from a phase shift of 0 rad, $-2\pi/3$ rad or $+2\pi/3$ rad applying to all quantities of the respective leg. Therefore, the analysis can be made on a per-phase basis and then the indices a, b, and c, representing the three phases, can be consistently dropped.

The converter should impose a constant direct voltage, V_d, between the two dc poles. It is assumed that a constant differential-mode dc-side current, $i_\mathrm{dc} = I_\mathrm{d}$, is flowing as a consequence. In practice, a closed-loop controller is generally required to adjust the dc-side voltage so that this will be the case, something that is discussed in more detail in Chapter 3. However, since the aim at this stage is to understand the steady-state behavior, this is not taken into account. Although the decoupled circuit model allows for unbalance dc-side currents and voltages, these are assumed to be zero since they are generally not present in normal operation of the system (i.e. v_ds and i_ds are set to zero). In most cases there is a transformer connecting the converter to the ac grid that lacks a midpoint connection, meaning that the path for i_ds is broken up.

From Figure 1.18(b) it is evident that to fulfill the objectives the common-mode phase-leg voltages should equal half of the desired pole-to-pole dc voltage, i.e.

$$v_\mathrm{c} = \frac{V_\mathrm{d}}{2}. \tag{1.29}$$

This choice will also eliminate any currents circulating between the phase legs since there are no voltages driving such currents.

As discussed above, unlike the two-level converter, the MMC does not provide a physical, measurable, ac-side voltage. Instead, it behaves like a set of voltage sources, v_s, behind an inductance, amounting to $L/2$; see Figure 1.18(a).

$$v_\mathrm{s} = \hat{v}_\mathrm{s} \cos(\omega_1 t). \tag{1.30}$$

Obviously, the voltages for the three phases a, b, and c are phase-shifted by 0 rad, $-2\pi/3$ rad, and $+2\pi/3$ rad, respectively. Since the ac network is presumed to be symmetric, a symmetric set of currents will, as a consequence, flow in the three connections of the ac terminal. Thus,

$$i_\mathrm{s} = \hat{i}_\mathrm{s} \cos(\omega_1 t - \varphi). \tag{1.31}$$

Notably, the power angle φ can be negative, implying inductive behavior of the converter. As in the case of the two-level converter, power balance between ac and dc sides needs to be sustained since the converter does not possess a large energy storage. It will again read

$$\frac{3}{2}\hat{v}_\mathrm{s}\hat{i}_\mathrm{s} \cos(\varphi) = V_\mathrm{d} I_\mathrm{d}. \tag{1.32}$$

Also, in the same fashion as with the two-level converter, the modulation index is defined to link the magnitudes of the ac-side and dc-side voltages, although the ac-side voltage is replaced by the inner emf v_s since there is no explicit ac-side voltage in the MMC,

$$m_\mathrm{a} = \frac{\hat{v}_\mathrm{s}}{V_\mathrm{d}/2}. \tag{1.33}$$

Again, this also permits a reformulation of the power balance as

$$3m_\mathrm{a}\hat{i}_\mathrm{s} \cos(\varphi) = 2I_\mathrm{d}. \tag{1.34}$$

The next issue is to determine the submodule string voltages and currents. These can be obtained directly by inserting the desired terminal quantities v_c, v_s, i_c, and i_s into Equation (1.20). For any phase leg the upper and lower submodule string voltages are obtained as

$$v_u = \frac{V_d}{2} - \hat{v}_s \cos(\omega_1 t) \tag{1.35}$$

$$v_l = \frac{V_d}{2} + \hat{v}_s \cos(\omega_1 t). \tag{1.36}$$

Thus, each phase arm provides a dc voltage component as well as an ac voltage component, where the dc components form a common mode, whereas the ac components are in anti-phase. Likewise, the arm currents will be

$$i_u = \frac{I_d}{3} + \frac{1}{2}\hat{i}_s \cos(\omega_1 t - \varphi) \tag{1.37}$$

$$i_l = \frac{I_d}{3} - \frac{1}{2}\hat{i}_s \cos(\omega_1 t - \varphi). \tag{1.38}$$

A very interesting observation at this stage is that the conversion between ac and dc apparently occurs *within* the six submodule strings and that the ac and dc quantities are present simultaneously at their two terminals. Thanks to the topology of the converter, and the opposing signs of the currents and voltages, these quantities are separated so that pure dc quantities appear at the dc terminal and pure alternating voltages and currents appear at the ac terminal. The MMC can in fact be perceived as six ac/dc converters each handling one-sixth of the power.

An important issue is the choice of the sum capacitor voltage of the submodule strings. As noted in Section 1.5.1, for a half-bridge submodule string with total capacitor voltage V_c^{Σ} the alternating-voltage magnitude range is maximized when the direct voltage is half of this value. Therefore, the sum capacitor voltage of the submodule string in each arm is set equal to the dc-side voltage:

$$V_c^{\Sigma} = V_d. \tag{1.39}$$

Slight deviations from this choice are possible, and may be beneficial under certain circumstances, but in most cases this is the preferred capacitor voltage set point. It is evident that the semiconductor valves of an MMC phase leg will need to handle a total capacitor voltage of $2V_d$. This is twice the corresponding value for a two-level converter with the same dc-side voltage. Still, the total semiconductor rating is not necessarily doubled since the current rating of the semiconductors can be lower. Later in this section, a more detailed treatment of component ratings is made.

The power exchange with each of the submodule strings will now be considered. It is of interest since it governs the average capacitor voltage ripple. See also [11] for a more in-depth treatment of this topic. Instantaneous power expressions of the submodule strings of a phase leg can be found by multiplying Equations (1.35) and (1.37) and using the power balance (1.34). After some simplification they can be written as

$$p_u = \frac{1}{8} V_d \hat{i}_s [2\cos(\omega_1 t - \varphi) - m_a^2 \cos(\omega_1 t)\cos(\varphi) - m_a \cos(2\omega_1 t - \varphi)] \tag{1.40}$$

for the upper arm and

$$p_l = -\frac{1}{8} V_d \hat{i}_s [2\cos(\omega_1 t - \varphi) - m_a^2 \cos(\omega_1 t)\cos(\varphi) + m_a \cos(2\omega_1 t - \varphi)] \tag{1.41}$$

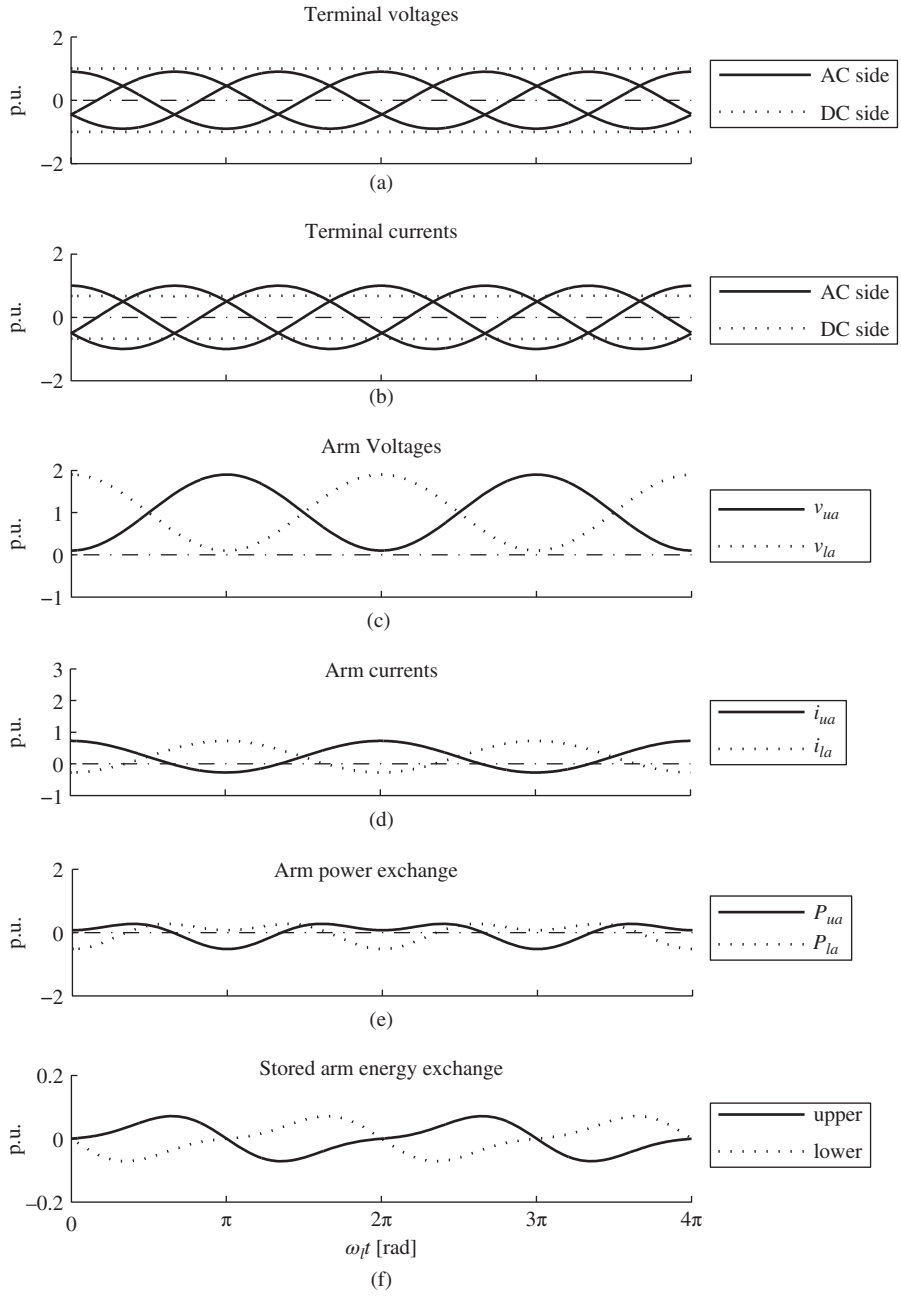


Figure 1.19 MMC with half-bridge submodules. Waveforms during a few cycles of steady-state operation with $m_a = 0.9$ and $\varphi = 0$.

for the lower arm. A first (rather trivial) observation from these expressions is that upholding the power balance at the converter level leads to power being balanced on the arm level since there is no constant term. That is, the condition for stable operation of the submodule strings is fulfilled according to Equation (1.14). Furthermore, it is clear that there will be significant low-frequency power pulsations in the submodule strings. First, there is an oscillation at the ac-side fundamental frequency. These terms have opposite signs in the expressions for the upper and lower phase arm, meaning that fundamental frequency power moves back and forth between the arms of the leg during operation. Moreover, there is a second harmonic term, proportional to the modulation index. This latter term is common to both submodule strings and thus corresponds to energy exchange with the entire phase leg. It relates to the second-harmonic power oscillation present in any single-phase voltage source, see Equation (1.7), which was derived for a two-level converter. For the two-level case these pulsations normally cancel out between the phase legs and therefore do not give rise to voltage ripple in the dc link. In an MMC, on the other hand, both the fundamental and second harmonic power ripple normally need to be absorbed by the submodule capacitors resulting in significant voltage ripple. For this reason, the total energy storage capacity of the capacitors, which also determines the size and cost of the capacitors, needs to be considerably larger in the MMC. For an application intended for operation at low frequency, such as a motor drive, this issue becomes particularly critical. As the impedance of the capacitors is increased ($X = 1/\omega C$) it will not be economically feasible to absorb the fluctuation by the submodule capacitors according to Equations (1.40) and (1.41). Instead, methods have to be found for redistributing energy within the converter using circulating currents; see [12]. Figure 1.19 shows steady-state waveforms of the variables discussed above from an MMC operating with only active power. The capacitor energy fluctuation is normalised with regard to the energy converted during one fundamental cycle.

1.5.2.4 Limits of Operation

The treatment of the MMC with half-bridge submodules has so far assumed that the submodule strings behave like ideal voltage sources and that there is voltage present at the dc terminal of the converter at all times. As discussed in Section 1.5.1, there are limitations to the capability of the strings to provide voltage, which influence the operating range of the converter; see Figure 1.13. In particular, the ac-component amplitude in the voltage can never exceed the dc component. For the MMC, this implies that the peak ac-side phase voltage may never exceed half of the dc-side pole-to-pole voltage. In other words, the modulation index is limited to the interval $m_a \in [0, 1]$. For a three-phase system, where there is no direct connection between the dc side and the ac side, a zero-sequence component can be added to the phase voltage references to extend the modulation index to $2/\sqrt{3} \approx 1.155$. Still, when the network connected at the dc terminal cannot sustain a voltage, the alternating voltage also has to be zero.

An extreme consequence of this circumstance occurs when the dc-side terminal of the converter is shorted. In a converter used for HVDC transmission this situation arises whenever a short-circuit fault on the dc line occurs. This is particularly common with dc overhead lines, and is usually caused by a lightning strike to the line. Since all ac-side inner emfs will then be zero, the converter loses control of all currents. This can also be understood by studying Figure 1.20, which shows an equivalent schematic diagram of an MMC with the dc-side shorted. Notably, the unipolar voltages that can be provided by the submodule strings would only add to the dc-side short-circuit currents, and the submodules thus have to be blocked or

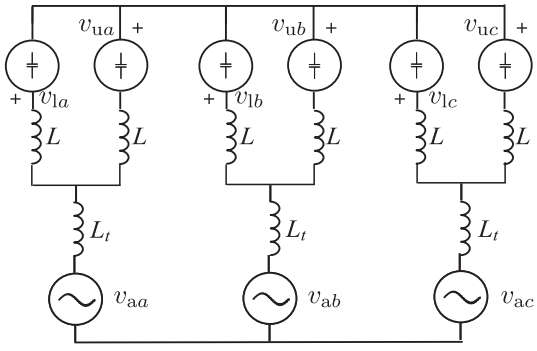


Figure 1.20 Schematic of an MMC at dc-side short-circuit.

bypassed. As a result, the converter will appear as a three-phase short-circuit from the ac side and essentially behave as a rectifier of the short-circuit currents. This state will generally persist until circuit breakers on the ac side open, which generally takes a few cycles (i.e. several tens of milliseconds). Therefore, the short-circuit currents will be determined by the short-circuit power of the ac grid and the overall ac-side reactance of the converter. The point-of-wave of the fault instance will determine the maximum instantaneous current, with the worst case being

$$I_{sc} = 2\sqrt{2}\frac{V_a}{Z_a + Z_s} \tag{1.42}$$

where Z_a is the short-circuit impedance of the grid and Z_s represents the overall ac-side impedance of the converter when blocked. This latter quantity is composed of the arm inductance and any reactance in series with the converter. The second part in most cases consists of the short-circuit reactance of a transformer connecting the converter to the grid. Notably, the short-circuit current will not be split between the upper and lower arms, as the ac-side current does during normal operation.

The dc short-circuit behavior presents several important issues for the design and fault handling strategy of the system. First, the peak short-circuit currents, according to Equation (1.42) will generally be much higher than the normal operating currents; see Figure 1.21, which shows a typical ac-side phase current during a symmetric fault. These currents will flow through diodes in the converter, and may well damage these if appropriate protective measures are not taken. Such measures can be implemented in several ways. First, the series reactance Z_s can be increased to limit the fault currents (e.g. by increasing the arm inductances). Also, a fast bypass switch (typically implemented by a thyristor) can be connected in parallel to each submodule. At a dc-side short-circuit these thyristors are fired and thus divert the currents away from the diodes. This method makes use of the high surge current capability of thyristors. Finally, the surge-current capability of the diodes may be dimensioned to handle the fault currents. This generally implies increasing the active area of the diodes significantly. All of the methods imply added cost, and often a combination is the most cost-effective solution. In Chapter 9 a more in-depth treatment of converter protection concepts including handling of dc-side short-circuits is provided.

A further issue is the fact that the converter, as discussed, will short also its ac terminal, which is undesirable. Obviously, no active power exchange is possible when a dc short-circuit

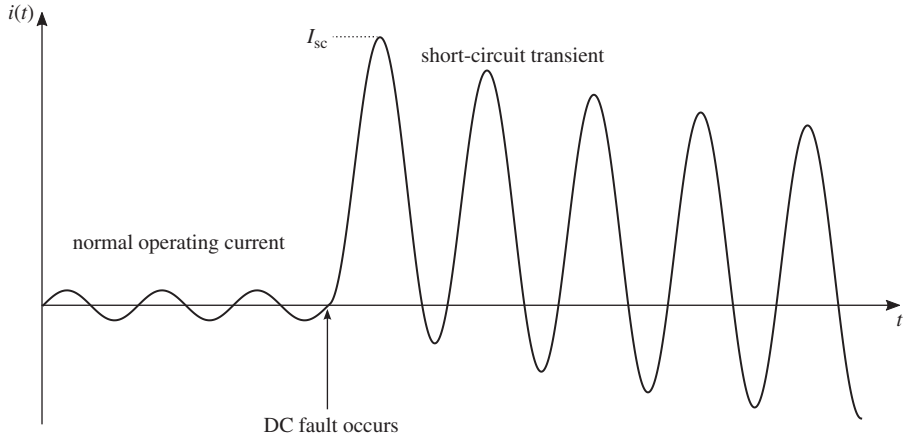


Figure 1.21 One of the ac-side currents during a stiff dc-side short-circuit fault in a half-bridge MMC.

fault occurs, but the behavior is similar to a three-phase symmetric grid fault until the ac breakers have cleared it. It may have detrimental effects on the operation of the ac grid such as a temporary voltage sag or worse.

A final matter that must be taken into account with regard to the handling of dc-side short-circuits is related to the wider operation of the dc system. The circumstance that current control is lost will generally also delay the recovery of the dc network. This is particularly serious for converters connected to an HVDC grid. If one or several converters feed short-circuit current into the fault, it will be more difficult to disconnect the faulty part.

Connecting fast dc breakers that can interrupt short-circuit currents on the dc side can solve most of the mentioned problems. If such switchgear can separate the converter from the dc lines in a very short timeframe (a few milliseconds), there will be no currents fed into the dc network. Also, the converter can stay in operation feeding reactive power into the ac grid. Other strategies for handling dc-side faults are based on using alternative converter topologies that can limit or control dc fault currents. Several such topologies have been proposed and some are described in the section 1.5.3.

1.5.2.5 Component Rating Issues

This section briefly treats the fundamental rating requirements of the half-bridge MMC based on the discussion of the converter topology and its operation in the previous sections. A more in-depth coverage of component rating follows in Chapter 2.

It is generally a fair assumption that the cost of semiconductors in an MMC is strongly related to the sum of the submodule capacitor voltages and the peak current in the arms. The semiconductor valves need to withstand the capacitor voltage when they are in their off-state, which will define their blocking capability requirements. As discussed previously, the capacitor voltage will generally contain significant ripple components. These will, to a certain extent, drive up the peak voltage during operation, which must also be taken into account when dimensioning both the submodule capacitors and the semiconductors. Therefore, the total blocking

voltage of all semiconductor valves in an MMC is generally more than twice that of a two-level converter of similar rating.

As regards the current rating, the low switching frequency at which the MMC can operate means that the switching losses are low in comparison to those of a two-level converter. Therefore, the devices will in most cases not be thermally constrained (i.e. the maximum junction temperature will not determine the required rating). Instead, the needed semiconductor current rating will be defined by the safe operating area limitations of the devices, meaning that the peak instantaneous current during operation is the critical parameter. For steady-state operation it can be obtained by identifying the maximum value during a cycle of the arm currents according to Equations (1.37) or (1.38):

$$\hat{i}_{\mathrm{u,l}} = \frac{I_{\mathrm{d}}}{3} + \frac{\hat{i}_{\mathrm{s}}}{2}. \tag{1.43}$$

By using the energy balance equation (1.34) to link the ac- and dc-side currents the expression can be rewritten as

$$\hat{i}_{\mathrm{u,l}} = \hat{i}_{\mathrm{s}} \left(\frac{1}{4} m_{\mathrm{a}} \cos \varphi + \frac{1}{2} \right). \tag{1.44}$$

Sinusoidal and stationary conditions are assumed. The part within brackets is always below unity, which implies that the peak arm current is lower than the peak ac-side phase current. Hence, the current-wise rating of each semiconductor valve can generally be lower in an MMC than in a two-level converter of similar rating, where the valves always have to switch the full ac-side current. This will, to a certain extent compensate for the fact that the overall sum of the device blocking voltages is at least doubled. The maximum instantaneous voltage the submodule string has to deliver will determine the required total capacitor voltage. This quantity will in its turn decide the number of submodules. It can be estimated as

$$\hat{v}_{\mathrm{u,l}} = \hat{v}_{\mathrm{s}} + \hat{V}_{\mathrm{d}} = \hat{v}_{\mathrm{s}} \left(1 + \frac{1}{m_{\mathrm{a}}} \right). \tag{1.45}$$

for $|\cos \varphi| = 1$, which is the worst case.

According to the reasoning above, the cost of semiconductors and capacitors in a submodule string is, in the first approximation, proportional to the maximum instantaneous values of the current and the voltage at its terminals. Therefore, the product of the peak string voltage and current can be used as an indicator of the cost, and thus help in understanding how different design choices affect it. To this end, the *semiconductor power* P_{sc} is defined as

$$P_{\mathrm{sc}} = k_{\mathrm{c}} \hat{v}_{\mathrm{u,l}} \hat{i}_{\mathrm{u,l}}. \tag{1.46}$$

The coefficient k_{c} represents the number of semiconductors in a submodule. It assumes the value 2 for a half-bridge MMC and 4 for a full-bridge MMC. In case comparisons between converters with different number of phase arms should be made, k_{c} should also involve the number of phase arms. For an MMC intended for active power transfer, P_{sc} can be obtained using Equations (1.44) and (1.45) as

$$P_{\mathrm{sc}} = \hat{v}_{\mathrm{s}} \hat{i}_{\mathrm{s}} \left(1 + \frac{1}{m_{\mathrm{a}}} \right) \left(\frac{1}{2} + \frac{1}{4} m_{\mathrm{a}} \right). \tag{1.47}$$

After some simplification, the semiconductor power can be rewritten in terms of the phase-leg apparent power ($S = \hat{v}_s \hat{i}_s / 2$), as

$$P_{sc} = k_c S \frac{1}{2} \left(m_a + 3 + \frac{2}{m_a} \right). \tag{1.48}$$

The extrema of this function are now sought. Differentiating the expression within brackets with respect to m_a and setting the resulting expression to zero yields

$$1 - \frac{2}{m_a^2} = 0. \tag{1.49}$$

The only feasible solution is $m_a = \sqrt{2}$. The second derivative is positive for all valid values of m_a, so there is a minimum at this point. However, the dependency on m_a is rather weak for applicable values of m_a. This is evident from Figure 1.22, which shows the normalized semiconductor power as a function of m_a.

Importantly, the reasoning above about component ratings will only give an indication of the actual requirements. In practice, faults and other abnormal operating modes that may be encountered will often determine the necessary ratings of the semiconductors and passive elements. Therefore, practical dimensioning of MMCs, and other power converters, will generally require detailed calculations and simulations that take into account different fault cases as well as the properties of the control system. However, the stresses incurred during contingencies can often be sufficiently considered by using the steady-state values and include a margin to account for the additional rise in currents and voltages.

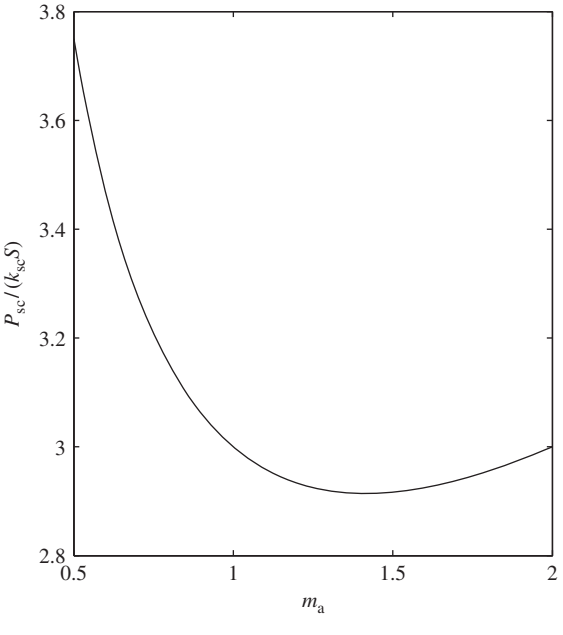


Figure 1.22 Semiconductor installed power versus modulation index for an MMC.

One important such abnormal case, which may impact the rating of components, is a dc-side short-circuit. As discussed above, it leads to immediate loss of the capability to control the currents. The converter will appear as a short-circuit from the ac side and as a rectifier of the short-circuit currents. These currents may exceed the normal operating case several times, depending on the size of the arm reactors and the reactance in series with the converter (such as the leakage reactance of a transformer connecting the converter to the grid), according to Equation (1.42). They will flow in the anti-parallel diodes of the valves parallel to the terminal of each submodule [diode *D2* in Figure 1.11(a)]. Although the surge current capability of diodes tends to be superior to that of semiconductor switches, such as IGBTs, the current spike encountered may make it necessary to increase the active area of these diodes. Otherwise, other measures can be implemented to protect the diodes, as discussed in Chapter 2, but this will also come at additional cost.

1.5.3 Other Cascaded Converter Topologies

As discussed in the previous sections, the conventional MMC with half-bridges offers several benefits over the two-level converter for high-power applications. Thanks to its scalability, it has removed the upper limit in terms of voltage for VSCs in power grids. Also, the topology offers an excellent combination of harmonic properties and low power losses. Still, the topology suffers form some significant drawbacks. Like the two-level converter, it loses control of both ac-side and dc-side currents in case of a dc-side short-circuit; see Section 1.5.2, which makes it less useful in HVDC grids, at least when not equipped with fast dc-breakers. Also, the amount of stored energy in the submodule capacitors is large, leading to a high capacitor cost.

A number of other modular converters have been proposed prior to, and after, the development of the half-bridge MMC. For certain applications these show significant advantages. This section, therefore, briefly describes some of these topologies and their merits and drawbacks in comparison to the half-bridge MMC.

1.5.3.1 STATCOM with Cascaded Full-Bridges

There are many applications where reactive power compensation is desired, for instance to compensate for non-resistive or fluctuating loads. It allows for better utilization of the grid since the amount of reactive power that may displace the useful active power is reduced; see Figure 1.23. Also, in case it is used to compensate for a rapidly fluctuating load such as an *electric arc furnace* (EAF), used in the steel industry, it can mitigate the fast grid voltage variations (flicker) that would otherwise result. In case fast response times are desired, a VSC connected to the grid is often used, whose sole purpose it is to generate or absorb reactive power. Such a device is usually referred to as a *static synchronous compensator* (STATCOM). They may be installed separately, which is often the case for industrial installations, or as part of a larger installation for reactive power compensation. Early STATCOMS were often implemented by two-level converters or three-level NPC converters (see Section 1.4.1) connected to the grid by step-up transformers [13, 14]. Generally, several converters had to be connected in parallel through the transformers to handle the great power required. Also high-voltage three-level NPC converters were used for this purpose [15]. This way parallel connection could be avoided, and in some cases the converter could be connected directly to the grid without a

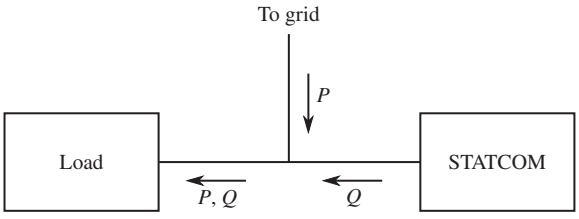


Figure 1.23 Basic principle of reactive power compensation. In case a power source is compensated the active power, P, will be negative.

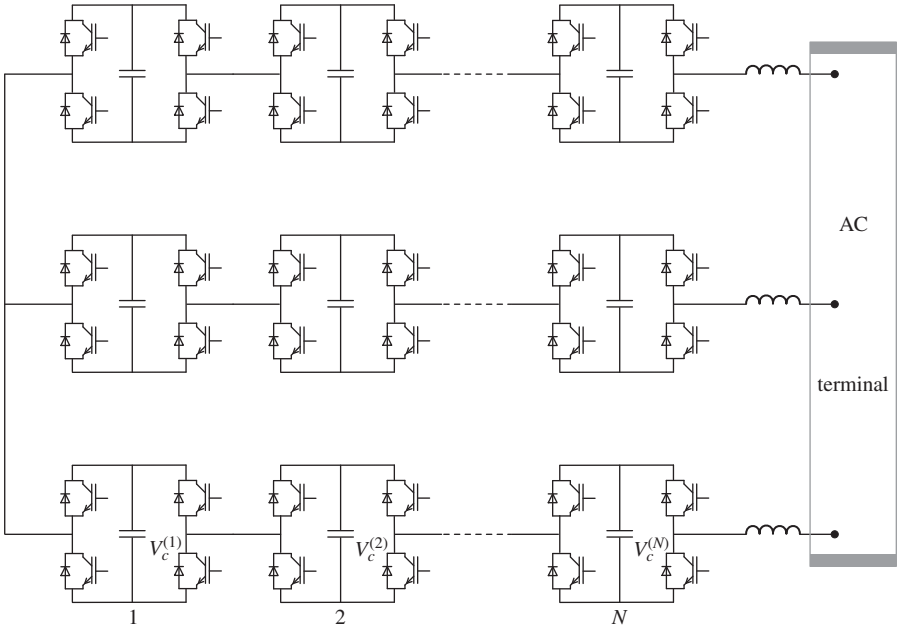


Figure 1.24 Cascaded full-bridges converter for providing reactive power.

transformer, thus reducing the equipment cost. As in the case of two- and three-level converters for HVDC, direct series-connection of power semiconductor elements is required in these cases to handle the high voltage at the converter terminals. This implies challenges in terms of voltage sharing between the semiconductors, static as well as dynamic. Also, semiconductor switches with guaranteed short-circuit failure mode (see Section 2.1.6) are required to ensure fault-tolerance.

A more straightforward way to provide a VSC capable of delivering reactive power at the scale required in power grids and for compensating large industrial loads is shown in Figure 1.24. H-bridge submodule strings are connected in either delta- or wye-connection forming a three-phase ac terminal; see Figure 1.25. In series with each string a small reactor (in per-unit terms) is connected, to limit harmonic currents and to allow for control of the arm

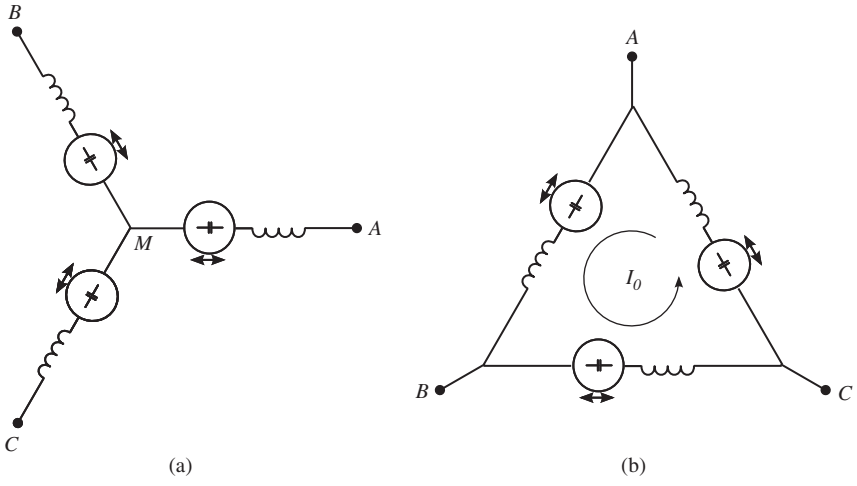


Figure 1.25 Cascaded full-bridges STATCOM in (a) wye and (b) delta configuration.

currents. This is likely to be the simplest cascaded topology. As evident from the figure, the converter only has an ac terminal, since the only task of the converter is to provide or absorb reactive power. Cascaded full-bridges converters of this kind date back to the 1970s with an early reference being a patent filing from MIT [16]. This filing appears to cover mainly single phase systems and the application as a STATCOM was not foreseen. In 1996 a three-phase version of this converter intended as a STATCOM was presented [17], likely for the first time. For practical use the converter topology was first adopted by the manufacturer Alstom [7] for a STATCOM that should form part of a larger FACTS installation. This early utility application of the topology made use of gate-turn-off (GTO) thyristors to implement the four valves of each submodule. The low switching frequency made possible by the cascaded approach was particularly valuable given the high switching losses of the GTO thyristors. The concept has since been taken up by several manufacturers and is currently in widespread industrial use [18].

The benefits over two-level converters are fundamentally the same as with other cascaded converters. A great number of levels can be achieved in the output voltage, enabling acceptable harmonic performance even at very low switching frequencies. The modular approach gives scalability, and any desired rating in terms of reactive power can be achieved by adding more submodules and thus increasing the operating voltage. The voltage can then be adjusted to suit the grid by a transformer. This is different from the case of HVDC transmission, where the dc-side voltage and current have to be adapted to suit the current handling capability of the HVDC transmission cable or overhead line. Furthermore, vital fault tolerance can be implemented by including redundant submodules in the strings. However, as in the case of other cascaded converters, there are a number of drawbacks. Most significantly, the fact that the dc capacitors are distributed in the phase arms impedes power exchange between the submodule strings of the phases. This is especially critical for a converter that should be able to compensate for loads that may be severely unbalanced, such as EAF. In a two-level converter, power exchange between the phases occurs easily since the phase legs lack energy storage and are all connected to a common dc link; see Section 1.2.2.

The energy pulsation, which has to be managed by the submodule capacitors, can be derived as follows for balanced steady-state operation. First, the voltage across the string and the current through it are assumed to be sinusoidal, with the current lagging the voltage by a power angle, φ:

$$\begin{aligned} v(t) &= \hat{v}\cos(\omega_1 t) \\ i(t) &= \hat{i}\cos(\omega_1 t - \varphi). \end{aligned} \tag{1.50}$$

The overall power exchange with the string is as usual obtained by multiplying the instantaneous string voltage and current

$$p(t) = \frac{1}{2}\hat{v}\hat{i}[\cos\varphi + \cos(2\omega_1 t - \varphi)]. \tag{1.51}$$

The first term is constant, so the requirement of power balance over time in this case mandates that the only feasible power angles are $\varphi = -\pi/2$ rad and $\varphi = \pi/2$ rad, which will eliminate this term. It corresponds to either the pure consumption or the pure generation of reactive power, respectively. This is expected, since the converter has no dc terminal at which active power could be exchanged. In either of these cases there will be a second harmonic fluctuation that will result in a submodule capacitor ripple common to all submodules. This is analogous to the conditions of the half-bridge MMC, but the MMC also has a fundamental frequency component in the ripple. The energy fluctuation under these circumstances can be found by integrating Equation (1.51) over time:

$$e(t) = \frac{\hat{v}\hat{i}}{4\omega_1}\sin(2\omega_1 t - \varphi). \tag{1.52}$$

As mentioned, the phase arms of a full-bridge STATCOM may either be configured in wye connection or delta connection, as seen in Figure 1.25. In terms of power rating these two cases are obviously equivalent. That is, the amount of reactive power that can be provided given submodule strings with certain voltage and current ratings is equal. Only the base impedance of the system (i.e. ratio of rated voltage to rated current of the converter) will differ, by a factor of three. This can easily be realized by observing that at symmetric conditions the line-to-line voltage V_Δ and the phase currents I_Δ in the delta-connected case will relate to the corresponding submodule string quantities V, I as

$$\begin{aligned} V_\Delta &= V \\ I_\Delta &= \sqrt{3}I, \end{aligned} \tag{1.53}$$

whereas for a wye-connected converter the corresponding relations will be

$$\begin{aligned} V_Y &= \sqrt{3}V \\ I_Y &= I. \end{aligned} \tag{1.54}$$

Thus, with given submodule string ratings,

$$\frac{V_Y}{I_Y} = 3\frac{V_\Delta}{I_\Delta}. \tag{1.55}$$

The wye-connected configuration is therefore more beneficial when there is a desire to match a certain voltage at the terminals by the least number of submodules. As discussed, however, in many cases the voltage can be adapted to the grid by a transformer. Then, the terminal voltage of the converter matters less. Apart from this obvious difference, there are a few other aspects to be considered when choosing between the wye and delta configurations. As mentioned, a STATCOM may be required to produce a negative-sequence current in order to compensate for a load that can be severely unbalanced, such as an EAF. This will generally make it difficult to prevent imbalances between the overall capacitor energies of the phase arms. That is, the sum capacitor voltages, V_c^{Σ}, of the three phases will tend to diverge rapidly. However, by using the delta configuration, it is possible to inject a zero-sequence current component, I_O, that can be used to counteract such a divergence, as indicated in Figure 1.25(b). By properly adapting the magnitude and phase displacement of the zero-sequence current, power redistribution between the submodule strings may be performed to that effect, as described in, for example, [19].

On the other hand, use of the wye-connected STATCOM offers the possibility of adding zero-sequence (common-mode) components to the string voltages. If the midpoint M is not connected, or if there is a transformer without a connected midpoint, such components do not affect the external behavior of the converter. However, a zero-sequence voltage at the fundamental frequency can be used to redistribute energy between the phase arms in a similar way as a zero-sequence current can be used with the delta-connected circuit. Thus, there is a possibility for balancing the capacitor energies during operation under unbalanced conditions also using the wye-connected STATCOM. Furthermore, third-harmonic zero-sequence injection in order to allow for an increase of the fundamental output voltage is possible. In a similar fashion as in the case of, for example, a two-level converter such a component at the third harmonic order can allow for an increase of the modulation index from $m_\mathrm{a} = 1.0$ to $m_\mathrm{a} = 2/\sqrt{3}$. This leads to a corresponding increase of the power rating of the converter, thus reducing the cost per unit of reactive power.

1.5.3.2 Full-Bridge MMC

The shortcomings of the ordinary MMC with half-bridges in terms of dc-side fault handling capability can be overcome by replacing the half-bridges with full-bridges. The bipolar voltage that can be provided by full-bridge strings permits the converter to control both ac-side and dc-side currents even in the case of a stiff dc-side short-circuit. This can be understood by considering Figure 1.20 and replacing the half-bridge strings by full-bridge strings. Under such circumstances the converter will topologically resemble a cascaded-submodule wye-connected STATCOM, as described in the previous section, where the submodule strings of each phase leg appear connected in parallel. Given that no direct voltage has to be imposed by the arms during a dc-side fault, the peak ac-side emf that can be provided by the converter then rises to the sum of the submodule capacitor voltages V_c^{Σ}. It normally equals the dc-side voltage, V_d, and at a nominal modulation index of $m_\mathrm{a} = 1.0$ it exceeds the peak value of the driving voltage of the ac grid twofold. Therefore, it is more than sufficient for controlling the currents.

Furthermore, in normal operation the use of full-bridges can allow for an extension of the possible operating range as discussed in Section 1.5.1. Equations (1.17) and (1.18), visualized in Figure 1.13, define the reachable operating regions in terms of alternating and direct voltage components, at a given sum capacitor voltage, V_c^{Σ}, for a single submodule string with either half-bridges or full-bridges. Given that for an MMC the dc-side voltage equals the sum of the

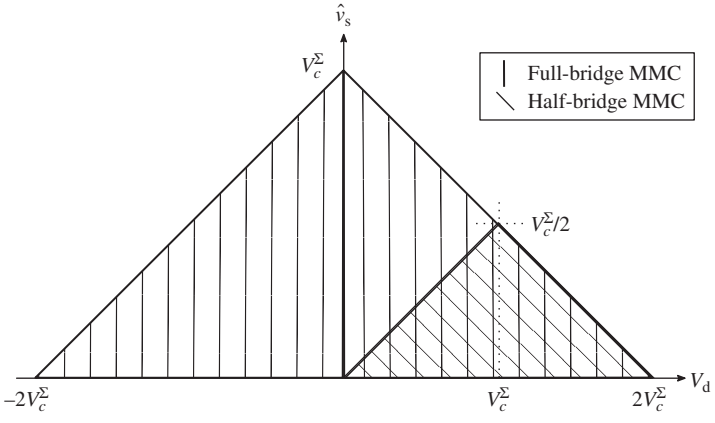


Figure 1.26 Operating region in terms of alternating and direct voltage of half-bridge and full-bridge MMCs given a sum capacitor voltage per arm of V_c^Σ. Impact of capacitor voltage fluctuation is not taken into account.

output voltages of the strings in the upper and lower arms, whereas the ac-side inner emf v_s is half of the difference between these–see Equation (1.19)–the corresponding regions for an entire MMC built from either type of submodules can be constructed; see Figure 1.26. The difference between the submodule types lies in the region where $V_d < V_c^\Sigma$. In this region a converter equipped with full-bridges can provide an ac-side emf higher than half of the direct voltage ($\hat{v}_s > V_d/2$). Thus, infinite modulation index is in theory possible.

It should also be noted that the operating region of the full-bridge converter is symmetric with regard to the $\hat{v}_s$-axis so that the direct voltage can also be negative. This is an attractive feature, for instance in HVDC applications, where dc polarity reversals may occur, such as when interoperability with CSC technology is required.

Importantly, the reasoning above is only valid when the overall capacitor voltages remain approximately constant. In practice the capability to provide voltage components will be affected by the ripple in the capacitor voltages, although this is generally a second-order effect. As long as the average capacitor energy is in the range of several tens of Joules per kilowatt of rated power, this extension or reduction of the operating area will not be dominant (at 50 or 60 Hz operating frequency).

On the same topic, since the operating range can be extended, it can also be of interest to investigate the impact on the fluctuation of the stored arm energies, and thus on the capacitor voltage ripple, in points outside the range possible with the conventional MMC. In particular, by increasing the modulation index beyond 1.0 the capacitor energy variation can be significantly reduced [20]. By observing Equations (1.40) and (1.41) it is evident that with $m_a = \sqrt{2}$ the terms corresponding to power exchange at the fundamental frequency will cancel out when only active power is exchanged on the ac side ($\varphi = 0$ rad or $\varphi = \pi$ rad). The expressions for the power exchange with the upper and lower submodule strings in a phase leg will both take the following form:

$$p_u = p_l = -\frac{1}{8} V_d \hat{i}_s m_a \cos(2\omega_1 t - \varphi). \tag{1.56}$$

Thus, under these circumstances, the power exchanged between the upper and lower phase arms disappears. Only the inevitable fluctuation at the second harmonic frequency remains, since it is related to the power exchange with the entire phase leg. Figure 1.27 shows steady-state waveforms of an MMC operating in this point. The dc-side voltage and current have been set to 1.0 p.u., as in Figure 1.19, to allow for comparisons. The magnitude of the ac-side emf increases to 1.41 p.u. and the currents on the ac side are reduced by the same factor to preserve power balance. As predicted by Equation (1.56), the curves corresponding to the power exchanged with the submodule strings will coincide and only contain a second harmonic component. This also applies to the energy fluctuations in the submodule capacitors [chart(f)] since these quantities are time integrals of the power exchanged. Comparing Figures 1.19 and 1.27, it is evident that the capacitor energy fluctuation is reduced by approximately half under the given circumstances. Therefore, a full-bridge MMC intended for operation at elevated modulation indices could potentially be designed with smaller submodule capacitors. However, this only holds at pure active power exchange at the ac side. At significant production or absorption of reactive power the energy ripple will increase as the fundamental-frequency variation will be present, as explained in [20].

At this point it should be noted that the power angle φ refers to the active and reactive power exchanged with the inner emf of the converter. This will deviate slightly from the reactive power exchanged with the entire converter since half of the arm inductance appears in series with the inner emf as seen from the ac side–see Figure 1.18(a)–and this inductance consumes a certain amount of reactive power.

In terms of semiconductor expenditure the full-bridge MMC appears less attractive. For a converter intended for operation in the same fashion as a half-bridge MMC, that is with modulation index below 1.0 (or below $2/\sqrt{3}$ with third harmonic injection), the required overall semiconductor active area will in the first approximation be doubled. For a given dc-side voltage the same number of submodules is required, but each submodule has two phase legs instead of one, whereas the maximum instantaneous current will be the same. However, since the converter can control the currents during dc-side short-circuits, certain savings are possible in terms of the rating of the diodes. As mentioned in Section 1.5.2, for a half-bridge MMC the diodes in the valves parallel to the submodule terminals will need to conduct the ac-side short-circuit currents in case the dc-side voltage disappears. In case no other means for protecting these diodes against surge currents are present in the system, this translates to a significant over-rating of the diodes, which can possibly be avoided in a full-bridge converter.

Under the same operating conditions, the semiconductor conduction losses will be doubled since the current will always pass though two valves in each submodule. However, the average switching frequency of the valves can in theory be halved, maintaining the same output voltage distortion and submodule capacitor-voltage ripple. This can, for instance, be achieved by only switching one of the phase legs and permanently keeping one valve of the other phase leg in the conducting state. Therefore, the overall semiconductor switching losses will remain the same as in the half-bridge case.

Since the full-bridge MMC can be operated at peak alternating voltages higher than the direct voltage, the semiconductor rating requirements of a converter designed for such operation are also of interest. However, at a given dc-side voltage (which is most often the case in HVDC applications) any increase in the ac-side emf magnitude will entail an increase in the required total capacitor voltage (i.e. that more submodules are required), according to Equation (1.18). Maintaining the same power, the ac-side currents will be reduced while the dc-side

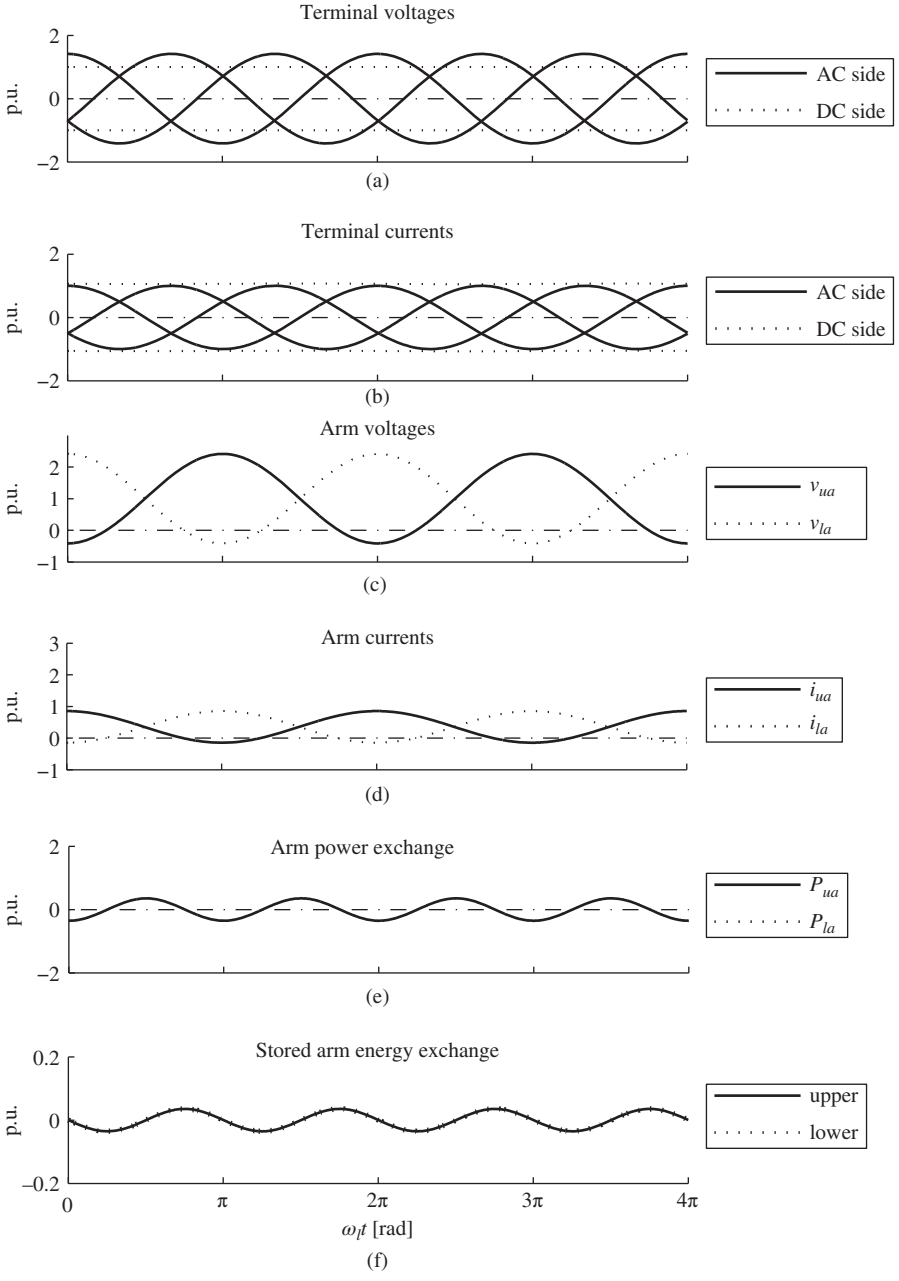


Figure 1.27 MMC with full-bridge submodules. Waveforms during a few cycles of steady-state operation with $m_a = \sqrt{2}$ and $\varphi = 0$. Note how the fundamental-frequency term of the submodule string energy ripples disappears at this modulation index.

current is unchanged. To understand the overall influence on the semiconductor expenditure, the previously derived Equation 1.48 in Section 1.5.2 is useful. It links the semiconductor cost, measured as the product of the peak submodule string current and voltage, to the modulation index at $\cos\varphi = 1$. It was found that the cost has a minimum for $m_a = \sqrt{2}$ (i.e. in the region only reachable by a full-bridge converter). A plot illustrating the relationship can be found in Figure 1.22. The difference in P_{sc} when m_a is increased from 0.9 to $\sqrt{2}$ is only 5%. The possibility of operation at elevated modulation indices, enabled by full-bridges, can therefore not compensate for the fact that the number of semiconductors is doubled with full-bridges ($k_c = 4$ instead of 2). The total semiconductor expenditure is, therefore, approximately doubled for a converter using full-bridges, regardless of how it is operated.

Behind this reasoning also lies the assumption that a transformer is present at the ac terminal, whose turns ratio can be adapted to suit the chosen output voltage of the converter. Also in terms of power losses, designing an MMC for operation at elevated modulation indices does not appear to offer any benefits. For applications where the dc voltage may be chosen freely, such as back-to-back HVDC interconnections, operating the full-bridge MMC with lower dc voltage may, however, be beneficial.

1.5.3.3 Alternate-Arm Converter

The quest for converter circuits with the capability of blocking the dc-side current at faults has also resulted in other solutions. The so-called *alternate-arm converter* (AAC) is shown in Figure 1.28. Its arms combine strings of full-bridge submodules and valves of the kind found in a normal two-level converter, as shown in the figure. These latter valves are labeled *director switches*. It was proposed by the manufacturer Alstom Ltd [21], which has also filed several patent applications related to the topology and its control. The full-bridge submodule strings

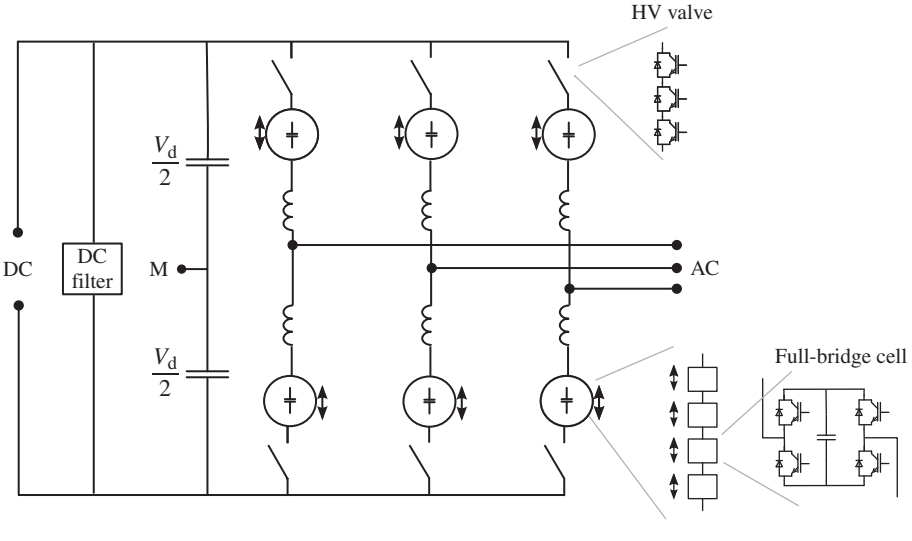


Figure 1.28 Schematic diagram of the AAC.

give this converter the capability of controlling the currents during dc-side faults. Indeed, during a stiff dc-side short-circuit, when $V_d = 0$, the equivalent schematic will resemble that of the full-bridge MMC, under the same conditions.

The basic mode of operation of a phase leg is based on having the director switches each conduct during half of the fundamental cycle. The upper switch conducts during the positive half-cycle, and during this interval the upper submodule string provides the ac-side emf. Thus, the string voltage should be $V_d/2 - v_s$ during this time. As earlier, V_d and v_s represent the dc-side voltage and the ac-side emf, respectively. Conversely, the director switch in the lower phase arm is put in the on-state during the half-cycle with negative ac-side emf, and the corresponding lower submodule string provides a voltage to the ac side during this period, (i.e. $V_d/2 + v_s$). Figure 1.29 shows current and voltage waveforms during a couple of fundamental cycles.

The operation thus resembles the standard two-level converter in the sense that the two arms of the same phase alternately conduct, hence the name of the converter. This is in contrast to the MMC, where the two submodule strings of a phase leg implement voltage sources that conduct current continuously. A further important difference compared to the MMC is the behavior towards the dc side. The MMC is a multilevel VSC seen from both the ac and dc networks to which it is connected. Each phase leg of the AAC instead acts as a current source as seen from its dc terminal, consistently injecting one half-cycle of the alternating current waveform into one of the dc poles and the other half-cycle into the other pole. This follows from the operating mode of the converter where the director switches only permit current to flow into one of the dc poles at a time. Like the two-level converter, the AAC therefore requires a capacitor across the dc terminal to smoothen the direct voltage. However, there is a significant difference in terms of the harmonic content of the currents injected into the dc link. A three-phase two-level converter mainly produces high-frequency components, resulting from the switching process, since the second-harmonic fluctuations cancel out between the phase legs, as explained in Section 1.2. The AAC, on the other hand, will inject significant current harmonics at multiples of six times the fundamental (6th, 12th, 18th, etc.). This occurs since the AAC phase legs inject half-cycle current waveforms into the dc poles, whose sum over the three phases is periodic at six times the fundamental frequency, as evident from Figure 1.29(b).

As discussed previously the power flow of any submodule string always needs to be balanced over time so that no net energy exchange occurs during an entire fundamental cycle. One of the consequences is that the power flow at the ac and dc terminals of the converter also needs to be balanced over a fundamental cycle. Therefore, the direct coupling between ac and dc side currents that exists in the AAC implies that there will also be a fixed ratio between the ac-side and dc-side voltages to maintain power balance. The average power flow at the ac terminal of one of the phase legs, as usual, equals

$$P_a = \frac{1}{2}\hat{v}_s\hat{i}_s \cos(\varphi) \tag{1.57}$$

since the ac-side current and voltage can be assumed to be sinusoidal. Keeping in mind that the current injected into the positive dc terminal has the waveform of a half-cycle of a sinusoid, phase shifted by φ rad, the corresponding dc-side expression is

$$P_d = V_d \frac{1}{\pi}\int_0^{\pi} \hat{i}_s \sin(x - \varphi)dx, \tag{1.58}$$

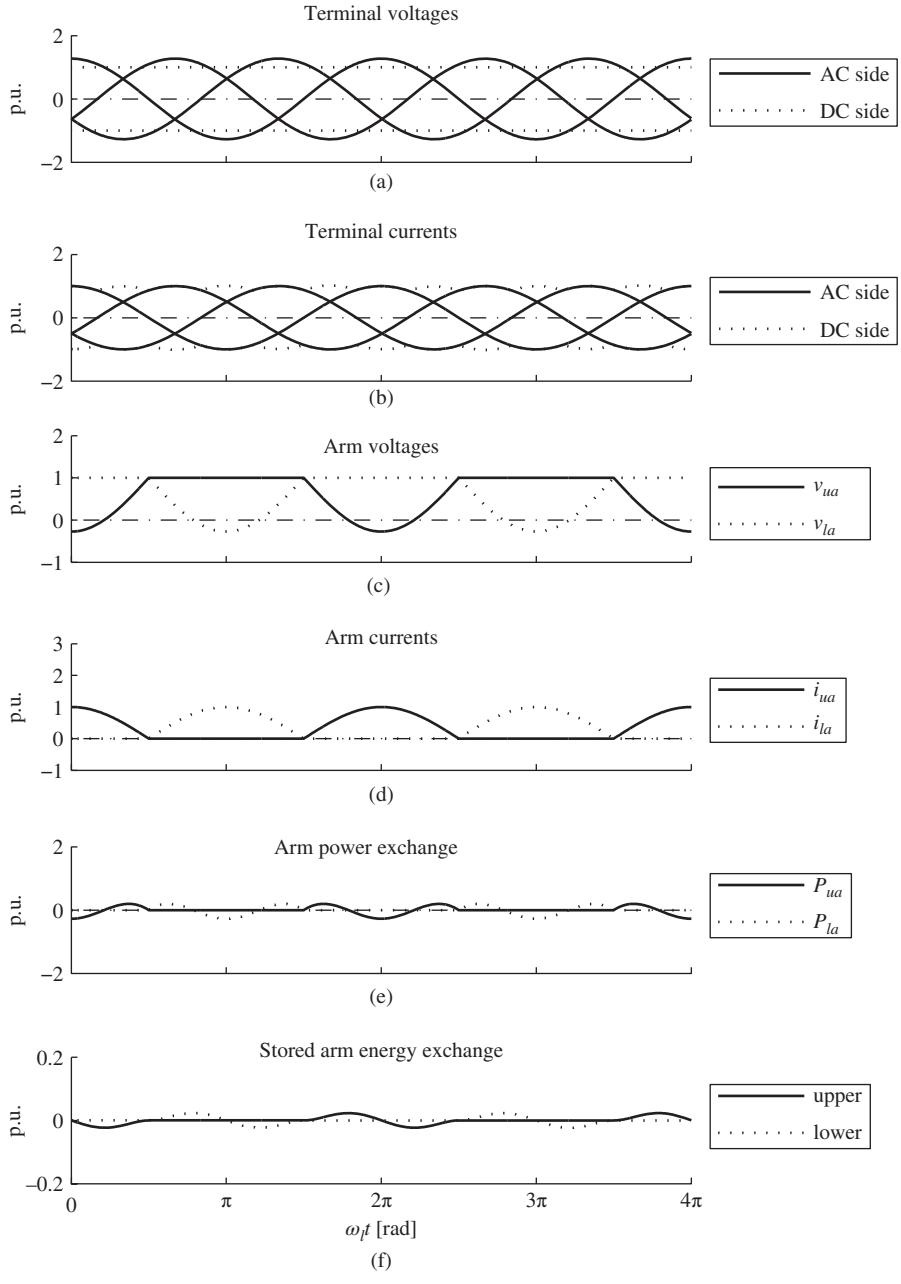


Figure 1.29 Typical waveforms of the AAC in steady-state operation.

which by evaluation of the integral can be rewritten

$$P_{\mathrm{d}} = \frac{2}{\pi} V_{\mathrm{d}} \hat{i}_{\mathrm{s}} \cos \varphi. \tag{1.59}$$

During the other half-cycle the ac-side current is injected into the other dc pole resulting in the same average power flow. Equating the right-hand sides of Equations (1.57) and (1.59) and dividing by $\hat{i}_{\mathrm{s}}$ and the power factor, which appear on both sides, yields

$$\hat{v}_{\mathrm{s}} = \frac{2}{\pi} V_{d}. \tag{1.60}$$

The operating range is thus limited, and the converter only works in this specific operating point, commonly labeled the *sweet-spot*. Outside the sweet-spot there will be no natural balancing of dc- and ac-side power flows, leading to uncontrolled drift of the submodule capacitor voltages and collapse of the converter operation. Notably, the sweet-spot corresponds to a modulation index of

$$m_{\mathrm{a}} = \frac{4}{\pi} \tag{1.61}$$

which is higher than what can normally be achieved by a two-level converter or a half-bridge-based MMC. As noted in the previous section, an MMC with full-bridges can in theory operate with any modulation index.

The modulation index normally stays fairly constant during the operation of a grid-connected converter since the alternating and direct voltages in most cases do not depart significantly from their nominal magnitudes. This is in contrast to the case of a motor drive, where alternating voltage levels from zero and upwards may be required, depending on the speed of the motor, to maintain constant flux linkage. Still, even for a grid-connected converter, a certain flexibility in terms of the voltage ratio is required to compensate for ac and dc voltage variations and also to allow for reactive power interaction, which requires that the converter emf differs in magnitude from the grid voltage. Thus, the fixed voltage ratio would render the AAC useless for most practical applications. For this reason a few methods have been developed for balancing the power flows also at other modulation indices.

First, it is possible to introduce a short overlap period during which the director switches of both the upper and lower arms are conducting simultaneously. During such a period, a current will flow through the entire phase leg thus exchanging energy between the upper and lower arm submodule strings and the dc terminal. The overlap periods lead to additional losses since more current will flow through the phase arms. Also, the amount of dc-side harmonic distortion will increase, owing to the overlap periods since they result in short current bursts being injected into the dc terminal. Notably, the overlap period will need to be longer the farther from the sweet-spot the converter is to be operated.

Another balancing strategy is based on having a controllable zero-sequence current at the third harmonic frequency flowing on the ac side [22]. In order for this to be possible the converter can be connected to a delta-wye transformer with the wye-connected windings toward the converter. To provide a path for the zero-sequence currents the midpoint formed by these windings is connected to the dc-link midpoint (denoted M in Figure 1.28). Since a transformer is generally connected between the converter and the ac grid, this arrangement does not necessarily imply any significant additional cost. The third-harmonic currents do not give rise to any average power exchange with the dc link. Also, since they have zero phase sequence they will circulate in the grid-side delta winding of the transformer and thus not transfer any power to or

from the ac side. Instead, they will cause power interaction between the phase arms. This is due to the fact that the director switches connect each phase arm during half a fundamental cycle, corresponding to 1.5 cycles at the third harmonic, which will give a net contribution to altering the charge of the submodule capacitors of the concerned arm. A disadvantage of this method is that the third harmonic component will cause a voltage ripple across the dc link capacitors. This ripple is particularly unattractive from a harmonics mitigation perspective since it is of common-mode nature and therefore especially prone to cause EMI. It is therefore likely to require additional filtering to allow for compliance with distortion limits.

It can be concluded that the discussed balancing methods can indeed compensate for the unbalanced power flow caused during operation away from the sweet-spot. However, they both rely on using additional currents. These currents will increase power losses and potentially drive up the rating requirements of the semiconductors. Furthermore, as mentioned earlier, they cause additional harmonic distortion at the dc side of the converter which may necessitate additional filtering to comply with norms and regulations.

As discussed in Section 1.5.2 the half-bridge MMC suffers from large energy pulsations in the phase arms during operation, which implies that the overall stored energy in the submodule capacitors needs to be large to limit the voltage ripple. This can to a certain extent be mitigated by using full-bridge submodules thanks to the possibility of operating with modulation indices far beyond one, whereby the energy pulsations occurring between upper and lower phase arms can be reduced. For the AAC the arm power pulsation can be derived by assuming sinusoidal ac-side quantities, whereby the upper arm voltage and current is

$$\begin{aligned} v_{\mathrm{u}} &= V_{\mathrm{d}}/2 - \hat{v}_{\mathrm{s}} \sin(\omega_1 t) \\ i_{\mathrm{u}} &= \hat{i}_{\mathrm{s}} \sin(\omega_1 t - \varphi). \end{aligned} \tag{1.62}$$

during the interval when the upper director switch is conducting ($0 < \omega_1 t < \pi$). Multiplying these expressions, and some simplification, yields the following equation for the power exchanged with the upper arm during the concerned interval:

$$p_{\mathrm{u}} = \frac{V_{\mathrm{d}}}{2}\hat{i}_{\mathrm{s}} \sin(\omega_1 t - \varphi) - \frac{1}{2}\hat{v}_{\mathrm{s}}\hat{i}_{\mathrm{s}}[\cos(\varphi) - \cos(2\omega_1 t - \varphi)]. \tag{1.63}$$

During the other half-cycle ($\pi < \omega_1 t < 2\pi$) the current, and thus the power, is zero. The corresponding equations for the lower phase arm will be the same but phase shifted by half of a fundamental cycle. In the sweet-spot, according to Equation (1.60), Equation (1.63) simplifies to

$$p_{\mathrm{u}} = \frac{1}{2}\hat{v}_{\mathrm{s}}\hat{i}_{\mathrm{s}} \left\{ \frac{\pi}{2} \sin(\omega_1 t - \varphi) - \cos(\varphi) - \cos(2\omega_1 t - \varphi) \right\}. \tag{1.64}$$

As evident from this equation the power fluctuation to be handled by the submodule capacitors contains a fundamental frequency term and a second harmonic term, like in the MMC. In addition there is a constant term. However, since the current is only present in the arm during the interval $0 < \omega_1 t < \pi$ the power flow can average to zero. Furthermore, the constant and sine terms will to a significant extent cancel out during the period. Therefore, the energy fluctuation and thus the capacitor voltage ripple is reduced. As evident from Figure 1.29(f) the capacitor energy fluctuation is low in comparison to the MMC. The choice of operating point and normalization of the signals used in Figures 1.19, 1.27, and 1.29 were made so as to allow for comparisons. A comprehensive analysis of the capacitor energy pulsations of the

AAC confirms these findings [23]. Thus, potentially the AAC can be designed with less capacitive energy storage than the MMC. However, operation far from the sweet-spot, employing the discussed means of balancing, will generally increase the energy fluctuations, and a proper analysis of each case is required.

In terms of overall power semiconductor expenditure and power losses the AAC is generally perceived as falling between the half-bridge MMC and the full-bridge MMC [24]. In the first approximation the required maximum output voltage of all full-bridge submodules per arm is half the pole-to-pole dc-side voltage. Thus, the total capacitor voltage per arm has to be rated for this value as well, which is half of what is required for a half-bridge MMC. However, since each full-bridge has two phase legs, the number of semiconductor elements for the submodule strings will be similar. The director switches, on the other hand, need to withstand the ac-side peak phase voltage, which causes extra semiconductor expenditure. Furthermore, to implement the director switches direct series connection of semiconductor elements is generally required since there are no available elements that can withstand the voltages encountered in a converter for transmission applications. This represents a step away from a truly modular approach to designing converters, and will generally imply additional costs. For such, series-connected, devices there is always a need to provide even voltage sharing, both static, during blocking, and dynamic, during the switching processes. Possibly, the dynamic voltage sharing can be simplified by the circumstance that the switchings mainly occur at zero voltage but the valve design also has to take into account abnormal operating cases when zero-voltage switching cannot be fulfilled.

As regards current rating, the peak arm current will also in this case likely determine the rating of semiconductors of both the full-bridge strings and the director switches. It will amount to the peak ac-side current, which in most cases is more than in the half-bridge MMC; see Equation 1.44.

A final issue that needs consideration is the harmonic properties of the converter. The inner ac-side inner emf is a multilevel voltage much like that of the MMC. Therefore, the need for filtering on the ac side should be minimal. In many applications the arm reactors together with the leakage inductance of a transformer, connecting the converter to the grid, will be sufficient to keep the ac-side distortion within permissible limits. However, unlike the MMC, which also acts as a voltage source toward the dc side, the AAC, as mentioned, resembles a diode bridge seen from the dc terminal. Therefore, the dc-side current contains harmonic components at multiples of six times the fundamental. Therefore, to comply with the stringent requirements concerning harmonic distortion in HVDC applications, the AAC likely also requires a filter, in addition to the dc capacitor, to prevent these harmonics from propagating to the network connected on the dc side, as indicated in Figure 1.28.

In summary, the AAC represents a possible alternative to the MMC for HVDC applications. It appears to be seriously considered for this purpose by the manufacturer GE, formerly Alstom. The component expenditure and the power losses appear favorable, especially when the capability of blocking dc faults is taken into account. In particular, the size of the submodule capacitors could be reduced compared to the MMC given that the overall energy fluctuations of the submodule strings are smaller.

However, the fixed ratio between direct and alternating voltages (the sweet-spot) implies an important restriction to the operation of the converter. The proposed methods for allowing operation away from the sweet-spot also cause certain drawbacks in terms of increased losses and harmonic distortion. Furthermore, the AAC is not modular to the same extent as the

MMC. In addition to the submodules it requires series-connected valves capable of blocking high voltage, as well as a relatively large dc capacitor dimensioned for the full pole-to-pole dc-side voltage. Also, the harmonic distortion at the dc side is considerably higher than that of the MMC.

1.6 Summary

The two-level converter enjoys extremely widespread use for low-voltage motor drives as well as for grid connected applications, such as the integration of RES and uninterruptible power supplies. This topology benefits from its simplicity, and the easy power transfer between phase legs which leads to minimal requirements on the size of the capacitor energy storage.

In the voltage range beyond a few kilovolts two-level converters become harder to implement because of the lack of power semiconductors with sufficient blocking capability. Direct series connection of devices to handle this issue is possible, but it is an expensive technology that has never gained widespread use. Instead, multilevel converters are in most cases more suited for these higher voltages. These split the switched direct voltage among several dc capacitors so that semiconductor series connection can be avoided. Also, the relationship between switching frequency and harmonic distortion of the output voltage is much more favorable. This is due to both the increase in the number of voltage levels and the decoupling of the pulse frequency from the switching frequency.

For medium-voltage applications up to several kilovolts diode-clamped topologies currently dominate the market. These share the benefit of not requiring large dc capacitors with the two-level converter. However, extension to more than three levels is cumbersome, owing to the many clamping diodes required, and the fact that these all need to be connected to the common dc link. Therefore, diode-clamped converters are not suited for applications in power transmission and distribution systems, where tens or hundreds of kilovolts are to be handled.

At such levels of voltage instead cascaded converters, employing series-connection of converter submodules, are rapidly gaining market share. This is happening at the expense of CSCs that previously reigned supreme in this power range. A number of important factors reinforce this development.

First, the scalability in terms of voltage, and thereby power, is excellent. The voltage rating can be increased by simply adding more submodules. Since the commutation paths are internal to the submodules, the impact of stray elements is not more critical than in a low-voltage converter. Furthermore, since the number of levels can easily be increased, the switching frequency can be reduced to only a few times the fundamental while still fulfilling requirements concerning harmonic distortion. This implies that semiconductor devices of high blocking voltage can be used without excessive switching losses. Moreover, the modular design implies benefits in terms of design and manufacturing, since the converter largely consists of a number of identical units.

On the negative side, cascaded converters generally suffer from considerable internal energy fluctuations at low frequency, which have to be absorbed by the submodule capacitors. This implies that the total energy stored in the capacitors needs to be much larger than in, for instance, a two-level converter. The cost of the capacitors is increased, and the large stored energy also implies challenges for the handling of internal short-circuit faults. The energy pulsations occur at multiples of the fundamental frequency, which is particularly critical for a converter that should be able to operate at low frequency (e.g. in a motor drive application).

Generally, additional measures have to be taken to balance the energy pulsations between the phase arms in these cases.

The introduction of the MMC with half-bridge submodules was a major step forward, since it was the first truly submodule-based converter to allow ac/dc conversion. It has sparked intense development efforts, leading to the commercialization of this technology within less than ten years. Currently, several HVDC links are already in operation that rely on MMCs for the conversion between ac and dc. This means that VSCs can compete successfully with CSCs also in the high-power range. One weakness, however, is the loss of current control that occurs whenever the direct voltage is absent.

The possibilities of cascaded converters have also been exploited in other ways. Particularly the full-bridge STATCOM has found many practical applications. MMCs with full-bridges are also seriously considered for HVDC applications thanks to the capability of maintaining current control even during dc-side short-circuit faults. Full-bridges also offer a radically increased operating range, but the semiconductor cost and the power losses will be considerably higher.

In the coming chapters various aspects of the design, operation, and applications of the MMC are described and explained in more detail.

References

[1] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, no. 5, pp. 518–523, 1981.

[2] B. Bijlenga, "HVDC device for converting between alternating voltages and direct current voltages," US Patent 6 480 403, 2002.

[3] B. D. Railing, J. J. Miller, P. Steckley, G. Moreau, P. Bard, L. Ronström, and J. Lindberg, "Cross-Sound Cable project: Second generation VSC technology for HVDC," in *Proceedings of the Cigré Session*, Paris, France, 2004.

[4] I. Mattsson, A. Ericsson, B. D. Railing, J. J. Miller, B. Williams, G. Moreau, and C. D. Clarke, "Murraylink: The longest underground HVDC cable in the world," in *Proceedings of the Cigré Session*, Paris, France, 2004.

[5] T. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," *Proceedings of the 23rd Annual IEEE Power Electronics Specialists Conference*, 1992.

[6] K. Ilves, A. Antonopoulos, L. Harnefors, S. Norrga, L. Ängquist, and H.-P. Nee, "Capacitor Voltage Ripple Shaping in Modular Multilevel Converters Allowing for Operating Region Extension," *Proceedings of the 37th Annual Conference of the IEEE Industrial Electronics Society (IECON 2011)*, 2011, pp. 4403–4408.

[7] J. D. Ainsworth, M. Davies, P. J. Fitz, K. E. Owen, and D. R. Trainer, "Static VAr compensator (statcom) based on single-phase chain circuit converters," *IEE Proceedings: Generation, Transmission and Distribution*, vol. 145, no. 4, pp. 381–386, 1998.

[8] P. W. Hammond, "A new approach to enhance power quality for medium voltage AC drives," *IEEE Transactions on Industry Applications*, vol. 33, no. 1, pp. 202–208, 1997.

[9] R. Marquardt, A. Lesnicar, and J. Hildinger, "Modulares Stromrichterkonzept für Netzkupplungsanwendung bei hohen Spannungen," *Proceedings of the ETG-Fachtagung, Bad Nauheim, Germany*, 2002.

[10] T. Westerweller, K. Friedrich, U. Armonies, A. Orini, and D. Parquet, "Trans Bay Cable: World's first HVDC system using multilevel voltage-sourced converter," *Proceedings of the Cigré Session*, Paris, France, 2010.

[11] K. Ilves, S. Norrga, L. Harnefors, and H.-P. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 77–88, 2014.

[12] A. Antonopoulos, L. Ängquist, S. Norrga, K. Ilves, L. Harnefors, and H.-P. Nee, "Modular multilevel converter ac motor drives with constant torque from zero to nominal speed," *IEEE Transactions on Industry Applications*, vol. 50, no. 3, pp. 1982–1993, 2014.

[13] S. Mori, K. Matsuno, T. Hasegawa, S. Ohnishi, M. Takeda, M. Seto, S. Murakami, and F. Ishiguro, "Development of a large static var generator using self-commutated inverters for improving power system stability," *IEEE Transactions on Power Systems*, vol. 8, no. 1, pp. 371–377, 1993.

[14] C. Schauder, M. Gernhardt, E. Stacey, T. Lemak, L. Gyugyi, T. Cease, and A. Edris, "Development of a ±100 MVAr static condenser for voltage control of transmission systems," *IEEE Transactions on Power Delivery*, vol. 10, no. 3, pp. 1486–1496, 1995.

[15] T. Larsson, R. Grünbaum, and B. Ratering-Schnitzler, "SVC Light: A utility's aid to restructuring its grid," *Proceedings of the IEEE Power Engineering Society Winter Meeting 2000*, vol. 4, pp. 2577–2581, Singapore, 2000.

[16] R. H. Baker and L. H. Bannister, "Electric power converter," US Patent 3 867 643, Feb. 18, 1975.

[17] F. Z. Peng, J.-S. Lai, J. McKeever, and J. VanCoevering, "A multilevel voltage-source inverter with separate DC sources for static var generation," *IEEE Transactions on Industry Applications*, vol. 32, no. 5, pp. 1130–1138, 1996.

[18] M. Pereira, D. Retzmann, J. Lottes, M. Wiesinger, and G. Wong, "SVC PLUS: An MMC STATCOM for network and grid access applications," *Proceedings of the 2011 IEEE PowerTech*, Trondheim, Norway, 2011.

[19] F. Peng and J. Wang, "A universal STATCOM with delta-connected cascade multilevel inverter," *Proceedings of the IEEE 35th Annual Power Electronics Specialists Conference*, vol. 5, pp. 3529–3533, 2004.

[20] K. Ilves, S. Norrga, and H.-P. Nee, "On energy variations in modular multilevel converters with full-bridge submodules for AC-DC and AC-AC applications," *Proceedings of the 15th European Conference on Power Electronics and Applications (EPE)*, Lille, France, 2013.

[21] D. Trainer, C. Davidson, C. Oates, N. MacLeod, D. Critchley, and R. Crookes, "A new hybrid voltage-sourced converter for HVDC power transmission," *Proceedings of the Cigré Session*, Paris, France, 2010.

[22] F. Moreno, M. Merlin, D. Trainer, K. Dyke, and T. Green, "Control of an alternate arm converter connected to a star transformer," *16th European Conference on Power Electronics and Applications*, Lappeenranta, Finland, 2014.

[23] M. Merlin, T. Green, P. Mitcheson, F. Moreno, K. Dyke, and D. Trainer, "Cell capacitor sizing in modular multilevel converters and hybrid topologies," *Proceedings of the 16th European Conference on Power Electronics and Applications*. Lappeenranta, Finland: IEEE, 2014.

[24] S. Norrga, X. Li, and L. Ängquist, "Converter topologies for HVDC grids," *Proc. 2014 IEEE International Energy Conference (ENERGYCON)*, pp. 1554–1561. Dubrovnik, Croatia: IEEE, 2014.