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Why Surfaces and Interfaces of Electronic Materials

1.1 The Impact of Electronic Materials

This is the age of materials – we now have the ability to design and create new materials with properties not found in nature. Electronic materials are one of the most exciting classes of these new materials. Historically, electronic materials have meant semiconductors, the substances that can emit and react to light, generate and control current, as well as respond to temperature, pressure, and a host of other physical stimuli. These materials and their coupling with insulators and metals have formed the basis of modern electronics and are the key ingredient in computers, lasers, cell phones, displays, communication networks, and many other devices. The ability of these electronic materials to perform these functions depends not only on their inherent properties in bulk form but also, and increasingly so, on the properties of their surfaces and interfaces. Indeed, the evolution of these materials over the past 70 years has been for ever decreasing size and increasing complexity, features that have driven ever increasing speeds and the ability to manage ever larger bodies of information. In turn, these are enabling our modern day quality of life.

1.2 Surface and Interface Importance as Electronics Shrink

Surfaces and interfaces are central to microelectronics. One of the most common micro-electronic devices is the transistor, whose function can illustrate the interfaces involved and their increasing importance as the scale of electronics shrinks. Figure 1.1 shows the basic structure of a transistor and the functions of its interfaces. Current passes from a *source* metal to a *drain* metal through a semiconductor, in this case, Si. Voltage applied to a *gate* metal positioned between the source and drain serves to attract or repel charge

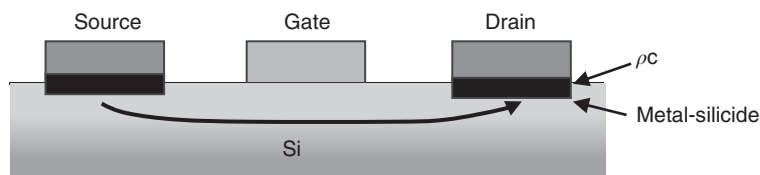


Figure 1.1 Source–gate–drain structure of a silicon transistor. (Brillson 2010. Reproduced with permission of Wiley.)

from the semiconductor region, the “channel”, through which current travels. The result is to control or “gate” the current flow by this third electrode. This device is at the core of the microelectronics industry.

The interfaces between the semiconductor, metal, and insulator of this device play a central role in its operation. Barriers to charge transport across the metal–semiconductor interface are a major concern for all electronic devices. Low resistance contacts at Si source and drain contacts typically involve metals that produce interface reactions, for example, Ti contacts that react with Si with high temperature annealing to form TiSi_2 between Ti and Si, as shown in Figure 1.2a. These reacted layers reduce such barriers to charge transport and the contact resistivity ρ_C . Such interfacial silicide layers form low resistance, planar junctions that can be integrated into the manufacturing process for integrated circuits and whose penetration into the semiconductor can be controlled on a nanometer scale.

The gate–semiconductor interface is another important interface. This junction may involve either: (i) a metal in direct contact with the semiconductor where the interfacial barrier inhibits charge flow or (ii) as widely used in Si microelectronics, a metal–insulator–semiconductor stack to apply voltage without current leakage to the semiconductor’s channel region (Figure 1.2b). Lattice sites within the insulator and at the insulator–semiconductor interface can trap charges and introduce electric dipoles that oppose the voltage applied to the gate metal and its control of the channel current. A major goal of the microelectronics industry since the 1950s has been to minimize the formation of these localized charge states.

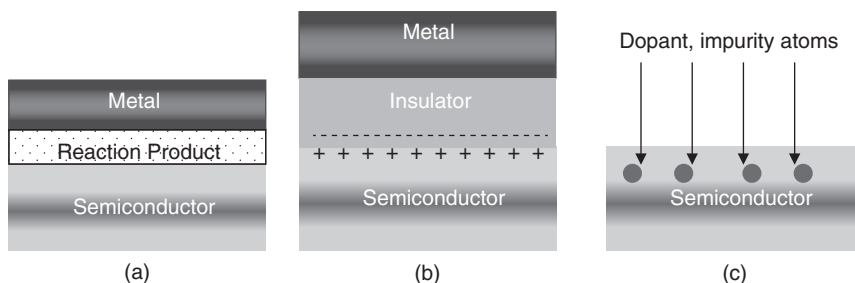


Figure 1.2 Interfaces involved in forming the transistor structure including: (a) the source or drain metal–semiconductor contact with a reacted interface, (b) the gate metal–semiconductor contact separated by an insulator in and near which charges are trapped, and (c) dopant impurity atoms implanted below the surface of a semiconductor to control its carrier concentration. (Brillson 2010. Reproduced with permission of Wiley.)

A third important interface involves the implantation of impurity atoms into the semiconductor to add donor or acceptor “dopants” that control the transistor’s n- or p-type carrier type and density within specific regions of the device. This process involves acceleration and penetration of ionized atoms at well-defined depths, nanometers to microns, into the semiconductor, as Figure 1.2c illustrates. This ion implantation also produces lattice damage that high temperature annealing can heal. However, such annealing can introduce diffusion and unintentional doping in other regions of the semiconductor that can change their electronic activity. Outdiffusion of semiconductor constituents due to annealing is also possible, leaving behind electronically active lattice sites. Precise design of materials, surface and interface preparation, thermal treatments, and device architectures are required in order to balance these competing effects.

At the circuit level, there are multiple interfaces between semiconductors, oxides, and metals. For Si transistors, the manufacturing process involves (i) growing a Si boule in a molten bath that can be sectioned into wafers, (ii) oxidizing, diffusing, and implanting with dopants, (iii) overcoating with various metal and organic layers, (iv) photolithographically patterning and etching the wafers into monolithic arrays of devices, and (v) dicing the wafer into individual circuits that can be mounted, wire bonded, and packaged into chips. Within individual circuit elements, there can be many layers of interconnected conductors, insulators, and their interfaces. Figure 1.3 illustrates the different materials and interfaces associated with a $0.18\text{ }\mu\text{m}$ transistor at the bottom of a multilayer Al–W–Si-oxide dielectric assembly [1]. Reaction, adhesion, interdiffusion, and the formation of localized electronic states must be carefully controlled at all of these interfaces during the many patterning, etching, and annealing steps involved in assembling the full structure. The materials used in this multilayer device architecture have continued to change over decades to compensate for the otherwise increasing electrical resistance as interconnects between layers shrink into the nanometer regime. These microelectronic materials and architectures continue to evolve in order to achieve higher speeds, reliability, and packing density. This continuing evolution highlights the importance of interfaces since they are an increasing proportion of the entire structure as circuit sizes decrease and become ever more complex.

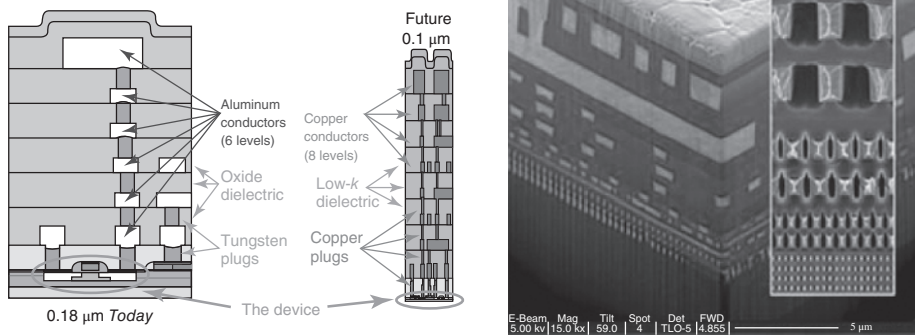


Figure 1.3 Multilayer, multi-material interconnect architectures at the nanoscale. Feature size of interconnects at right is 45 nm [1].

Besides transistors, many other electronic devices rely on interfaces for their operation. For example, solar cells operate by converting incident light into free electrons and holes that separate and generate current or voltage in an external circuit. The charge separation requires built-in electric fields that occur at metal–semiconductor or semiconductor–semiconductor interfaces. These will be discussed in later chapters. Transistors without metal gates are another such device. Channel current is controlled instead by molecules that adsorb on this otherwise free surface, exchanging charge and inducing electric fields analogous to that of a gate. Interfaces are also important in devices that generate photons, microwaves, and acoustic waves. These devices require low resistance contacts to inject current or apply voltage to the layer that generates the radiation. Otherwise, power is lost at these contacts, reducing or totally blocking power conversion inside the semiconductor. Semiconductor cathodes that emit electrons when excited by incident photons are also sensitive to surface conditions. Surface chemical treatments of specific semiconductors are required in order to promote the emission of multiple electrons when struck by single photons, useful for electron pulse generation or photomultipliers.

For devices on the quantum scale, surfaces and interfaces have an even larger impact. A prime example is the quantum well, one of the workhorses of optoelectronics. Here a semiconductor is sandwiched between two larger gap semiconductors that localize both electrons and holes in the smaller gap semiconductor. This spatial overlap between electrons and holes increases electron–hole recombination and light emission. Since the quantum well formed by this sandwich is only a few monolayers thick, the allowed energies of electrons and holes inside the well are quantized at discrete energies, which promotes efficient carrier population inversion and laser light emission. Imperfections at the interfaces of these quantum wells introduce alternative pathways for recombination that reduce the desired emission involving the quantized states. Such recombination is even more serious for three-dimensional quantum wells, termed *quantum dots*. Another such example is the *two-dimensional electron gas* (2DEG) formed when charges accumulate in narrow interfacial layers, only a few tens of nanometers thick, between two semiconductors. The high carrier concentration, high mobility 2DEG is the basis of *high electron mobility transistors* (HEMTs). As with quantum wells, lattice defects at the interface can produce local electric fields that scatter charges, reduce mobility, and alter or even destroy the 2DEG region. Yet another quantum-scale structure whose interfaces play a key role is the *cascade laser*, based on alternating high- and low-bandgap semiconductors. In this structure, charge must tunnel through monolayer thin barrier layers, formed by the higher band gap semiconductors, into quantized energy levels. Here again, efficient tunneling depends on interfaces without significant imperfections that could otherwise introduce carrier scattering.

In addition to carrier scattering and recombination, the alignment of energy levels between constituents is a major feature of interfaces. How energy levels align between a semiconductor and a metal, as well as between two semiconductors, is a fundamental issue that is still not well understood. The interface band alignment determines the barriers to charge transport between constituents and the carrier confinement between them. There are several factors that can play a role: (i) the band structure of the constituents at the junction, (ii) the conditions under which the interface forms, and (iii) any subsequent thermal or chemical processing. Hence, it is important to measure and understand the properties of these interfaces at the microscopic, indeed atomic, level in order to learn and

control how surfaces and interfaces impact electronics. The future of electronics depends on our ability to design, measure, and control the physical properties of these surfaces and interfaces. This book is intended to describe the key properties of these surfaces and interfaces along with the tools and techniques used to measure them.

1.3 Historical Background

1.3.1 Contact Electrification and the Development of Solid State Concepts

The recognition that contacts to materials could be electrically active dates back to the Greco-Roman times and the discovery of *triboelectricity*, the charge transfer between solids generated by friction – for example, the generation of static electricity by rubbing cat's fur with amber. Two millennia later, Braun discovered *contact rectification*, the unequal flow of charge in two directions, by applying positive and negative voltage to metal contacts with selenium [2]. In 1905, Einstein explained the *photoelectric effect* at metal surfaces based on light as wave packets with discrete energies [3]. This established both the particle behavior of light and the concept of work function, an essential component in the description of energy bands in solids. These energy bands will be discussed in Chapter 2 and form the basis for discussing all the physical phenomena associated with surfaces and interfaces of electronic materials.

The theory of energy bands in solids was first developed by Wilson [4,5] and forms the basis for interpreting semiconductor phenomena. Siemens *et al.* [6] and Schottky *et al.* [7] showed that contact rectification at the interface exhibited behavior that was distinct from that of the semiconductor interior. Subsequently, Mott [8], Davidov [9,10], and Schottky [11–13] each published theories of contact rectification that involved an energy band bending region near the interface. Mott proposed an insulating region between the metal and semiconductor to account for current–voltage features of copper oxide rectifiers. Davidov showed the importance of thermionic work function differences in forming the band bending region. Schottky introduced the concept of a stable space charge in the semiconductor instead of a chemically distinct interfacial layer. Appropriately, this interface concept became the *Schottky barrier*. Bethe's theory of thermionic emission of carriers over an energy barrier [14], based partly on Richardson's earlier thermionic cathode work [15] provided a picture of charge transport across the band bending region that accounted for the rectification process in most experimental situations. These developments laid the foundation for describing barrier formation and charge transfer at semiconductor interfaces.

1.3.2 Crystal Growth and Refinement

The understanding and control of semiconductor properties began with advances in the growth and refinement of semiconductor crystals. Once researchers learned to create crystals with ultrahigh purity (as low as one impurity atom in ten billion) and crystalline perfection, they could unmask the inherent properties of semiconductors, free of effects due to lattice impurities and imperfections, and begin to control these properties in electronic devices. Beginning in the 1940s, crystal pulling and zone-refining techniques became available that could produce large, high-purity semiconductor single crystals.

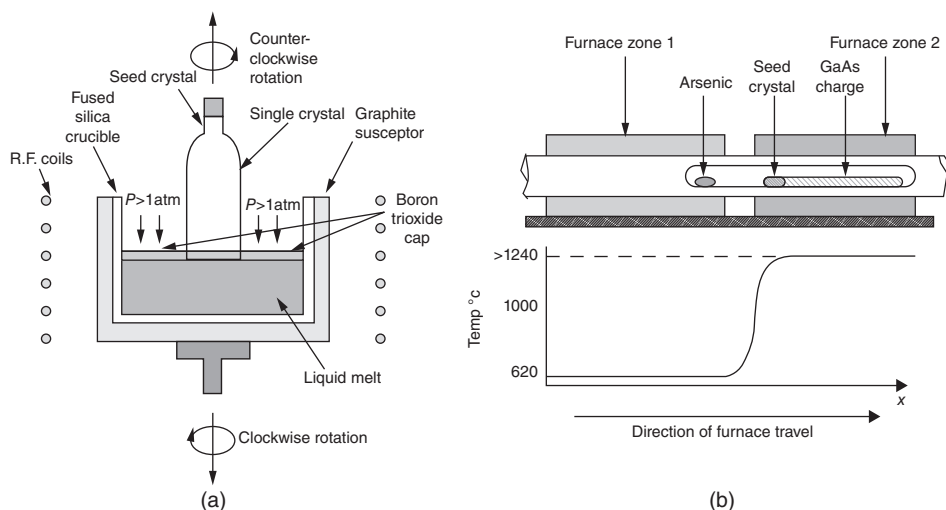


Figure 1.4 (a) LEC growth of GaAs crystal pulled from a molten bath inside a heated crucible. (Lammers, D www.semiconductor.net/article/CA6513618.html. Used under CC-BY 3.0 <https://creativecommons.org/licenses/by-sa/3.0/deed.en>.) (b) Horizontal Bridgman growth of GaAs traveling through the temperature gradient of a furnace.

Figure 1.4a illustrates the *liquid encapsulated Czochralski* (LEC) method of growing large single crystals from a molten bath in which a seed crystal nucleates larger boules of crystal as the seed is gradually raised out of the melt. Figure 1.4b shows how molten semiconductor constituents are nucleated at a seed over which a furnace is gradually pulled from high to low temperature.

The crystal thus produced is then passed again through a melt zone along its length, causing impurities to segregate from high to low temperature regions in a process termed *zone-refining* [16]. Numerous other crystal growing techniques such as liquid phase epitaxy (LPE), pulsed laser deposition (PLD), and molecular beam epitaxy (MBE) are now available that are capable of producing multilayer crystal structures with atomic-scale precision. Figure 1.5 illustrates the LPE and MBE methods. These and other techniques are able to create materials not found in nature and having unique properties that enable a myriad of devices.

1.3.3 Transistor Development and the Birth of Semiconductor Devices

Semiconductor surfaces and interfaces have been an integral part of the transistor's development. Motivated by the need to replace vacuum tubes as amplifiers and switches in telecommunications equipment, researchers at Bell Labs succeeded in demonstrating transistor action in 1947 using closely spaced point contacts on germanium crystals [18]. Figure 1.6 shows this early transistor configuration, which relied on high purity crystals supplied by Purdue University [19] to obtain carrier diffusion lengths long enough to reach between contacts. Contrast this early transistor with the nanoscale device structures pictured in Figure 1.3. Developing this first transistor, Bardeen, Shockley, and Brattain found that gate modulation of the charge and current inside the semiconductor was much weaker than

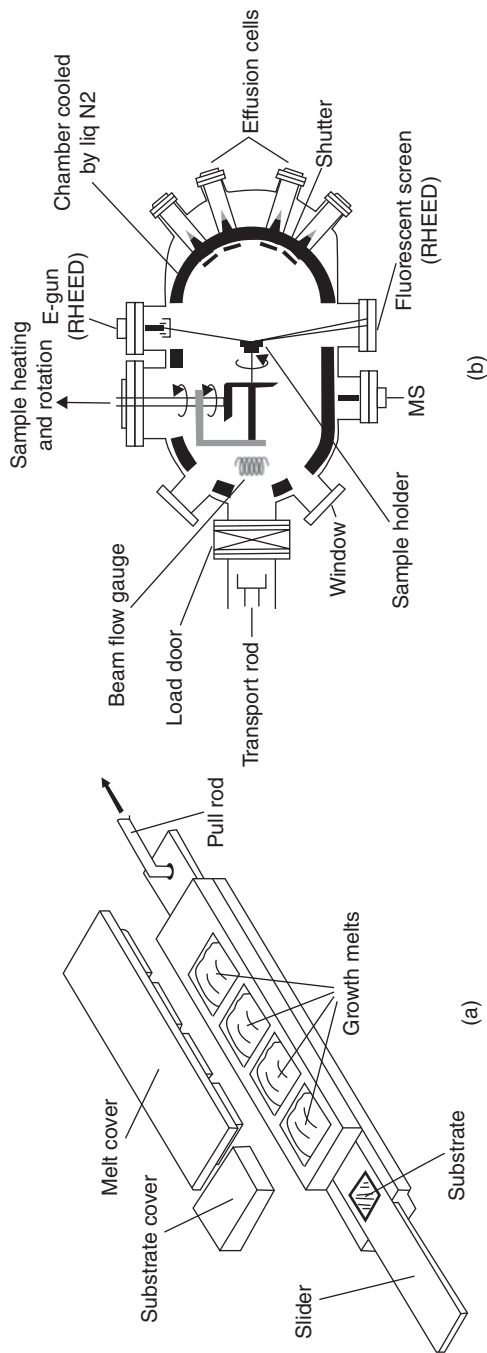


Figure 1.5 (a) LPE method in which a growth substrate slides under pockets of melted constituents that condense to form a stack of semiconductor layers on the substrate. (b) MBE method in which constituents evaporated from individual crucibles of pure elements deposit layer-by-atomic layer monitored by reflection high energy diffraction (RHEED) on a heated substrate in vacuum. (Barron, W. D <http://cnx.org/content/m25712/latest>. Used under Creative Commons Attribution 4.0 License.)

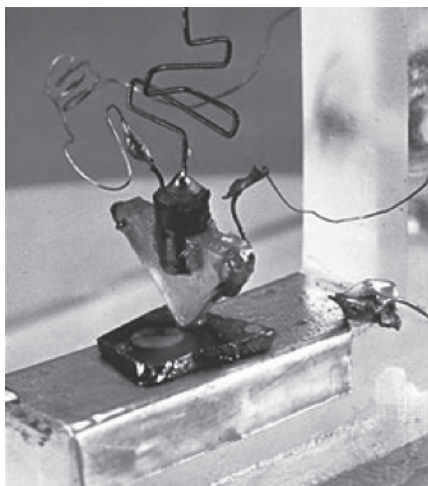


Figure 1.6 A point contact transistor with three gold contacts on a germanium crystal [18].

expected. This led to the discovery that electric charges immobilized on the semiconductor surface were responsible, which Bardeen correctly interpreted as electronic states localized at the semiconductor interface [20]. By reducing the density of these states and their influence on the field effect pictured in Figure 1.1, Bardeen *et al.* could demonstrate the transistor action clearly, for which they received the 1956 Nobel Prize. The interface concepts developed with the transistor continue to drive the evolution of future electronics technology. By the early 1950s, semiconductor electronics began to develop rapidly. First came the switch from germanium to silicon, since the native oxide of silicon was much more resistant to water vapor than that of germanium [21]. By 1958, the first integrated circuits appeared [22], based on arrays of transistor circuits on silicon wafers. The 1950s and early 1960s saw the development of many other devices, including photodiodes, sensors, photomultipliers, and light emitting diodes. All required high purity semiconductor as well as refined techniques to form their electrical contacts. This led to the development of high-vacuum technology, including the pumps, chambers, and pressure gauges to be discussed in Chapter 5. These tools could be used to control both the localized states at the transistor's semiconductor–insulator interface and those at Schottky barriers of the metal–semiconductor junctions found in most of these devices. Early Schottky barrier experiments involved semiconductor crystals cleaved in medium vacuum, $\sim 10^{-6}$ Torr and in a stream of evaporating metal atoms to minimize contamination [23]. This work presaged the use of *ultrahigh vacuum* (UHV) to obtain atomically-clean surfaces and interfaces.

1.3.4 Surface Science and Microelectronics

The use of ultrahigh vacuum technology with chamber pressures of 10^{-10} Torr or less began in the late 1960s and marked the birth of *surface science* as a field that spans multiple disciplines and that continues to grow. With the ability to prepare clean surfaces and maintain their cleanliness for long periods of time, researchers were now able to study a wide

range of electronic, chemical, and atomic structural phenomena. Beginning in the 1970s, much of this work aimed to understand the nature of surface and interface states that could account for the insensitivity of transistors to applied bias voltage. For the oxide interface with silicon, researchers found that careful surface cleaning and precise high temperature gas ambient annealing – processes developed using surface science techniques – could reduce interface state densities by orders of magnitude. By the mid-1970s, the materials science or microelectronic metallurgy of the various electronic material interfaces helped refine the monolithic (extended surface) electronic circuitry on silicon wafers. This work was instrumental in understanding and predicting the interfacial reactions at silicon–metal interfaces, for example, Figure 1.2a [24,25].

Another major challenge was the insensitivity of band bending and Schottky barriers to different metals at the metal–semiconductor interface. This was attributed to surface or interface states that “pinned” the semiconductor Fermi level in a narrow range of energies within the band gap. Initial studies of metal contacts to compound semiconductors suggested that the ionicity of the semiconductor played a role in creating such states [26], and theoretical calculations of the abrupt surface termination of the bulk crystal structure supported this. However, surfaces of many compound semiconductors, particularly those prepared without steps or other defects, exhibited an absence of such states in the semiconductor band gap. Instead, measurements of the bonding structure at many compound semiconductor surfaces revealed atomic rearrangements that served to remove surface states from within the semiconductor band gap. Theoretical studies confirmed that these surface atomic rearrangements or reconstructions in general minimized bond energies and removed such *intrinsic* surface states from the semiconductor band gap.

Other models to account for this *Fermi level pinning* were: (i) adsorbate bonding that forms electrically-active defects at the semiconductor surface; (ii) wave function tunneling that forms localized states close to the interface; (iii) chemical reactions that produce interfacial layers with new dielectric properties and/or defects. During this period, literally thousands of studies, both experimental and theoretical, were devoted to testing these models of Fermi level pinning. While metal deposition on one type of III-V semiconductor exhibited barrier insensitivity for many adsorbates, researchers found that the same compounds grown with higher crystalline perfection could exhibit wide barrier height ranges. Wave function tunneling based on intrinsic semiconductor properties provided a mechanism for theoretical predictions of barriers heights and their systematics for different semiconductors with an inert metal [27–30]. However, experimental results show serious inconsistencies with predicted barrier height values for both ionic [31] and covalent semiconductors [32].

Starting in the late 1980s, researchers found that metals deposited on semiconductors could produce chemical reactions, even near room temperature [33,34]. Surface science techniques were uniquely capable of detecting such reactions even though such reactions and atomic rearrangement often took place on a monolayer scale. The chemical composition of these reactions, the diffusion of atoms out of the semiconductor lattice, and the correlation of their reactivity with Schottky barrier heights suggested that such reactions produced native point defects within the semiconductor where atoms had outdiffused [35,36]. Such defects are electrically active and mobile and can segregate near surfaces and interfaces [35,37]. They also have energy levels that can account for reported Fermi level pinning energies of different semiconductors [36].

The 1980s saw the invention and development of the *scanning tunneling microscope* (STM). With this instrument, researchers were now able to image the arrangement of individual atoms on semiconductor surfaces, resolving many questions previously unanswered by less direct techniques. Derived from STM in the 1990s, *atomic force microscopy* (AFM) provided a new way to measure surface morphology on a nanometer scale and to probe semiconductors and insulators lacking the conductivity required for STM. Also related to the STM was *ballistic electron energy microscopy* (BEEM), which revealed heterogeneous electronic features across semiconductor surfaces that reflected multiple local Schottky barrier heights within the same macroscopic contact. These insulator–semiconductor and metal–semiconductor studies also provided insights into the mechanisms controlling heterojunction band offsets, which establish the basic properties of many micro- and optoelectronic devices.

1.4 Next Generation Electronics

New electronic materials and device architectures have emerged over the past two decades where surfaces and interfaces play an integral role. These include: high dielectric constant (hi-K) insulators, complex oxides, magnetic semiconductors, spin conductors and insulators, nano-scale and quantum-scale structures, two-dimensional (2D) semiconductors, and topological insulators. All of these new materials and device architectures pose challenges for researchers and technologies because of their ultra-small dimensions. In turn, these dimensions magnify the effects of diffusion and reaction that can occur with the very high temperatures and chemically reactive environments that such materials may encounter. As with previous generations of electronic development, we expect a synergy between the science and technology of electronic materials. This dual track of progress will again involve an interplay between growth, characterization, device design and testing that will require many of the techniques described in this book.

This chapter aimed to motivate the study of electronic materials' surfaces and interfaces. Their properties influence band structure, charge densities and electronic states on a scale ranging from microns down to atomic layers. Although these phenomena exist on a microscopic scale, they manifest themselves electrically on a macroscopic scale. Indeed they already dominate electronic and optical properties of current electronics. Coupled with this “race to the bottom” are atomic and nanoscale techniques to characterize the electronic, chemical, and geometric properties of these electronic material structures. This introductory book aims to provide the essential framework to understand the physical properties of electronic material surfaces and interfaces and the techniques developed to measure them.

1.5 Problems

1. Give one example each of how surface and interface techniques have enabled modern CMOS (*complementary metal-oxide semiconductor*) technology (a) structurally, (b) chemically, and (c) electronically.
2. Name three desirable solar cell properties that could be affected by interface defects.
3. Name three interface effects that could degrade quantum well operation.

4. As electronics shrinks into the nanoscale regime, actual numbers of atoms become significant in determining the semiconductor's physical properties. Consider a $0.1\ \mu\text{m}$ Si field effect transistor with a $0.1 \times 0.1\ \mu\text{m}^2$ cross-section and a doping concentration of $10^{17}\ \text{cm}^{-3}$. How many dopant atoms are in the channel region? How many dopant atoms are there altogether?
5. Assume the top channel surface has 0.01 trapped electrons per unit cell. How many surface charges are present? How much do they affect the channel's bulk charge density?
6. Even small numbers of interface states inside electronic devices can have large effects. For a GaAs field effect transistor with gate length $0.2\ \mu\text{m}$ with a $0.1\ \mu\text{m}$ thick $\times 0.5\ \mu\text{m}$ wide cross-section and doping density of $5 \times 10^{17}\ \text{cm}^{-3}$, how many dopant atoms are in the channel region? How many atoms are there altogether? If there are 0.02 electrons per unit cell at the gate-channel interface, how many electrons are there altogether? How large an effect can these interface states have on the transistor properties? Explain.
7. What fraction of atoms is within one lattice constant of the channel surfaces?
8. Figure 1.2a indicates that reaction products can form between metal contacts and Si. Describe the advantages of depositing multilayers of Ti rather than Au on this surface if a submonolayer of air molecules is present at the Si surface prior to deposition.
9. Figure 1.4 illustrates the complexity of the transistor chip structure. Describe three interface effects that could occur in these structures that could degrade electrical properties during microfabrication.
10. Si emerged as the material of choice for microelectronics. (a) Give five reasons why. (b) What feature of the Si/SiO₂ is the most important for device operation and why?
11. Give two reasons and two examples why GaAs, InP and many other III-V compound semiconductors are used for quantum-scale optoelectronics.
12. Which would you choose for high power, high-frequency transistors, GaAs or GaN?

References

1. <http://it-material.de/category/wirtschaft/computerindustrie/chip-herstellung/> (accessed 1 Feb.2016).
2. Braun, F. (1874) Über die stromleitungdurchschwefelmetalle. *Ann. Phys. Chem.*, **53**, 556.
3. Einstein, A. (1905) Concerning an heuristic point of view toward the emission and transformation of light. *Ann. Phys.*, **17**, 132.
4. Wilson, A.H. (1931) The theory of electronic semi-conductors. *Proc. R. Soc. Lond.*, **A133**, 458.
5. Wilson, A.H. (1931) The theory of electronic semi-conductors II. *Proc. R. Soc. Lond.*, **A134**, 277.
6. Siemens, G. and Demberg, W. (1931) Über detektoren. *Z. Phys.*, **67**, 375.
7. Schottky, W., Störmer, R., and Waibel, F. (1931) On the rectifying action of cuprous oxide in contact with other metals. *Z. Hochfrequenztechnik*, **37**, 162.
8. Mott, N.F. (1939) The theory of crystal rectifiers. *Proc. R. Soc. Lond. A*, **171**, 27.

9. Davidov, B. (1938) On the photo-electromotive force in semiconductors. *J. Tech. Phys. USSR*, **5**, 87.
10. Davidov, B. (1939) On the contact resistance of semiconductors. *Sov. J. Phys.*, **1**, 167.
11. Schottky, W. (1939) Zur Halbleitertheorie der sperrschicht- und spitzengleichrichter. *Z. Phys.*, **113**, 367.
12. Schottky, W. and Spenke, E. (1939) Zur quantitativen Durchführung der Raumladungs- und Randschichttheorie der Kristallgleichricht. *Wiss. Veröffentl. Siemens-Werken*, **18**, 225.
13. Schottky, W. (1942) Vereinfachte und erweiterte Theorie der randschichtgleichrichter. *Z. Phys.*, **118**, 539.
14. Bethe, H.A. (1942) Radiation Laboratory Report No. 43-12, Massachusetts Institute of Technology, November.
15. Richardson, O.W. (1921) *The Emission of Electricity from Hot Bodies*, Longmans-Green, Harlow, Essex.
16. Pfann, W.G. (1958) *Zone Melting*, Wiley, New York.
17. Barron, A. (2009) *Molecular Beam Epitaxy*. OpenStax QA, July 13, 2009. <http://legacy-textbook-qa.cnx.org/content/m25712/1.2/>.
18. Courtesy of AT&T Archives and History Center.
19. Bray, R. (2014) *The Origin of Semiconductor Research at Purdue*, Purdue University, Department of Physics http://www.physics.purdue.edu/about_us/history/semiconductor_research.shtml
20. Bardeen, J. (1947) Surface states and rectification at a metal semi-conductor contact. *Phys. Rev.*, **71**, 717.
21. Teal, G.K. (1976) Single crystals of germanium and silicon – basic to the transistor and integrated circuit. *IEEE Trans. Electron Devices*, **ED-23**, 621 and references therein.
22. <http://www.ti.com/corp/docs/kilbyctr/kilby.shtml>
23. Mead, C.A. and Spitzer, W.G. (1964) Fermi level position at metal-semiconductor interfaces. *Phys. Rev.*, **134**, A713.
24. Poate, J.M., Tu, K.N., and Mayer, J.W. (1978) *Thin Films – Interdiffusion and Reactions*, John Wiley & Sons, Inc.
25. Mayer, J.W. and Lau, S.S. (1990) *Electronic Materials Science: For Integrated Circuits in Si and GaAs*, Macmillan, New York.
26. Kurtin, W., McGill, T.C., and Mead, C.A. (1970) Fundamental transition in the electronic nature of solids. *Phys. Rev. Lett.*, **22**, 1433.
27. Flores, F. and Tejedor, C. (1979) Energy barriers and interface states at heterojunctions. *J. Phys. C*, **12**, 731.
28. Cohen, M.L. (1980) Electrons at interfaces. *Adv. Electron. Electron Phys.*, **51**, 1.
29. (a) Tersoff J. (1984) Schottky barrier heights and the continuum of gap states. *Phys. Rev. Lett.*, **52**, 465; (b) Tersoff, J. (1984) Theory of semiconductor heterojunctions: The role of quantum dipoles. *Phys. Rev. B*, **30**, 4874(R).
30. Mönch, W. (1990) On the physics of metal-semiconductor interfaces. *Rep. Prog. Phys.*, **53**, 221.
31. Allen, M.W. and Durbin S.M. (2010) Role of a universal branch-point energy at ZnO interfaces. *Phys. Rev. B*, **82**, 165310.

32. (a) Mönch, W. (1989) Mechanisms of barrier formation in Schottky contacts: Metal-induced surface and interface states. *Appl. Surf. Sci.*, **41/42**, 128; (b) Mönch, W. (1988) Chemical trends in Schottky barriers: Charge transfer into adsorbate-induced gap states and defects. *Phys. Rev. B*, **37**, 7129.
33. Brillson, L.J. (1978) Transition in Schottky barrier formation with chemical reactivity. *Phys. Rev. Lett.*, **40**, 260.
34. Brillson, L.J. (1978) Chemical reactions and local charge redistribution at metal-CdS and CdSe interfaces. *Phys. Rev. B*, **18**, 2431.
35. Brillson, L.J., Brucker, C.F., Katnani, A.D. *et al.* (1981) Chemical basis for InP-metal Schottky-barrier formation. *Appl. Phys. Lett.*, **38**, 784.
36. Brillson, L.J., Dong, Y., Doust, D. *et al.* (2009) Massive point defect redistribution near semiconductor surfaces and interfaces and its impact on Schottky barrier formation. *Physica B*, **404**, 4768.
37. Mosbacher, H.L., Strzhemechny, Y.M., White, B.D., *et al.* (2005) Role of near-surface states in ohmic-Schottky conversion of Au contacts to ZnO. *Appl. Phys. Lett.*, **87**, 012102.

Further Reading

- Orton, J. (2004) *The Story of Semiconductors*, Oxford University Press, Oxford.
- Turton, R. (1995) *The Quantum Dot, A Journey into the Future of Microelectronics*, Oxford University Press, Oxford.
- Roulston, D.J. (1999) *An Introduction to the Physics of Semiconductor Devices*, Oxford, New York.