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IMPORTANCE OF CLOCK SIGNAL IN MODERN MICROELECTRONIC SYSTEMS

1.1 CLOCK TECHNOLOGY: ONE OF THE FOUR FUNDAMENTAL TECHNOLOGIES IN IC DESIGN

Today's typical electronic systems contain millions of electrical signals. They make the system perform what it is designed to do. Among these, the most important one is the clock signal. From an operational perspective, the clock is the timekeeper of the electrical world in a chip/system. From a structural perspective, the clock generator is the heart of a chip; the clock pulse is the heart beat; the clock signal is the blood; and the clock distribution network is the vessel.

The timekeeper has played and is playing a critical role in human life. History shows that the progressive advancement of our civilization is only made possible by the steady refinement of the timekeeper: the clock [Fra11]. The same is true for electronic systems. The purpose of electronic systems is for processing information. The efficiency of performing this task is highly dependent on the time scale used. This time scale is controlled by the clock signal. It has two key aspects: its size (the absolute clock frequency) and its resolution (the capability of differentiating nearby frequencies; resolution can also be viewed as frequency granularity and/or time granularity). In addition, another characteristic is important in the electronic system: the speed at which the time scale can be switched from one to another (the clock frequency switching speed).

From the day of Robert Noyce [Noy61] and Jack Kirby's [Kil64] first integrated circuit in 1959 to today's systems of billions of transistors on a chip, the art of

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From Frequency to Time-Average-Frequency: A Paradigm Shift in the Design of Electronic Systems, First Edition. Liming Xiu.

integrated circuit (IC) design can be roughly individualized into three key areas: *processor* technology, *memory* technology, and *analog* technology. Processor technology focuses its attention on how to build efficient circuits to process information. Using transistors to do logic and arithmetic operations with high efficiency is its highest priority. Memory technology is the study of storing information in a circuit. Its aim is to store and retrieve information in large amounts and at high speed. Analog technology squares its effort at circuits that interface electrical systems with humans (or the world of physical phenomena). Inside electronic systems, information is processed in binary fashion. Once outside, information is used by us in proportional style since our five senses are built upon proportional relationships. The analog circuit is the bridge in between. During the past several decades, advancements in these three circuit technologies have made today's electronic systems very powerful. However, the driver of these three technologies, the clock, has not seen fundamental breakthroughs. The time scale is not flexible: The available clock frequencies are limited and the switching between frequencies is slow. To improve the electronic system's information processing efficiency further, the next opportunity is with the method of clocking: (1) We need a flexible on-chip clock source and (2) and it needs to be available to chip designers at a reasonable cost. Now is the time for clock to be recognized as a technology, as illustrated in Figure 1.1.

There are four key challenges in the generation of a clock signal: high clock frequency, low noise, small frequency granularity (also loosely referred to as arbitrary frequency generation), and fast frequency switching (also loosely referred to as instantaneous frequency switching). The first two have been studied intensively by researchers. The last two have not drawn much attention. Another challenge lies in distributing the generated clock signal to all the places that require a clock. Clock distribution is a difficult problem both functionally and physically. From a functional perspective, a cell requiring a driving clock might need the clock signal to come from different sources in different operating modes. The logical path from a source to any destination (clock sink) is controlled by the selector, frequency divider, and gater, as illustrated on the left in Figure 1.2. These elements ensure that a clock sink sees the appropriate clock signal at the appropriate time. From a physical point of view,

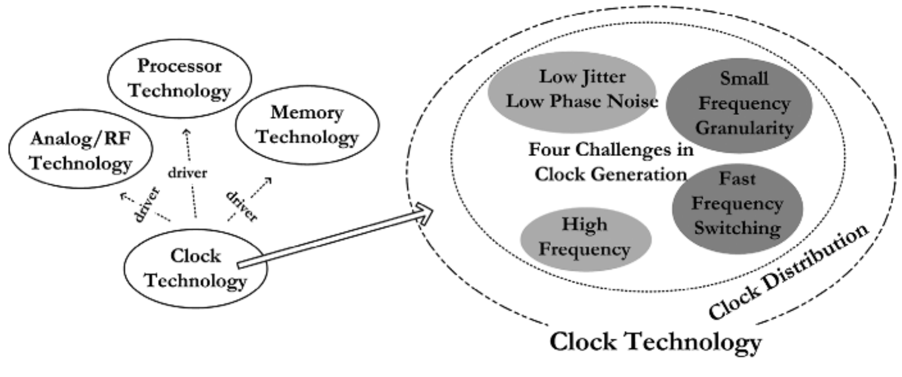

FIGURE 1.1 Clock as a technology.

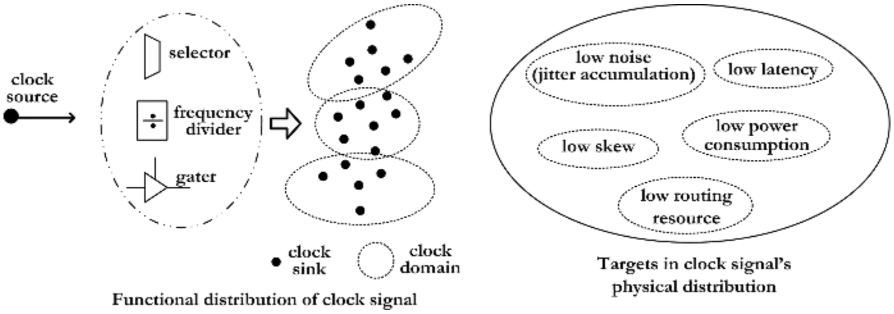

FIGURE 1.2 Clock distribution.

a clock signal from a source might need to be delivered to cells that are spread in a large area. The task of physical distribution has to be carried out with high fidelity (low noise, low skew), small delay (low latency), and low cost (in terms of routing resource and power consumption). These goals are presented on the right-hand side of Figure 1.2.

Clocking is an important and challenging topic in both academic research and engineering practice. IC clocking is closely tied to the two functions in modern chip design: communication and computation. IC clocking also plays an important role in determining the amount of energy consumed in performing these tasks. There are countless papers dedicated to its study in scientific journals and conference proceedings. It is perhaps the most studied topic in electrical engineering. There are also many books devoted to this area of study; most of them focus on the phase-locked loop (PLL) [Gar05, Bes07, Ega07, Raz03, Fri95]. For those reasons, it is fair to recognize IC clocking as one of the four fundamental circuit design technologies. This book is not focused purely on the PLL, which is only part of the clock story (that of clock signal generation). It addresses the IC clocking issue in a much larger scope: clock frequency, clock generation, clock distribution, and clock application. The essence of this book is to influence the landscape of IC design from the clocking side, starting from the fundamental concept of clock frequency.

1.2 CLOCK SIGNAL GENERATOR: THE KNOWLEDGE-AND-SKILL GAP BETWEEN ITS CREATOR AND ITS USER

When a clock signal is used in an electronic system, it involves two groups of engineers: designers of the clock generator and users of the clock signal. This scenario is illustrated in Figure 1.3. These two groups possess different knowledge-and-skill sets. The clock generator designer (usually a PLL designer) focuses his or her attention on creating a circuit that produces an electrical pulse train. The main interest in this task is the quality of the pulse train: the available frequency range, the granularity of its frequency, the frequency switching speed, and the amount of noise embedded in the pulses. The key skill required lies in the area of analog circuit design. Understanding the noise generation mechanism in semiconductor devices is also important.

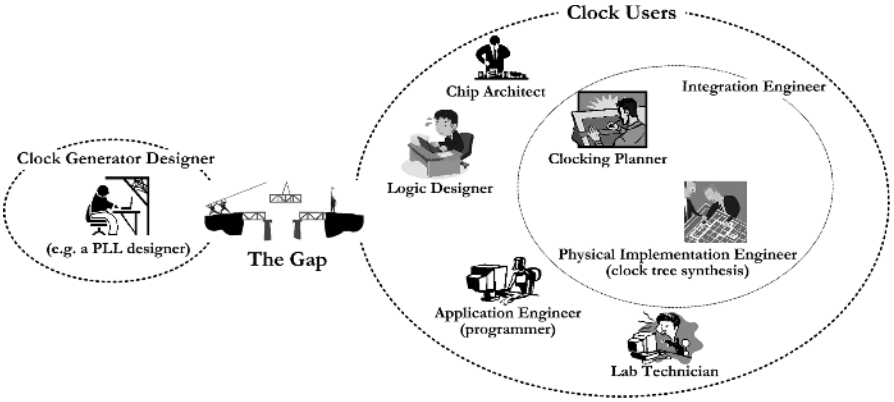

FIGURE 1.3 Clock signal generator: the gap between its creator and its users.

Clock users can be divided into several subgroups. The chip architect is responsible for designing the chip system. Communication between various parts of the chip, as well as the task of computation, is controlled by the clock signals. Thus, the chip architect must have a solid understanding of how the various clock signals are used to perform the computation and communication tasks in the chip. In some design cases, it is possible to have over 100 clock domains in a large system. All have to be carefully designed by the chip architect. A logic designer helps the chip architect realize the chip functional specifications using hardware description language [such as very high speed integrated circuit (VHSIC) Hardware Description Language (VHDL) and verilog] or higher level system languages. A large amount of simulation must be performed by the logic designer to ensure the correctness of the chip functionality. In such simulations, among perhaps millions of on-chip signals, the clock signal is the most studied one. When something unexpected happens in a simulation, the first signal that the designer turns his or her attention to is usually the clock signal.

Integration engineers receive the chip design in a words-and-diagrams description and turn it into a functioning system represented by metals and semiconductor devices. In this process, clock implementation is a crucial part. Where chip clocking is concerned, the clocking planners take the instructions of the chip architect and turn them into an implementable plan. In this task, the clocking planner needs not only to fulfill functional requirements but also to pay attention to a variety of chip testing concerns. The physical implementation engineer (also called a place-and-route engineer) takes the logical plan from the clocking planner and realizes it using metals and standard cells. This work is commonly termed clock tree synthesis. Finally, the application engineer needs to have a firm grip of the chip's clock structure so that the bare chip can be programmed to do its task.

The subjects dealt with by these two groups of engineers are significantly different. The clock circuit designer deals with transistors. Clock users deal with various entities such as functional blocks [e.g., Digital Signal Processor (DSP), Universal Serial Bus (USB), double data rate synchronous dynamic random-access memory (DDR)], standard cells, Hardware Description Language (HDL) coding and simulation, Static

Timing Analysis (STA) timing analysis, place and route, etc. They speak different languages and use different tools. Although the ultimate goal is to make the chip perform as designed, the immediate aims of each type of engineer are very different. The knowledge-and-skill sets required by those engineers are sophisticated enough that a large gap exists between the two groups. For example, a PLL designer oftentimes does not know (or does not have to care) how the chip architect or clocking planner would use his or her PLL. Sometimes, this is caused by a lack of knowledge of other fields. Other times, this could be due to the organizational boundaries of different groups (or different companies).

Within the world of clock circuit designers, the PLL has traditionally been the architecture of choice for the on-chip clock generator. The PLL is a beautiful blend of digital and analog circuits in one piece of hardware. From a given reference time scale, it can generate other time scales. However, due to its use of a *compare-then-correct* feedback mechanism, the choice of time scales that can be produced is limited (it is difficult to make frequency granularity small). Equally harsh is the problem that the change of time scale (frequency switching in PLLs) takes a very long time. Although the PLL has played a key role in making today's electronic systems magnificent, these two problems are limiting the chip architect's capability for creating further innovation at the chip level.

The root of these two problems is partially due to this gap. As a clock circuit designer, the goals of arbitrary frequency generation and fast frequency switching are difficult to achieve, especially simultaneously (in contrast, arbitrary voltage generation and fast voltage switching are easy to do). On the other hand, chip/system architects, from the day the clock signal is introduced into the field of chip design, have not asked the clock circuit designer about these two features since they know that it is difficult. As a result, the clock circuit designer does not have the motivation. The problems associated with these two point-of-views are cause-and-effect of each other: The system architect does not know that it can be done; the circuit designer does not know that it is needed. The goal of this book is to break this lock, to provide a vision that it can be done and it is useful.

This gap, when properly addressed, could be the birthplace for important innovations.

1.3 HOW IS SENSE-OF-TIME CREATED IN ELECTRICAL WORLD?

Today's typical electronic systems contain millions of electrical signals. Signals are the medium for carrying information among electronic devices (transistor, diode, capacitor, resistor, inductor, etc.). Without clearly defined signals, an electronic system cannot perform any useful function except being a heat generator that converts electrical energy into thermal energy. Any electrical signal can be described by using two and only two physical properties: level and time. This is depicted on the left-hand side of Figure 1.4. These two properties correspond to the two fundamental phenomena of the universe: the mass of materials and the flow-of-time. The mass of a material represents the strength of a signal; it is the number of electrons currently being processed by an operating device. It shows its impact through the voltage (or

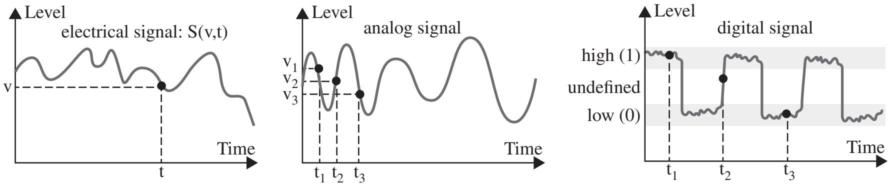

FIGURE 1.4 Electrical signal through level and time (left), analog signal (middle), and digital signal (right).

current) level. This level (the mass of the material) always varies with the flow-of-time. Therefore, level is only identifiable through a snapshot of the level taken at a particular moment in the flow-of-time. In the electrical world, similar to our social world, the flow-of-time must be quantified and each moment must be indexed through some mechanism. By the use of these two fundamental properties, an electrical signal can be expressed as $S(v, t)$, where v represents the level strength and t is the moment in the flow-of-time.

There are two ways to describe a signal level: analog and digital. In the analog approach, a proportional relationship is established between the intended information and the level. In other words, as shown in the middle drawing of Figure 1.4, every point on the *Y*-axis (level) is meaningful; the level is treated as a continuous variable. On the other hand, a binary relationship is the foundation of the digital methodology. As illustrated on the right-hand side of Figure 1.4, level is only distinguished by two regions: high and low. Other measurements of level have no meaning. Information is expressed only through these two values. For example, the snapshot of level at moment t_2 is invalid from the digital circuit designer's point of view.

The human body is naturally equipped with the capability of sensing the flow-of-time. To coordinate various events in our lives, however, the flow-of-time needs to be quantified and explicitly expressed in a certain way. Mechanical vibration serves this purpose as evidenced by the billions of watches and clocks used in today's society. Since level (the flow of electrons) is the only physical property that can be sensed by an electronic device, the flow-of-time in the electrical world must be quantified through this medium. In fact, in the electrical world, the flow-of-time shows its form by crossing a predefined threshold (as will be explained next). This is, in general, also a type of vibration—electrical oscillation.

In the electrical world, at the device level, the basic building elements are the transistor, diode, resistor, capacitor, inductor, etc. All these devices interact with each other through voltage and current (more precisely, through electrons). By manipulating the voltage/current magnitude, information is processed. Behind the scenes, the supporting mechanism is the fact that voltage/current magnitude is proportional to the number of electrons flowing through these devices. At the circuit level, information can be treated in two different ways: digital and analog. A digital circuit uses two states—on and off—represented by 0 and 1. In an analog circuit, information is established by a proportional relationship. At the functional level, information is collected by a sensing circuit, manipulated by a processing circuit (amplification/

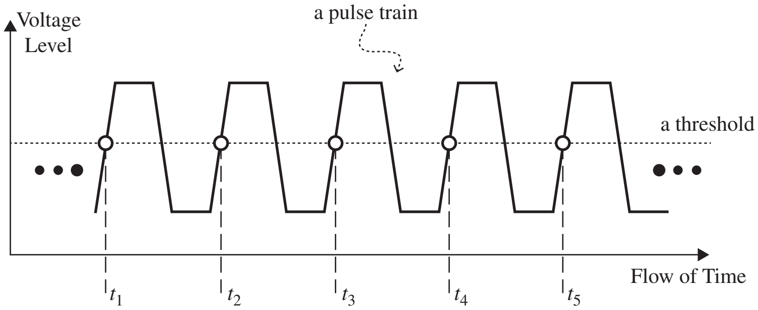

FIGURE 1.5 Using voltage-crossing-a-threshold and indexing to create the sense-of-time.

attenuation, screening/filtering, and logical/arithmetic operation), transformed between digital and analog formats by a converter circuit, and applied to an actuator circuit carrying out the action. At the architectural level, the information processing task can be classified as computation and communication.

From an operational perspective, the electronic system carries out its tasks through events. This is similar to our social world: Activities are composed of individual events, where tasks are accomplished through making events occur in an orderly fashion, that is, doing things in sequence. This requires a timekeeping mechanism—thus the invention of the clock (and later the watch). Similarly, for an electronic system to be useful, its events have to be organized by a timekeeper. By taking advantage of electrical devices' natural capability of differentiating voltage level, a marker system using voltage-crossing-a-threshold is created to indirectly mark the moments in time. The flow-of-time is created by indexing the markers. In this approach, a train of electrical pulses is established. During the process of the level oscillating between high and low states, a moment in the flow-of-time can be identified within each low-to-high (or high-to-low) transition. These moments are recorded and indexed by numbers, resulting in $t_1, t_2, t_3, \ldots$, as shown in Figure 1.5. These markers are the references for other functional events in the electronic system. This special train of pulses is termed a clock signal. Each individual pulse (a complete high-to-low or low-to-high cycle) is termed a clock cycle, which is identifiable by its index number. Mathematically, the most important requirement (actually the only requirement) imposed on this clock pulse train is that these moments of time $(t_1, t_2, t_3, \ldots)$ must be predictable. The accuracy in predicting them must be made as good as possible. The reason is that they are the markers used for coordinating other events. Any error in determining the locations of these moments can lead to a reduction in the effectiveness of organizing other activities. The larger the uncertainty of these locations (which is called clock noise or jitter), the less effective the pulse train is as a timing marker.

Clock frequency is defined as the number of pulses within a time window of one *second* (the second is defined from the atomic clock, based on the fundamental properties of nature [NIS09, Jon00]). To create a clock signal with a precise and stable frequency, the number of pulses has to be well controlled. This is however extremely difficult since electrical devices do not bear sense-of-time naturally. External help is

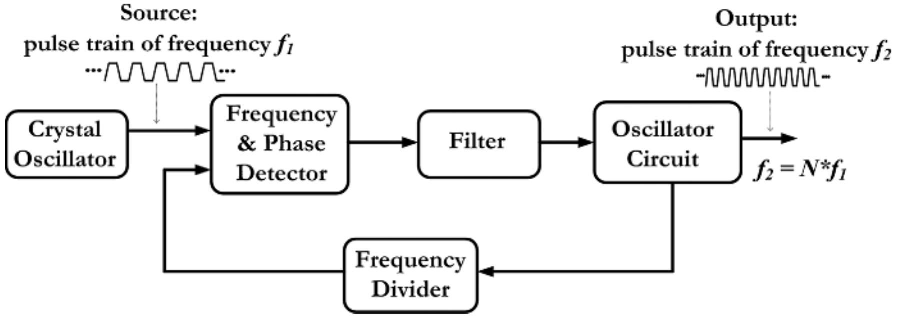

FIGURE 1.6 Using PLL to generate other frequencies from a reference frequency.

needed. Traditionally, a quartz crystal rock has been chosen to serve this purpose due to its high-precision mechanical vibration when a voltage is applied to it. An electrical supporting circuit is built around the crystal to convert the highly accurate mechanical vibrations to electrical pulses. The resulting circuit is called a crystal oscillator. For several decades, it has been the timing reference for almost every electronic system [Ger67, Vit88, Wal95].

Although highly accurate, the frequency of a crystal oscillator is fixed at a single value. As a result, the choice of timing marker is limited. This restrains the flexibility in the design of the electronic system. To cope with this difficulty, a special circuit called a phase-locked loop (PLL) has been created. Relying on negative feedback, the PLL utilizes the mechanism of *compare-then-correct* to create pulse trains of other frequencies using the fixed-frequency crystal oscillator as a reference. Its principal structure is depicted in Figure 1.6. The PLL is one of the foundational circuits in circuit design. It can be found in almost every modern chip. However, the solution is not perfect. Due to the feedback used, the PLL output has two problems: (1) The frequency cannot be arbitrarily generated (only some multiples of the reference frequency are available) and (2) switching from one frequency to another takes a long time. These two issues were not of high concern for system architects in the past when there were many other more immediate problems. However, to improve the electronic system's processing efficiency further, now is the time to reinvestigate them in depth.

From the clocking principle illustrated in Figure 1.5, it can be understood that the operable "time" inside an electronic system is realized by a frequency source (a pulse train at a certain frequency) followed by a counter. The counter, which is driven by this frequency source, records the index of each pulse as the "physical time" flows forward. Together, a clock source of a certain frequency and a counter make up a time scale. This mechanism is depicted on the left in Figure 1.7. As shown, the time inside the electronic system is represented by cycles that have elapsed since the start of counting. "Time (cycle)" refers to the integration of frequency over time. The value of the frequency can be derived by taking the first derivative of the time (cycle). Consequently, as shown on the right-hand side, noise on the frequency

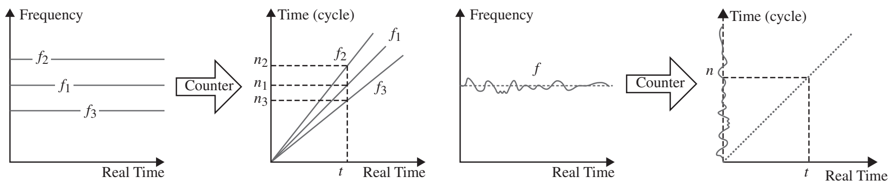

FIGURE 1.7 A time scale is a clock source of a fixed frequency plus a counter (left); noise in frequency source leads to error in timekeeping (right).

source (instability of its frequency) will be converted into error in time (cycle). Several important observations can be made regarding the relationship between time (cycle) and frequency:

1. **Time Granularity** Time granularity is inversely proportional to the value of frequency. In other words, the higher the frequency, the finer the resolution in time will be.
2. **Frequency Granularity and Time Scale** Having more frequencies available from a clock source leads to more choices of time scales. The number of choice for the time scale depends on the frequency granularity of the clock source.
3. **Change of Time Scale** The switching speed from one time scale to another depends on how fast the frequency can be changed from one to another by the clock source.

The time scale is used to control the pace of the operation inside an electronic system. It indicates the effectiveness of a system to process information. On the other hand, the power consumed by an electronic system is directly related to the time scale chosen. For this reason, the time scale (and thus frequency) is one of the most important factors in electronic system design.

1.4 ALL MICROELECTRONIC SYSTEMS ARE FREQUENCY DRIVEN

An electronic system is used for processing information. Tasks included are collecting input information from an external environment, processing the collected information, and sending out the processed information to the external environment. These three functional blocks of input interface, digital processing, and output interface can be realized by individual chips or by a variety of functional blocks in a single SoC (System-on-a-Chip). Large or small, all electronic systems are driven by clocks of various frequencies. This fact is graphically depicted in Figure 1.8.

In the social world, information takes a continuous form. It exists in every moment in the flow-of-time. For information to be processed by an electronic system which does not itself have a sense-of-time, oftentimes information is sliced into pieces by a clocking mechanism (the action of sample and hold). Figure 1.9 shows a high-level

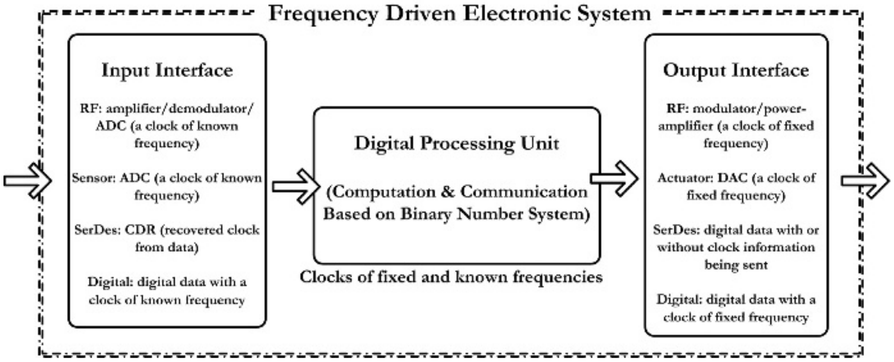

FIGURE 1.8 Electronic system is driven by clocks of various frequencies.

abstract view of how information is treated in an electronic system. After slicing, information is indexed and quantized through the use of numbers. In the input interface of Figure 1.8, for radio frequency (RF) and sensor applications, the slicing is done through an ADC (analog-to-digital converter). For SerDes and digital input cases, the input information is already in the sliced format (by previous processing units). On the output side, the processed information can be sent out in either sliced or continuous format. The processing unit between the input and output interfaces is used to manipulate the received information and consequently to create new information. This task can be classified into two subtasks of *computation* and *communication*. Computation includes logical and arithmetic operations. Communication is the action of moving data among interacting parties. The backbone of both computation and communication is the clock.

In modern systems, there can be hundreds of clock signals operating in a chip simultaneously to achieve sophisticated functions. Using the illustration in Figure 1.5, all clock signals are mathematically the same except one attribute for their identification: *the number of pulses existing in the time frame of one second*. This is termed the *clock frequency*. In the generic system of Figure 1.8, the clocks have unique frequencies that can differ from each other in large or small degrees. From this perspective, all electronic systems can be characterized as clock-driven systems. In a more abstract view, *an electronic system is a frequency-driven system*.

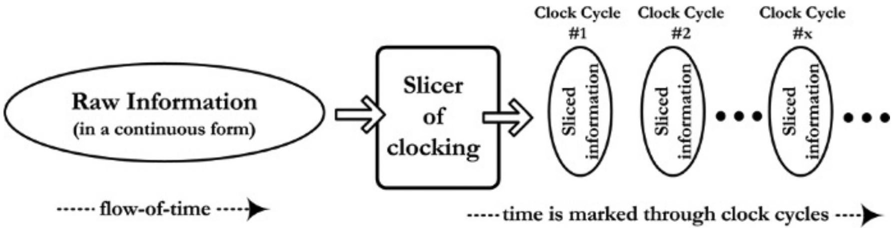

FIGURE 1.9 Information is sliced into pieces through clocking.

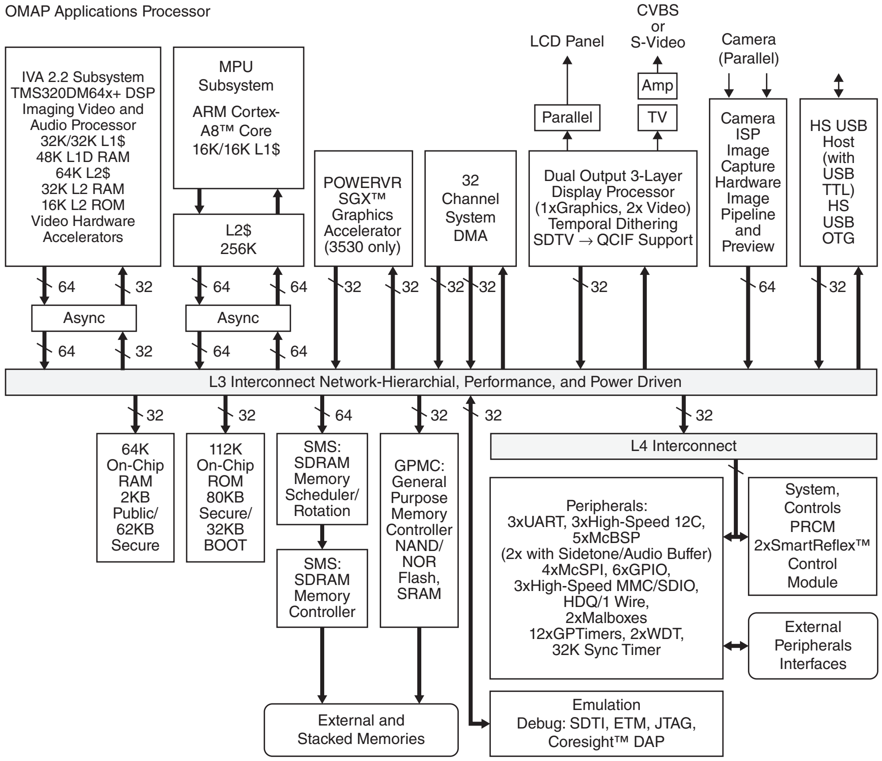

FIGURE 1.10 Video processor OMAP3530/25 system block diagram: a system of many functions integrated on-chip [Oma09]. Courtesy Texas Instruments Inc.

Figure 1.10 is an example of a very large scale integrated (VLSI) system. It is an Open Multimedia Application Platform (OMAP) processor which has several different types of processors on-chip [Oma09]. The core processor is ARM Cortex-A8; the DSP processor is TMS320DM64x+DSP. There is also a graphic accelerator POWER VR SGX. In addition to the processors, many other functions are integrated on-chip as shown, such as memory systems and various peripherals. All these functional blocks are running at their optimum frequencies, for example, AMR at 720 MHz, C64x DSP at 520 MHz, and USB at 48 MHz. The chip's frequency plan is very complex, as shown in Figure 1.11. A dedicated clock manager system is created to generate the various clock frequencies required. From this example, the message is very clear: An electronic system is frequency driven.

There are two trends in designing today and tomorrow's electronic systems: integrating more functional blocks into a system and increasing clock frequency (for faster information processing). These trends have an impact on almost all aspects of chip design. From the clocking point of view, they present two challenges. The first one is the efficiency in data communication between functional blocks that are often running at different frequencies: *the communication challenge in the environment of*

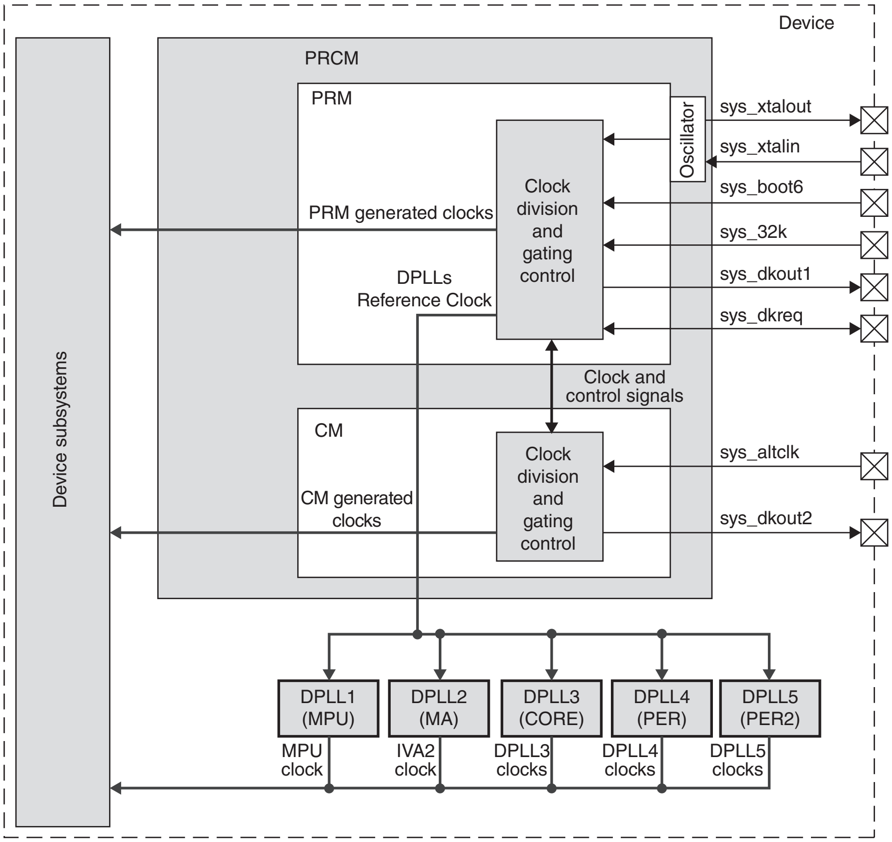

FIGURE 1.11 Video processor OMAP3530/25 clock manager for generating various clock signals of different frequencies [Oma09]. Courtesy Texas Instruments Inc.

heterogeneous clocking. As illustrated on the left in Figure 1.12, there could be many blocks in a large SoC system that perform different functions. Very likely, each will have its own optimum operating clock frequency (i.e., the best time scale suitable for the task it performs). When data exchange between blocks is required, the difference in their clock frequencies presents a major design challenge. This issue is typically handled by using a first-in-first-out (FIFO) memory in between for temporarily storing data. Depending on the magnitude of the frequency difference, the size (and thus the cost) of the memory could be very large. If an adaptive clock generator with the capability of arbitrary frequency generation and fast frequency switching is available, the severity of this problem can be mitigated. This issue will be discussed in more detail in later chapters.

The second problem is the *electromagnetic interference (EMI) associated with a high-frequency clock signal*. A high-frequency clock (fine time scale) enables fast information processing. It has, however, undesirable side effects on the electronic devices operating in its surrounding environment. EMI reduction requires a flexible

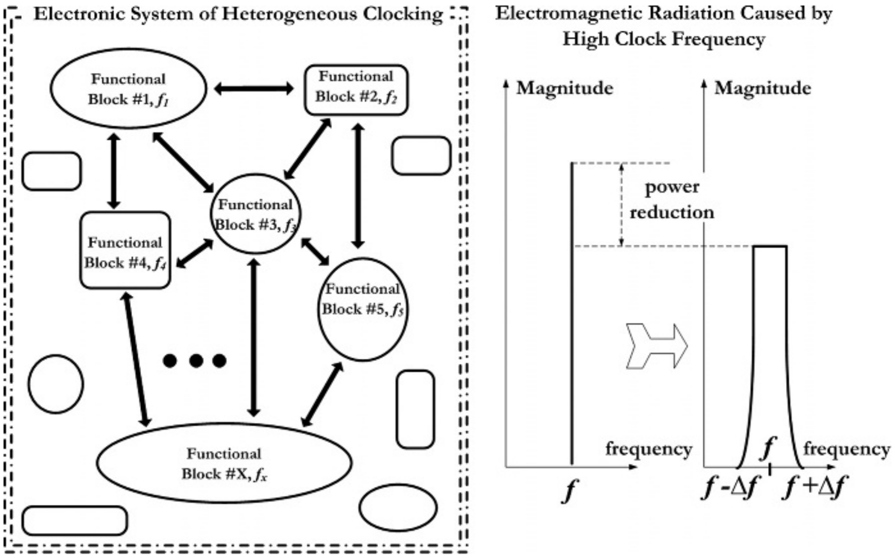

FIGURE 1.12 Multiple functional blocks of different operating frequencies leads to heterogeneous clocking (left); strong EMI of high clock frequency calls for its reduction (right).

clock generator capable of generating many frequencies. As shown on the right-hand side of Figure 1.12, by spreading a single clock frequency to a group of frequencies, the power radiated by the clock generator can be reduced significantly. This issue will also be addressed in depth in a later chapter.

If we move from the chip level to a higher level, today's electronic system design presents an even more challenging problem in terms of timekeeping: *establishing a common view of time among networked systems*. As illustrated on the left in Figure 1.13, the majority of today's electronic devices are networked [e.g., the latest trend of Internet of Things (IoT)]. To create a temporal sequence in a networked environment so that events can occur in a sequential order, a common view of time needs to be established. The drawing on the right illustrates the method of generating *time* (time

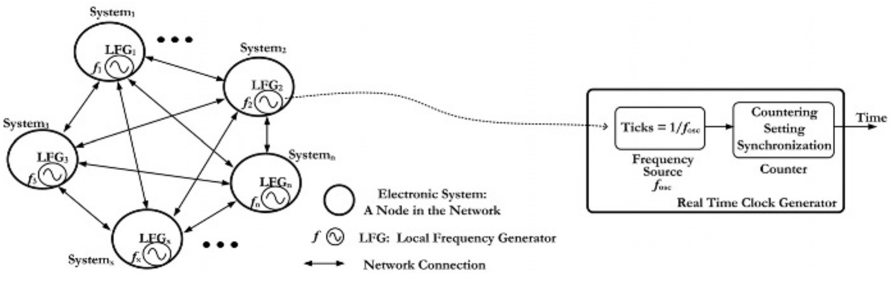

FIGURE 1.13 Future systems are networked: calling for a common view of time among all systems (left); method of generating *time* in each system (right).

here refers to time as used in our daily life: days, hours, minutes, seconds). A frequency source is used to generate ticks, which are then used to drive a counting mechanism. The counting mechanism is responsible for generating the real time locally in each system. It is also responsible for synchronizing its time with that of the rest of the systems in the network. Further, in some applications, it is synchronized with an external time reference, such as the UTC (Coordinated Universal Time) [All97].

In practice, each system in the network has its own clock generator [local frequency generator (LFG)] with a unique oscillation frequency. Usually, these frequencies are not matched perfectly among those devices in the networked system. As a consequence, the time flows among these systems will be out of synchronization (due to drift) even if they are initially set to the same time point. To coordinate time-sensitive events within the network, these timekeepers must be synchronized. The standard protocols NTP (Network Time Protocol) and PTP (Precision Time Protocol, IEEE 1588) are the two best-known examples for this purpose [Fer13]. NTP carries out its time synchronization task at the software level; the best result achieved is in the range of tens of milliseconds. PTP refines the synchronization mechanism and, consequently, the synchronization precision is improved to the microsecond range. Both NTP and PTP, however, address the time synchronization problem in algorithm and architecture level and do not consider hardware implementation in great detail. To improve the synchronization precision further (such as to the nanosecond range), an effective way is to refine the time and frequency granularity at the hardware level. When nanosecond network time synchronization is achieved, countless application possibilities will emerge that can significantly improve the network's information processing efficiency.

In summary, all electronic systems are frequency driven. Modern electronic system design calls for a new clock source that is flexible in its ability to generate frequency. This is a new requirement commanded by the ever-increasing complexity of modern systems. It is a new challenge. It is also a new opportunity.

1.5 A NEW KID IN TOWN: THE CLOCK ARCHITECT

The modern large SoC has passed the milestone of one billion transistors on a chip. Designing such a complex entity requires a group of highly skilled professionals. Among them, without question, the chip architect plays a leading role. His or her job description includes following the market trend, understanding customer requirements, being familiar with competitors' products, and designing a product that is appropriately aligned with his or her company's marketing strategy. His or her must-have knowledge and skill are computer architecture and communication protocol. He or she is also required to be familiar with various IPs (Intellectual Property) available on the market. His or her primary goal is to design a product that is computation and communication efficient (using minimum energy to perform a given task) and, more importantly, is right for the market.

When the target product is gradually moved from the design stage to the implementation stage, however, the knowledge and skill of a chip architect are probably no longer adequate. The knowledge and skill needed at this stage are related to electrical engineering (rather than computer engineering). The focus is shifted from "defining what we want in this chip" to "how to realize them by creating various events using on/off switching activities." Since the clock signal is the conductor of this symphony of events, this signal must be treated with extreme care. Further, since the creation of a clock signal is closely tied to the use of transistors and metals, the clock signal designer must have expertise in transistor level circuit design. This leads to a new type of IC design professional: the clock architect.

The clock architect is neither a chip architect nor a PLL designer. He or she must be able to use the clock signal to organize the large amount of events occurring in the chip. Given the tasks demanded from the chip architect, he or she must fulfill them using the least amount of resources in terms of power consumption and silicon area. By appropriately using the tools of clock frequency, clock frequency range, clock frequency granularity (resolution), and clock frequency switching speed, a good clock architect can make the difference between a successful product and a failed product.

The clock architect is not the integration engineer (e.g., the clock tree synthesizer) whose main focus is "how to implement the clock plan using silicon and metal". The clock architect stands at a higher level of planning the frequency game. In the past, when the clock generator could only produce a few frequencies and the switching between frequencies was slow, there was not much room for the clock architect to make a significant difference. However, with the small frequency granularity and fast frequency switching of today's clock generator, frequency planning becomes a major piece of design work that requires dedicated attention.

With the features of small frequency granularity and fast frequency switching becoming a reality, the clock architect is provided with the capability of programming the "clock frequency" of a clock generator just as the software programmer programs the instruction set of a processor. *In short, the clock architect deals with frequency.*

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