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SiP Design and Simulation Platform

1.1 From Package to SiP

Package is the term commonly used to refer to the protective housing and related accessories of a single Integrated Circuit (IC) bare chip cut down from wafer; it is mainly used to protect the silicon chips. Because silicon chips are very fragile, even very fine dust or water droplets can destroy their functionality, so it is necessary to protect IC chips with package. Another feature of package is to amplify the scale; because the chip itself is usually very small, the scale is increased by package, making it easier to use in subsequent board-level PCB systems. The third function of package is electrical connection: via package, the chip exchanges information with the outside world.

Depending on the process or material, package product is usually divided into three types: plastic package, ceramic package and metal package. Plastic package is mainly used in commercial products and has the advantage of low cost, but the thermal dissipation, stability and air tightness are relatively poor. Ceramic package and metal package are suitable for industrial products as well as in the aerospace, military and other harsh fields, have excellent heat dissipation and air tightness, and high reliability. Meanwhile, ceramic and metal package have the advantage that they can be disassembled easily for fault finding and problem "zeroing". Figure 1.1 shows the three different kinds of package.

IC package typically includes DIP, QFP, BGA, etc. With improvements in technology, packaging technology developed rapidly, along the DIP→QFP→BGA→CSP direction. Package density is becoming higher, scale is increasing quickly, and number of pins is growing fast. Single-chip package has not met the requirements of system design; packaging products are developing from small scale to large scale, from single-chip package to multi-chip package.

Multi-chip package has attracted more and more attention, with most directed to System in Package (SiP).

SiP, as the name suggests, refers to the integration of a system in a package body. Typically, this system requires encapsulating multiple chips able to complete a specific task, such as system-level package-integrated CPU, DRAM, Flash and other IC chips. At present, with the development of package technology, SiP has gradually developed to 3D stacked-chip package.

SiP System-in-Package Design and Simulation: Mentor EE Flow Advanced Design Guide,
First Edition. Suny Li (Li Yang).

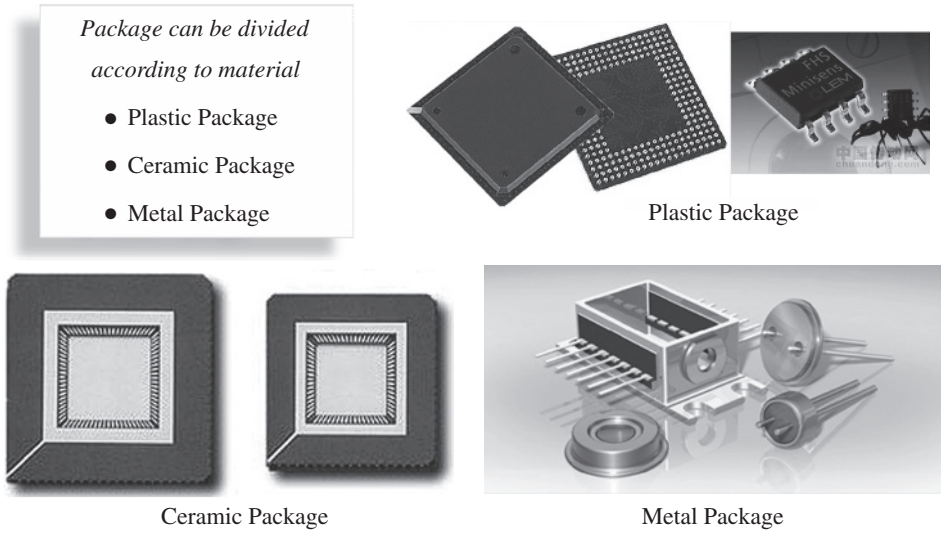


Figure 1.1 Three different kinds of package.

Multi-chip package is not a new concept; MCM (Multi-Chip Module) technology has been popular for many years, and has been widely used in specific areas such as the military, aerospace and aviation.

MCM is a kind of package; as opposed to SiP, small chips are usually used in MCM, which can accomplish relatively simple functions compared to SiP. In MCM the chips are usually in 2D layout.

The bare chips used in MCM usually have a single function, and are smaller and simple. MCM uses 2D flat package, which also means that it is not easy to increase the capability of MCM, it is difficult to shrink in size, and there are other disadvantages.

SiP combines the advantages of both MCM and large-scale IC package.

SiP package is specifically intended for large-scale, multi-chip, 3D packaging. Its stereoscopic 3D nature is mainly reflected in the two aspects of chip stacking and substrate cavity. Figure 1.2 shows the process of IC package and MCM evolving to SiP.

The new trend in SiP technology development is that traditional package design by IC chip manufacturers is being gradually transformed to a new arrangement whereby the

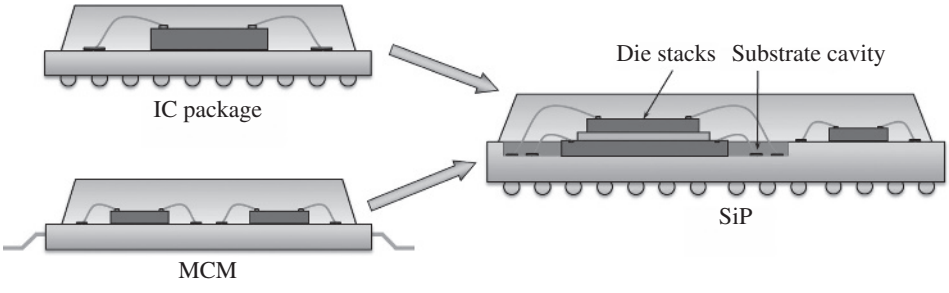


Figure 1.2 Evolution from IC package and MCM to SiP.

system user is beginning to consider and design the package. In the past, chip manufacturers usually packaged chips and then delivered them to the user.

Now, with the development of SiP technology, miniaturization and low-power design requirements, more and more system users want to get the bare dies, and build their system based on bare dies and packaging.

It follows that market demand for bare chips will greatly increase, as more and more designers want to know how to get the bare chips.

As these demands continue to grow, traditional IC agents will continue to expand their bare chips business in order to meet the growing demands of the market.

If the demand does not reach a certain number, orders for bare chips from IC manufacturer are usually made via agents. There will be some delay for the customer. So, the SiP designer, in the early stages of project, should fully consider the order channels and order cycles. When the market demand for bare chips reaches a certain level, and when there is a continuing demand, bare chips agents would consider increasing their inventories to meet customer needs.

The bare chip market is developing, and is driven by the rapidly growing demand for SiP technology. In turn, developments in the bare chip market promote the application and popularity of SiP technology.

Because SiP or package design is gradually shifting from the IC chip manufacturer to the system user and system users are most concerned with system design, the collaboration of package design and system design will also become increasingly important. Package design itself will become a key link to system design, with designers required to realize the function of the entire system in a unified platform. Figure 1.3 shows the relationship between IC bare chips, SiP package and the PCB board-level system.

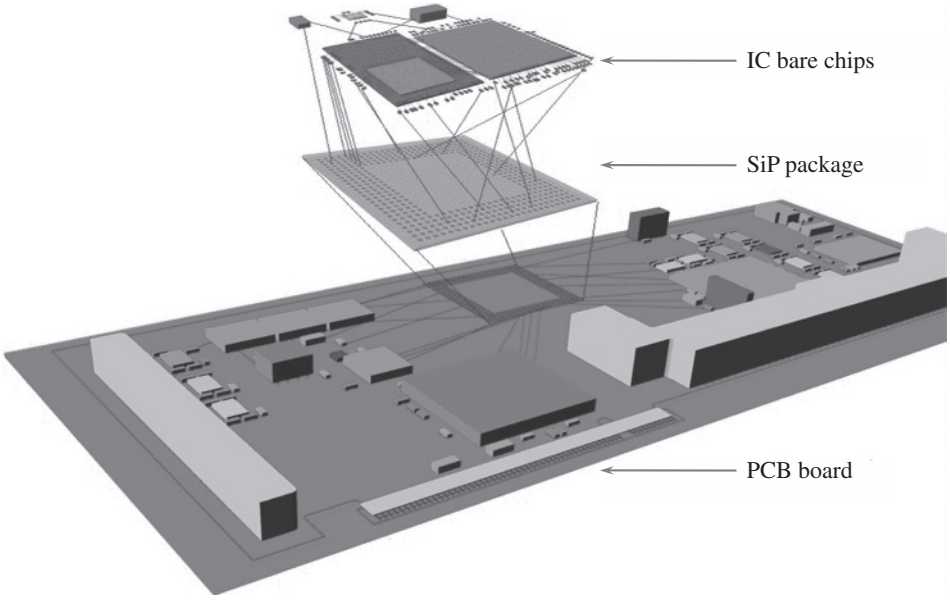


Figure 1.3 The relationship between IC bare chips, SiP package and the PCB board-level system.

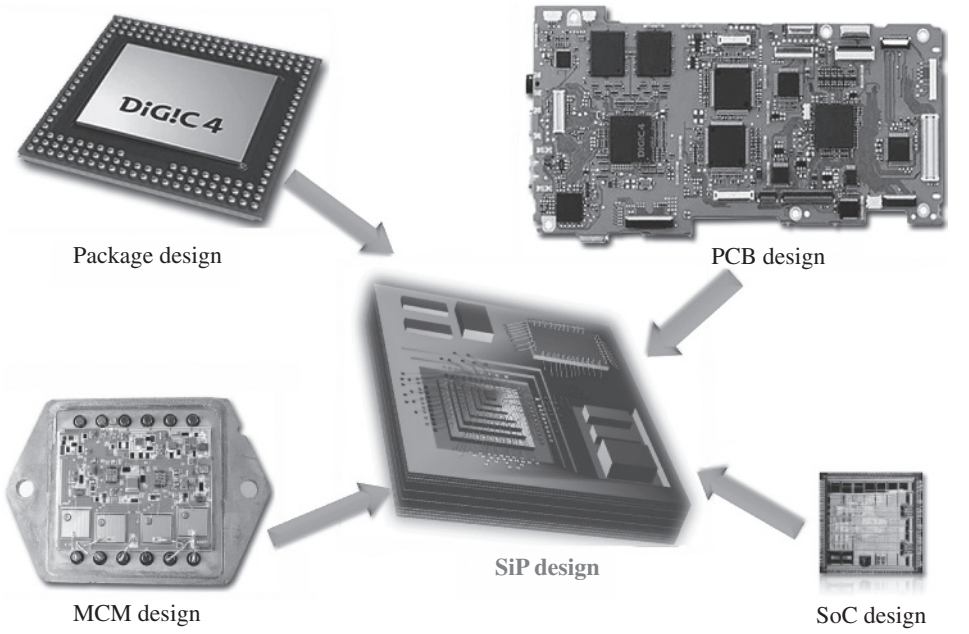


Figure 1.4 SiP is receiving attention from a wide range of areas.

SiP is getting much attention, not only from traditional package designers, but also from traditional MCM designers and PCB designers, and even SoC designers have begun to keep a watchful eye on SiP. Refer to Figure 1.4.

As compared with traditional package, SiP is a system-level package, and can accomplish system functions independently.

Compared with MCM, SiP is a 3D multi-chip package, with the 3D embodied in chip stacks and substrate cavities, while the scale and function of SiP are also greatly increased compared to MCM.

Compared with PCB, the advantage of SiP technology is mainly in terms of miniaturization, low power consumption and high performance. To realize the same function as PCB, SiP only needs about 10–20% of the area and 40% of the power of a corresponding PCB, and also has a relatively large performance improvement over PCB.

Compared with SoC, the advantage of SiP is mainly embodied in short cycles, low cost and ease of success. To achieve the same function, only 10–20% of the development time required for SoC is needed for SiP, the cost of SiP development is typically about 10–15% that of SoC, and SiP is more likely to succeed. Therefore, SiP is often seen as a low-cost, short-term, alternative solution to SoC by many users.

Often, SiP is a forerunner at the start of an SoC project, used to make a rapid and low-cost SiP product. When SiP is successful, giving some initial results on the project, and receiving recognition and support from all, the project then shifts to SoC research and development.

With increasing demand for high-performance, high-speed and versatile design, designers are more concerned about signal integrity, power integrity, crosstalk, EMC/EMI, and

functional simulation and verification. A common solution is to use simulation tools to assist in the design flow; HyperLynx SI/PI/Thermal, HyperLynx DRC, HyperLynx 3DEM solver and HyperLynx Analog are commonly used simulation tools.

For high-density, small-size and low-power-consumption design, designers require design rules such as trace width and clearance, smaller passive components, for example, resistors and capacitors, HDI (High Density Interconnection) technology, and buried and blind via technology.

Moreover, design software and product technics support the use of many passive components embedded in the substrate; this is called EP (Embedded Passive) technology, and consists of bare dies mounted directly on the circuit board; this is called COB (Chip On Board) technology.

With the application and maturity of these technologies, PCB system designers began to focus on a new technology, which is the integration of all these technologies: this is SiP technology.

In contrast with PCB, to realize the same function SiP requires only 10%~20% area and 40% power consumption of original PCB; refer to Figure 1.5.

1.2 The Development of Mentor SiP Design Technology

The Mentor company is the largest EDA software supplier of PCB board-level system design in the world. Mentor provides the most advanced solutions for electronics companies and research institutions worldwide.

Mentor has held the absolute leading position in the PCB design market for many years. Statistical data from the global PCB design market (third-party statistics) show that Mentor has more than 50% of the market share, dominating the market and far outstripping competitors.

In May 2009, based on version EE2007.5, Mentor launched the Expedition advanced packaging bundle (Expedition AdvPkg) to support SiP design. Before launching this module, Mentor had no tool for package or SiP design specifically; however, Mentor's related technology can be traced back a few decades.

First, let us recall the processes of the Mentor package and SiP technology accumulation and development.

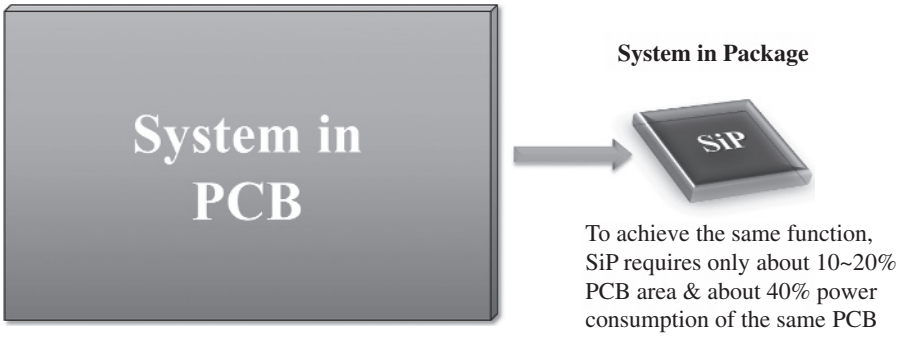


Figure 1.5 Size and power consumption comparison between PCB and SiP.

BoardStation, also called EN (ENTERPRISE), is an excellent Mentor PCB board-level system design platform, mainly used by high-end PCB designers.

In BoardStation there is a module called Hybrid Station, mainly used in hybrid circuits and MCM design, which has a wide range of applications in MCM and mixed-signal circuit design. At present, there are still a number of companies and research institutes worldwide which use this design platform for their projects.

In the 1990s, Mentor acquired DDE's Supermax ECAD. Supermax ECAD is an excellent tool, used mainly for embedded passive, MCM, Hybrid IC package and RF design. As multi-functional layout software, the distinctive feature of Supermax ECAD is the ability to support RF, EP, package and MCM design.

Mentor developed these technologies, and gradually integrated and consolidated them into a new software product: Expedition Enterprise Flow, EE Flow for short.

With the development of technology and design needs, Mentor is gradually shifting its high-end PCB board-level design platform, focused on Expedition Enterprise Flow; the latest version is EE7.9.5.

At the same time, Expedition Enterprise also continues to absorb advanced technology and functionality from other products, covering new areas of design. The Expedition AdvPkg bundle is the new product, which incorporates many of Mentor's advantages in relation to MCM, hybrid circuits, RF, embedded passive components (EP) and other technologies.

Therefore, we can say that while the Expedition AdvPkg bundle is a relatively new product, the technology is very mature, and its technological development can be traced back to the 20th century.

In Figure 1.6, we can see the inheritance and development process of the Mentor SiP design platform and advanced packaging technology.

1.3 The Mentor SiP Design and Simulation Platform

1.3.1 SiP Platform Introduction

Mentor provides a comprehensive SiP/MCM, advanced package and PCB design and simulation platform, as shown in Figure 1.7.

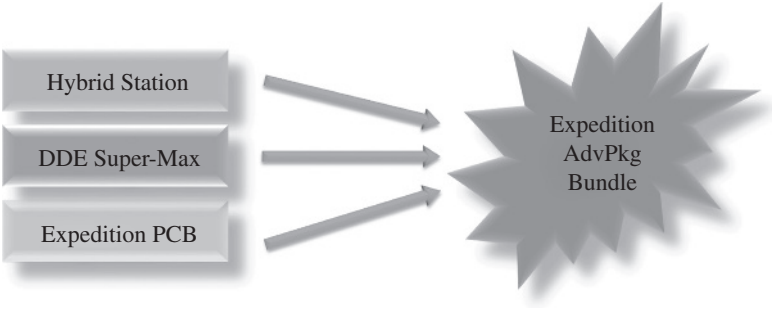


Figure 1.6 Development of the Mentor SiP platform.

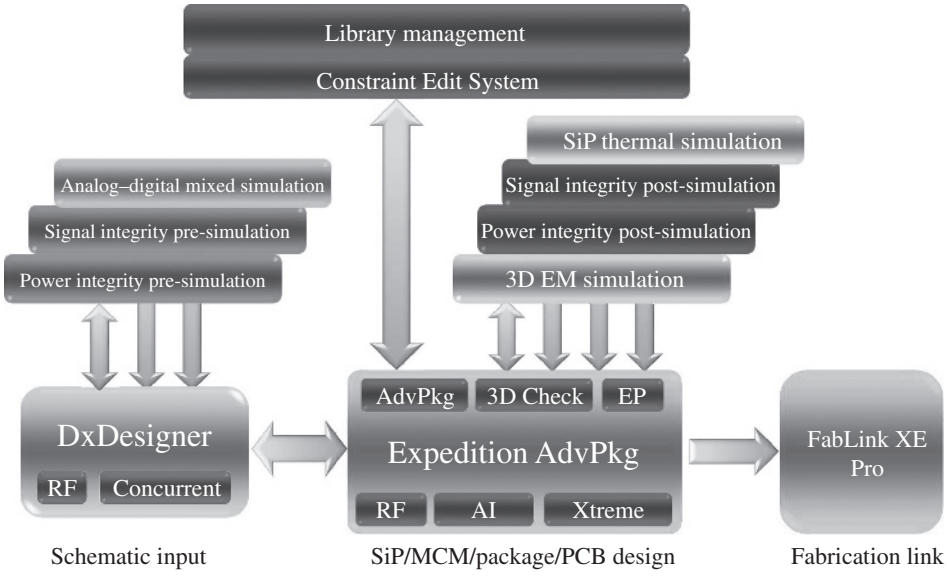


Figure 1.7 Mentor SiP/MCM/advanced package/PCB design and simulation platform.

For SiP design needs, the Expedition AdvPkg bundle comprises AdvPkg, 3D Check, EP, RF and AI (Advanced Interconnection), as well as FabLink XE Pro modules, specialized support for SiP/MCM, advanced packaging design, data output and validation.

Meanwhile, for SiP simulation, Mentor offers the mixed digital–analog simulation tool HyperLynx Analog, the thermal simulation tool HyperLynx Thermal, the signal integrity analysis tool HyperLynx SI, the power integrity analysis tool HyperLynx PI, the 3D electromagnetic simulation tool HyperLynx 3D EM and the EMI/EMC check tool HyperLynx DRC.

Mentor's design and simulation flow for SiP/MCM and advanced package is a Windows-based software platform, compatible with both Linux and Solaris. Mentor EE Flow supported platforms and processors are shown in Figure 1.8.

System Requirements

Release EE 7.9.5 Supported Platforms and Processors

Linux RHEL 4 x86
Linux RHEL 4 x86-64
Linux RHEL 5 x86
Linux RHEL 5 x86-64
Linux RHEL 6 x86/x86-64
Linux SLES 10 x86
Linux SUSE 11 x86/x64
Solaris 10 UltraSPARC
Windows 7 x86/x64
Windows Server 2008 x86/x64
Windows Server2003 x86
Windows Vista x86/x64
Windows XP x86

Figure 1.8 Mentor EE Flow supported platforms and processors.

1.3.2 Schematic Input

DxDesigner is the schematic input tool in the SiP design platform.

In addition to conventional schematic, DxDesigner supports RF input, and its RF components library is synchronized with the Agilent ADS RF library.

In relation to the schematic design phase, DxDesigner is provided with a mixed-circuit simulation tool, to simulate the function of circuits, so as to ensure that "design is correct" from the outset.

Meanwhile, designers can also use the SI pre-simulation tool to do "what if" analysis of the signal integrity of the design, so as to determine the components selection, net topology planning, terminal-matching and substrate laminate structure parameters of the design.

Using the PI pre-simulation tool, designers can plan power plane partition, distribution of power nets, and the number and variety of decoupling capacitors in the schematic design phase, and reasonably control the power plane impedance.

In addition, DxDesigner supports concurrent schematic design for multiple people designing one schematic at the same time; it does not require any partitioning. This technology is especially important for large and complex projects.

1.3.3 Concurrent System Design

Because SiP design and PCB design were eventually carried out by system designers, collaborative design between them became closer and closer. Mentor was sensitive to this new trend, and developed collaborative design capabilities, which also became a key feature of Mentor tools.

As shown in Figure 1.9, multiple designs are managed in one project, including two SiP designs and one PCB board design; each design can be completed independently.

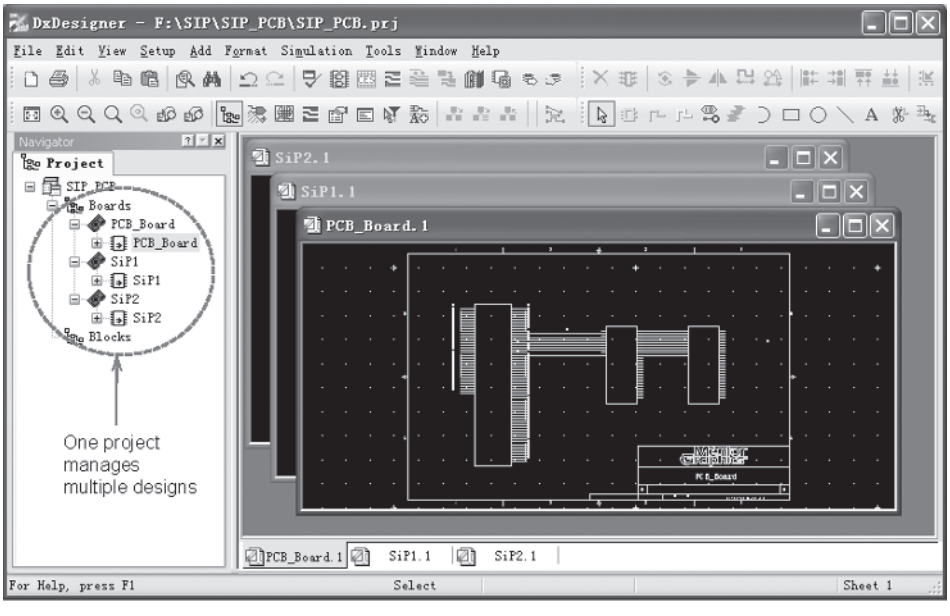


Figure 1.9 One project manages multiple designs, and realizes SiP and PCB collaborative design.

There is a mutual relationship between the three designs, because both SiPs are ultimately installed on the PCB board to work together.

This way of managing projects is more reasonable than having three separate designs, because in considering subsequent PCB system design, the pin assignment of SiP design can be optimized.

1.3.4 SiP Board Design

In the field of PCB board design, Mentor accounted for more than 50% of the global market share, far more than its competitors. Mentor extended its powerful advantages from PCB board design to the SiP design area; all the powerful features of PCB design are also used in SiP design.

Currently, layout is one of the core modules of SiP design. Mentor developed six core design features based on Expedition PCB, features which support the user with all kinds of needs in the SiP design procedure, as shown in Figure 1.10.

1) AdvPkg core design function

   AdvPkg(Advanced Packaging)core design function supports wire bonding and substrate cavity, with no level limit on IC chip stacks, and complex multi-step cavity design, as shown in Figure 1.11.

   AdvPkg also supports both automatic bonding of complex bond wire and automatic generation of power ring.

   Mentor bond wire models can be created using a variety of types of curve fitting, which are more accurate and closer to the actual bonding wire. These models can help designers improve design accuracy, thereby increasing product yield. The Mentor bond wire model is shown in Figure 1.12.

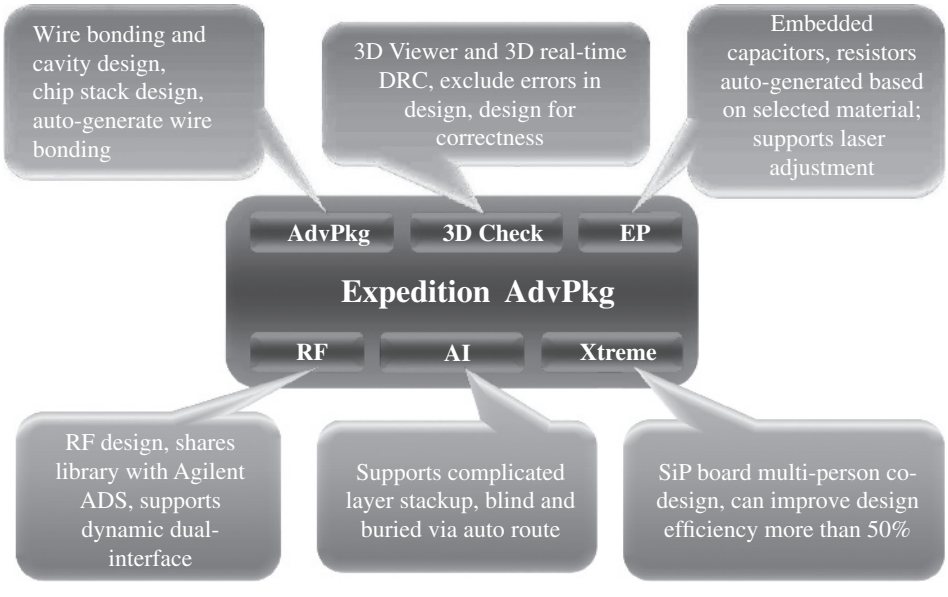


Figure 1.10 The six core design functions of Mentor SiP layout. *(See color plate section for the color representation of this figure.)*

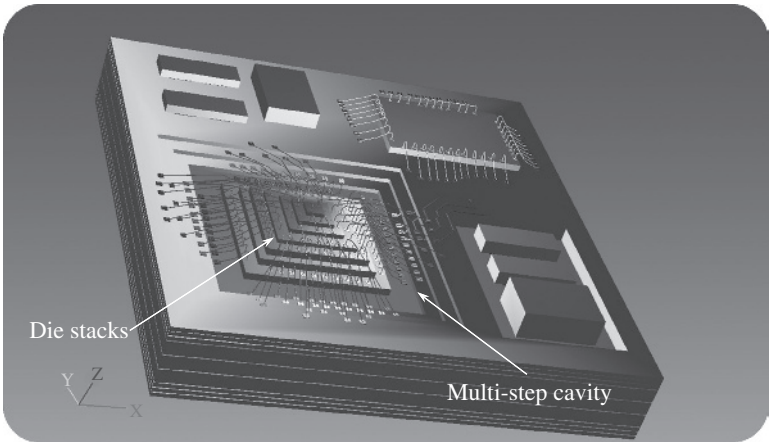


Figure 1.11 Chip stacks and multi-step cavity.

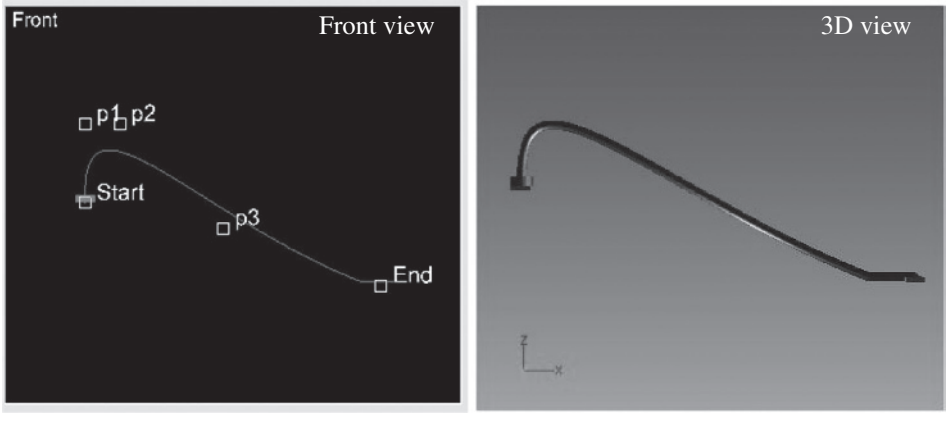


Figure 1.12 Mentor bond wire model.

2) 3D check function

The 3D check function supports 3D viewing and checking. It supports interactive 3D real-time DRC check of layout design; it allows checks of the chips, including bond wire and cavity, routing, copper, through-hole vias, buried and blind vias, buried resistors and capacitors, etc. By using 3D real-time DRC check, designers can avoid errors at design time, and ensure design is correct. This interactive 3D real-time DRC is shown in Figure 1.13.

Differing from the traditional method, the Mentor tool is better in relation to understanding the 3D design and check, and realizing 3D real-time inspection during the design process, to ensure design is correct.

In traditional methods, 3D checking is usually executed after design finish, and the designer needs additional tools for 3D inspection. It is similar to checking routing results in a Gerber browser. Typically, design finish is too late for this kind of post-processing 3D inspection, which can seriously affect the accuracy and efficiency of SiP design.

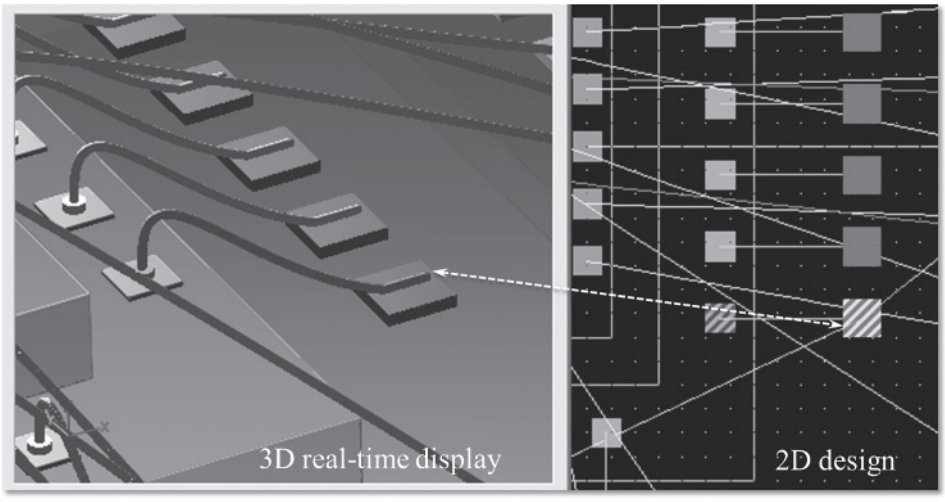


Figure 1.13 Interactive 3D real-time DRC.

3) EP function
   EP function supports embedded passive components, namely buried resistors and buried capacitors. This function supports the automatic integration of embedded resistors and capacitors.

   Depending on the selected material and resistance or capacitance parameters, required resistors or capacitors can be automatically integrated. Laser adjustment is also supported. Expedition supports multiple types of resistor and capacitor, as shown in Figure 1.14; the designer can use resistors and capacitors in any of the substrate layers. Using EP technology, we can greatly save on surface space and reduce the solder joints, thereby increasing the reliability of the design.
4) RF design function
   The RF(Radio Frequency)design function can realize RF circuit design. It supports RF parameter transfer between schematic and layout, and supports RF circuits passing through a dynamic link tool to and from ADS/AWR, as shown in Figure 1.15.

   The RF function can also meet some special design requirements in layout, such as gradient-width trace, stitched via and spiral inductor in power supply.
5) AI function
   The AI feature supports automatic routing of blind and buried vias in complex layer structures, and displays the layer numbers through which the buried or blind vias pass in layout, as shown in Figure 1.16.

   Intelligent AI automatic routing algorithms can greatly improve the routing completion rate and routing efficiency of the design.
6) Xtreme concurrent team design function
   The Xtreme concurrent team design function is suitable for complex SiP projects, with multiple designers concurrently designing one substrate board. It does not require any design segmentation, and provides design data updates to each designer in real-time. It greatly reduces the difficulty of design and alleviates the pressure on designers. Based on statistical data from real projects, Xtreme can improve design efficiency by as much as 50%.

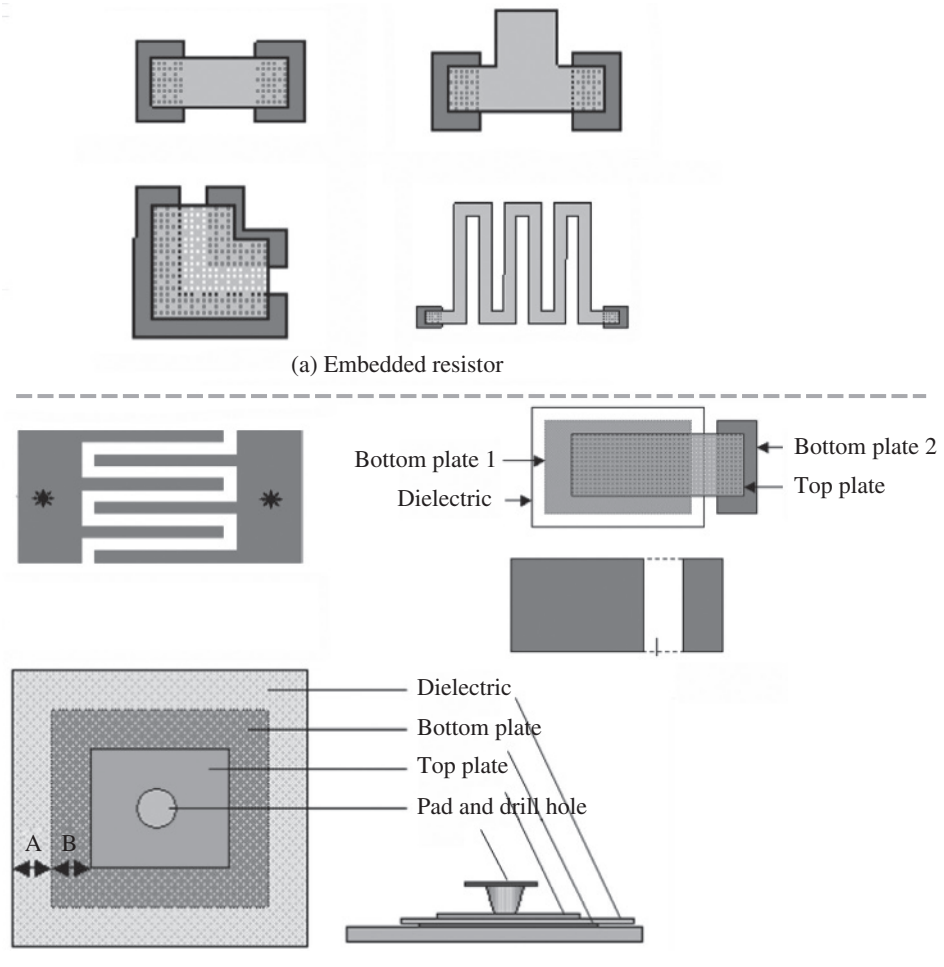


Figure 1.14 Expedition supports four kinds of EP resistor and three kinds of EP capacitor.

It is particularly important for complex SiP design, for which timeframes are very tight. Traditional methods generally do not have such a concurrent design function.

Figure 1.17 shows a diagrammatic sketch of Xtreme concurrent team design.

The SiP six core layout design functions are integrated into the design process of Expedition, belonging to the same environment as PCB design.

Therefore, all the advanced features of Expedition PCB can be used for SiP design, such as bus topology planning and bus routing, intelligent high-speed automatic routing, flexible routing, circuit copy, design reuse, and constraint management and other advanced features can be configured according to the design needs.

In addition to providing powerful layout features, Mentor provides a wide range of simulation and verification tools to support SiP design, including signal integrity, power integrity, thermal analysis, EMI/EMC, etc.

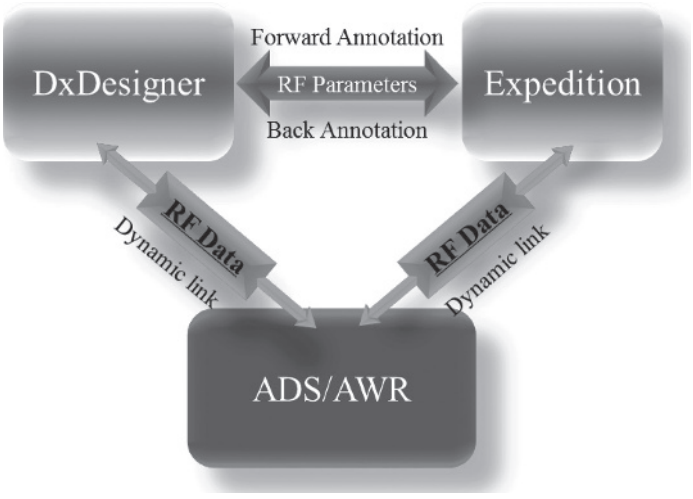


Figure 1.15 RF design data and RF parameter transfer.

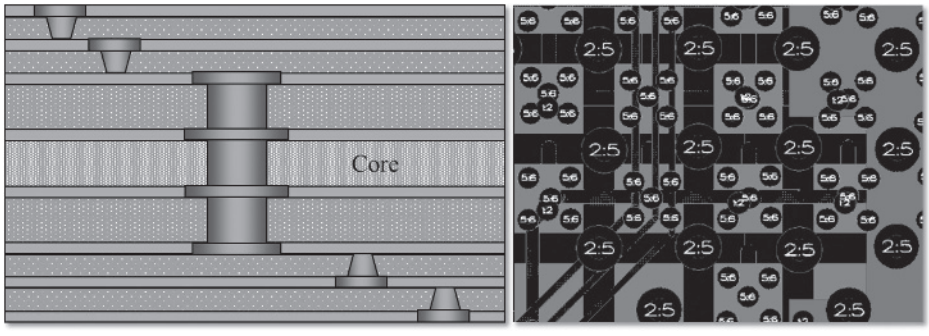


Figure 1.16 Blind and buried via setup and application.

1.3.5 Signal Integrity and Power Integrity Simulation

The HyperLynx SI signal integrity analysis tool supports SI, crosstalk and EMC simulation, using oscilloscope and spectrum analyzer displays. HyperLynx SI is embedded with FCC, CISPR and VCCI, which are three international EMC standards, and supports users in defining their own standards.

HyperLynx PI power integrity analysis tools support DC voltage, current density, AC decoupling and plane noise analysis. Waveform display is provided in two dimension and three dimension. Figure 1.18 shows screenshots of HyperLynx SI and PI.

1.3.6 Thermal Analysis

HyperLynx Thermal is a thermal analysis tool, allowing the designer to diagnose SiP heat-related issues at the early design stage. HyperLynx Thermal analyzes hot issues accurately and reliably, so as to avoid overheating or thermal failure in SiP products. Figure 1.19 shows a snapshot of one MCM's thermal analysis result comprising temperature and thermal gradient.

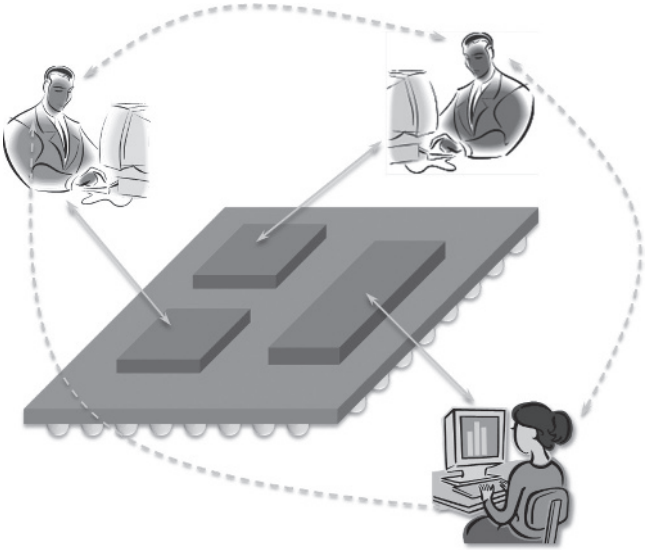


Figure 1.17 Sketch of Xtreme concurrent team design.

1.3.7 The Advantages of the Mentor SiP Design and Simulation Platform

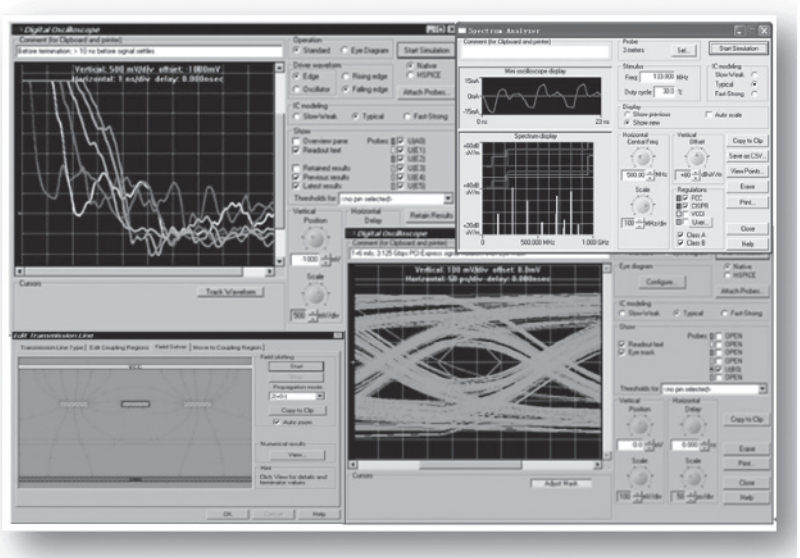
The Mentor SiP design and simulation platform supports SiP/MCM/package and traditional PCB design, with signal integrity, power integrity, EMC analysis and thermal analysis functions. Completeness of design, simulation and validation ensures high-quality completion of complex SiP projects.

1.3.7.1 Characteristics of Mentor SiP Design and Simulation Platform

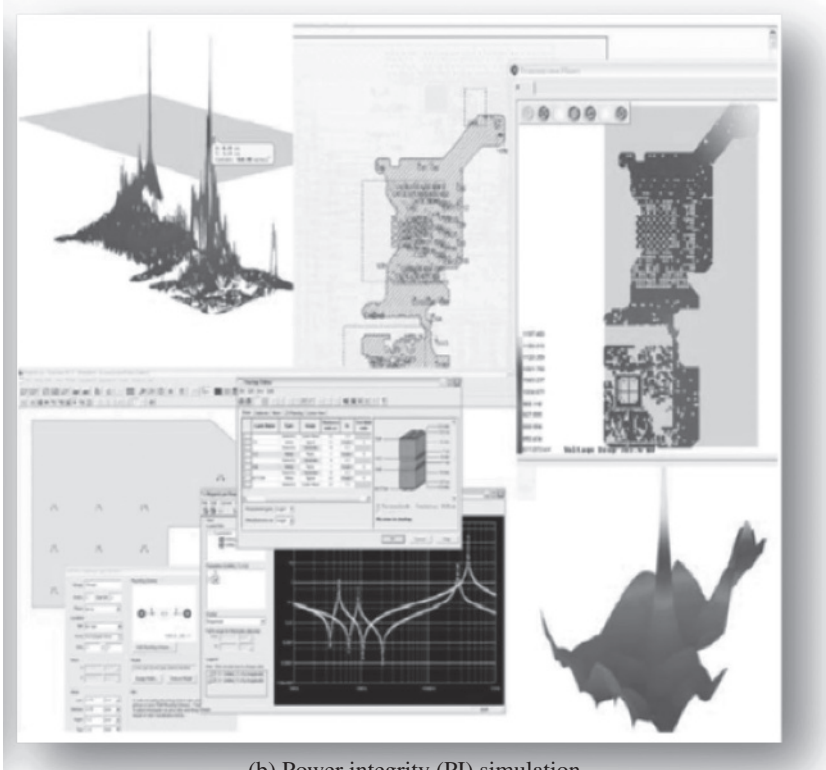
1) Comprehensive solution, design and simulation in a unified platform.
2) Real-time 3D DRC checks.
3) Intelligent automatic synthesized embedded passive components, graphical user interface, easy to use.
4) Intelligent blind and buried via automatic routing, no design layer and volume limit.
5) RF design-sharing libraries with ADS/AWR, dynamic data interface, easy to learn and use.
6) Thermal analysis tool for SiP/MCM/package.
7) Supports multi-player concurrent design, greatly improves efficiency.
8) Supports cooperative design with mechanical software, ECAD-MCAD real-time collaborative design.

1.3.7.2 Design Areas of Mentor SiP Design and Simulation Platform

a) Classification according to technology
   1) RF and wireless SiP design
   2) Digital SiP design
   3) General IC package design

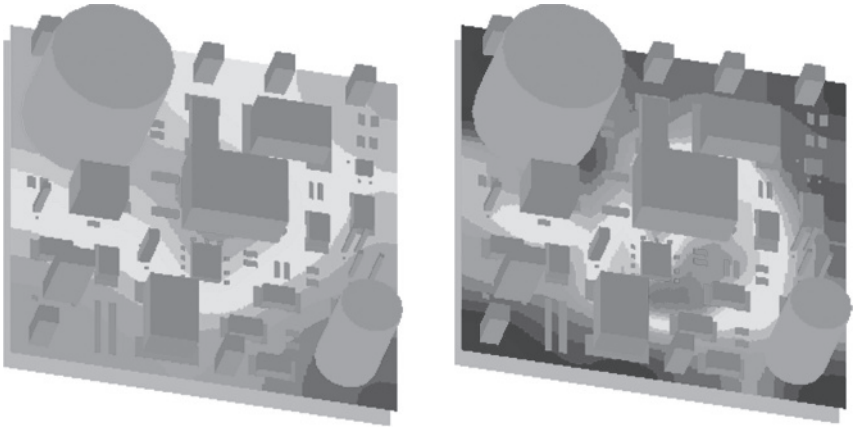


(a) Signal integrity (SI) simulation



(b) Power integrity (PI) simulation

Figure 1.18 Screenshots of HyperLynx SI and PI.



(a) Temperature (b) Thermal gradient

Figure 1.19 Snapshot of HyperLynx Thermal analysis.

4) MCM design
5) Large-scale flip-chip design.

b) Classification according to industry
1) Aerospace, aviation, shipping and other military industries
2) Power system, such as smart power grid
3) Communication, semiconductor, etc.
4) Automotive electronics
5) Intelligent applications such as Internet of things.

1.4 The Introduction of the Finished Project

Since Mentor launched the SiP design and simulation platform, it has attracted many companies and research institutes in China and worldwide. Many of them have designed high-performance SiP products with the Mentor platform.

In China, with the support of Mentor application engineers, several research institutes have completed a variety of complex, high-performance SiP projects with the Mentor platform.

For example:

1) Rudder control MCM design and thermal analysis, Microelectronics Center, Beijing, 2008.
2) RF-baseband mixed SiP design, Institute of Chinese Academy of Sciences, 2009.
3) 5-digital-chip SiP design, research institute in Beijing, 2010.
4) 6-digital-chip SiP design, a Microelectronics Corporation, 2011.
5) 3-SoC-chip SiP design, a Microsystem Institute, 2011.
6) 6-chip dual-cavity ceramic SiP design, research institute in Beijing, 2011.
7) 3-chip design of multi-cavity ceramic SiP, a Beijing company, 2011.
8) 4-chip mixed SiP design, Institute of Chinese Academy of Sciences, 2012.
9) Large-scale flip chip package design, Institute of Chinese Academy of Sciences, 2012.

Figure 1.20 shows one of the user projects completed on the Mentor SiP platform. This project has already successfully progressed to small-batch production, delivered to back-end PCB board-level applications in real projects.

At present, many customers are designing SiP, MCM or package with the Mentor platform, as follows:

1) 5-chip with dual-cavity ceramic SiP design, a research institute in Beijing.
2) 7-chip with multi-cavity ceramic SiP, a technology company in Beijing.
3) 3-chip power system integrated control SiP design, a research center in Nanjing.
4) 6-chip analog and microwave SiP design, an institute in Xian.
5) RF-digital mixed SiP design, a Microsystem research institute in Xian.
6) Flex-circuit SiP package designs, Institute of Chinese Academy of Sciences.

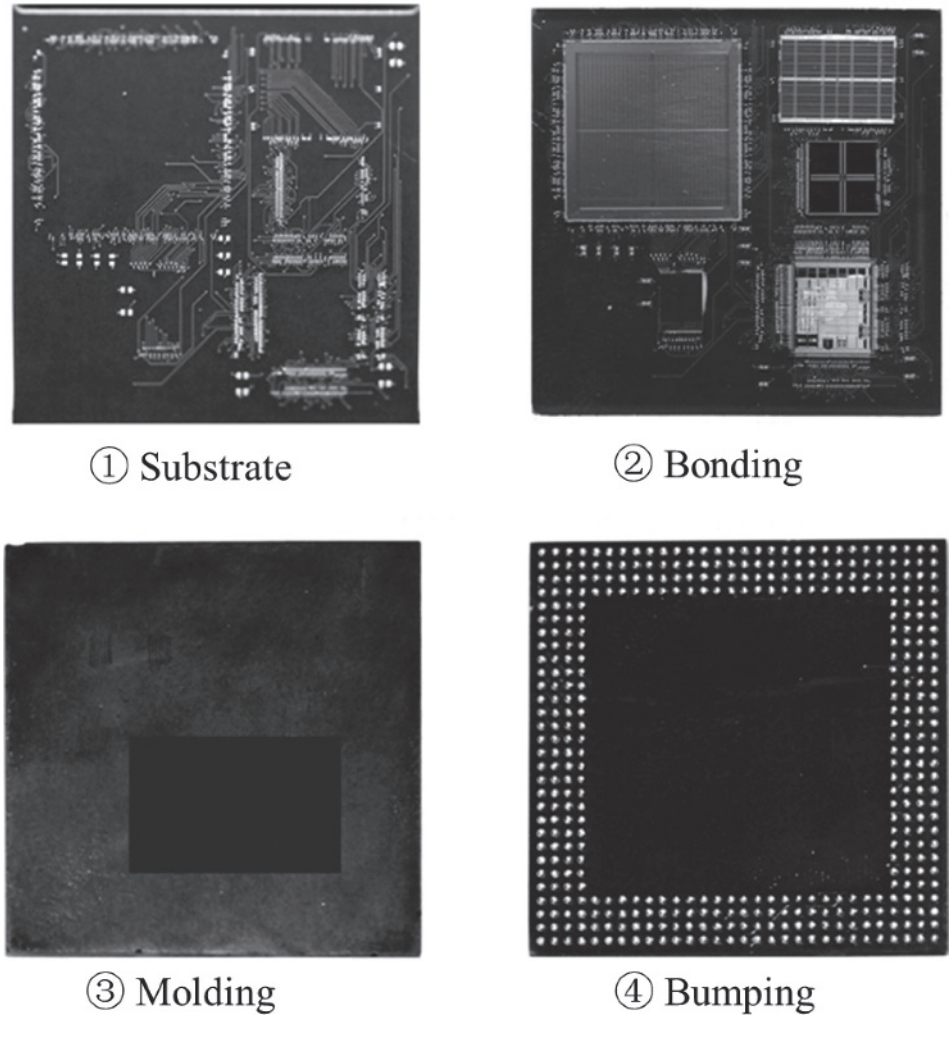


Figure 1.20 One of the finished customer projects using the Mentor SiP platform. *(See color plate section for the color representation of this figure.)*