1

INTRODUCTION

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1.1 BACKGROUND

Recent progress in computers and mobile equipment requires further efforts in developing higher-density nonvolatile semiconductor memories. A breakthrough in the field of nonvolatile memories was the invention of the flash memory [1], which is a new type of EEPROM (electrically erasable and programmable read-only memory), as shown in Fig. 1.1a. The first paper discussing the flash memory was presented in 1984 IEDM (International Electron Device Meeting). The flash memory has many advantages in comparison with other nonvolatile memories. Therefore, the flash memory explosively accelerated the development of higher-density EEPROMs.

In 1987, a NAND structured cell was proposed by Masuoka et al. [2]. This structure can reduce the memory cell size without scaling of device dimension. The NAND structure cell arranges a number of bits in series, as shown in Fig. 1.1b [2]. The conventional EPROM cell has one contact area per two bits. However, for a NAND structure cell, only one contact hole is required per two NAND structure cells (NAND string). As a result, the NAND cell can realize a smaller cell area per bit than the conventional EPROM.

Applications of flash memory became quite wide due to nonvolatility, fast access, and robustness. Flash memory application can be classified into two major markets (Fig. 1.1). One is for code storage applications, such as PC BIOS, cellular phones, and DVDs. The NOR-type cell is best suitable for this market due to its fast random access speed. The other is for file storage applications, such as the digital still camera

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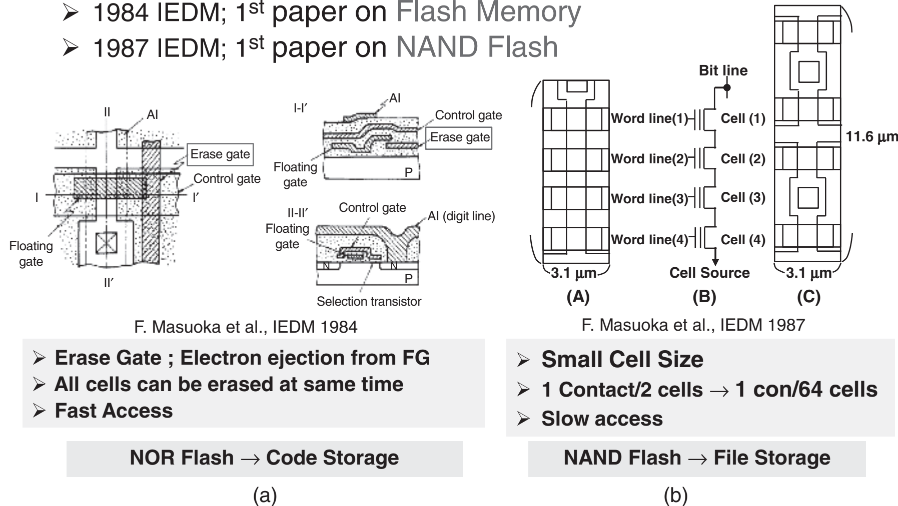

FIGURE 1.1 Invention of flash memory and NAND flash memory. (a) Flash memory. All cells in the memory chip can be erased at the same time by applying erase voltage to the erase gate [1]. (b) NAND flash memory [2]. Memory cells are connected in series to share contact area. Comparison between (A) NAND cell and (C) conventional EPROM (NOR flash cell). (B) shows the equivalent circuit of the NAND structure cell having 4 cells.

(DSC), silicon audio, the smartphone, and the tablet PC. The NAND-type cell is suitable for file storage market.

Figure 1.2 shows the memory hierarchy of computer system before mass production of NAND Flash. SRAM and DRAM had been used as cash memory and main memory, respectively. And magnetic memories, such as HDD, had been used as a nonvolatile mass-storage device. NAND flash memory had been targeted to replace magnetic memory [54]. Actually, from the production start of NAND flash memory in 1992, the NAND flash memory has been widely applied to new emerging applications and has replaced magnetic memory, as shown in Fig. 1.3. At first, a photo film had been completely replaced by the memory cards of NAND flash memory. Next, the floppy disk was replaced by USB drive memory. The mobile music equipment with cassette tape was replaced by the MP3 player using flash memory storage. Also, NAND flash memory had created new market of smartphones and tablet PCs. And now, the application is extending to the SSD (solid-state drive) market, not only for the consumer but also for the enterprise server. Therefore, over 20 years, NAND flash memory has created new large-volume markets and industries of consumer, computer, mass storage, and enterprise server. NAND flash production volume was tremendously increased. The overall NAND market is expected to reach $40 billion in 2016 [55]. NAND flash has become an explosive innovation and has greatly contributed to the improvement of our lives with the advent of convenient mobile equipment such as smartphones and tablet PCs.

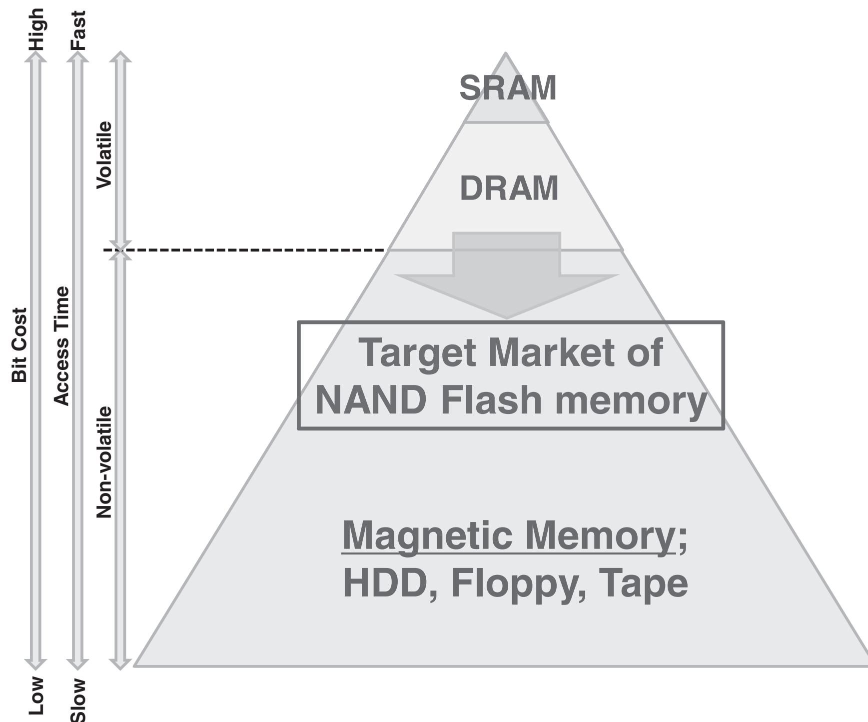

FIGURE 1.2 Target market of NAND flash memory.

Table 1.1 shows the history of NAND flash memory development, based on technical papers from 1987 to 1997. During the 10 years from the first NAND flash paper in 1987, all of the fundamental and important NAND flash technologies were established, such as page programming [7, 8], block erase, the uniform program and uniform well erase scheme [9, 12, 13], bit-by-bit verify [15, 21], the ISPP (incremental step pulse program) [25, 26, 29], the self-aligned STI cell [22, 51, 56], the shield

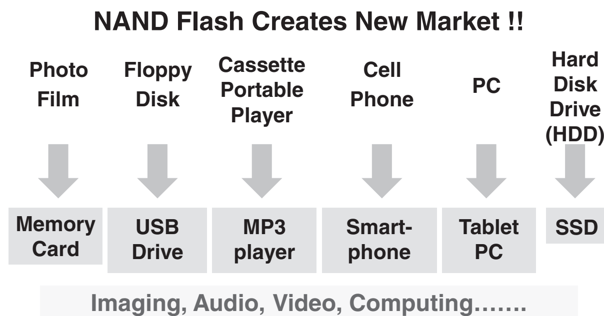

FIGURE 1.3 NAND flash memory creates a new market.

TABLE 1.1 History of the NAND Flash Memory (~1997)

Year		Authors	References	Conference/Journal
1984	Flash Memory, first paper	F. Masuoka et al.	[1]	IEDM 1984
1987	NAND-type flash memory, 1st paper	F. Masuoka et al.	[2]	IEDM 1987
1988	NAND-type flash memory	R. Shirota et al.	[3]	VLSI 1988
	Drain-FN program	M. Momodomi et al.	[4]	IEDM 1988
1989	4-Mb NAND-type flash memory	Y. Itoh et al./M. Momodomi et al.	[5, 6]	ISSCC1989/ JSSC
	Page program	M. Momodomi et al./Y. Iwata et al.	[7, 8]	CICC1989/ JSSC
1990	Well erase reliability	S. Aritome, et al	[9]	IRPS 1990
	4-Mbit tight V_t distribution	T. Tanaka et al./M. Momodomi et al.	[10, 11]	VLSI 1990/JSSC1991
	Well erase	R. Kirisawa et al.	[12]	VLSI 1990
	Bipolarity program/erase	S. Aritome et al.	[13]	IEDM 1990
	Double patterning	R. Shirota et al.	[14]	IEDM 1990
1992	Bit-by-bit verify	T. Tanaka et al.	[15]	VLSI 1992
1993	Reliability of flash	S. Aritome et al.	[16]	Proceedings of IEEE
	0.4-µm 64-Mb-cell technology	S. Aritome et al.	[17,18]	SSDM 93/ JJAP
1994	SILC	H. Watanabe et al.	[19]	VLSI 1994
	Cycling and data retention reliability	S. Aritome et al.	[20]	IEICE
	Intelligent program, shield BL scheme	T. Tanaka et al.	[21]	JSSC
	Self-aligned STI cell (SA-STI cell)	S. Aritome et al.	[22]	IEDM 1994
1995	32-Mb NAND	K Imamiya et al./Y. Iwata et al.	[23, 24]	ISSCC1995/ JSSC
	32-Mb NAND with increment step program pulse (ISPP), self-boost	K. D.Suh et al.	[25, 26]	ISSCC1995/ JSSC
	Read disturb, SILC	S. Satoh, et al	[27, 28]	ICMTS1995/ED
	Increment step program pulse (ISPP)	G. J. Hemink et al.	[29]	VLSI 1995
	Double V_t select gate	K Takeuchi et al.	[30, 31]	VLSI 1995/ JSSC
	SWATT cell	S. Aritome et al.	[32, 33]	IEDM 1995/ ED

1996	128-Mb MLC	T. S. Jung et al.	[34, 35]	ISSCC 1996/ JSSC
	64 Mb	J. K. Kim et al.	[36, 37]	VLSI1996/ JSSC
	SILC	G. J. Hemink et al.	[38]	VLSI 1996
	On-chip ECC	T. Tanzawa et al.	[39, 40]	VLSI1996/ JSSC
	Booster plate	J. D. Choi et al.	[41]	VLSI 1996
	High- speed NAND	D. J. Kim et al.	[42]	VLSI 1996
	SILC in STI	H. Watanabe et al.	[43]	IEDM 1996
	Shared bit line	W. C. Shin et al.	[44]	IEDM 1996
1997	Nonvolatile virtual DRAM using NAND	T. S. Jung et al.	[45, 46]	ISSCC 1997/ JSSC
	Three-level cell (1.5 bits/cell)	T. Tanaka et al,	[47]	VLSI 1997
	Multi-page cell	K Takeuchi et al.	[48, 49]	VLSI 1997/ JSSC
	Parallel program	H. S. Kim et al.	[50]	VLSI 1997
	0.25 μm SA-STI cell	K. Shimizu et al.	[51]	IEDM 1997
	Program disturb	S. Satoh et al.	[52]	IEDM 1997
	Triple poly-booster gate	J. D. Choi et al.	[53]	IEDM 1997

Requirements for NAND Flash

➢ **Low Bit Cost**
Small cell size & Scalability → Self-Aligned STI (SA-STI)
Multi-bit cell (MLC)

➢ **High-Speed Program**
Parallel (Low power) Program → Page program
Bit-by-bit verify
V_{pgm} step up (ISPP)

➢ **High Reliability**
Less degradation on tunnel oxide
→ Uniform P/E scheme

FIGURE 1.4 Requirements for NAND flash memory of the file storage market.

bit-line scheme [21], and so on. These technologies could satisfy the requirements of file storage memory.

Requirements for file storage memory are low bit cost, high-speed programming, and high reliability, as shown in Fig 1.4 [56].

The most important requirement for file storage applications is the low bit cost. The cost of a memory device is mainly determined by the die size of the memory chip and by the fabrication process cost, which is mainly dependent on depreciation of investment on factory. Then it is very important to combine small die size with a simple and low-cost fabrication process. In order to reduce the die size, reduction of unit memory cell size is as important as scaling feature size. Ideal memory cell size is $4 * F^2$ (F stands for feature size), because both *X* and *Y* directions are determined by line (F) and space (F). However, in early 1990s, it was difficult to realize $4 * F^2$ cell size of NAND flash memory due to wide ($>2 * F$) isolation width of LOCOS (local oxidation of Si). The self-aligned shallow trench isolation cell (SA-STI cell) was proposed and implemented to the NAND flash memory product. An isolation width could be scaled down from 2–3F in the LOCOS cell to F in the SA-STI cell. Therefore, the cell size could be drastically scaled down.

The SA-STI cell has been used in mass production for a long time, from 1998 to the present, because of a lot of advantages, such as small cell size, high reliability, and excellent scalability. However, below the 20-nm feature size, it is becoming very difficult to manage physical limitations, such as the floating gate capacitive coupling effect, RTN (random telegraph noise), the high-field problem, and so on. The recent feature size for production could reach to 15–16 nm [57]. It is not still clear whether memory cell size can be scaled down further or not.

Another way to reduce the effective cell size is the “multilevel cell.” The logical bits are stored in one physical memory cell; for example, 2 logical bits are stored in one physical memory cell (MLC; 2 bits/cell). And 3 bits/cell and 4 bits/cell are called TLC and QLC. The mass-production start of the MLC was in 2000 by using 0.16-μm technology. The process technology to fabricate a multilevel cell device is basically as same as the process of single bit cell (SLC); however, the operations for

a multilevel cell are much different from SLC operation. It is very important to make a tight V_t distribution width in the multilevel cell, in order to have high performance and reliability.

The next requirement for file storage application is high-speed programming, as shown in Fig. 1.4. In NAND flash memory, the uniform program/erase (P/E) scheme has been used as a de facto standard over 20 years. Unlike a NOR flash, no huge hot-electron injection current is required for programming, but a uniform P/E scheme has produced very low power consumption for programs even when the number of memory cells to be programmed is increased. Therefore the NAND flash memory can be easily programmed in large pages (512-byte to 32-Kbyte cells) so that the programming speed per byte can be quite fast (∼ 100 Mbytes/s). In addition, several advanced program operations, such as bit-by-bit verify, V_{pgm} step up (ISPP: incremental step pulse program), ABL (all bit line) architecture, and so on, had been developed for high-speed programming.

The other important requirement for file storage applications is "high reliability," as shown in Fig. 1.4. A high voltage (>20 V) is applied to a control gate to produce a Fowler–Nordheim (FN) tunneling current on the tunnel oxide during programming. The electric field in tunnel oxide reaches values greater than 10 MV/cm, which is normally caused by oxide breakdown in other semiconductor devices. This means that flash memory uses a breakdown-like operation in normal program and erase. Due to applying a high field, tunnel oxide has been degraded by an electron/hole trap, interface state generation, and stress-induced leakage current (SILC). Major reliability degradation aspects of flash memory are related to this tunnel oxide degradation by programming and erase cycling. Even if a tunnel oxide is degraded, stored data have to be sustained in memory cells for long time, as nonvolatile memory. Data retention time after programming and erase cycling is a key of NAND flash reliability.

In addition, read disturb and program disturb are also an important reliability phenomena in NAND flash [13,16]. During read and program operation, pass voltages are applied to unselected word lines (WLs) in the NAND string. Several kinds of disturb stress are applied to an unselected cell in a cell array. Read disturb and program disturb are caused in these unselected cells in a string in a cell array.

Reliability specifications for NAND flash memory are dependent on applications such as digital still cameras, MP3 players, SSDs (solid-state disks) for PCs, SSDs for data servers, and so on. Target specifications of a NAND flash are generally as follows. In order to guarantee the specifications of NAND, every effort has been made regarding devices, processes, operations, circuits, memory systems, and so on.

Program and erase cycles (P/E cycles): 1-K to 100-K cycles

Data retention: 1–10 years

Read cycles: 1E5 – 1E7 times

Number of page program time (NOP): 1 time for MLC,TLC,QLC, 2–8 times for SLC

In 2007, three-dimensional (3D) NAND flash device technology of BiCS (bit cost scalable) was proposed [58] in order to scale down the NAND flash memory cell

further. BiCS technology has a new low-cost process concept. The vertical poly-Si channel is fabricated by through-holes in stacked multilayer word lines. After the BiCS proposal, several three-dimensional (3D) NAND flash cells have been proposed [59–63]. Due to the vertical stacked cell structure, the 3D cell has an advantage of reducing effective cell size without scaling the feature size of F. In 2013, the mass-production start of 3D NAND flash was announced. The device was a 128-Gbit MLC 3D V-NAND flash with a 24-cell stacked charge trap cell [64]. To proceed to a lower bit cost of the 3D NAND cell, a number of stacked cells are needed to increase intensively. Many technical issues, such as a high-aspect etching, data retention of a charge trap cell, a new program disturb mode, cell current fluctuation, and so on, have to be solved or managed. After overcoming these critical issues, it is expected that a 1-terabit or 2-terabit NAND flash memory device will be available around 2020.

1.2 OVERVIEW

The NAND flash memory device technologies are reviewed in this book. The chapters focus on the scaling of the NAND flash memory cell, the high-performance operation of NAND flash, the improvement of NAND flash reliability, and three-dimensional (3D) NAND flash technologies, because they are very important for present and future NAND flash memory.

After describing a background of NAND flash technology in Chapter 1, Chapter 2 presents a basic structure and operations of NAND flash memory. The structures of single-cell and NAND-cell array are described. Cell operations of read, program, and erase are introduced. And then multilevel NAND cell technology is discussed to realize low-cost NAND flash memory.

The scaling history and scenario of planar (two-dimensional) NAND flash memory cells are reviewed in Chapter 3. The layout of the NAND flash memory cell is simple: Parallel word lines (WL) are perpendicular to parallel bit lines (BL). WL pitch is normally $2 * F$, (F: feature size), which is limited by lithography technology. However, BL pitch was normally $3 * F$ or more in the case of LOCOS isolation. This is because the isolation width needed to be $2 * F$ or more to prevent a relatively high (~8 V) punch-through between NAND cell channels (strings) during programming. Thus, it was crucial to scale down isolation width, in order to scale down memory cell size to satisfy the requirement of low bit cost.

First, LOCOS isolation cell technologies are presented (Section 3.2). The LOCOS isolation width can be minimized with improving device performance by the field-through implantation technique (FTI) after LOCOS formation. Next, the self-aligned STI cell with the FG (floating gate) wing is discussed (Section 3.3). The FG wing is applied to reduce the aspect ratio of cell structure. And then, the self-aligned STI cell without FG wing is discussed (Section 3.4). This cell has been used from the 90-nm generation cell to the present cell (1Y-nm cell), as a defacto standard. And the planar FG cell is introduced as an alternate cell structure (Section 3.5). Also, the sidewall transfer transistor cell (SWATT cell) is described (Section 3.6). Due to sidewall transfer transistor, the V_t read window margin can be greatly improved. Then,

fast programming speed can be expected. And then, recent advanced NAND flash memory cell technologies of the dummy word-line scheme and the *p*-type floating gate are discussed in Section 3.7.

Another important technology for low bit cost is the multilevel cell (MLC), which is a stored multilogical bit in a single memory cell. To implement MLC, smart operation schemes are crucial to produce reasonable performance and reliability. In Chapter 4, the advanced operations for a multilevel NAND flash are discussed. It is very important to make tight V_t distribution width during programming for better performance and reliability. Most of the operation schemes focus on this point.

For the scaling memory cell, it is becoming very difficult to control the V_t distribution width due to the occurrence of several physical limitations, including the floating-gate capacitive coupling effect, electron injection spread, RTN, and the high-field problem. These physical limitations make the V_t distribution width wider, and then the, cell V_t setting margin (read window margin) is degraded. The recent feature size for production could reach values below 20 nm. The read window margin is seriously degraded. Then it is important to clarify how much scaling limitation factors have an impact on the V_t margin beyond the 20-nm feature size. Thus, the scaling challenges of the self-aligned STI cell are discussed beyond 20 nm in Chapter 5.

The reliability of two-dimensional NAND flash memory cell is discussed in Chapter 6. Reliability of flash memory is attributed to data retention or read disturb after program/erase cycling endurance. Program and erase operation schemes have a serious impact on reliability of a flash memory cell. Then, many program/erase schemes were proposed to satisfy the requirement of reliability and performance. It is very important to clarify the cell degradation mechanism and the best scheme of program/erase in order to achieve the requirement of reliability and performance. Chapter 6 describes the reliability aspect of NAND flash cell. The uniform program/erase scheme has several advantages in NAND flash reliability by comparing program/erase endurance, data retention, and read disturb characteristics in several program and erase schemes.

The three-dimentional (3D) NAND flash cells are presented in Chapter 7. After describing motivation and history of 3D NAND flash, many types of three-dimensional cells are introduced. Advantages and performances are compared in several 3D cells, including BiCS cell, TCAT/V-NAND, SMArT cell, VG-NAND, and DC-SF cell.

After that, the challenges of 3D NAND cells are discussed in Chapter 8. To realize low-cost NAND flash memories, serious issues have to be solved or managed by improving process, structure, device, performance, and reliability

The future trend of NAND flash memory is discussed in Chapter 9. The perspectives on future NAND flash technologies are also discussed.

Corresponding to the above discussions, the following topics are described in this book:

1. Principle of NAND flash memory.
2. Scaling scenario of 2D NAND flash memory cell.

3. Practical framework of scaling down of 2D NAND flash memory cell.
4. The LOCOS isolation technology to scale down NAND flash memory cell.
5. The self-aligned STI technology.
6. Low-cost NAND flash process flow.
7. The planar FG cell.
8. The SWATT cell for MLC (multilevel cell).
9. Advanced operations for MLC.
10. Basic and advanced program operations for tight programmed V_t distribution width in MLC.
11. Page program sequence for MLC (2 bits/cell).
12. Page program sequence for TLC (3 bits/cell)
13. The scaling challenges of a 2D NAND flash cell.
14. The solutions to overcome the scaling limitation of a 2D NAND flash cell.
15. The factors analysis of physical scaling limitation of a 2D NAND flash cell.
16. Detail mechanism of the floating gate capacitive coupling interference, Electron injection spread, RTN, and so on., as scaling limiter.
17. Investigation on the reliability of NAND flash in several program and erase schemes, in order to clarify the dependence of program and erase scheme.
18. Investigation of the program disturb and read disturb phenomena to optimize operation of NAND flash cell.
19. Introduction of several three-dimensional (3D) NAND flash memory cells.
20. Scaling challenges of 3D NAND flash memory.
21. Detail mechanism of program disturb, cell current fluctuation, and so on., in 3D NAND flash cell.
22. Future trend of NAND flash memory technologies.

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