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Introduction

1.1 Development History of Packaging

Since the invention of the first semiconductor transistor in 1947, the electronic industry has experienced rapid development following Moore's law in the past decades. Packaging plays a key role in the electronic industry: it integrates numerous packaging components (i.e., chip, solder, printed circuit board [PCB], encapsulant, and cooling device) together to form a full-featured electronic system. The rapid development of the electronic industry raises numerous requirements for packaging. On the one hand, packaging is moving toward high integration, high frequency, high power, and low cost. On the other hand, packaging is expected to be more energy efficient, environment-friendly, and sustainable. These requirements pose several challenges for packaging including material development, process innovation, electrical design, and thermal management.

Nowadays, a single-chip package contains most functions of an electronic system and chips are the core component of the package. However, bare chips are far from application due to several problems. First, chips should be connected with the external circuit by pin, bonding wire, or solder ball. Second, chips are very sensitive to external factors including external mechanical force, moisture, and dust. Therefore, the chips should be isolated from these external factors by encapsulation. Third, chips generate heat during operation, which raises the chip junction temperature. If, without excellent thermal management, the chip junction temperature reaches an extremely high value, this would cause serious efficiency drop, lifetime reduction, and even chip failure. These problems are becoming more serious due to the increasing requirement for high integration, high frequency, and high power. For electronic connection, high integration of chips results in dense pin, bonding wire, and solder joint. For chip isolation, to place more chips on a fixed-size circuit, the encapsulation should be more compact. For thermal management, the high integration and high power of chips result in extremely high heat flux, which requires advanced cooling technologies such as vapor chamber, microchannel, microjet cooling, and spraying cooling. The main function of packaging is to solve the three problems listed earlier. Therefore, packaging is also regarded as chip packaging. It not only plays an important role in placing, fixing, sealing, and protecting the chips but also connects the chips with the external circuits and provides thermal management for chips.

In the past decades, packaging has undergone rapid development. In general, the development of packaging can be divided into three stages. The first stage is the through-hole insertion technology before the 1980s. This technology inserts the chip pins directly into the through holes of PCB. Because the technology requires extremely high alignment of the pins and holes, it presents low packaging density and frequency. The second stage is the surface-mount technology that emerged in the mid-1980s. It mounts the chips on the PCB through tiny pins. Compared to the through-hole insertion technology, it enhances the electrical characteristics of chips and improves the automation degree of production significantly. Although this technology has advantages of high density, small pin spacing, low cost, and suitability for surface mounting, it still fails to meet the packaging requirements of some advanced electrical systems. The third stage is the ball grid array (BGA) and chip scale package (CSP) technologies after the 1990s. During this period, the electronic industry developed rapidly, so the previous packaging technologies no longer met the packaging requirements. In this situation, the BGA and CSP were developed. They utilize the solder balls as input/output (I/O) pins, which greatly increases the package density. The emergence of BGA and CSP led to the explosive growth of the electronic industry.

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Thermal Management for Opto-electronics Packaging and Applications, First Edition. Xiaobing Luo, Run Hu, and Bin Xie.
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During the development of packaging, a lot of packaging technologies have been developed, such as transistor outline (TO) package, dual in-line package (DIP), quad flat package (QFP), thin small outline package (TSOP), BGA, CSP, flip-chip package (FCP), multichip module (MCM), and 3D packaging. From TO to 3D packaging, the technical indicators of packaging have greatly improved, such as closer chip area to package area ratio, higher integrating density, better thermal management, denser pins, closer pin spacing, smaller weight, and higher reliability. As the packaging requirements increase, some packaging technologies have been gradually eliminated. However, some advanced packaging technologies have been used until today, such as BGA, CSP, MCM, and 3D packaging, which will be introduced in the following text.

1.1.1 BGA

With the development of electronic industry, the number of I/O pins and power consumption of chips increase dramatically. Therefore, the traditional QFP and TSOP technologies can no longer meet the packaging demand. To solve this problem, the BGA packaging technology was developed in 1998. It synthesizes solder balls at the bottom of the package and uses them as I/O pins to connect with the PCB. Compared to the QFP and TSOP, it has many advantages:

① Dense I/O pins but larger pin pitch, which improves the assembly yield greatly.
② Good electrical and thermal performance.
③ Small size. Compared to the QFP, its thickness is reduced by more than 1/2 and its weight is reduced by more than 3/4. Compared to the TSOP, its packaging size is reduced by more than 2/3.
④ Small signal transmission delay and higher frequency.
⑤ High reliability.

Attributing to these advantages, it became the best choice for high-density, high-performance, multifunction, and high I/O pins packaging as soon as it was invented.

1.1.2 CSP

Although the rise and development of BGA solved the difficulties faced by QFP and TSOP, it still occupies a large substrate area. In order to integrate more chips on a fixed-size PCB, the CSP was invented in 1994. The perimeter of a CSP is no more than 1.2 times the perimeter of the chip it contains, thereby allowing more chips to be arranged in the same area and reducing the overall electrical system significantly. The structure of the CSP is similar to that of the BGA with smaller solder balls and ball spacing, so that more I/O pins can be arranged at the same size package. Compared to the prior packaging technologies, the CSP has several advantages:

① Small size and low weight. The size and weight of the CSP are smaller than any other packages. For packages with the same I/O number, the CSP technology reduces the weight of the package by more than 4/5 and the size of the package by 2/3–9/10, when compared with the QFP.
② Large number of I/O pins. For same size package, the number of I/O pins of the CSP is ~3 times that of QFP and ~1.5 times that of the BGA package.
③ Good electrical performance. The interconnection length of the CSP between the chip and the package shell is much shorter than that of QFP and BGA packages, so it has lower signal transmission delay and higher frequency.
④ Good thermal performance. Because the thickness of the CSP is extremely less, the heat generated by the chips can be easily transferred to the outside of the packaging.

Although the CSP technology was invented more than 20 years ago, it is still in the early development stage and many problems remain to be solved, such as the packaging standard and I/O pins alignment. It is undeniable that the CSP will be one of the mainstream packaging technologies in the future.

1.1.3 MCM

The rapid development of electronic systems raises high demand for multifunction and multichip packaging technologies. However, the traditional packaging technologies only contain one chip in the package and integrate numerous packages on a PCB, which increases the system size and leads to low reliability and high signal transmission delay caused by the long interconnecting wire between the packages. To tackle this issue, the MCM packaging technology was developed.

It integrates two or more large-scale chips together in one packaging shell, so the signal transmission delay between the chips is reduced greatly due to the tiny chip spacing. The MCM has many advantages:

① Low signal transmission delay and high signal transmission speed. Compared to the single-chip package, the MCM increases transmission speed by 4–6 times.

② Compact size and low weight. The chips in the MCM package can be tiled on a single layer or stacked on multiple layers. The multiple-layer structure can decrease the packaging size significantly, resulting in low weight. Compared to the single-chip packaging, it decreases the weight by more than 80%.

③ High reliability. The failure of the electronic systems is mainly caused by failure of circuit interconnections, while the MCM reduces such interconnections, thereby improving the reliability of the electronic system.

④ Multiple functions. The MCM integrates chips with various functions together to form multifunctional electronic systems directly.

Although the MCM has many advantages, it is not as widely applied in industrial production as the BGA and CSP technologies. There are two reasons: the cost of the MCM is much higher than other packaging technologies and the MCM package presents poor thermal performance because the heat cannot be quickly dissipated to the outside due to the high chip integration along the vertical direction. For most commercial electronic systems, the BGA and CSP technologies would be a better choice due to their relatively low cost.

1.1.4 3D Packaging

In recent years, the development of the electronic industry has failed to obey Moore's law, which predicts that the number of transistors on a chip will double every 24 months, due to the physical limitations present in the complementary metal-oxide semiconductor (CMOS) processing technology. The 3D packaging is expected to break this limitation. By stacking more than two chips in the vertical direction through silicon via (TSV), the 3D packaging assembles more chips on the electronic system without increasing the size of the PCB. Compared to the 2D packaging, it has advantages of higher assembly density, lower cost, smaller size, lower power consumption, higher signal transmission speed, and smaller signal transmission delay. So far, the 3D packaging is rarely applied in the industrial production because there are many problems that need to be solved, such as the cost and reliability of the TSV and redistribution layer (RDL) and the severe thermal issue caused by the high chip integration along the vertical direction.

From the TO in the 1970s to the current 3D packaging, packaging technology has undergone tremendous development in materials, processes, and applications. With the further development of the electronic industry, more changes are taking place in the field of packaging.

① High thermal conductivity packaging materials. The low thermal conductivity of some key packaging materials, i.e., thermal interface material (TIM), encapsulant, and chip substrate, has become a serious problem that blocks further development of high integration and power electronic systems. For the TIM and encapsulant, the scholars and industry are trying to enhance their thermal conductivity by adding high thermal conductivity particles, such as graphene nanoplatelets (GNP), carbon nanotube (CNT), hexagonal boron nitride (hBN), and metallic oxide. And the concentration and arrangement of the particles are optimized by considering the material properties of the liquid matrix and particles. For the chip substrate, high thermal conductivity materials, i.e., silicon (Si), silicon carbide (SiC), aluminum nitride (AlN), beryllium oxide (BeO), and diamond, are developed to replace the conventional sapphire (Al_2O_3).

② Advanced cooling technologies. For some electronic systems with high chip power and integration, the local heat flux could reach an extremely high level $>500\ W\ cm^{-2}$, which requires advanced cooling technologies to dissipate the heat immediately. Therefore, conventional air cooling technologies can no longer meet the cooling requirement. To solve this issue, liquid cooling technologies with microchannel, vapor chamber, and phase change materials have been developed.

③ Environmental packaging material. To protect the environment, it is meaningful to use lead-free, halogen-free, and easy-clean packaging materials. In recent years, the use of lead-free solders has been attracting extensive attention. However, most of the lead-free solders have relatively high melting point and poor wettability, which results in voids in the solder layer and thereby worsens the reliability of the electronic devices. Therefore, it is very important to develop lead-free solders with a low melting point and good wettability. Besides, the conductive adhesive could also be a prior choice.

④ Reliability of the electronic systems. Most chips are sensitive to moisture, oxide, and high temperature environment. Therefore, it is of great importance to investigate the effect of these factors on the reliability of electronic systems and enhance the reliability by developing advanced packaging technologies.

1.2 Heat Generation in Opto-electronic Package

In general, the chips can be regarded as resistors, and the heat power of the chips is proportional to the driven current and equal to the input electrical power in most cases. However, for some electronic packages with opto-electro chips, only part of the input electrical power is converted into heat and the heat generation mechanism can be extremely complex. The accumulation of heat increases the chip junction temperature sharply and induces many thermal problems including thermal stress, performance degradation of the chip, and mechanical and electrical reliability of the package. The opto-electro packages have undergone rapid development in recent decades due to their wide application in solid-state lighting. Therefore, it is of importance to understand the heat generation mechanism of the opto-electro chips.

Light-emitting diode (LED) is a typical opto-electro chip, so we use it as an example in the following text to make the description clearer. The LED was invented by Holonyak and Bevacqua in 1962 [1], and widely applied to general lighting until Nakamura et al. [2] invented blue LED chips with high power and light efficiency in 1991. As a typical type of solid-state lighting, LED converts part of the input electrical power into light power. Compared to the conventional lighting sources (i.e., incandescent lamp and fluorescent lamp), it has the advantages of high light efficiency ($>100\ \mathrm{lm\cdot W^{-1}}$), long lifetime (>50,000 hours), high reliability, compact size, and environmental protection. Therefore, it has become the mainstream light source in the twenty-first century [3, 4].

Figure 1.1 shows the working principle of LED. The core functional structure of the LED chip is the PN junction that is composed of P-type semiconductor and N-type semiconductor. In P-type semiconductor, the carriers that transport electrical energy are holes, while in N-type semiconductors, the carriers that transport electrical energy are electrons. Under the drive of an electric field, the electrons and holes move relatively and recombine in the multiquantum well (MQW) layer to emit light. In addition, part of the electrical power is converted into heat due to the nonradiative combination of electrons and holes, Shockley–Read–Hall (SRH) recombination, Auger recombination, surface recombination, current crowding and overflow, light absorption, etc.

1.2.1 Heat Generation Due to Nonradiative Recombination

Figure 1.2 shows the schematic of the band gap of the semiconductor material, which has an electronic band structure determined by the crystal properties of the material. The discrete energy distribution is affected by the absolute temperature. Above absolute zero temperature, the existing energy levels are filled with electrons according to the Boltzmann distribution. The free electrons range from their bounds to a freely moving state, which is called a conduction band (CB). The valance band (VB) is the highest range of electron energies in which electrons are bounded. The difference between CB and VB is called the band gap or forbidden band, since ideally there is no electron energy state within this region [5].

The freely moving electrons in the meta-stable state exist in the CB until they fall to the VB and recombine with an electron hole. This process is referred to as recombination. There are two types of recombination within the active region of LED chips, i.e., radiative recombination and nonradiative recombination. For radiative recombination, the electron fills a hole in the VB by releasing a photon with energy equal to the band gap energy of the semiconductor material [6]. This process is the

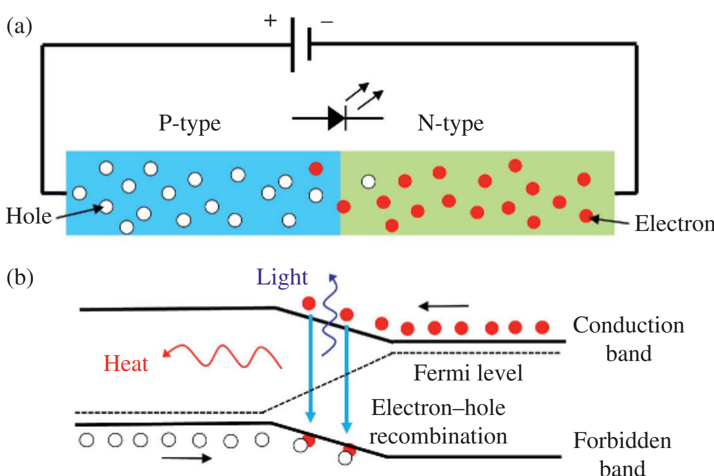

Figure 1.1 (a, b) Working principle of a typical LED chip.

foundation of the LED working mechanism. For nonradiative recombination, the releasing energy exists in the form of atom vibrations within the crystal, such as phonons; if the energy is not collected, it dissipates as heat. Apparently, the nonradiative recombination should be minimized for high device performance and low heat generation [7].

In the active layer of the LED chips, there are two major nonradiative recombination processes, i.e., defect-related SRH recombination and Auger recombination, which will be described in detail next.

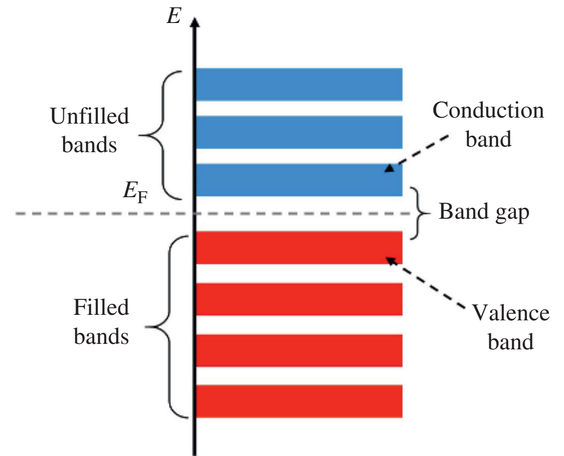

Figure 1.2 Schematic of the band gap of the semiconductor material.

1.2.2 Heat Generation Due to Shockley–Read–Hall (SRH) Recombination

Figure 1.3 shows the band diagram which illustrates the recombination process. In Figure 1.3, the SRH recombination is used to describe the recombination of the electron and hole at the undesired energy level, which is created within the band gap by defects in the lattice. They were first investigated by Shockley, Read, and Hall in 1952 and were used as a model to study the nonradiative recombination caused by defects [8].

Defects in the crystal structure are the main cause of SRH nonradiative recombination. These defects include unwanted foreign atoms and crystallographic defects. All of the defects have energy-level bands that are different from the major semiconductor atoms. Therefore, one or more new energy levels can be generated within the forbidden band gap. Unfortunately, these energy levels within the gap of the semiconductor are efficient recombination centers, especially when the deep level is near the middle of the gap. Detailed analytical expressions are obtained for the lifetime estimation of the SRH recombination [7]. These expressions reveal that when the trap level is at or close to the mid-gap energy, the lifetime is twice the minority lifetime and the probability of SRH recombination is increased. Moreover, the increase in temperature will raise the nonradiative recombination probability. For simplicity, the recombination rate can be estimated by $\text{Rate}_{\text{SRH}} = k_{\text{SRH}}n$, where k_{SRH} is the SRH recombination coefficient and n is the carrier concentration [9].

1.2.3 Heat Generation Due to Auger Recombination

Auger recombination describes the process in which the electron in CB gives off excess energy and recombines with a hole in VB. During this process, the excess energy is obtained by a second electron or hole instead of emitting the energy as a photon. The newly excited electrons or holes release their energy through collision with the crystal lattice and return back to the band edges.

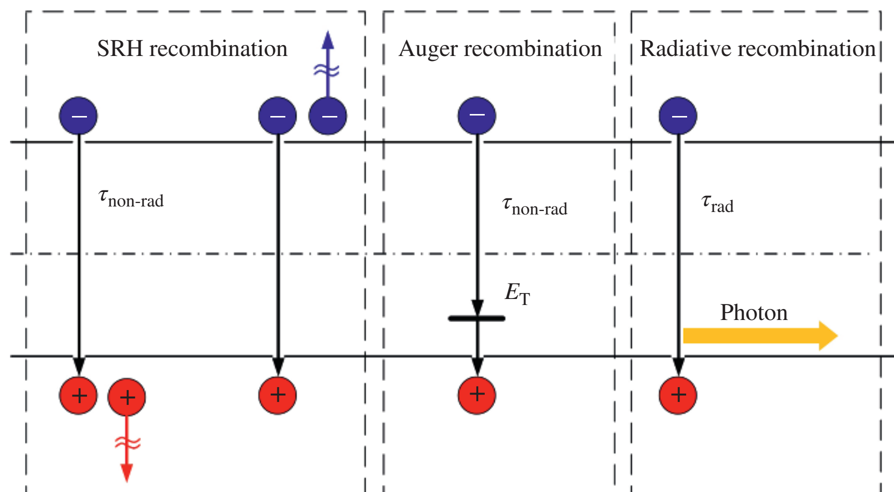

Figure 1.3 Band diagram illustrating: SRH recombination, Auger recombination, and radiative recombination. Adapted from Schubert [7].

The probability of Auger recombination increases with the concentration of charge carriers since this process is based on the ability of the charge carriers to exchange energy. The rate of Auger recombination can be expressed as $\text{Rate}_{\text{Auger}} = k_{\text{auger}}n^3$, where k_{auger} is the Auger recombination coefficient and n represents the carrier concentration. The coefficient k_{auger} on the scale of 10^{-28}–10^{-29} $\text{cm}^6 \cdot \text{s}^{-1}$ for III–V semiconductors plays an important role [10]. Normally, k_{auger} decreases with increased energy band gap. According to the reported Auger recombination coefficients in Table 1.1, the simulation work adopts 10^{-30} $\text{cm}^6 \cdot \text{s}^{-1}$ for GaN-based LED chip design, which exhibits good prediction of device performance [15]. More detailed discussions about the Auger recombination coefficients can be found in reports by Cho et al. [16]. At low carrier concentrations, the Auger recombination is neglected for practical reasons. However, at very high excitation intensity or carrier injection in the current situation, n is much higher and Auger recombination should be considered.

Table 1.1 Auger recombination coefficients reported for GaN-based LED chips.

Material	Auger recombination coefficient ($\text{cm}^6 \cdot \text{s}^{-1}$)	Reference
$In_{0.10}Ga_{0.90}N/GaN$	1.5×10^{-30}	[11]
InGaN/GaN	3.5×10^{-31}	[12]
$In_xGa_{1-x}N$ ($x \sim 9\%$–15%)	1.4–2.0×10^{-30}	[13]
GaInN/GaN	2.5×10^{-31}	[14]

1.2.4 Heat Generation Due to Surface Recombination

Nonradiative recombination also occurs at the semiconductor surface. At surfaces, the periodicity of the crystal lattice ends. Therefore, the band diagram will change at the surface since the strict periodicity of the crystal arrangement is perturbed. Additional electronic states will appear within the forbidden gap of the material [17]. Fortunately, surface recombination can be greatly reduced if the injected carriers are away from the surface. This can be realized by carrier injection under one contact, which is smaller than the LED chip.

1.2.5 Heat Generation Due to Current Crowding and Overflow

Heat generation within the active region of LED chips due to the nonradiative recombination is introduced. Here, the focus will be placed on heat generated outside the LED active region. Particularly, heat generation due to current crowding and overflow will be considered. The solutions are largely attributed to efficient LED chip design at the epitaxial and device levels.

In the realm of semiconductor physics, current crowding is used to describe a nonhomogeneous distribution of current density through the semiconductor at the vicinity of the contacts and over the PN junctions. As shown in Figure 1.4(a), in conventional LED chips, the GaN layer grows on insulating substrates (e.g., sapphire) where electrons laterally spread from N-pad to P-pad. Due to this geometry, the finite resistance of the Ohmic contact and the confinement layer causes the current to “crowd” near the edge of the contact. As shown in Figure 1.4(b), the current density distribution can be undesirably nonuniform. The current density could drop from 99 $\text{A} \cdot \text{cm}^{-2}$ at N-pad to 11 $\text{A} \cdot \text{cm}^{-2}$ at P-pad [18].

Due to the nonlinear distribution of the current density, the crowding phenomenon becomes more severe in high-power LEDs operating at high current density. The remarkable current concentration at the edges of P-type and N-type electrodes has a detrimental effect on the device performance. On the one hand, the local increase in carrier density leads to a high recombination rate, causing nonuniformity of light emission in the active region. This will induce localized overheating of the heterostructure at certain points and the formation of hotspots, whereas a large portion of the device remains inactive during operation. On the other hand, the nonhomogeneous distribution of current will increase the electromigration effect, and voids will be formed. Overall, current crowding will induce the local overheating of the heterostructure, lower the device performance, and increase the series resistance.

Various solutions have been proposed to reduce the current crowding problem, such as multifingered chip design [19]. Through simulation, Joshi et al. report that the current crowding problem is finally eliminated by a combination of multi-finger with delta-doping design. Vertical chip configuration can also solve this problem. Figure 1.5 presents the schematic

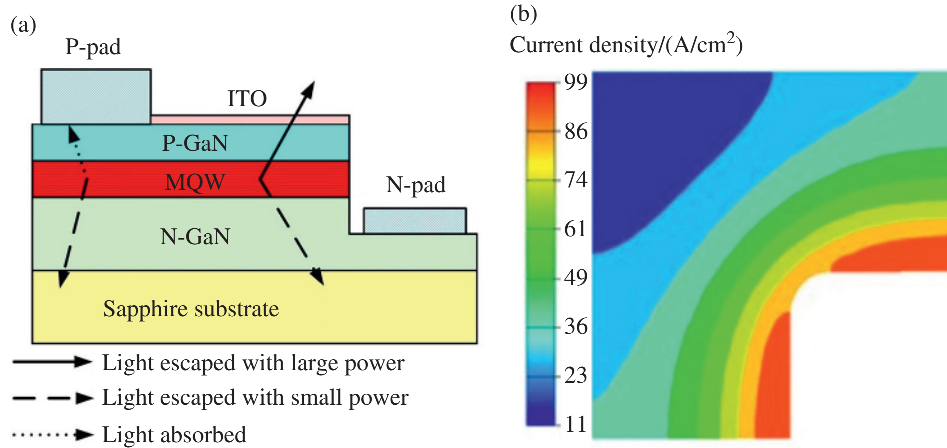

Figure 1.4 (a, b) Current crowding in GaN/InGaN LEDs on insulating substrates. Adapted from Cao et al. [18].

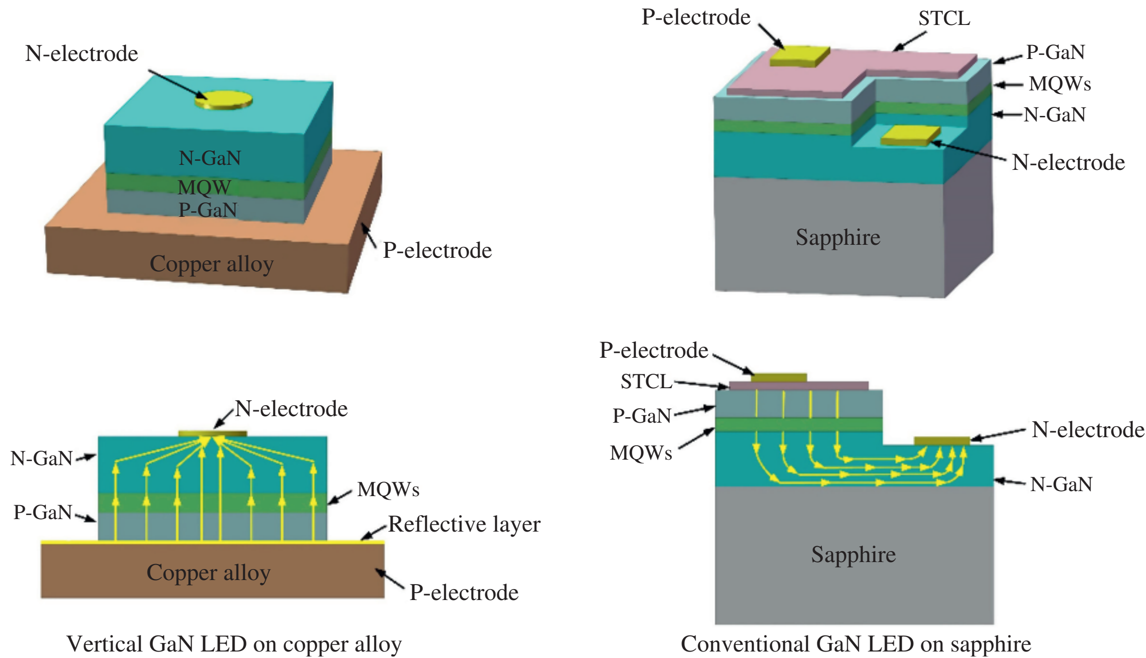

Figure 1.5 Schematic of current injection. Adapted from Joshi et al. [19].

for current injection in conventional chips and vertical chips, respectively. Compared to conventional chips (right side of Figure 1.5), vertical LED chips (left side of Figure 1.5), whose GaN layer is grown on a conducting substrate (e.g., SiC) directly or is transferred to a metal substrate by a laser lift-off process, can also reduce current crowding.

Current overflow, also referred to as electron leakage, describes the process in which the energetic electrons move from the N-type through the active region and recombine with holes in the P-type GaN without being confined in the active region. Since only the carriers confined in the active region are able to participate in the radiative recombination, the recombination caused by electron overflow generates unwanted heat. Current overflow is mainly caused by the higher carrier mobility of the electrons [20] (about 200 $cm^2 \cdot V^{-1} \cdot s^{-1}$) than that of the holes (about 10 $cm^2 \cdot V^{-1} \cdot s^{-1}$) [21]. The longer current spreading length caused by the higher mobility leads to fewer holes than electrons being injected into the active region. This is the reason why the AlGaN electron blocking layer (EBL) is usually adopted on the P-side of the active region.

1.2.6 Heat Generation Due to Light Absorption

Photons generated by radiative recombination may not be able to escape from the LED chip if they are totally internally reflected at the semiconductor/air interface. If the incident angle of the light ray is close to normal, they are effectively extracted outside of the LED chip; otherwise, they will be trapped inside [7] and converted into heat. This occurs because of the large refractive index difference of GaN ($n = 2.5$)/air ($n = 1$) interface. Total internal reflection (TIR) occurs when the incident angle exceeds the critical value $\theta_c = \arcsin(n_1/n_2)$, which can be calculated based on Snell's law. The TIR leads to a narrow escape cone of only 23.5°, with an escape probability of only 4% from the top surface of the LED [22].

Techniques have been developed to improve light extraction efficiency (LEE), including photonic crystal, periodic surface texturing, surface roughing, patterned sapphire substrate, and reflectors using Al or Au electrodes.

Thin-film flip-chip (TFFC) design is widely used in current commercial LEDs, which possess high LEE as compared to that of conventional LED package design. Thin-film LEDs could be realized by removing the sapphire substrate by the laser lift-off technique. On the other hand, flip-chip LEDs are achieved by submounting the P-GaN on a high-reflectance metallic mirror to form the vertical LED configuration. This allows the photons to emit from the thicker N-GaN layer side and enables a more flexible surface texturing and patterning process on NGaN to enhance LEE without potential effect on the InGaN QW's active region. The TFFC LEDs combine these two techniques and therefore show great potential to enhance LEE.

1.3 Thermal Issues and Challenges

The increasing power and integration density of chips bring several thermal issues and challenges, including thermal management and mechanical and electrical reliability.

1.3.1 Thermal Management

Thermal management is an important function of packaging; it transfers the heat from the tiny chips to the large-scale heat sink to maintain the chip temperature below the reliable operating temperature. There are two main issues related to the thermal management; one is the hotspot of packages and the other is the temperature distribution uniformity inside the package. The hotspot mainly takes place inside the chips because chips are the primary heat source of most packages. In addition, the temperature distribution of the package also greatly depends on the chip power and chip arrangement. Therefore, the key issue lies in the thermal management of package: to transfer the heat of the chips to the environment as soon as possible and minimize the temperature difference between the chips and other packaging components.

There are three heat dissipation paths: conduction, convection, and radiation. Typically, the reliable operating temperature of most chips is below 120 °C, so the radiation of the chips as well as other packaging components can be ignored. Therefore, conduction and convection are the main heat dissipation paths. The heat generated in the chips transfers to the heat sink by conduction through several packaging materials and thermal interfaces and then it transfers from the heat sink to the environment by convection. There are four types of thermal resistance that should be taken into consideration: material bulky resistance, thermal interfacial resistance, thermal spreading resistance, and heat sink-to-ambient resistance. Thermal bulky resistance is determined by the dimension and thermal conductivity of the material. Thermal interfacial resistance highly depends on the contact condition of TIMs and their adjacent solid packaging materials, which is determined by the liquid properties of the TIMs, such as the viscosity, surface tension, and wettability, on the adjacent rigid packaging materials. If the TIMs fail to wet their adjacent rigid packaging materials, air/vapor voids form between these two packaging components, which induce extremely high thermal interfacial resistance due to the extremely low thermal conductivity of air/vapor. The thermal interfacial resistance could be the key thermal resistance in a package with multiple-layer packaging structure, such as MCM and 3D packaging. Thermal spreading resistance depends on the size difference between two packaging components and the thermal boundary conditions. For most of the packages, the chip size is much smaller than the PCB as well as other packaging components. The heat transfer from the tiny chips to other large-scale packaging materials could suffer extremely high thermal spreading resistance, which is the main reason for inducing the hotspot on chips and nonuniform temperature distribution in packages.

Heat sink-to-ambient resistance varies greatly with the thermal management technologies. In general, the thermal management technologies could be divided into passive cooling and active cooling. The key difference between these two

methods is that active cooling requires an external power source to generate airflow or liquid flow to take the heat away from the heated surface quickly, while passive cooling dissipates the heat by natural convection, heat conduction, and phase change. Compared to active cooling, passive cooling offers the advantages of simple structure, easy fabrication, flexibility, low cost, and high reliability. However, the heat dissipation capacity and efficiency of passive cooling are always limited by its dimensions and structure. Therefore, passive cooling technologies are becoming outdated as they cannot meet the packaging requirements of high-power electronic packages. Active cooling technologies, such as external forced convection, pumped loops, refrigeration, microchannel cooling, microjet cooling, and spray cooling, have higher heat dissipation capacity and efficiency than passive cooling technologies. Although active cooling technologies suffer low reliability and high system complexity, they are expected to solve the bottleneck issue of the thermal management of high-power electronic packages. Moreover, as the chip size decreases and chip power increases, microscale thermal management technologies are attracted extensive attention in recent decades. They achieve extremely low thermal resistance and high heat transfer coefficient at the high heat flux region and, therefore, offer excellent hotspot cooling and significantly improve the temperature distribution uniformity of the packaging. These technologies can also be passive or active, in which the passive cooling could be vapor chamber and microchannel, while the active cooling could be Peltier cycle thermoelectric devices and Stirling refrigeration cycle. However, the miniaturization of thermal management systems brings challenges to packaging processes, material synthesis, and system integration, which still have a long way to go.

1.3.2 Mechanical/Electrical Reliability

As introduced earlier, the electronic packages suffer from hotspots in high heat flux regions and nonuniform temperature distribution inside the packages if without excellent thermal management. These two thermal problems could worsen the mechanical/electrical reliability or even cause catastrophic failure of the packages. The mechanical reliability is caused by two reasons: one is the thermal stress inside the package induced by the temperature difference of various packaging components and the other is the thermal degradation/quenching/carbonization of the chips and other packaging components induced by overheating.

The thermal stress inside the packages can induce cracking of chips, TIMs, electrodes, and bonding wires. Die attaching is the key packaging process for improving the mechanical reliability of packages. In the die attaching process, chips or power modules are bonded on the substrate or PCB through TIMs. As mentioned earlier, the thermal interface resistance that lies between the TIMs and their adjacent rigid packaging materials could be the key thermal resistance in the package with a multiple-layer packaging structure. The high thermal interface resistance makes it difficult for the heat generated by the chip to be transferred to the substrate, PCB, and other packaging components. As a result, the heat accumulates inside the chips and packages, which causes hotspots in chips and nonuniform temperature distribution in packages. The deformation of the high-temperature region is much more serious than that of the low surface temperature region, which causes the thermal stress. Cracking of packaging components happens if the thermal stress is much higher than the fatigue stress of the packaging materials. Increasing the thermal conductivity, reducing the thickness of TIMs, and promoting the contact condition of TIMs with their adjacent rigid packaging materials can reduce the thermal interface resistance, thereby reducing the temperature difference and improving the mechanical reliability of the packages. In addition, developing advanced microscale thermal management technologies to offer higher heat transfer coefficient at the high heat flux region could also reduce the temperature difference inside the packaging, thereby improving the mechanical reliability of the packages.

Thermal degradation/quenching of the chips and other packaging components worsens the electrical/optical/thermal performance and decreases the lifetime of the packages, while carbonization of the packaging components causes irreversible failure to the packages. These issues are particularly prominent in opto-electro packages. In the opto-electro packages, both light and heat are generated from chips/fluorescent materials (phosphors and quantum dots) and then transmitted or conducted through many packaging materials and interfaces. Meanwhile, part of the transmitted light converts into heat along the light propagation. In return, the accumulation of heat leads to rise in temperature and thermal degradation/quenching of the chips/fluorescent materials, thereby generating more heat. Therefore, more severe challenges lie in the research of the thermal reliability of opto-electro packages, such as temperature dependence of the electro-opto conversion of chips and opto-heat conversion of fluorescent materials, light scattering, reflection, and absorption.

In summary, the increasing power and integration density of chips pose significant challenges to the upstream chip manufacturing/designing and material synthesis, midstream packaging processes, and thermal management technologies. Among these challenges, thermal management is thought to be the key issue for supporting Moore's law that is well known in the semiconductor industry. However, the existing thermal management technologies are far from meeting the

development requirements of the semiconductor industry. Different from the existing thermal management technologies that aim at lowering the working temperature of the whole package and the electrical system, the fundamental goal of the future thermal management technologies is to cool the hotspot in chip/packaging and minimize the temperature difference inside the packaging and the electrical system. To face the challenges mentioned earlier, great progress should be made in numerous scientific fields, including chip manufacturing/designing, packaging processes, material synthesis, and system integration and reliability testing.

1.4 Organization Arrangement

In this book, we will introduce the thermal management for opto-/electronic packaging and applications in 10 chapters. In this chapter, the development history of opto-/electronic packaging, heat generation in opto-electro package, and related thermal issues and challenges were presented. In Chapter 2, the basic concepts of thermal conduction and thermal resistance are presented and thermal management solutions based on thermal conduction are introduced, including high thermal conductivity materials, tunable interfacial thermal conduction, heat pipe, vapor chamber, phase change materials, and thermal metamaterials. In Chapter 3, the basic concept of thermal convection and solutions are introduced; air cooling and liquid cooling technologies are also discussed. In Chapter 4, the basic concept of thermal conduction radiation and solution are presented and radiative cooling and near-field thermal radiation are introduced. In Chapter 5, the opto-thermal, electro-thermal, and opto-electro-thermal interactions are presented. In Chapter 6, thermal conductivity enhancing principles and solutions of TIMs are presented, including modeling and validation of thermal interface resistance and thermal conductivity manipulation of TIMs. In Chapter 7, the packaging-in thermal management for quantum dots-converted LEDs is presented. In Chapter 8, the application of phase change material in downhole devices is introduced. In Chapter 9, liquid cooling for high heat flux electronic devices is presented. In Chapter 10, we will give a summary of the contents included in this book.

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