1

Electrical Analysis – Terminology and Theorems

This first chapter is an introduction to some of the basic definitions and terms you must understand in order to perform electrical analysis with efficiency and speed. By electrical analysis, I imply finding the various relationships that characterize a particular electrical network. To excel in this field, as in any job, you need to master a few tools. Obviously, they are innumerable and I am sure you have learned a plethora of theorems during your student life. Some names now seem distant simply because you never had a chance to exercise them. Or you actually did but implementation was so obscure and complex that you left quite a few of them aside. This situation often happens in an engineer's life where real-case experience helps clean up what you have learned at school to only retain techniques that worked well for you. Sometimes, when what you know fails to deliver the result, it is a good opportunity to learn a new procedure, better suited to solve your current case. In this chapter, I will review some of the founding theorems that I extensively use in the examples throughout this book. However, before tackling definitions and examples, let us first understand what the term *transfer function* designates.

1.1 Transfer Functions, an Informal Approach

Assume you are in the laboratory testing a circuit encapsulated in a box featuring two connectors: one for the input, the second for the output. You do not know what is inside the box, despite the transparent case in the picture! You now inject a signal with a function generator to the input connector and observe the output waveform with an oscilloscope. Using the right terminology, you *drive* the circuit input and observe its *response* to the stimulus. The input waveform represents the *excitation* denoted u and it generates a *response* denoted y. In other words, the excitation variable propagates through the box, undergoes changes in phase, amplitude, perhaps induces distortion etc. and the oscilloscope reproduces the response on its screen.

The waveform displayed by the oscilloscope is a *time-domain* graph in which the horizontal axis x is graduated in seconds while the vertical axis y indicates the signal *amplitude* (positive or negative). Its dimension depends on the observed variable (volts, amperes and so on). The input waveform is denoted in lower case as it is an *instantaneous* signal, observed at a time – the *instant* $t - u(t)$. A similar notation applies to the output signal, $y(t)$. In Figure 1.1, you see a low duty ratio square-wave injected in the box engendering a rather distorted waveform on the output.
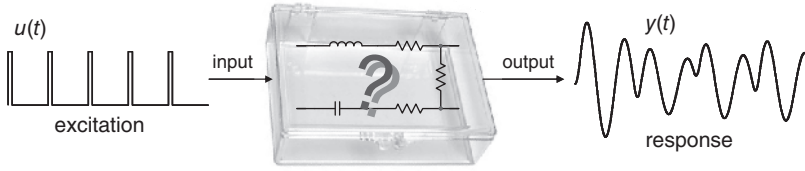
Figure 1.1 A black box featuring an input and an output signal. What is the relationship linking output and input waveforms?

This ringing signal tells us that the box could associate resonant elements, probably capacitors and inductors but not much more than that. If we change the excitation, what type of shape will we obtain? Knowing what is inside the box will let us predict its response to various types of excitation signals.

There are several available ways to characterize an electrical linear circuit. One of them is called *harmonic analysis*. The input signal is replaced by a sinusoidal waveform and you observe how the stimulus propagates through the box to form the response. This is shown in Figure 1.2:

The excitation level must be of reasonable amplitude – understand *small* – so that the response signal is not distorted. The input signal dc bias must also be set accounting for the physical constraints imposed by the active circuit so that upper- or lower-rail saturation is avoided. In other words, the box internal circuitry is not *overdriven* and remains *linear* during the analysis. Linearity is confirmed if the output signal is sinusoidal with the same frequency as the input sine and only varies in amplitude and phase while you ac-sweep the network. This is a so-called *small-signal* analysis. In the Laplace domain, you perform such harmonic analysis when you set $s = j\omega$ in which $\omega = 2\pi f$ represents the angular frequency expressed in radians per seconds (rads/s). Laplace analysis with $s = j\omega$ applies to linear circuits only.

Should you increase the input signal amplitude or change the operating bias point, slewing or clipping may happen. In this case, you explore the box *large-signal* or *nonlinear* response. This is a characterization different than the small-signal approach and it offers another insight into the circuit operation. Let us keep linear and once the right input amplitude is found, i.e. a signal of comfortable amplitude is observed on the oscilloscope screen, the frequency is varied step by step while output amplitude/phase couples are recorded in an array. At each frequency point f, we store the ratio of the response amplitude $Y(f)$ in volts to the excitation amplitude $U(f)$ in volts also. At each frequency point f, we save the phase information linking both input and output waveforms. As U and Y are complex variables affected by a magnitude and a phase, we can write:

$$A_v(s) = \frac{Y(s)}{U(s)} \tag{1.1}$$

A_v represents a *transfer function*, a mathematical relationship linking a response signal Y to an excitation signal U. Please note that the excitation signal U resides in the transfer function
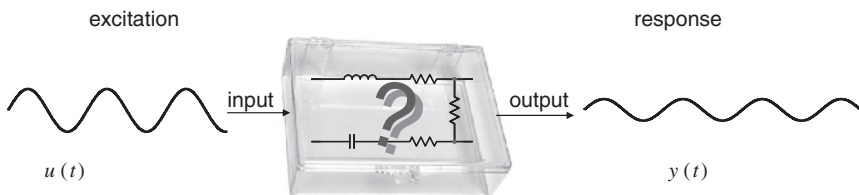

Figure 1.2 The black box is now driven by a sinusoidal stimulus for a small-signal analysis.

denominator while the response Y sits in the numerator. It will always be this way throughout the book.

The transfer function is a complex variable characterized by a magnitude noted $|A_v(f)|$ and an argument, $\angle A_v(f)$ also noted $\arg A_v(f)$. The ratios $Y(f)/U(f)$ we have stored correspond to the transfer function magnitude (also called *modulus*) observed at a frequency f while the phase difference between Y and U represents the transfer function argument or phase at the considered frequency. The transfer function magnitude dimension depends on the observed variables as we will later see. Here, because volts are involved for both variables, the transfer function magnitude is *dimensionless* or *unitless*. Furthermore, $|A_v|$ can only be greater than or equal to zero. It is what makes the difference between an amplitude which can take on any value, positive, null or negative and a magnitude which can only be zero or positive. If it is 0, there is no output signal. If $|A_v|$ is less than 1, we talk about *attenuation*. Now, if $|A_v|$ is greater than 1, it is designated as a *gain*. If the magnitude can only be a null or positive number, what about a gain of -2 then? It simply characterizes a stage offering a gain of 2, lagging or leading the excitation signal phase by $180°$.

1.1.1 Input and Output Ports

It is convenient to represent our box as a two-port circuit. A *port* is a pair of connections that can input or output signals such as voltage and current. Figure 1.3 shows an illustration of this principle where you see two connecting ports, one input and one output.

Under some conditions, a port can take on the input and output roles at the same time. Imagine you want to measure the output impedance of the box. To realize this measurement, you classically implement Figure 1.4 where a current across the output terminals is injected while the voltage across the same terminals is observed This is what is called a *single injection*, i.e. one stimulus and one response. In this experiment, the box input port is shorted (see Appendix 1A). The excitation variable is the current $I_{out}(s)$ injected into the port while the response is the voltage $V_{out}(s)$ collected across the port's terminals. The output impedance Z obtained from the ratio of the port voltage to the injected
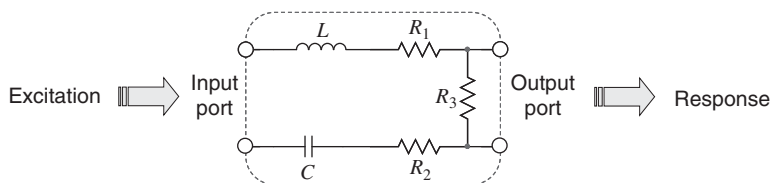

Figure 1.3 The input port receives the excitation signal while the output port delivers the response.
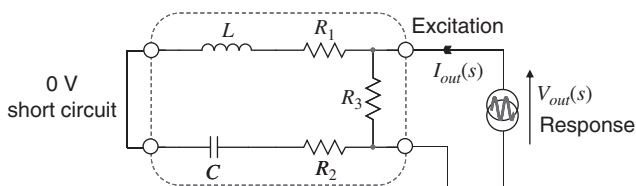

Figure 1.4 A port can be both an input and an output at the same time. Here, an output impedance measurement.

current is a transfer function. It has the dimension of an impedance expressed in ohms:

$$Z_{out}(s) = \frac{V_{out}(s)}{I_{out}(s)} \tag{1.2}$$

I_{out}, the excitation signal lies in the denominator while the response, V_{out}, stands in the numerator. We will come back on this important peculiarity.

If input and output connectors are fixed, physical ports, which let you respectively inject and observe signals, nothing prevents one from creating other observation ports as needed. Simply remove a resistor, a capacitor or an inductor and its connecting points become a new port. This port can now be used as a new input stimulus or as an output variable you want to observe. As already mentioned, this newly created port can also play the role of an input and output port at the same time. In that case, the box originally featuring one input and one output, becomes a two-input/two-output system as illustrated in Figure 1.5 in which the inductor has been removed. Using adequate terminology, we analyze the system by performing a *double-injection*: two stimuli – inputs 1 and 2 – giving two responses, outputs 1 and 2.

In this example, the voltage across the removed inductor terminals is the response while the injected current is the excitation signal. By dividing the port voltage by the injected current, we have the resistance offered by the port terminals when the element initially connected has been removed. In other words, we 'look' at the resistance offered by the inductor port as shown in Figure 1.6 where the symbol R? and the arrow imply this exercise. Expressed in a different manner, we find the equivalent *output resistance* exhibited by the port when 'driving' the inductor, hence the name *driving point* resistance or *driving point impedance* abbreviated as DPI. Combining resistance and inductance gives us a time constant τ ('tau') associated with this inductive element:

$$\tau = \frac{L}{R} \tag{1.3}$$

To conduct this exercise and find the resistance R, you can directly look at the sketch and infer the resistive series-parallel arrangement without solving a single equation. This exercise is called *network inspection*: you simply observe the network in certain conditions (for instance in dc, or when V_{in} is set to 0) and find resistance values by observing how components are connected together. For example, in Figure 1.6, what resistance do you 'see' looking into the inductor port while capacitor C is
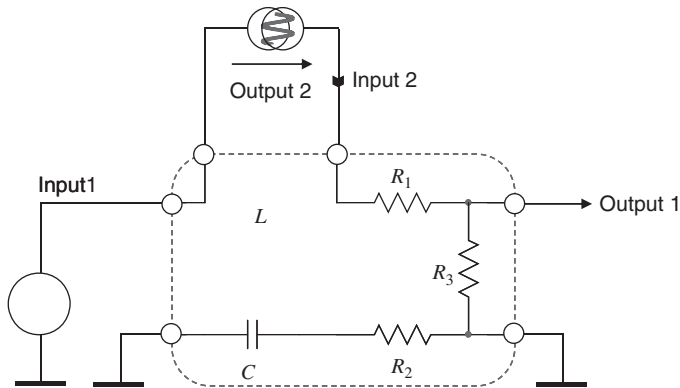

Figure 1.5   If you remove a component from this circuit, its connections become a connecting port. You can bias this port and consider it as a new input, or as a new output, or both of them at the same time.
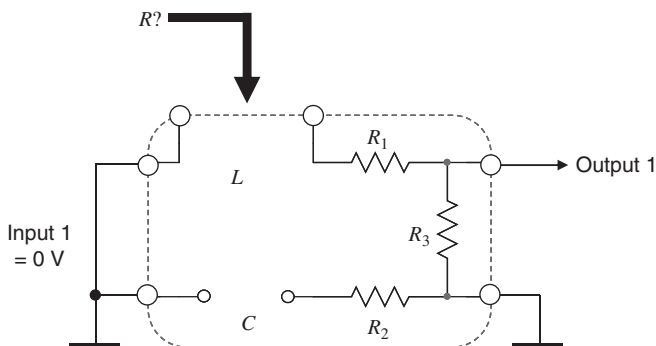
Figure 1.6 Removing the inductor lets you look at the port output resistance that drives the inductor. Associating the port resistance and the inductance leads to a time constant. Here, the resistance seen at the inductor port is $R_1 + R_3$.

disconnected for the exercise? R_1 appears first and then R_3 in series goes to ground and returns to the inductor left terminal via the shorted input source. R_2 is open and plays no role:

$$R = R_1 + R_3 \qquad (1.4)$$

Applying (1.3) with (1.4) gives the definition for the time constant involving L:

$$\tau_1 = \frac{L}{R_1 + R_3} \qquad (1.5)$$

A similar exercise can be conducted with the capacitor to also unveil the resistance R that drives this element. In this case, the time constant associated with the capacitance is simply:

$$\tau = RC \qquad (1.6)$$

Assuming a shorted inductance in this particular illustration, what resistance value do you see in Figure 1.7 when looking into the capacitor port? The left terminal is grounded while the second
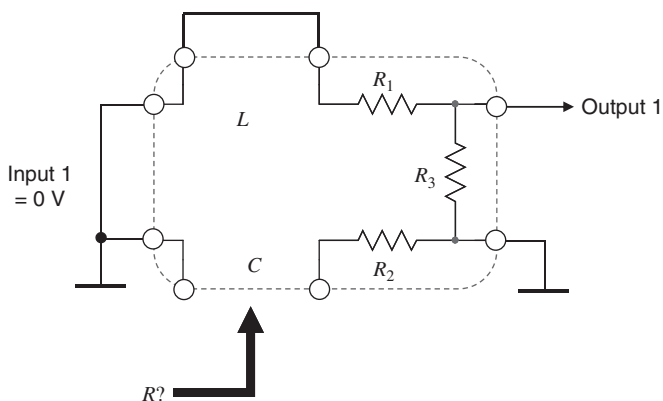

Figure 1.7 Removing the capacitor lets you conduct a similar exercise to unveil the time constant associated with this component. In this case, the resistance seen at the capacitor port is R_2.

terminal also goes to ground via R_2. R_1 and R_3 play no role since their series combination goes from one ground to the other one. Therefore:

$$R = R_2 \tag{1.7}$$

The time constant involving the capacitor is simply:

$$\tau_2 = R_2 C \tag{1.8}$$

We have two storage elements, C and L, and there are two time constants. For each storage element, there is an associated time constant.

Rather than looking into a capacitive or an inductive port, we could also remove a resistor and define what resistance drives it, the exercise remains the same. Sometimes, looking into the port to 'see' the resistance is not as straightforward, especially when controlled sources are involved. In this case, you need to add a test current generator as in Figure 1.5 and define the voltage generated across the considered terminals. The resistance offered by the port being the port voltage divided by the test current generator. This test generator will later be labeled I_T and the voltage across its terminals V_T.

What we just described is part of the technique foundations we will later describe: find resistances offered across the connecting terminals of resistive, capacitive or inductive elements once they have been temporarily removed from the circuit under certain conditions. Breaking a complex passive or active circuit into a succession of *simple* configurations where time constants are unveiled will help us characterize a network featuring poles and zeros. The Extra Element Theorem (EET) and later, the *n* Extra Element Theorem (*n*EET), make an extensive usage of these methods and it is important to understand this prerequisite. Appendix 1A will refresh our memory regarding available methods to derive output impedances while Appendix 1B collects several examples to let you exercise your skills at finding these resistances.

1.1.2 Different Types of Transfer Function

Depending where you inject the excitation and where you observe the response, you can define six types of transfer functions as detailed in [1]. For the sake of simplicity, input and output ports are ground-referenced but could also be differential types. The first one, is the voltage gain A_v already encountered in the above lines and it appears in Figure 1.8 together with an operational amplifier (op amp) in an inverting configuration. In all the following illustrations, the op amp is considered a perfect element (infinite open-loop gain, infinite bandwidth, zero output and infinite input impedances). You sweep the input voltage with a sinusoid, the stimulus, and observe the voltage at the op amp output, the response. In Laplace notation, you compute A_v as:

$$A_v(s) = \frac{V_{out}(s)}{V_{in}(s)} \tag{1.9}$$

A_v is dimensionless, sometimes expressed in [V]/[V].

The second one is the current gain, A_i, this time involving input and output currents as shown in Figure 1.9. The excitation signal is now the input current I_{in} while the observed variable is the output current I_{out}:

$$A_i(s) = \frac{I_{out}(s)}{I_{in}(s)} \tag{1.10}$$

A_i is dimensionless, sometimes expressed in [A]/[A].

The third transfer function is called a *transadmittance* – short name for transfer admittance – and is denoted Y_t. You observe the output current while the input is excited by a voltage source.
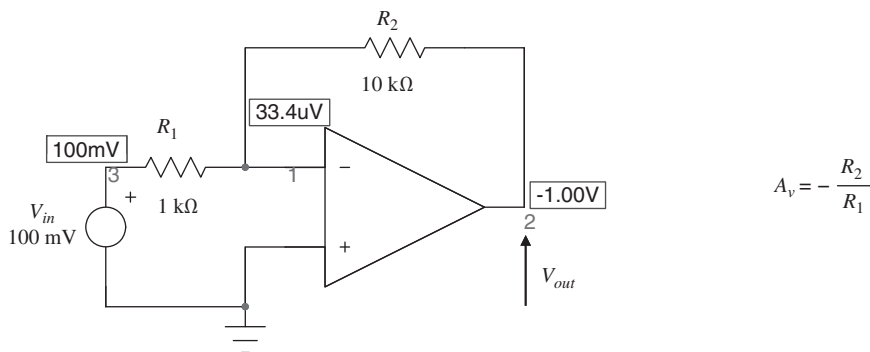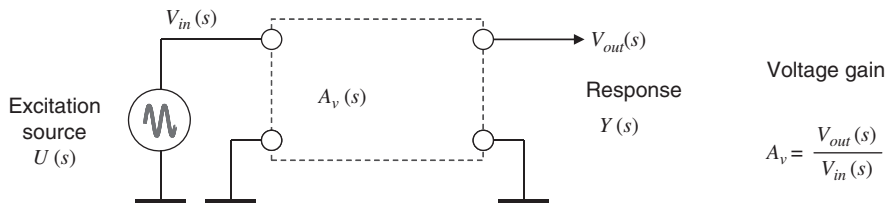
Figure 1.8 The voltage gain A_v is the first transfer function and links the output voltage to the input voltage.
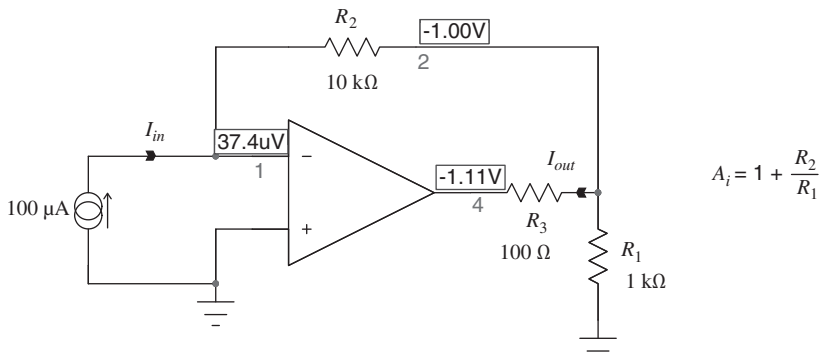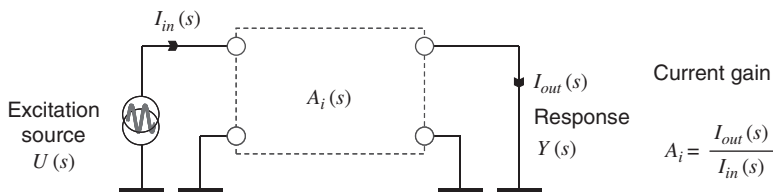

Figure 1.9 The current gain A_i is the second transfer function and links the output current to the input current.
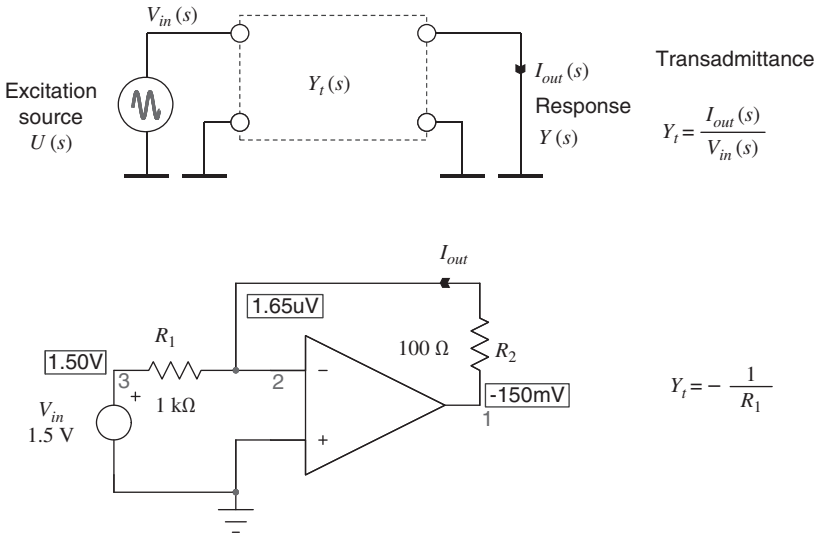
Figure 1.10 The transadmittance Y_t links the output current to the input voltage. Here the current in R_2 is imposed by V_{in} and reaches 1.5 mA. The transadmittance gain is -0.001 A/V or -1 mS.

The measurement configuration is shown in Figure 1.10. The definition is as follows:

$$Y_t(s) = \frac{I_{out}(s)}{V_{in}(s)} \tag{1.11}$$

If the two preceding gains were dimensionless, the transadmittance is expressed in ampere per volt, [A]/[V] or siemens [S]. Similarly, we can define the fourth transfer function in which, this time, the input is excited by a current source while the output voltage is the response (Figure 1.11). The ratio of these two variables is designated as a *transimpedance* – short name for transfer impedance – denoted Z_t and expressed in volt per ampere, [V]/[A] or ohm [Ω]:

$$Z_t(s) = \frac{V_{out}(s)}{I_{in}(s)} \tag{1.12}$$

Transimpedance amplifiers are often used in case you want to amplify a photodiode current for instance. You will find in [2] a design example of such a circuit.

In the four previous transfer functions, the involved quantities – excitation and response signals – appear at two different places in the network. We conveniently considered the box input and output terminals for the examples, but definitions apply equally for relationships between any ports in the network. For the two remaining transfer functions, impedance Z and admittance Y, excitation and response signals are observed at the same port terminals. It is therefore important to distinguish how we create the excitation signal and what is considered the response signal. You can argue that it is not a problem to reverse excitation and response because impedance and admittances are reciprocal to each other. However, if we want to stick to our transfer function definition in which the excitation waveform lies in the denominator while the response appears in the numerator, then, for a *driving point impedance* (DPI) function $Z_{dp}(s)$, the excitation signal is a current source and for a driving point admittance function $Y_{dp}(s)$, the stimulus is a voltage source.
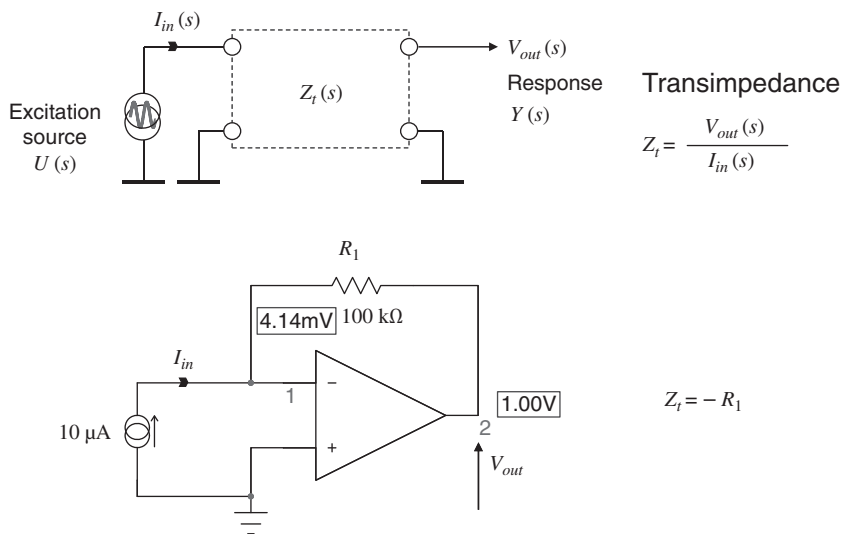
Figure 1.11 The transimpedance Z_t links the output voltage to the input current. In the op amp example, resistor R_1 brings a transimpedance gain of $-100\,\text{kV/A}$.

The 5$^{\text{th}}$ transfer function is thus the port input impedance $Z(s)$ whose generalized transfer function is given below:

$$Z_{dp}(s) = \frac{V_1(s)}{I_1(s)} \tag{1.13}$$

If you consider V_{in} and I_{in} or V_{out} and I_{out}, you respectively measure the network input and output impedances by injecting a test current in the port and measuring the voltage across the port terminals. Figure 1.12 shows sources arrangement for this specific measurement. The dimension of an impedance is ohm, $[\Omega]$.

Finally, the 6$^{\text{th}}$ transfer function is the *admittance*, the inverse of an impedance. You measure an admittance by exciting the concerned port with a voltage source which produces a current, the response (Figure 1.13). The generalized transfer function of an admittance is:
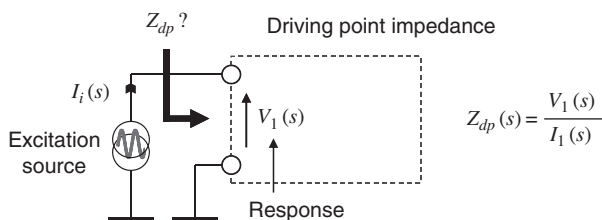
$$Y_{dp}(s) = \frac{I_1(s)}{V_1(s)} \tag{1.14}$$

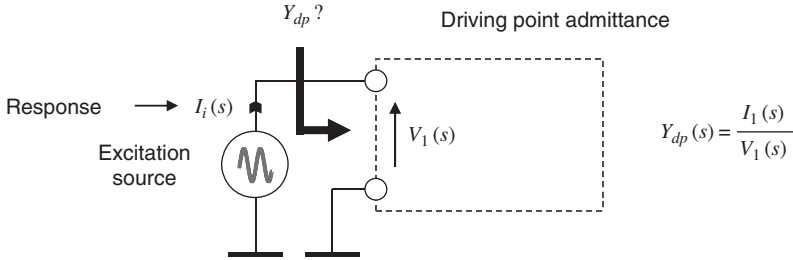**Figure 1.12** Impedances have the dimension of ohms. The excitation signal is a current.

Figure 1.13   Admittances have the dimension of Siemens. The excitation signal is a voltage.

If you consider I_{in} and V_{in} or I_{out} and V_{out}, you respectively measure the network input and output admittances.

Admittances are expressed in siemens, abbreviated [S]. Old notations such *mhos*, ℧ or Ω^{-1} are no longer in use in the International System of units (SI, after the French *Système International d'unités*).

As explained, when determining a port impedance, the excitation signal is a current source. In certain configurations, it is sometimes more convenient to actually calculate the admittance instead by exciting the circuit with a voltage source. The final result is simply reversed to obtain the impedance we are looking for. We will see an application of this principle in an example later on. Figure 1.14 below summarizes the 6 transfer functions we just described.
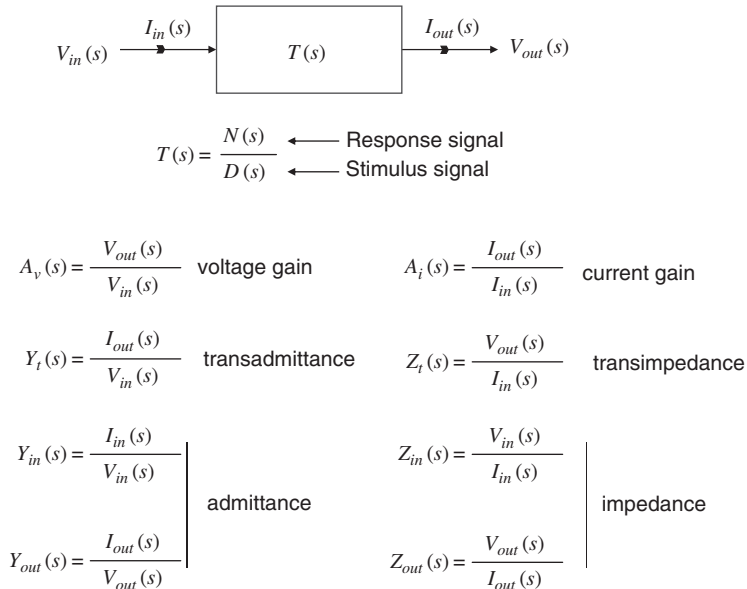

Figure 1.14   There are six different transfer functions, 4 of them have a stimulus and a response at different locations – different ports – while two of them, Z_{dp} and Y_{dp}, have stimulus and response at the same port.

1.2 The Few Tools and Theorems You Did Not Forget . . .

In the litany of theorems and analysis tools I had been taught during my university years, there are a few I did not forget because I exercise them almost every day in my engineer's job. Voltage and current dividers are the first in the tools list. They are of tremendous help when it comes to simplifying circuits and a quick refresh is given below. Among theorems, the first one is Thévenin's theorem, after the French electrical engineer, Charles Léon Thévenin, in 1883. The second is the dual of Thévenin's theorem, Norton's theorem, after the American electrical engineer, Edward Lawry Norton who described the theorem in his 1926 technical memorandum. The third one is obviously the superposition theorem whose extension will lay the foundations for the EET and, later, the nEET. Superposition and the EET are thoroughly detailed in Chapter 3.

Let's have a look at a few examples applying these tools, showing how Thévenin and Norton can help us simplify circuits in a quick and efficient way.

1.2.1 The Voltage Divider

This is one of the most useful tools I employ when analyzing electrical circuits. It works with all passive elements in dc or ac (direct or alternating voltages/currents) and the Thévenin theorem makes an extensive use of it. Figure 1.15 shows its simple representation.

The circulating current I_1 is the input voltage V_{in} divided by the total resistive path, $R_1 + R_2$:

$$I_1 = \frac{V_{in}}{R_1 + R_2} \tag{1.15}$$

The voltage across R_2 is the resistance value multiplied by current I_1:

$$V_{out} = I_1 R_2 \tag{1.16}$$

Substituting (1.15) in (1.16), we have:

$$V_{out} = V_{in} \frac{R_2}{R_1 + R_2} \tag{1.17}$$

If we divide both sides of the equation by V_{in}, we have the transfer function linking V_{out} to V_{in}:
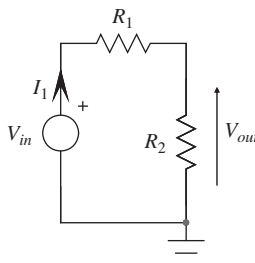
$$\frac{V_{out}}{V_{in}} = \frac{R_2}{R_1 + R_2} \tag{1.18}$$

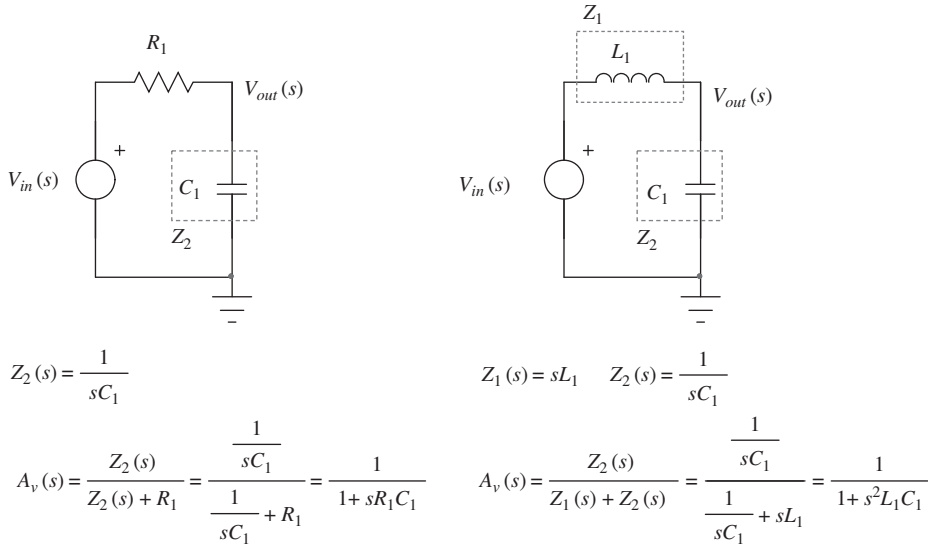**Figure 1.15** A resistive divider is a great tool to simplify circuits.

$$Z_2(s) = \frac{1}{sC_1} \qquad\qquad Z_1(s) = sL_1 \qquad Z_2(s) = \frac{1}{sC_1}$$

$$A_v(s) = \frac{Z_2(s)}{Z_2(s) + R_1} = \frac{\dfrac{1}{sC_1}}{\dfrac{1}{sC_1} + R_1} = \frac{1}{1 + sR_1C_1} \qquad A_v(s) = \frac{Z_2(s)}{Z_1(s) + Z_2(s)} = \frac{\dfrac{1}{sC_1}}{\dfrac{1}{sC_1} + sL_1} = \frac{1}{1 + s^2L_1C_1}$$

Figure 1.16 The divider equation works with passive elements such as capacitors and inductors.

When you see networks such as those of Figure 1.16, you can immediately apply (1.18) without writing a single line of algebra. In this example, (1.18) is updated with impedances rather than resistances:

$$A_v(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{Z_2(s)}{Z_1(s) + Z_2(s)} \tag{1.19}$$

Please note that (1.18) and (1.19) only work if R_2 or Z_2 are unloaded. Should you have another circuit connected across R_2 or Z_2 respectively in Figure 1.15 and Figure 1.16, (1.18) and (1.19) no longer work.

1.2.2 The Current Divider

This is another example of a very useful tool often involved in electrical analysis. Consider Figure 1.17a circuit in which you need to find the current flowing in R_3.

The total current I_1 is V_{in} divided by the resistive path connected to the source:

$$I_1 = \frac{V_{in}}{R_1 + R_2 || R_3} \tag{1.20}$$

In this expression, the '$||$' operator refers to the paralleling of R_2 and R_3:

$$R_2 || R_3 = \frac{R_2 R_3}{R_2 + R_3} \tag{1.21}$$

Mathematically, the parallel operator has precedence over the addition: $R_2 || R_3$ is first computed and then added to R_1.

The original sketch can then be updated to a simpler one as shown in Figure 1.17b. Kirchhoff's current law (KCL) tells us that the sum of the currents entering a junction equals the sum of currents
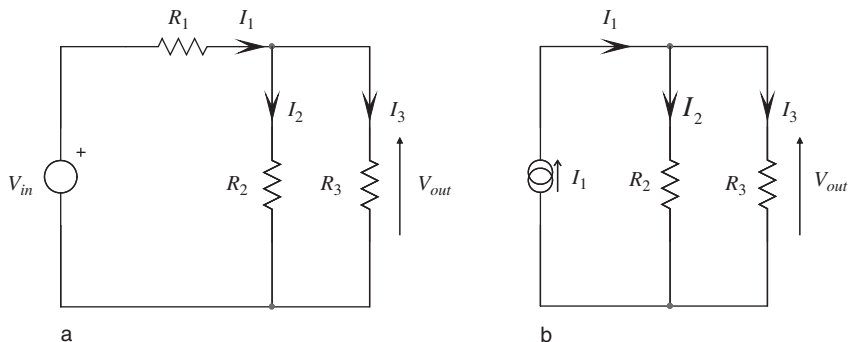
Figure 1.17   The current divider is another great simple tool.

leaving it. Thus:

$$I_1 = I_2 + I_3 \tag{1.22}$$

Currents I_2 and I_3 are defined by the voltage across their terminals, V_{out}:

$$I_3 = \frac{V_{out}}{R_3} \tag{1.23}$$

$$I_2 = \frac{V_{out}}{R_2} \tag{1.24}$$

Extracting V_{out} from (1.23) and (1.24) then equating results gives another relationship linking I_3 and I_2:

$$R_3 I_3 = R_2 I_2 \tag{1.25}$$

Extracting I_2 from (1.22) and substituting it in (1.25) leads to:

$$R_3 I_3 = R_2(I_1 - I_3) \tag{1.26}$$

Rearranging and factoring leads to the relationship linking I_3 and I_1:

$$I_3 = I_1 \frac{R_2}{R_2 + R_3} \tag{1.27}$$

This is the current divider expression which helps us get the current into R_2 or R_3 when I_1 splits between these elements. Figure 1.18 gives another representation. The current flowing in R_2 equals
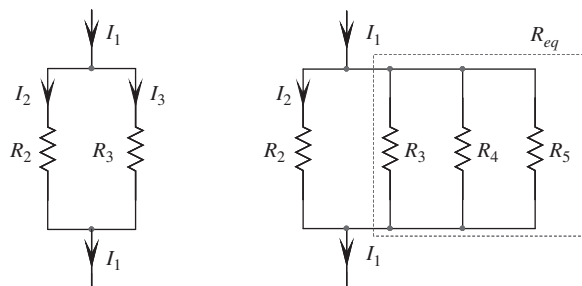

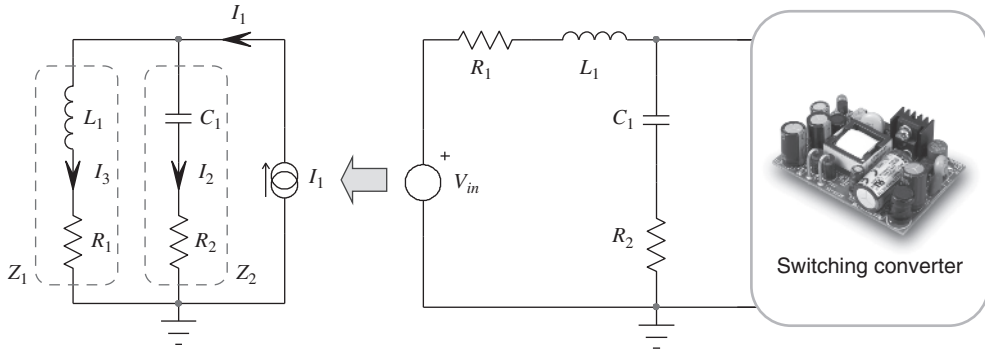**Figure 1.18**   The current divider is easily generalized to paralleled resistors.

Figure 1.19 Passive elements arranged to form a filter: how much current flows in L_1?

the main current I_1 multiplied by the resistance 'facing' R_2 (thus R_3) and divided by the sum of resistances, $R_2 + R_3$. The right side of Figure 1.18 generalizes the concept where more resistors are connected in parallel with R_3. If $R_{eq} = R_3 \| R_4 \| R_5$ then the current in R_2 is simply:

$$I_2 = I_1 \frac{R_{eq}}{R_{eq} + R_2} \tag{1.28}$$

This technique works equally well with energy-storing components as represented in Figure 1.19. This is a typical Electromagnetic Interference (EMI) filter found in switching converters. I_1 illustrates the converter current signature – its high-frequency input current – C_1 is the front-end capacitor while L_1 is the filtering inductor. With a perfect filter, all the alternating current would flow in C_1 while only direct current flows in L_1, providing the dc source with the right isolation to the switching current. Reality differs and what you need is the current really flowing in L_1 and check what attenuation this configuration brings. Apply the current divider expression to Figure 1.19 circuit and you have

$$\frac{I_3(s)}{I_1(s)} = \frac{Z_2(s)}{Z_1(s) + Z_2(s)} = \frac{R_2 + \dfrac{1}{sC_1}}{R_2 + \dfrac{1}{sC_1} + R_1 + sL_1} = \frac{1 + sR_2C_1}{1 + sC_1(R_1 + R_2) + s^2L_1C_1} \tag{1.29}$$

We did not write a single equation to derive this transfer function, we just *inspected* the figure and applied the current division law. This technique is called solving for a transfer function by *inspection*.

1.2.3 Thévenin's Theorem at Work

Any 2-port *linear* system made of resistors, capacitors, inductors, dependent/independent current/ voltage sources can be represented by an equivalent Thévenin model. This equivalent circuit is made of a complex generator V_{th} associated with a complex output impedance Z_{th}. When solving complex networks transfer functions, or if the current or voltage at a given point is needed, the idea is to apply Thévenin's theorem and break the complex circuit into a simpler representation with a Thévenin equivalent circuit in place. This idea behind Thévenin's approach is to model the I-V characteristics 'seen' by the load. You remove the load and model the equivalent source that drives it, affected by a certain output impedance/resistance. As such, Thévenin's and Norton's equivalent circuits do not
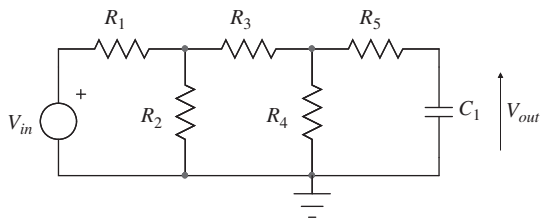
Figure 1.20 In this circuit, five resistors drive capacitor C_1. Rather than going through KCL and KVL, use the Thévenin's generator approach.

reflect the power dissipated by the network they replace. Use them carefully when evaluating powers or currents at certain points in the circuit.

Assume you need to calculate the transfer function $V_{out}(s)/V_{in}(s)$ of the circuit in Figure 1.20. This is a classical case to which we purposely added more resistors than in examples you can find in the web. The goal of using Thévenin is to reduce this complex circuit into a simple structure from which you can immediately deduce the transfer function by inspection. The first option is to use Kirchhoff's voltage and current laws (KCL and KVL) and write mesh and nodes equations. It is very likely that you will obtain the result but the chance also exists that you will make mistakes while writing these expressions. This is the so-called brute-force analysis. The second option uses Thévenin and represents a step towards *fast analytical circuit techniques* whose acronym is FACTs. We must find a place in the network where the insertion of our equivalent generator will simplify the analysis. Let's proceed step by step. We first cut the circuit after R_2 as shown in Figure 1.21 to isolate a first equivalent generator.

The Thévenin voltage is the voltage appearing across R_2 while separated from the rest of the circuit. We can apply the voltage divider law as R_2 is unloaded after the separation. Looking at the upper side of Figure 1.21, this voltage is simply:

$$V_{th1} = V_{in}(s)\frac{R_2}{R_1 + R_2}$$
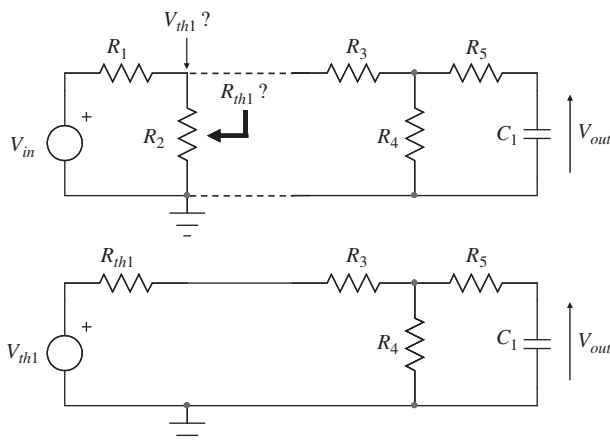
(1.30)

Figure 1.21 You must find a place in the circuit to identify a Thévenin equivalent generator.
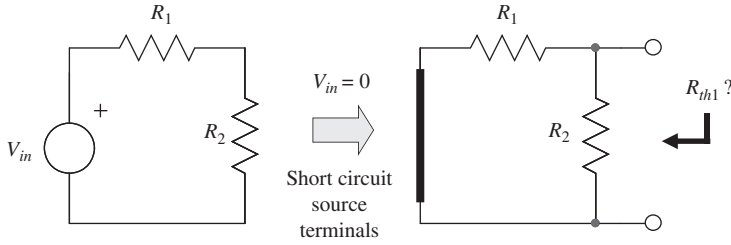
Figure 1.22   The output resistance is found by looking into the output port, across R_2 while the voltage generator is set to 0 V.

We have the Thévenin generator expression so what is its output resistance in this case? The output resistance, as explained in Appendix 1A, is found by setting the input voltage to 0 V and find the resistance seen across R_2's terminals (Figure 1.22).

The resistance is immediate:

$$R_{th1} = R_1 \| R_2 \tag{1.31}$$

We can now replace the input source associated with R_1 and R_2 by its equivalent Thévenin's generator. It appears in the upper side of Figure 1.23. We have an equivalent circuit that mimics the I-V characteristic driving the circuit made of R_3 and the rest of the elements. Coming back on our note regarding caution in using Thévenin (or Norton), you can see that the generator in Figure 1.22 dissipates power when unloaded $-V_{in}^2/(R_1 + R_2)-$ while the equivalent model involving V_{th} and R_{th} does not. Using Thévenin to calculate power levels or efficiency figures would lead to a wrong result.

Simplifying further on, before reaching the capacitor, another resistive divider is present. We can update the previous Thévenin generator by accounting for the presence of these elements. The voltage divider approach is still useful:

$$V_{th2} = V_{th1} \frac{R_4}{R_4 + R_3 + R_{th1}} = V_{in} \frac{R_2}{R_1 + R_2} \frac{R_4}{R_4 + R_3 + R_{th1}} \tag{1.32}$$
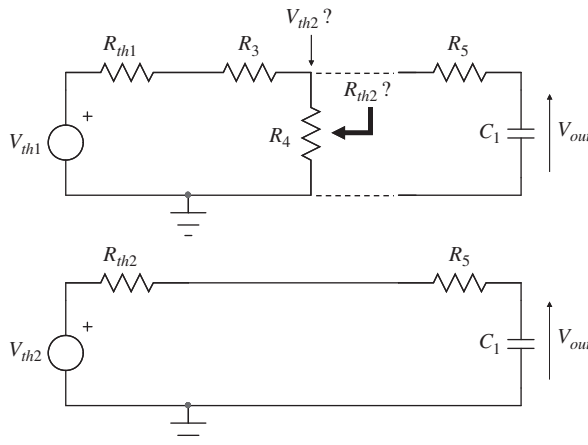

Figure 1.23   The Thévenin output resistance is found by looking into the output port, across R_4:
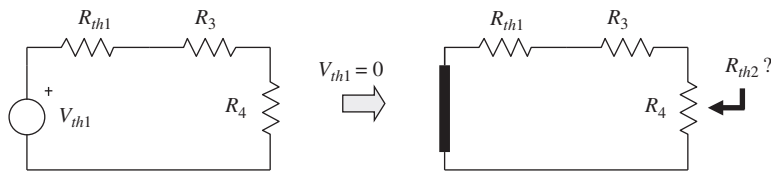
Figure 1.24 The first Thévenin generator is updated with the presence of R_3 and R_4:

The output resistance is found by setting V_{th1} to 0 and looking into R_4 terminals to obtain the resistance while R_4 remains in place (Figure 1.24).

$$R_{th2} = (R_{th1} + R_3) \| R_4 \tag{1.33}$$

The final circuit appears in the low side of Figure 1.23 where, again, a simple voltage divider appears. Its transfer function is that of the low-pass filter in the lower left corner of Figure 1.16 where the resistance is the sum of R_{th2} and R_5:

$$\frac{V_{out}(s)}{V_{th2}(s)} = \frac{1}{1 + s(R_{th2} + R_5)C_1} \tag{1.34}$$

V_{th2} must be replaced by its definition in (1.32) with V_{in} and $R_{th1/2}$ expressions brought back in (1.34). After the update, the final expression is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{R_2}{R_1 + R_2} \cdot \frac{R_4}{R_4 + R_3 + R_1 \| R_2} \cdot \frac{1}{1 + s\left[\left(R_1 \| R_2 + R_3 \right) \| R_4 + R_5 \right] C_1} \tag{1.35}$$

It is a rather large equation but we don't know if it is correct yet. Let's try a different approach. If we look at (1.34), the denominator expression includes a term in which C_1 is multiplied by a resistance, $R_{th2} + R_5$. The resulting RC term is a time constant. If we refer to our first steps when looking into ports (Figure 1.7), we said that the resistance 'seen' by the capacitor when looking into its port is further associated with the capacitor to form a time constant denoted τ. Well, let's try to do the same with our complex circuit from Figure 1.20. When calculating output impedance/resistance, the excitation source V_{in} plays no role and can be turned off. Turning off a voltage source is equivalent to replacing it with a short circuit, a 0-V source. We will see later a more rigorous explanation for this fact, let's accept it now. Once V_{in} is replaced by a strap and capacitor C_1 removed from the circuit, Figure 1.25 appears.

With a simple drawing like that, inspection is child's play. If we start from the left, we see R_1 paralleled with R_2, then in series with R_3 and the whole is paralleled with R_4. This total resistance is in series with R_5. Finally:

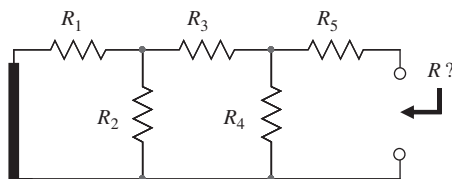$$R = R_5 + \left(R_1 \| R_2 + R_3 \right) \| R_4 \tag{1.36}$$

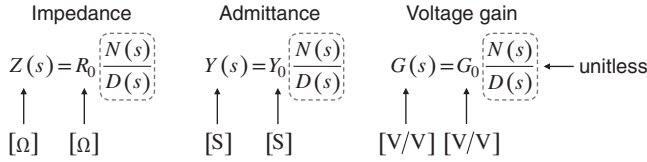**Figure 1.25** What resistance is 'driving' capacitor C_1?

Figure 1.26   In a properly-written transfer function, the leading term carries the unit (if any) while the numerator and the denominator are unitless.

This is the exact same definition we have for the resistive portion of (1.35) time constant. No Thévenin, no complex manipulations were involved to build this expression.

In (1.35), when s equals 0, we talk about dc condition, the 0-Hz response. In some transfer function equations we will derive in this book, the 0-Hz response can be null, infinite or finite as in our case. In (1.35), if you replace s by 0, the right-side denominator becomes 1 and the equation's left term remains alone: this is a dc term whose unit must be that of the transfer function under study. Here, we calculate a gain in [V]/[V] and it has no unit. Should we calculate an impedance, its dimension would be ohms. You mark this dc term by a subscripted 0 when you write it. It is usually accepted that its letter is the same as that of the transfer function you study: A_0 for $A(s)$, H_0 for $H(s)$, G_0 for $G(s)$ and so on. Exception is for R_0 when calculating an impedance $Z(s)$. Figure 1.26 illustrates this fact, valid regardless of the transfer function order.

Below appears the first generalized transfer function of a circuit described by (1.35) that we call H:

$$H(s) = H_0 \frac{1}{1 + s\tau} \tag{1.37}$$

in which

$$H_0 = \frac{R_2}{R_1 + R_2} \frac{R_4}{R_4 + R_3 + R_1 \| R_2} \tag{1.38}$$

and

$$\tau = \left(R_5 + \left(R_1 \| R_2 + R_3\right) \| R_4\right)C_1 \tag{1.39}$$

What physically happens in a circuit under dc condition or at a 0-Hz excitation? A capacitor becomes an infinite resistance (no current flows in it) and an inductor is replaced by a short circuit. When you analyze a circuit under dc conditions, you thus open all capacitors and short all inductors. This is, by the way, what SPICE does when it calculates a bias point prior to starting a simulation whether it is a .TRAN or .AC analysis. You have the corollary that at very high frequencies or infinite frequency, capacitors becomes short circuits and inductors become open circuits. When you analyze a circuit for s approaching infinity, then you short all capacitors and open all inductors from the network. We will come back to these important points, but let's focus on Figure 1.20 where C_1 has been removed. The new diagram appears in Figure 1.27.
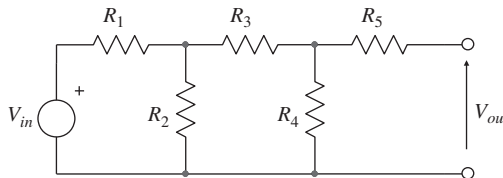

Figure 1.27   In dc conditions, capacitor C_1 is removed as no current flows in it.

In this drawing, R_5 does not play a role as no current flows through it. The dc transfer function is what we already derived in (1.32) when applying Thévenin two times. It is H_0 of (1.38). As a preliminary conclusion, we could have derived (1.35) in two steps, first by considering $s = 0$ and obtaining H_0, then by setting the excitation source to 0 V and looking into the capacitor ports to get the associated time constant.

In this approach, what we calculate is a simple gain involving resistors only (where capacitors or inductors are respectively open or shorted) further followed by an output resistance calculation, the one seen from the capacitor terminals. Assembling these elements according to (1.37) gave the transfer function. These are the first steps towards fast analytical circuit techniques also known as FACTs.

1.2.4 Norton's Theorem at Work

Any 2-port *linear* system made of resistors, capacitors, inductors, dependent or independent current or voltage sources can be represented by an equivalent Norton model. This equivalent circuit is made of a complex current generator I_{th} associated with a complex output impedance Z_{th}. Thévenin and Norton can be used interchangeably depending on the circuit you need to analyze. With similar output impedance Z_{th} in both approaches, I_{th} and V_{th} are linked by the simple formula $I_{th} = V_{th}/Z_{th}$.

Assume the filter shown in Figure 1.28 in which you see an inductor associated with three resistors. r_L symbolizes the inductor equivalent series resistance (ESR), its ohmic losses.

To obtain the transfer function, let's cut the circuit after R_2 and transform the input source involving R_1 and R_2 into a Norton generator. The result appears in Figure 1.29. First, the Norton current is found. This current is either equal to V_{th}/R_{th} or to the short circuit current when a strap is applied across R_2. In this case, the current I_{th} is simply V_{in}/R_1. The output resistance has already been evaluated in previous examples and is equal to the parallel arrangement of R_1 and R_2. Once the Norton transformation is done, you can place the equivalent generator into the circuit as proposed in Figure 1.30. In this case, the output voltage is simply:

$$V_{out}(s) = I_{th}(s)Z_1(s) = \frac{V_{in}(s)}{R_1}\left[R_{th}\|(r_L + sL_1)\right] \tag{1.40}$$

If you now develop this expression and rearrange the terms, you should obtain an expression similar to (1.41):

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{r_L R_2}{R_1 R_2 + r_L(R_1 + R_2)} \frac{1 + s\dfrac{L_1}{r_L}}{1 + s\dfrac{L_1(R_1 + R_2)}{R_1 R_2 + r_L(R_1 + R_2)}} \tag{1.41}$$
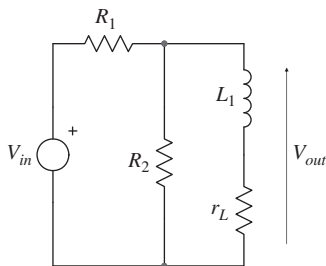

Figure 1.28 Norton's theorem can be applied to obtain the transfer function quickly.
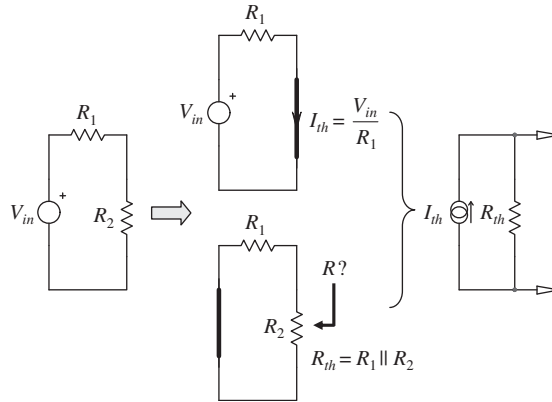
Figure 1.29   The Norton current generator sources current to a series-parallel arrangement involving inductor L_1.
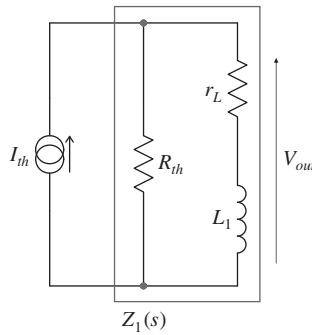

Figure 1.30   The output voltage is simply the current source times impedance Z_1.

We now see two time constants, one is in the numerator while the second lies in the denominator. We can rewrite this transfer function capitalizing on the notation introduced with (1.37):

$$H(s) = H_0 \frac{1 + s\tau_1}{1 + s\tau_2} \tag{1.42}$$

in which

$$H_0 = \frac{r_L R_2}{R_1 R_2 + r_L(R_1 + R_2)} \tag{1.43}$$

$$\tau_1 = \frac{L_1}{r_L} \tag{1.44}$$

and

$$\tau_2 = \frac{L_1}{R_{eq}} \tag{1.45}$$

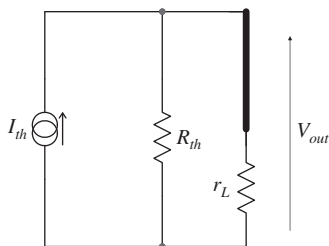where $R_{eq} = \dfrac{R_1 R_2 + r_L(R_1 + R_2)}{R_1 + R_2}$.

Figure 1.31   In dc conditions, the inductor is a short circuit: you replace it by a strap.

Now, rather applying ohm's law as in (1.40), let's see if we can already apply what we learned in the Thévenin example. First, the easiest thing, set s to 0 and solve the dc transfer function H_0. If a capacitor is an open circuit at dc, an inductor becomes a short circuit. In Figure 1.30, short the inductor and you have Figure 1.31. From this figure, the dc gain is immediate:

$$\frac{V_{out}(0)}{I_{th}(0)} = R_{th}\|r_L \tag{1.46}$$

Now substitute R_{th} and I_{th} definitions in (1.46) to obtain:

$$H_0 = \frac{(R_1\|R_2)\|r_L}{R_1} \tag{1.47}$$

No special development or rearrangement was necessary here. If you check, (1.47) is the same as (1.43). Should you start from Figure 1.28 instead and short the inductor in dc, you would find another definition for H_0, equal to (1.47) but expressed differently:

$$H_0 = \frac{r_L\|R_2}{(r_L\|R_2) + R_1} \tag{1.48}$$

In these above expressions, (1.47) and (1.48), resistors appear in an ordered series-parallel arrangement. This is not the case for (1.43) in which resistors are combined with each other without a noticeable relationship between them. An ordered arrangement helps gain insight into the formula without rearranging elements. For instance, in (1.47), you see that if r_L goes to infinity, the dc gain reduces to that of a simple voltage divider involving R_1 and R_2. Even simpler in (1.48) where H_0 simplifies immediately to $R_2/(R_1 + R_2)$. Equation (1.43) does not offer the same immediate insight; you would need to factor r_L and make it infinite to simplify the formula. In other words, you would need more effort to rearrange the complex formula and get the response you want. In that respect, (1.47) and (1.48) are designated as *low-entropy* expressions by analogy to thermodynamic laws.

The entropy of a system qualifies its degree of internal disorder: to produce the work the system has been designed for, you need to bring less external energy when its entropy is low. In our equations, with well-organized, well-ordered constitutive elements, insight is immediate and no further work is required to unveil gains, poles or zeros positions. On the other hand, in a *high-entropy* equation, where elements are in disordered form, you need to spend more energy to rearrange terms and reveal key relationships. We will see that FACTs naturally deliver low-entropy expressions whereas brute-force analysis often produces a correct but abstruse result.

Now that we have the dc gain H_0, let's go back to (1.42). Compared to (1.37), this time, we have two time constants. One is in the numerator while the other lies in the denominator. In Chapter 2, we will

learn that transfer functions are combining gains, poles and zeros. Without disclosing too many details now, zeros appear in the transfer function numerator N while poles are in the denominator D. In other words, τ_1 in (1.42) corresponds to the zero time constant while τ_2 characterizes the pole time constant. As already highlighted, both time constants involve a resistive term driving the considered element (C or L) that we sometimes can find by inspection.

The mathematical definition of a zero in a function $f(x)$ is the value of x for which f returns 0. In a transfer function, a zero noted s_z represents the root of the numerator N. When a network featuring zeros is evaluated at $s = s_z$, the numerator N of the corresponding transfer function cancels:

$$N(s_z) = 0 \tag{1.49}$$

For instance, in (1.41), when $s = -\frac{r_L}{L}$, a real value in the complex plane, the numerator equals 0. In this condition, the transfer function linking the response signal to the driving signal also returns 0:

$$\frac{V_{out}(s_z)}{V_{in}(s_z)} = \frac{N(s_z)}{D(s_z)} = \frac{0}{D(s_z)} = 0 \tag{1.50}$$

If the transfer function is 0 at $s = s_z$, then despite the presence of a driving signal V_{in}, the response V_{out} is also 0. From this simple observation, we can infer that the presence of a zero in a transfer function implies that the response is *nulled* when the *transformed* network is examined at $s = s_z$. Figure 1.32 illustrates this fact through a simple drawing.

The word *transformed* means that all energy-storing elements are replaced by their impedance expressed in the Laplace domain as shown in Figure 1.33. If the response is a null while a driving signal exists, it means that the excitation does not reach the output and is lost somewhere in the *transformed* network examined at $s = s_z$. Figure 1.34a and b illustrates two cases leading to $V_{out} = 0\,\text{V}$ in this particular condition.

A null in the response implies that no current circulates in resistor R_1 hence the label $I_{out}(s_z) = 0$. If you observe Figure 1.34a, the absence of current in R_1, despite the presence of a driving signal, is due to the series network Z_1 becoming a *transformed open* for $s = s_z$. The presence of this series infinite impedance blocks all current circulation and induces an output null at $s = s_z$. In Figure 1.34b, a current circulates in resistor R_2 but a *transformed short circuit* diverts all of it from resistor R_1 to ground, nulling the output. By observing the conditions for which an output null is created in the transformed circuit, we have the possibility to obtain the transfer function zeros just by inspecting the network.

Back to Figure 1.30 or Figure 1.28, what circuit association could bring a null to the output when the network is evaluated at $s = s_z$? R_{th} is fixed and frequency-invariant. However, the series association of L_1 and r_L could perhaps be a transformed short circuit at a certain s? The impedance of this network is:
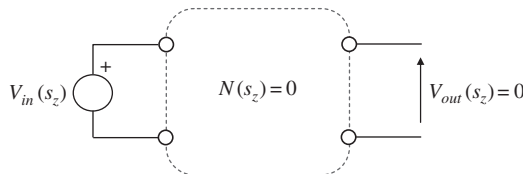
$$Z(s) = r_L + sL_1 \tag{1.51}$$

Figure 1.32 For $s = s_z$ the numerator of a transfer function featuring a zero cancels and the response is nulled.
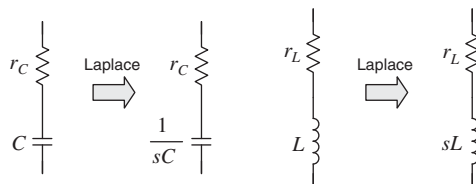
Figure 1.33 In the transformed world, capacitive and inductive elements must be replaced by their Laplace impedance expressions.

For what value of s will this expression be 0? In other words, what is the root of this equation? You have to solve:

$$0 = r_L + sL_1 \tag{1.52}$$

which leads to

$$s_z = -\frac{r_L}{L_1} \tag{1.53}$$

This is a complex root whose magnitude is:

$$\omega_z = |s_z| = \frac{r_L}{L_1} \tag{1.54}$$

In the next chapters, we will learn that:

$$\tau_1 = \frac{1}{\omega_z} = \frac{L_1}{r_L} \tag{1.55}$$

Now, if you go to the laboratory and solder a resistor in series with an inductor then drive the obtained element with an ac current source, there is no way you will cancel the response (the voltage across the network). Actually, as (1.53) suggests with this real zero, the only way to make the transformed impedance equal a short circuit would be to consider s in the entire complex plane and not only along the imaginary axis as we do when we set $s = j\omega$. The method offered above is thus an abstraction which translates the mathematical definition of a zero into the Laplace-transformed world. Despite its lack of physical significance, it is an extremely useful way to identify zeros and will be heavily used in what we will later call the *Null Double Injection* (NDI). By the way, an output null can be physically produced at a 0-Hz frequency when you have a zero at the origin as the origin is common to both real
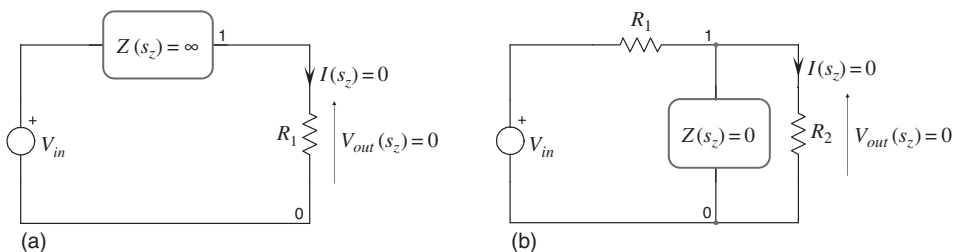

Figure 1.34 In the transformed circuit, when s equals s_z, a series infinite impedance or a transformed short circuit to ground prevents the driving signal from reaching the output and creates a null in the response: $V_{out}(s_z) = 0$
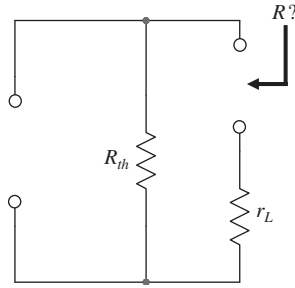
Figure 1.35 When the excitation signal is a current source, turning it off is similar to removing it from the circuit.

and imaginary axes. This is the case in a circuit where a capacitor lies in series with the signal path, for instance, or an inductor is paralleled with the response signal. The other case in which a null can be physically obtained is with a highly underdamped notch filter. As the transfer function numerator quality factor increases, the zero-pair approaches the imaginary axis and zeros become pure imaginary conjugates. When you excite this filter at a frequency f_z where both zeros are located, you truly observe a null in the output.

To find the second time constant τ_2, we can apply what we already learned: we suppress the excitation signal (no role in output resistances definitions) and look at the resistance that drives L_1. If we apply this concept to Figure 1.30, the output resistance seen at the inductor terminals does not depend on the current source I_{th}. We can then turn it to 0 A. Turning an independent current source off is similar to removing it from the circuit thus leaving an open circuit in place. This is what Figure 1.35 suggests.

What resistance do you see from the inductor terminals? r_L in series with R_{th}. If you replace R_{th} by its definition from Figure 1.29, you have:

$$R = r_L + R_{th} = r_L + \left(R_1 \| R_2\right) \tag{1.56}$$

The second time constant is thus:

$$\tau_2 = \frac{L_1}{r_L + \left(R_1 \| R_2\right)} \tag{1.57}$$

Should you do the same in Figure 1.28 but shorting V_{in} instead (excitation is 0 V) and look at the inductor port resistance you see, you will find (1.56).

Now associating (1.48), (1.55) and (1.57), we can write the transfer function describing Figure 1.28 in a normalized form. This is truly a low-entropy expression:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{r_L \| R_2}{\left(r_L \| R_2\right) + R_1} \frac{1 + s\dfrac{L_1}{r_L}}{1 + s\dfrac{L_1}{\left(R_1 \| R_2\right) + r_L}} \tag{1.58}$$

We can even rearrange it in a more readable format, where a zero and a pole now appear:

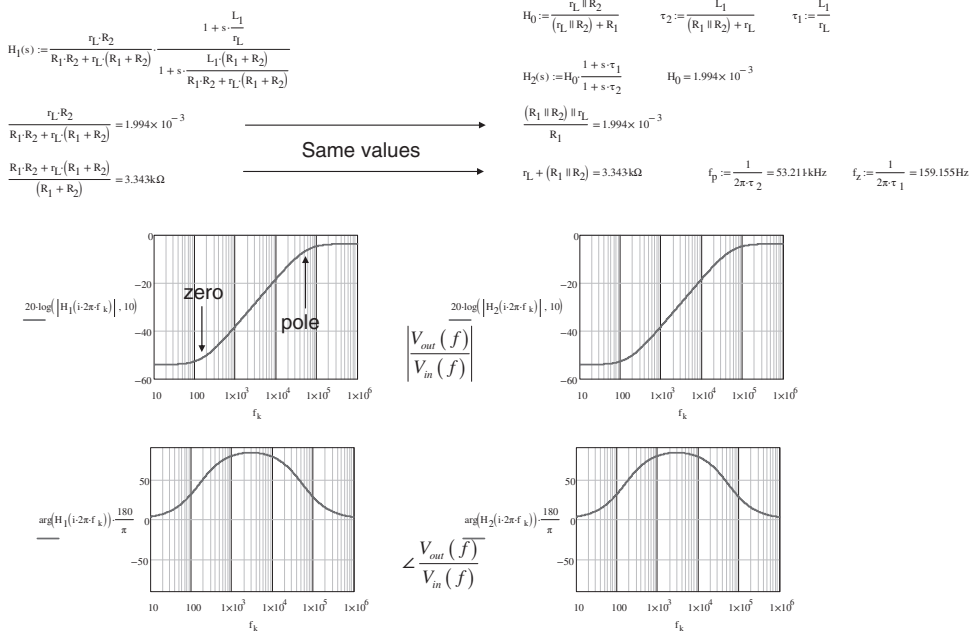$$\frac{V_{out}(s)}{V_{in}(s)} = H_0 \frac{1 + \dfrac{s}{\omega_{z_1}}}{1 + \dfrac{s}{\omega_{p_1}}} \tag{1.59}$$

$$H_1(s) := \frac{r_L \cdot R_2}{R_1 \cdot R_2 + r_L \cdot (R_1 + R_2)} \cdot \frac{1 + s \cdot \dfrac{L_1}{r_L}}{1 + s \cdot \dfrac{L_1 \cdot (R_1 + R_2)}{R_1 \cdot R_2 + r_L \cdot (R_1 + R_2)}}$$

$$H_0 := \frac{r_L \parallel R_2}{(r_L \parallel R_2) + R_1} \qquad \tau_2 := \frac{L_1}{(R_1 \parallel R_2) + r_L} \qquad \tau_1 := \frac{L_1}{r_L}$$

$$H_2(s) := H_0 \frac{1 + s \cdot \tau_1}{1 + s \cdot \tau_2} \qquad H_0 = 1.994 \times 10^{-3}$$

$$\frac{r_L \cdot R_2}{R_1 \cdot R_2 + r_L \cdot (R_1 + R_2)} = 1.994 \times 10^{-3}$$

Same values →

$$\frac{(R_1 \parallel R_2) \parallel r_L}{R_1} = 1.994 \times 10^{-3}$$

$$\frac{R_1 \cdot R_2 + r_L \cdot (R_1 + R_2)}{(R_1 + R_2)} = 3.343 \text{k}\Omega$$

Same values →

$$r_L + (R_1 \parallel R_2) = 3.343 \text{k}\Omega \qquad f_p := \frac{1}{2\pi \cdot \tau_2} = 53.211 \text{kHz} \qquad f_z := \frac{1}{2\pi \cdot \tau_1} = 159.155 \text{Hz}$$

Figure 1.36   Ac responses from the low and high entropy equations are identical.

where

$$H_0 = \frac{r_L \| R_2}{(r_L \| R_2) + R_1} \tag{1.60}$$

$$\omega_{z_1} = \frac{1}{\tau_1} = \frac{r_L}{L_1} \tag{1.61}$$

$$\omega_{p_1} = \frac{1}{\tau_2} = \frac{(R_1 \| R_2) + r_L}{L_1} \tag{1.62}$$

To verify our calculations, we have captured these equations into a Mathcad® sheet and plotted the ac response. Results appear in Figure 1.36.

In the upper left corner is the high-entropy expression whose ac response is plotted below. The right side shows the low-entropy version involving the time constants we quickly obtained by inspection. Values returned either way are strictly identical.

1.3   What Should I Retain from this Chapter?

In this first chapter, we have learned key information that are summarized below:

1. A transfer function is a mathematical relationship linking an excitation signal (the input) to a response signal (the output). Excitation and response can appear at different terminals or ports but can also be observed across a common port. This is the case for impedance and admittance transfer functions.

2. A transfer function is usually made of a numerator N and a denominator D but not always. When written in the form of a fraction, the zeros of the transfer function are the numerator roots while poles are the denominator roots.

3. A network featuring storage elements such as capacitors and inductors involve time constants. These time constants imply a resistive term R that 'drives' the concerned capacitor or inductor. This resistance can be observed, in certain conditions, by 'looking' into the considered element terminals while the said element is removed from the circuit. A time constant involving a capacitive term is $\tau = RC$ while a time constant characterizing an inductive term is $\tau = L/R$.

4. When the port output resistance is evaluated, we have seen that the input source does not play a role in the resistance expression. When evaluating a port output resistance, the excitation voltage source is turned off (set to 0 V) and is replaced by a short circuit (a strap). For the dual case, if the excitation source is a current generator, it must be set to 0 A or become an open circuit.

5. Fast Analytical Circuits Techniques (FACTs) consist of expressing a transfer function with the above time constants and gains in a clear and ordered form. This form is said to be of *low entropy* if you can tell where poles, zeros, and gains are located without having to rework the equation.

6. There are several important analysis techniques that you must know and be at ease with to start manipulating complex networks: the voltage divider, the current divider and Thévenin's/Norton's theorems. Superposition sets the foundations for the Extra Element Theorem we will discover in the next chapter.

7. By applying some of the simple techniques explored in this chapter, we were able to derive a transfer function without writing a single equation. In other words, we derived the transfer function by inspection. When circuits are not too complex, writing the transfer function by inspection is a real pleasure!

References

1. V. Vorpérian. *Fast Analytical Techniques for Electrical and Electronic Circuits*. Cambridge University Press, 2002, pp. 15–17.
2. Understand and apply the transimpedance amplifier. Planet Analog blog, http://www.planetanalog.com/document.asp?doc_id=527534&site=planetanalog (last accessed, 12/12/2015).

1.4   Appendix 1A – Finding Output Impedance/Resistance

As exemplified in the introductory figures, finding time constants associated with capacitors or inductors will often involve the derivation of the resistive term that 'drives' the considered capacitor or inductor. Besides capacitors and inductors, the exercise can also involve a simple resistor for which finding the resistance or impedance seen from its terminals is important. In other terms, what resistance is offered from the terminals the considered element is connected to?

There are several known methods to find the output impedance or resistance of a given network. They are reviewed in the appendix below. In the examples, we will use SPICE notations for the sake of simplicity: $1k = 10^3$, $1Meg = 10^6$, $1p = 10^{-12}$, $1n = 10^{-9}$, $1m = 10^{-3}$ and $1u = 10^{-6}$.

The Voltage Output is Divided by Two

For the first option, assume you have a resistive divider made of two resistors driving a capacitor. You have removed the capacitor as in Figure 1.7 and the circuit involving R_1 and R_2 appears in the left side of Figure 1.37. If you load that circuit with a resistance R, the output voltage takes a certain value V_{out}, lower than V_{in}. The drop is incurred to the output resistance we want and the current delivered to the load. If you now load the same circuit with a resistance equal to the circuit output resistance R_{th}, as in

the right side of Figure 1.37, you obtain an output value exactly half of the voltage obtained with no load ($I_{out} = 0$):

$$V_{in} \frac{R_2 \| R_{th}}{R_1 + R_2 \| R_{th}} = \frac{V_{th}}{2} \tag{1.63}$$

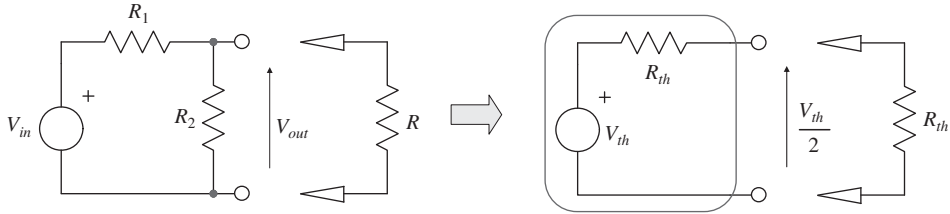This voltage, V_{th}, is the Thévenin voltage and R_{th} the Thévenin output resistance we want.

Figure 1.37 If you load a circuit with a resistance R equal to the output resistance R_{th} of that circuit, the output voltage is divided by 2.

Capitalizing on (1.63), you can write:

$$V_{in} \frac{R_2 \| R_{th}}{R_1 + R_2 \| R_{th}} = \frac{V_{in}}{2} \frac{R_2}{R_1 + R_2} \tag{1.64}$$

In this expression, the input voltage V_{in} does not play a role and disappears from both sides. If you solve (1.64) for R_{th}, you obtain the output resistance we want:

$$R_{th} = \frac{R_1 R_2}{R_1 + R_2} = R_1 \| R_2 \tag{1.65}$$

A Dynamic Output Resistance

A second method consists of calculating the output voltage in relationship to a current injected by the generator I_{out}, $V_{out} = f(I_{out})$. This is the method already introduced in Figure 1.4. Assuming the same two-resistor circuit in Figure 1.38, the output voltage across R_2 can be defined as follows:
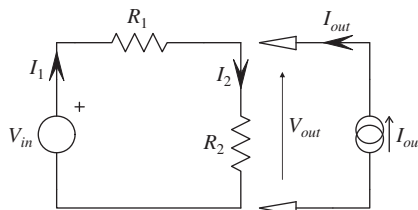
Figure 1.38 If you load the resistive network by a current source, the output voltage drops by a certain quantity, proportional to I_{out} and the network output resistance:

$$V_{out} = V_{in} - R_1 I_1 \tag{1.66}$$

I_1 is made of the output current I_{out} and I_2:

$$I_1 = \frac{V_{out}}{R_2} - I_{out} \tag{1.67}$$

Substituting (1.67) into (1.66):

$$V_{out} = V_{in} - R_1 \left(\frac{V_{out}}{R_2} - I_{out} \right) = V_{in} - \frac{R_1}{R_2} V_{out} + R_1 I_{out} \tag{1.68}$$

Rearranging and factoring V_{out} in the left side leads to:

$$V_{out}(I_{out}) = \frac{V_{in} + R_1 I_{out}}{1 + \dfrac{R_1}{R_2}} \tag{1.69}$$

The incremental or small-signal output resistance is found by differentiating (1.69) with respect to I_{out}:

$$\frac{\mathrm{d}V_{out}(I_{out})}{\mathrm{d}I_{out}} = \frac{R_1 R_2}{R_1 + R_2} = R_1 \| R_2 \tag{1.70}$$

The word *incremental* refers to measurements involving small voltage (dV) and current (dI) variations around a defined operating point. We talk about small variations so that the system remains *linear* when measurements are performed. To that respect, (1.70) is also referred to as the *small-signal* output resistance: the stimulus signal I_{out} is purposely kept of small amplitude so that V_{out}, the response, remains undistorted.
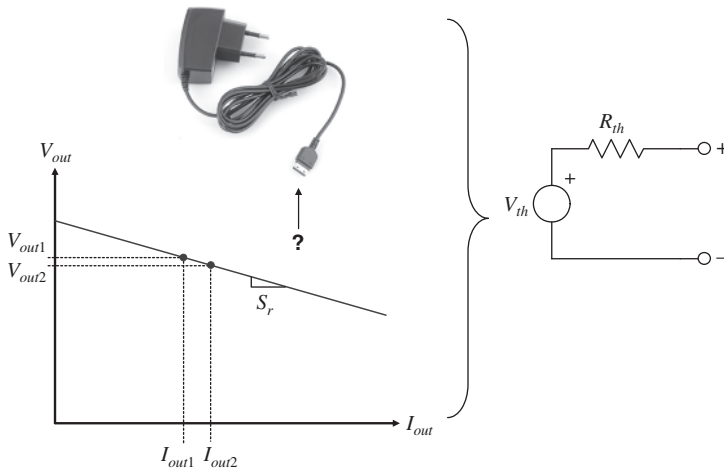
Figure 1.39   The slope of this I-V characteristic is negative. The unit is ohm and is obtained at a given operating point, I_{out1}.

You can find a practical application of (1.70). Assume you want to characterize the dynamic output resistance of a given power supply, such as the simple ac-dc charger in Figure 1.39. This measurement must be performed at the selected operating point of interest. For instance, what is the output

resistance at a 12-V output and a 1-A current? First, measure the power supply voltage at current I_{out1} and record the output value, V_{out1}. Then slightly increase the current to I_{out2}, and record the new output voltage V_{out2}. The output resistance at the given operating point is simply:

$$R_{out} = \frac{V_{out1}(I_{out1}) - V_{out2}(I_{out2})}{I_{out1} - I_{out2}} \qquad (1.71)$$

To make sure you keep the power supply in a linear zone, the output current variation at which the two output voltages are recorded must remain small. In other words, I_{out2} must be close to I_{out1}, perhaps 1 A and 1.1 A. Mathematically speaking, you performed a differentiation of the output voltage with respect to the output current at $I_{out} = I_{out1}$:

$$\lim_{I_{out2} \to I_{out1}} \frac{V_{out}(I_{out2}) - V_{out}(I_{out1})}{I_{out2} - I_{out1}} = \frac{\mathrm{d}V_{out}(I_{out})}{\mathrm{d}I_{out}} \qquad (1.72)$$

What you obtain with (1.72) is the linear or the small-signal dc or static output resistance of your converter measured at a given output current, 1 A in this example. Please note that (1.71) returns a negative value simply because I_{out} leaves the output port rather than entering it as in Figure 1.38. However, having a voltage drop across R_{th} that is proportional to the output current is the result of a positive resistance.

Setting the Source Contribution to Zero Volts

All elements involved in Figure 1.37 are linear. The source itself, V_{in}, is considered a perfect voltage generator with a zero output resistance. When we load this circuit, V_{in} remains constant. Again, considering the differentiation, we can write $\frac{\mathrm{d}V_{in}(I_{out})}{\mathrm{d}I_{out}} = 0$: the source contribution to calculating the small-signal output resistance or impedance is 0. Therefore, when we calculate the output resistance (or impedance) of a linear circuit in which a generator is involved, we can set the generator to 0 V or replace it by a strap. Should we need to repeat the exercise with a current generator in the circuit, setting the current to 0 A would be the same as disconnecting the current source from the circuit. Please note that controlled sources must not be put to 0 for this type of analysis.

This third method is exemplified in Figure 1.40 where V_{in} is set to 0 V and replaced by a short. The output resistance is found by looking at the resistance across R_2 terminals, while R_2 remains in place:

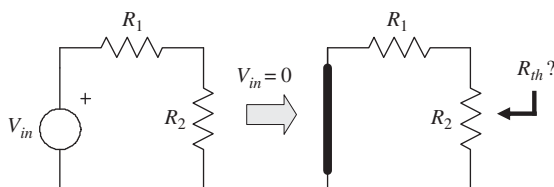$$R_{th} = R_1 \| R_2 \qquad (1.73)$$

Figure 1.40 The Thévenin output resistance is found by looking into the output port, across R_2.

A similar result to that of (1.65) and (1.70).

It works nicely also when storage elements are added to the circuit as in Figure 1.41a. The output impedance is found by setting the source to 0 V as shown in Figure 1.41b. The impedance is made of

R_1 paralleled with C_1:

$$Z_{th}(s) = R_1 \| \frac{1}{sC_1} \tag{1.74}$$

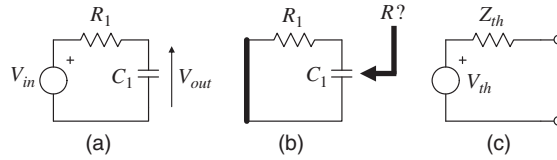(a)   (b)   (c)

Figure 1.41   A simple 1st-order network featuring a capacitor offers a frequency-dependent output impedance.

The equivalent Thévenin circuit appears in the right side of the figure, its generator value is:

$$V_{th}(s) = V_{in}(s) \frac{\dfrac{1}{sC_1}}{\dfrac{1}{sC_1} + R_1} = \frac{1}{1 + sR_1C_1} \tag{1.75}$$

The Short Circuit Current

The fourth and last method involves the short circuit current. In Figure 1.42, a Thévenin equivalent circuit is drawn. If you short circuit its output terminals, you have a current equal to:

$$I_{sc} = \frac{V_{th}}{R_{th}} \tag{1.76}$$

From an unknown circuit, if you have V_{th} and calculate or measure the short circuit current I_{sc}, you can find the Thévenin resistance. In Figure 1.37, the output voltage across R_2 is the circuit Thévenin voltage equal to:

$$V_{th} = V_{in} \frac{R_2}{R_1 + R_2} \tag{1.77}$$

If you now short circuit the output as shown in Figure 1.43, the current is simply:

$$I_{sc} = \frac{V_{in}}{R_1} \tag{1.78}$$
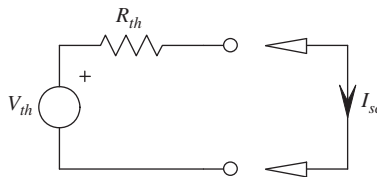
Figure 1.42   The short circuit current of a Thévenin equivalent circuit is the Thévenin voltage V_{th} divided by resistance R_{th}.
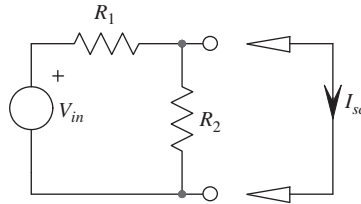
Figure 1.43 The Thévenin output resistance can also be found by calculating the short circuit current.

By applying (1.76), the Thévenin resistance is derived as:

$$R_{th} = \frac{V_{th}}{I_{sc}} = \frac{V_{in} \dfrac{R_2}{R_1 + R_2}}{\dfrac{V_{in}}{R_1}} = \frac{R_1 R_2}{R_1 + R_2} = R_1 \| R_2 \tag{1.79}$$

Dependent Sources

So far we have drawn circuits in which one single independent source was used, the V_{in} generator. Assume Figure 1.44 example in which a dependent source now appears in parallel with R_3. The term 0.19 has the dimension of siemens. What resistance drives capacitor C_1?
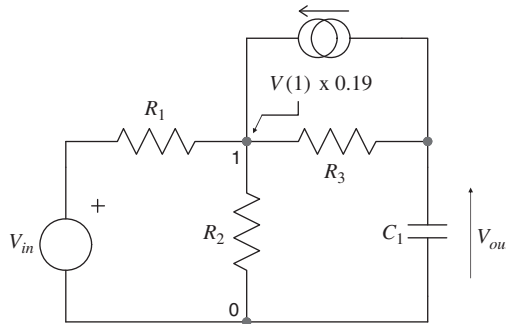
Figure 1.44 The presence of the dependent current source does not modify the circuit analysis: only the independent source is set to 0.

To find the answer, we can still set V_{in} to 0 but the controlled current source remains untouched as we previously said: it depends on $V(1)$, not V_{in}. Should it depend on V_{in} instead then it would be another *dependent* source and putting V_{in} to 0 would naturally remove that current source from the circuit.

The updated circuit appears in Figure 1.45. To find the resistance offered by the capacitor terminals, we connect a current test generator as suggested in Figure 1.46 and Figure 1.47. When doing so, we realize that the excitation signal is our current source while the response is the voltage developed across the considered terminals. It complies with our impedance transfer function definition introduced in the beginning of this chapter – see (1.13). The resistance offered by the port in
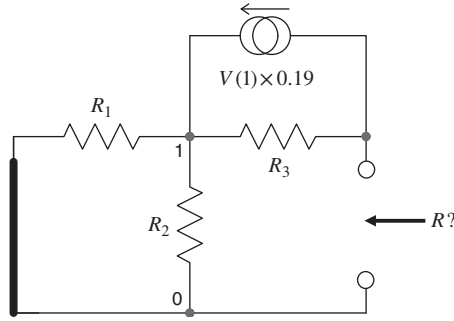
Figure 1.45 The independent source V_{in} is classically set to 0 V but the dependent source remains in the sketch:

Figure 1.47 is thus

$$R = \frac{V_T}{I_T} \tag{1.80}$$

From Figure 1.46 right side, we can write that the current flowing in the paralleled arrangement of R_1 and R_2 (R_{eq}) is:

$$I_{Req} = I_3 + 0.19 \cdot V(1) \tag{1.81}$$

with

$$R_{eq} = R_1 \| R_2 \tag{1.82}$$

The current flowing in R_{eq} is node (1) voltage divided by R_{eq}. Updating (1.81), we have:

$$\frac{V(1)}{R_{eq}} - 0.19 \cdot V(1) = I_3 \tag{1.83}$$
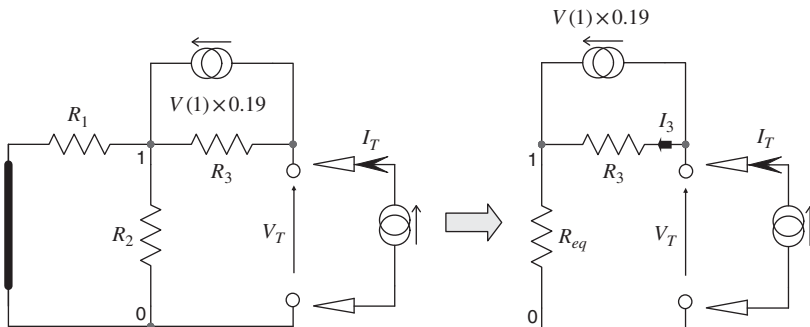
Figure 1.46 A current test generator is now biasing the capacitor terminals to determine its driving resistance.

The test voltage V_T is equal to the voltage across R_{eq}, V(1), plus the drop across R_3:

$$V_T = V(1) + I_3 R_3 = V(1) + V(1)R_3 \left(\frac{1}{R_{eq}} - 0.19 \right) \tag{1.84}$$
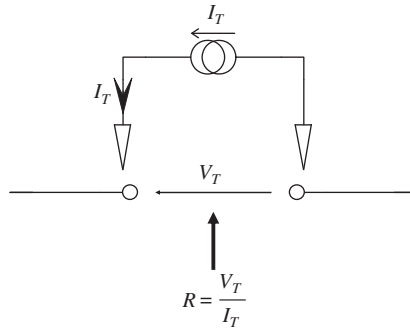
Figure 1.47 The test generator helps find the resistance offered by the terminals at which current (excitation) and voltage (response) are simultaneously observed.

$V(1)$ is the voltage across R_{eq} whose current is the test generator I_T. Therefore, $V(1)$ is equal to:

$$V(1) = I_T R_{eq} \tag{1.85}$$

Updating (1.84) with (1.85), leads to the definition of V_T:

$$V_T = I_T R_{eq}\left[1 + R_3\left(\frac{1}{R_{eq}} - 0.19\right)\right] \tag{1.86}$$

The resistance seen by the capacitor terminals is obtained by rearranging (1.86) in a transfer function form:

$$R = \frac{V_T}{I_T} = R_3 + \left(R_1\|R_2\right)(1 - 0.19R_3) \tag{1.87}$$

The time constant associated with capacitor C_1 is thus:

$$\tau = \left[R_3 + \left(R_1\|R_2\right)(1 - 0.19R_3)\right]C_1 \tag{1.88}$$

This example shows that a network involving controlled sources requires the use of KVL and KCL compared to other networks whose characteristics were derived by inspection only.

A Transistor-Based Circuit

A transistorized circuit is another typical example involving controlled sources. A simple amplifying circuit appears in Figure 1.48. Here, the exercise will consist of finding the resistance driving
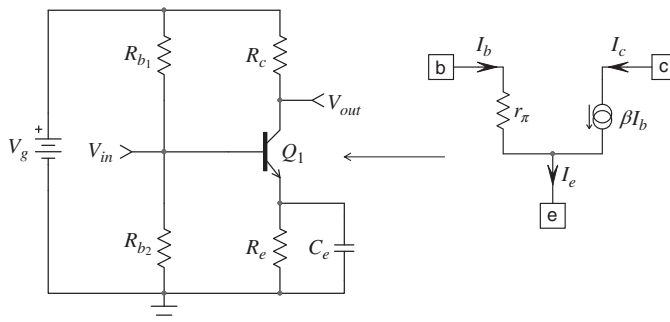
Figure 1.48 A simple amplifier built around a bipolar circuit.

capacitor C_e when that capacitor is removed from the circuit. Before proceeding, Q_1 is replaced by its (simplified) small-signal equivalent circuit, the hybrid-π model, that appears in the right side of the figure.

The excitation signal is the V_{in} source applied at the bias bridge made of R_{b1} and R_{b2}. To find the resistance seen at capacitor C_e terminals, V_{in} is turned off and its terminals are strapped. V_g is a dc supply and in this example, its ac contribution to the circuit is 0. You can imagine that V_g is decoupled by an infinite value capacitor so that R_{b1} and R_c upper terminals are at the ground level in ac: V_g is also replaced by a strap for the ac analysis. The updated circuit is shown in Figure 1.49.
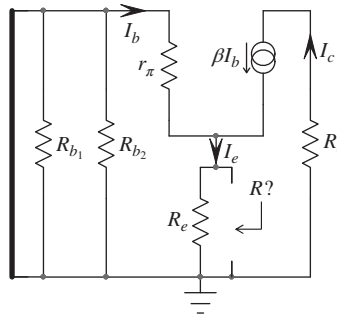
Figure 1.49   With a 0-V excitation voltage, the equivalent circuit nicely simplifies.

Further rearranging the network leads to a rather simple circuit as drawn in Figure 1.50. Here, you can observe that resistance R_e is connected in parallel with the capacitor terminals. It can therefore be temporarily removed from the analysis and, once the resistance seen from the terminals is identified, the final expression will bring R_e back in parallel with the intermediate result.

First, let's express the base current I_b equal to

$$I_b = -\frac{V_R}{r_\pi} \tag{1.89}$$

I_1 depends on the collector current as:

$$I_1 = (\beta + 1)I_b = -I_T \tag{1.90}$$

The intermediate resistance seen at the capacitor terminals is simply the ratio of V_R by the test current I_T:

$$R_{\text{int}} = \frac{V_R}{I_T} = \frac{r_\pi}{\beta + 1} \tag{1.91}$$

Bringing R_e back in the circuit gives the resistance seen at the capacitor terminals:

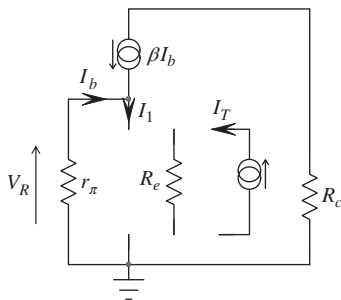$$R = R_e \| \left(\frac{r_\pi}{\beta + 1} \right) \tag{1.92}$$

Figure 1.50   The rearranged circuit reduces to a simple network.

The time constant of this circuit is now immediately available:

$$\tau = C_e \left[R_e \| \left(\frac{r_\pi}{\beta + 1} \right) \right] \tag{1.93}$$

SPICE Can Help Verify Results

In some complex circuits, the output resistance you have derived can be made of several series-paralleled combinations and a mathematical solver such as Mathcad® can be of great help to obtain the result quickly. However, how do you know if your derivation is correct? A SPICE simulator can help verify results quickly.

Assume the circuit in Figure 1.51 in which an inductor is inserted into a resistive circuit. What we want is the resistance 'seen' from the inductor terminals. Otherwise stated, what is the output resistance driving the inductor when the source is set to 0 V? We can see that resistance r_L is in series with L, this is the first term. Then, the left inductor terminal goes to ground via the paralleled combination of R_1 and R_2 and returns to the right terminal through R_3:

$$R = r_L + R_2 \| R_1 + R_3 \tag{1.94}$$
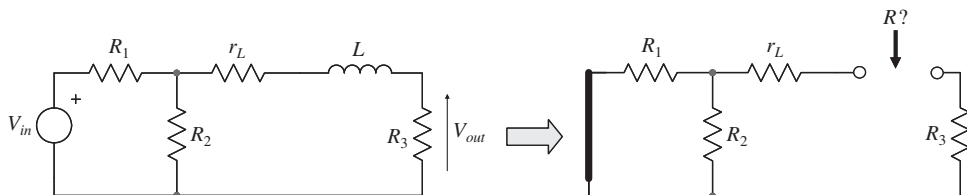
Figure 1.51   Find the resistance offered by the inductor terminals when the component is removed.
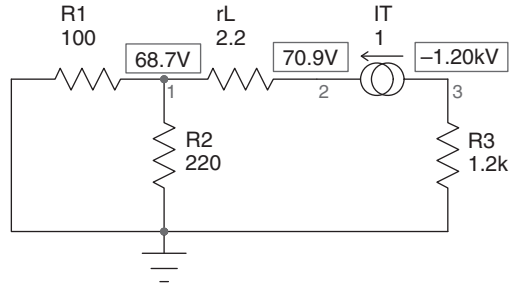
Figure 1.52 A SPICE dc simulation will give you the resistance seen from the inductor terminals.

If we apply Figure 1.52 values to (1.94) we find:

$$R = 2.2 + \frac{220 \times 100}{220 + 100} + 1.2k = 1270.95\,\Omega \qquad (1.95)$$

The simulation circuit uses a 1-A test source I_T injecting current into the inductor terminals when the source is set to 0 V. Involving a dc operating point simulation, the figure gives a voltage difference equal to $70.95 - (-1.2k) = 1270.95\,V$. Considering the 1-A generator, the resistance seen from the terminals is $1270.95\,\Omega$ as calculated by SPICE.

A similar exercise can be run on Figure 1.45 circuit where I_2, the test generator, injects 1 A into the capacitor terminals. With component values such as those labeled in Figure 1.53, the resistance seen from the capacitor port is equal to:

$$R = 2.2 + \left(22\|60\right)\left(1 - 0.19 \times 2.2\right) = 2.2 + 16.09756 \times 0.582 = 11.56878\,\Omega \qquad (1.96)$$
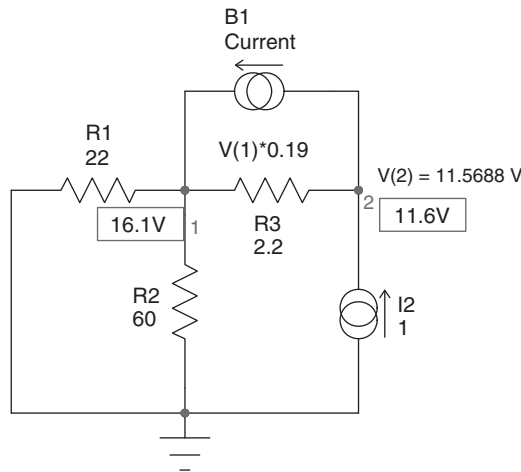
Figure 1.53 The SPICE simulation of the circuit involving the controlled current source confirms hand-calculated results.

The value rounded by the simulator in Figure 1.53 is 11.5688 V.

The technique involving SPICE is extremely useful when you deal with large and complex networks, especially those with a lot of dependent sources. Externally biasing the storage element terminals with the 1-A current generator and running a quick .OP bias point analysis has proven to be extremely efficient to trap errors and flaws in the analysis. Highly recommended!

1.5   Appendix 1B – Problems

We have gathered simple to more complex sketches in which you are asked to determine the dc transfer function and the resistance driving the storage element. Answers are at the end.
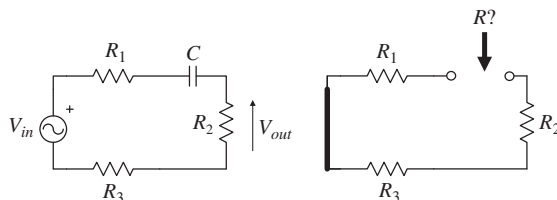
Figure 1.54   – Problem 1
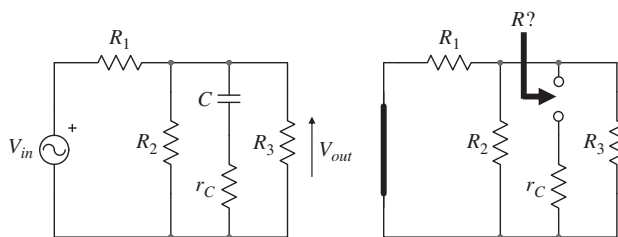
Figure 1.55   – Problem 2
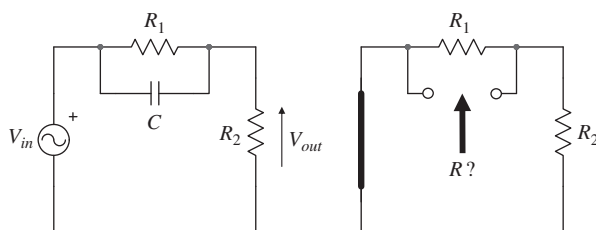
Figure 1.56   – Problem 3
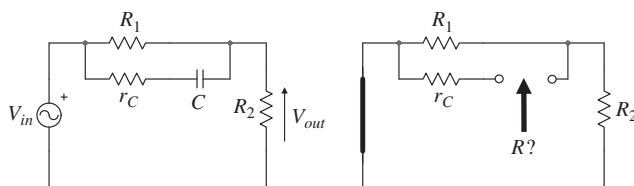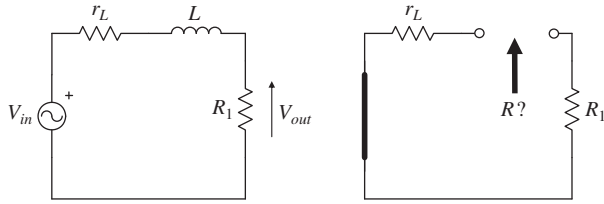
Figure 1.57   – Problem 4
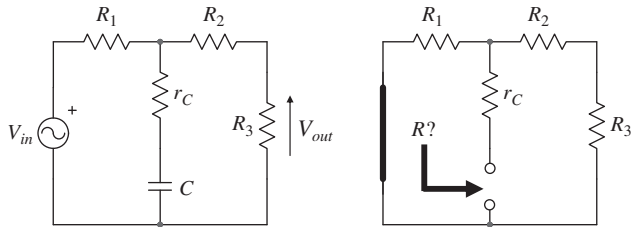
Figure 1.58   – Problem 5
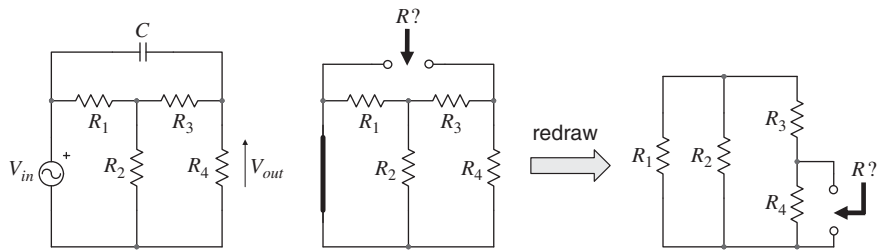

Figure 1.59   – Problem 6

Figure 1.60   – Problem 7
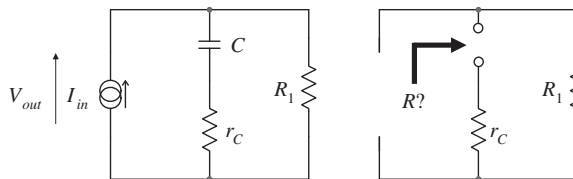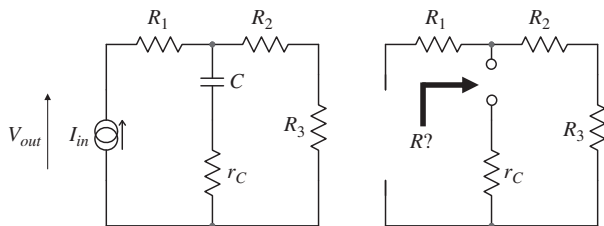

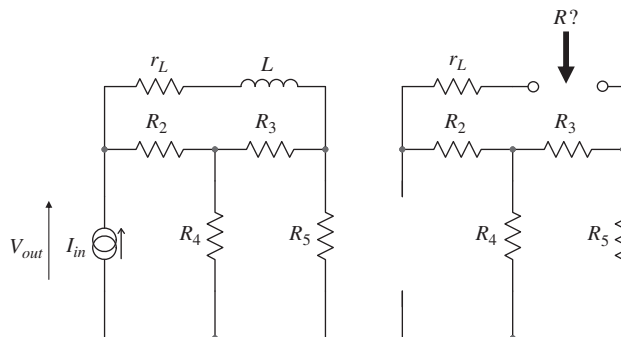**Figure 1.61**   – Problem 8

Figure 1.62   – Problem 9

Figure 1.63 – Problem 10

Answers

Problem 1:
$$R = R_1 + R_2 + R_3$$
$$\tau = (R_1 + R_2 + R_3)C$$
$$H_0 = 0$$

Problem 2:
$$R = \left(R_1 \| R_2 \| R_3\right) + r_C$$
$$\tau = \left[\left(R_1 \| R_2 \| R_3\right) + r_C\right]C$$
$$H_0 = \frac{R_2 \| R_3}{R_2 \| R_3 + R_1}$$

Problem 3:
$$R = R_1 \| R_2$$
$$\tau = \left(R_1 \| R_2\right)C$$
$$H_0 = \frac{R_2}{R_1 + R_2}$$

Problem 4:
$$R = R_1 \| R_2 + r_C$$
$$\tau = \left(R_1 \| R_2 + r_C\right)C$$
$$H_0 = \frac{R_2}{R_1 + R_2}$$

Problem 5:
$$R = r_L + R_1$$
$$\tau = \frac{L}{r_L + R_1}$$
$$H_0 = \frac{R_1}{R_1 + r_L}$$

Problem 6:
$$R = r_C + R_1 \| (R_2 + R_3)$$

$$\tau = \left[r_C + R_1 \| (R_2 + R_3) \right] C$$

$$H_0 = \frac{R_3}{R_1 + R_2 + R_3}$$

Problem 7:
$$R = R_4 \| \left(R_3 + R_1 \| R_2 \right)$$

$$\tau = \left[R_4 \| \left(R_3 + R_1 \| R_2 \right) \right] C$$

$$H_0 = \frac{R_4}{R_4 + R_3 + R_1 \| R_2} \frac{R_2}{R_1 + R_2}$$

Solving by inspection is not possible, use Thévenin's theorem for R_1 and R_2 driving R_3.

Problem 8:
$$R = r_C + R_1$$

$$\tau = (r_C + R_1) C$$

$$R_0 = R_1$$

Problem 9:
$$R = r_C + R_2 + R_3$$

$$\tau = (r_C + R_2 + R_3) C$$

$$R_0 = R_1 + R_2 + R_3$$

Problem 10:
$$R = r_L + R_2 + (R_5 + R_4) \| R_3$$

$$\tau = \frac{L}{r_L + R_2 + (R_5 + R_4) \| R_3}$$

$$R_0 = ?$$

It cannot be found by inspection. Solution in Chapter 3!