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Introduction

1.1 Overview of this Book

The three books in this series deal with *c*-axis-aligned crystalline indium–gallium–zinc oxide (CAAC-IGZO), an oxide semiconductor (see Figure 1.1): *Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Fundamentals* (hereinafter referred to as *Fundamentals*) [1], *Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Application to LSI* (this book, hereinafter referred to as *Application to LSI*), and *Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Application to Displays* (hereinafter referred to as *Application to Displays*) [2]. *Fundamentals* describes, for example, the material properties of oxide semiconductors, the formation mechanism and crystal structure analysis of IGZO, the fundamental physical properties of CAAC-IGZO, the electrical characteristics of field-effect transistors (FETs) with CAAC-IGZO active layer (hereinafter referred to as CAAC-IGZO FETs), and comparisons between CAAC-IGZO and silicon (Si) FETs. *Application to Displays* introduces applications of the CAAC-IGZO FET technology to liquid crystal and organic light-emitting diode displays, describing the process flows and characteristics of the FETs, the driver circuits for displays, the technologies for high-definition, low-power, flexible displays, and so on.

This volume, *Application to LSI*, aims to introduce the applications of CAAC-IGZO FET technology to large-scale integration (LSI) and broadly and concisely review the device physics of CAAC-IGZO FETs. On the basis of the distinct material features of these FETs disclosed in *Fundamentals*, such FETs have an attractive application field in LSIs, in addition to the display applications described in *Application to Displays*. Not only focusing on oxide semiconductor material aspects, this book will also describe device design and fabrication using such materials, combination with other technologies, and specific applications (see Figure 1.2).

Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Application to LSI, First Edition.
Edited by Shunpei Yamazaki and Masahiro Fujita.

Figure 1.1 Framework and summary of the book series

	Base technology	Problems to be solved	Evaluation
Oxide semiconductor material	Defect control	Increase in purity Impurity control	Structural and elemental analysis Film quality measurement
Oxide semiconductor device	Scale-down technology	Optimization of processes and device structures Consistency with current Si LSI manufacturing	Device physics
Combination with other technologies	Combination with passive elements Hybrid three-dimensional structure of oxide semiconductor and Si elements.	Further reduction in F^2 Development of lower-temperature processes Down-scaling issues	Electrical characteristics
Applications: Internet of Things (IoT), 8K television, mobile devices, etc.		Matching interfaces and performance with other systems	Device size Number of processes Power consumption

Figure 1.2 Scope of this book. The symbol F^2 means the square of the feature size F, used as an index of the memory cell size

Application examples of CAAC-IGZO FET technologies to LSIs are specifically described in the subsequent chapters.

1.2 Background

The integrated circuit (IC) has a huge market [3]. As shown in Figure 1.3, the total market size, including analog, micro, logic, and memory applications, is worth approximately 278 billion US dollars. Here, "micro" applications are microprocessor units (MPUs), microcontroller units (MCUs), and digital signal processors (DSPs); "logic" applications include specified logic and custom logic, such as field-programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs). CAAC-IGZO FETs address this vast IC market.

1.2.1 Typical Characteristics of CAAC-IGZO FETs

In the LSI field, reduction of power consumption has so far been achieved mainly by scaling down the FETs, employing advanced power management schemes, and more recently, subthreshold driving. Si FETs are currently scaled down to very small technology nodes, for example, gate lengths as small as 14 and 16 nm [4]. Such aggressive downscaling causes

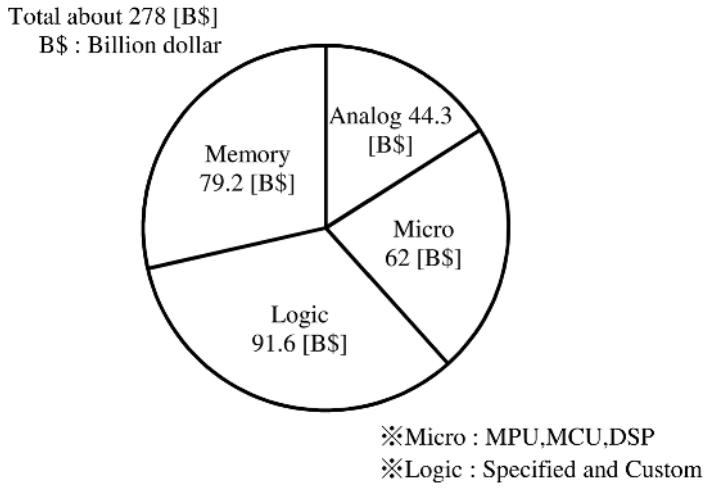


Figure 1.3 Market size of ICs in 2014. *Source*: Adapted from [3]

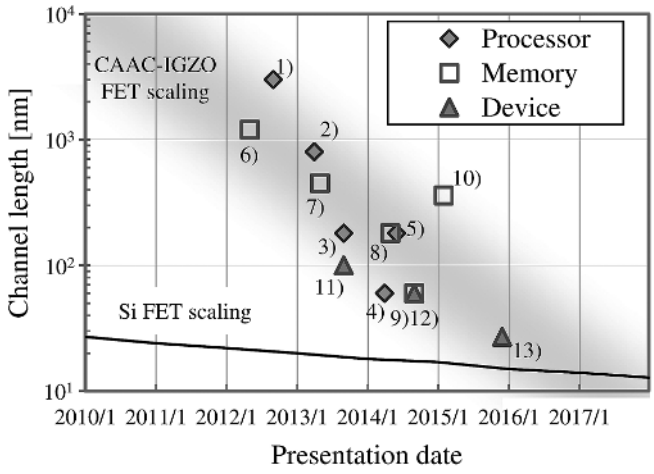
an increase in the FET off-state current (leakage current in the FET in the off state), which poses new obstacles to further reduction of system power [5].

As reported by Kato *et al.* [6], CAAC-IGZO FETs exhibit extremely low off-state current, for example, 1.35×10^{-22} A/μm (135 yA/μm, where y stands for yocto) for a FET with channel length/width of 3/50 μm. In contrast, the off-state current in a single-crystal Si (sc-Si) FET of the same structure and dimensions has an off-state current of 1×10^{-12} A/μm (1 pA/μm), i.e., 10 orders of magnitude larger. When CAAC-IGZO FETs are used in LSI devices, such as dynamic random access memory (DRAM), non-volatile memories, and central processing units (CPUs), their extremely low off-state current will therefore reduce the system power consumption tremendously.

As reported by Matsubayashi *et al.* [7], CAAC-IGZO FETs with a channel node of 20 nm maintain the extremely low off-state current, despite the aggressive downscaling. Figure 1.4 shows the miniaturization progress of CAAC-IGZO and Si FETs during the past four to five years [8]. In the graph, the upper gray band corresponds to the achieved scaling values of CAAC-IGZO FETs, whereas the lower solid line shows the target scaling values of Si FETs disclosed by International Technology Roadmap for Semiconductors [9]. CAAC-IGZO FETs for processors, memories, and devices are denoted by diamond shapes, squares, and triangles, respectively. The number next to each mark corresponds to the conference shown below the graph where the device was disclosed. As shown, the scaling of CAAC-IGZO FETs gradually approaches that of Si FETs in recent years, so if the scaling continues to progress at this speed, it will catch up with that of Si FETs later in 2016 or 2017.

1.2.2 Possible Applications of CAAC-IGZO FETs

CAAC-IGZO FETs can be used in various LSIs (hereinafter called CAAC-IGZO LSIs), for example, in non-volatile memories [10–13], DRAMs [14], normally-off CPUs [15–17], FPGAs [18,19], and image sensors [20,21]. Non-volatile memories and DRAMs employing



Processor:	**Memory:**	**FET:**
1) SSDM 2012	6) IMW 2012	11) SSDM 2013
2) COOL Chips 2013	7) IMW 2013	12) SSDM 2014
3) SSDM 2013	8) IMW 2014	13) IEDM 2015
4) COOL Chips 2014	9) SSDM 2014	
5) VLSI 2014	10) ISSCC 2015	

IEDM : International Electron Devices Meeting
IMW : International Memory Workshop
ISSCC : International Solid-State Circuits Conference
SSDM : International Conference on Solid State Devices and Materials
VLSI : Symposia on VLSI Technology and Circuits

Figure 1.4 Comparison of scaling between CAAC-IGZO FETs and Si FET. *Source*: Adapted from [8].

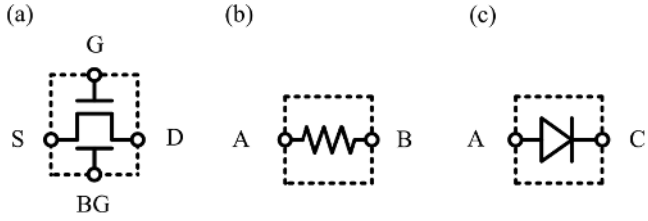


Figure 1.5 (a) CAAC-IGZO FET, an active element with four terminals (source S, drain D, gate G, back gate BG); (b) resistive element, a passive element with two terminals; and (c) diode, a two-terminal passive element with non-linear characteristics

CAAC-IGZO FETs are called non-volatile oxide semiconductor random access memory (NOSRAM) and dynamic oxide semiconductor random access memory (DOSRAM), respectively.

A CAAC-IGZO FET is an active element with four terminals: source, drain, gate, and back gate, as shown in Figure 1.5. New memory technologies that have recently attracted attention

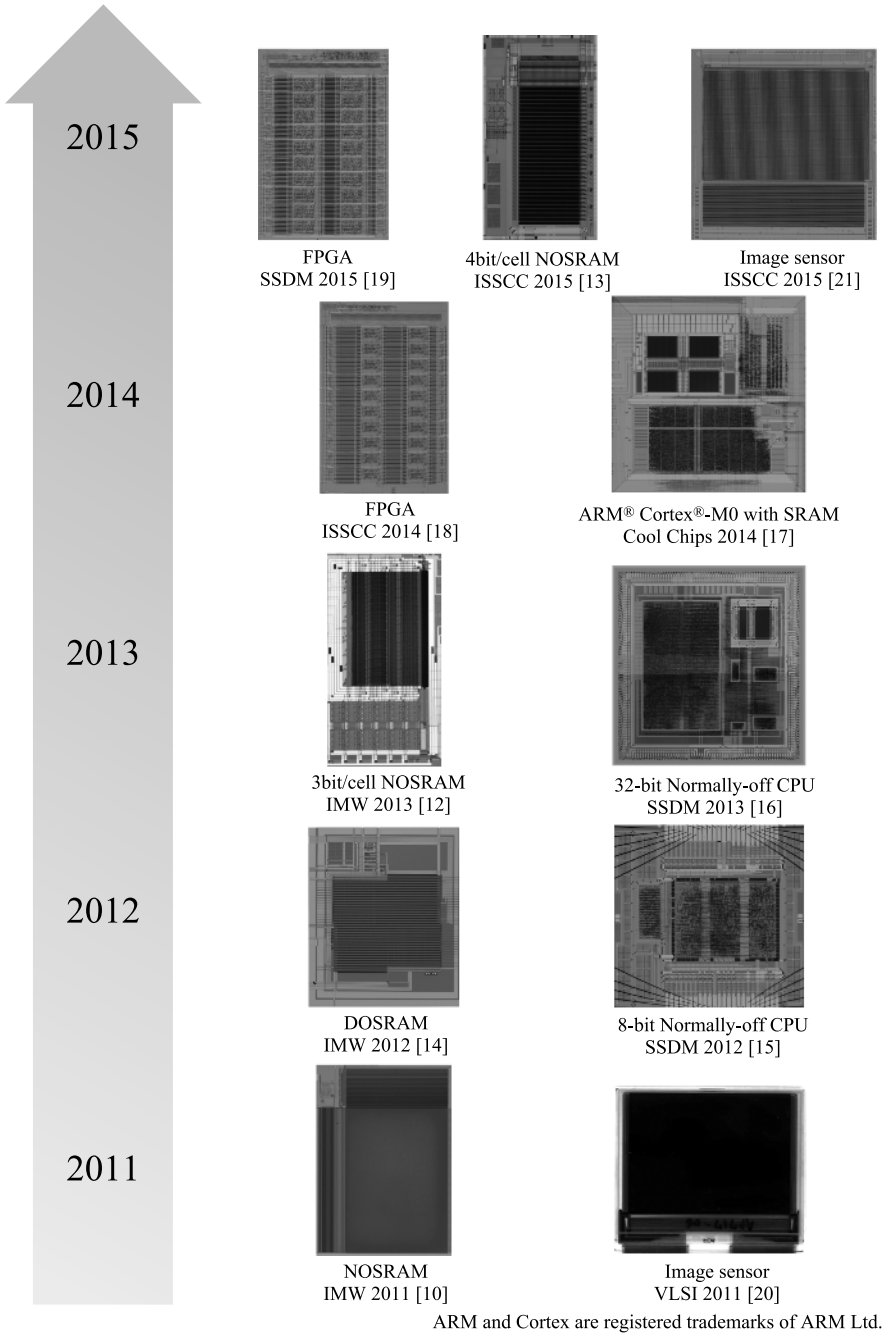


Figure 1.6 Examples of CAAC-IGZO LSIs fabricated between 2011 and 2015. *(For color detail, please see color plate section)*

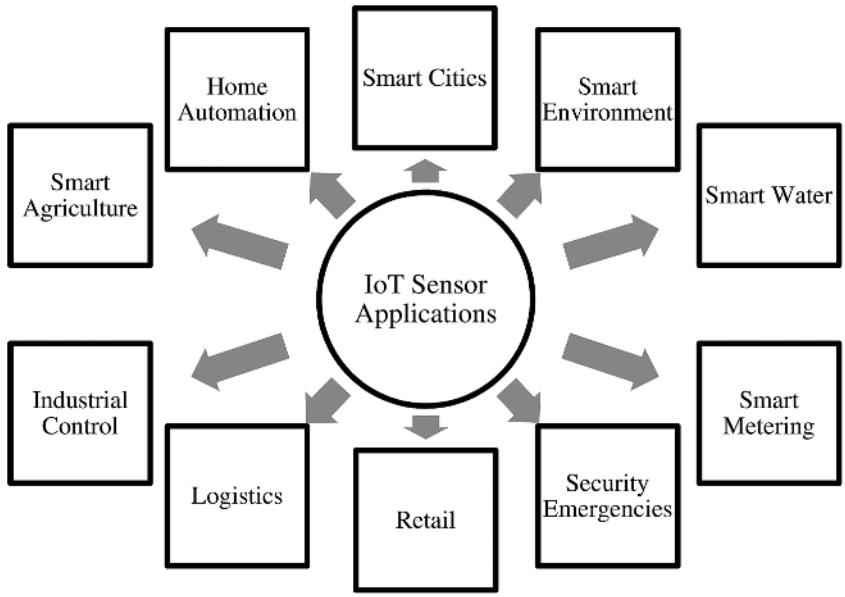


Figure 1.7 Application examples of IoT. *Source*: Adapted from [22,23]

include magnetoresistive random access memory (MRAM), resistive random access memory (ReRAM), phase change random access memory (PCRAM), and ferroelectric random access memory (FeRAM). These are all passive elements with two terminals, whereas CAAC-IGZO FETs with their four terminals may lead to new applications.

Figure 1.6 shows photographs of LSIs with CAAC-IGZO FETs that have been fabricated so far. Below each photograph, the type of LSI and the name of the conference where it was presented are written.

The concept of Internet of Things (IoT) is likely to be realized in the near future. In IoT, LSIs are used in various things to control them and collect and process information through the Internet. LSIs used for IoT should be inexpensive and autonomously powered, i.e., small in size and driven with low power, particularly in the idling state. It is therefore expected that CAAC-IGZO FETs, with their extremely low off-state current, will meet those requirements.

Janusz Bryzek, an advocate of IoT, proposes possible applications of IoT such as logistics, retail, security emergencies, and others (see Figure 1.7) [22,23]. He predicts that a total of one trillion sensors will be used in 2023 (i.e., he forecasts a huge possible market not only for the sensors themselves, but also for the necessary peripheral semiconductor circuits for preprocessing, temporary storage, and wireless transmission).

1.3 Summary of Each Chapter

The device physics, structure, and fabrication process of CAAC-IGZO FETs are briefly explained in Chapter 2, whereas application examples in LSIs and the like are described in and after Chapter 3.

Chapter 2 also includes a review of *Fundamentals*, followed by a description of various CAAC-IGZO FET structures and their basic electrical characteristics, both in general and with emphasis on the low off-state current. CAAC-IGZO FETs are resistant to the downsizing-induced reduction in field-effect mobility or short-channel effect, and unlike sc-Si FETs, the off-state current of CAAC-IGZO FETs does not increase at high temperatures. The possibility of downscaling is illustrated, with results of a CAAC-IGZO FET with channel node of 20 nm [7]. The fabrication process flow of an actual CAAC-IGZO FET with a typical structure is also explained. A hybrid structure that vertically combines Si and CAAC-IGZO FETs is also introduced.

Chapter 3 deals with NOSRAM, where the CAAC-IGZO FET technology is applied to non-volatile memories [10–13]. This non-volatile memory relies on the extremely low off-state current, and can operate at approximately 5 V (i.e., a quarter of the voltage of conventional flash memories). NOSRAM also exhibits an excellent write endurance. While conventional flash memory has a write endurance of approximately 10,000 cycles, NOSRAM endures one trillion writes, achieving a ten-million-fold increase. In addition, the electric potentials can be applied directly to the memory cell during data writing, thus providing accurate control over the accumulated electric charge. Therefore, NOSRAM enables multiple bits in one cell.

Chapter 4 presents DOSRAM in which the CAAC-IGZO FET technology is applied to the DRAM memory cell [14]. Compared with DRAM involving Si, DOSRAM features a long data retention period because the charge stored in the capacitor is hardly lost owing to the extremely low off-state current. Consequently, it requires less frequent refresh operations and therefore consumes less power than its Si FET-based equivalent. For the same reason, electric charges in a capacitor can be stored for a long time even at low capacitance. Accordingly, the capacitance required for data retention may be reduced, which is advantageous in miniaturization.

Chapter 5 describes a normally-off CPU deploying CAAC-IGZO FETs [15–17]. Similar to power gating, the power supply to a circuit stops when unused (the circuit switches to sleep mode) in a normally-off CPU, resulting in low power consumption. When a CPU circuit comprising Si FETs is subject to a power gating operation, there is an overhead in power consumption and performance due to saving and restoring of storage elements in the circuit. Consequently, power gating in short intervals has been problematic because the average CPU power consumption would increase instead. In contrast, a normally-off CPU implemented with CAAC-IGZO FETs reduces the overhead power consumption dramatically by exploiting the extremely low off-state current characteristics of CAAC-IGZO FETs, and shortens the time required for backup and recovery.

Chapter 6 provides an example wherein CAAC-IGZO FETs are applied to FPGAs [18,19]. An FPGA is an LSI that a user can configure after manufacture. In conventional FPGAs, the circuit configuration information is stored in a static random access memory (SRAM) that is used as configuration memory, but SRAM data are generally lost when the power is turned off. Consequently, setting information needs to be stored in the configuration memory every time the power is back on. If a non-volatile memory using a CAAC-IGZO FET replaces this SRAM, setting information is retained even when the power is turned off; thus, the memory does not need restoring in the configuration memory. Moreover, the area and power consumption compared with SRAM may be reduced. Therefore, the incorporation of a CAAC-IGZO FET is expected to produce an FPGA with higher density and lower power consumption. A power gating function can easily be implemented in FPGAs; consequently, turning off unused circuits

may further reduce power consumption. Normally-off operation suitable for fine-grained multi-context structures is also possible by developing the above-mentioned features. Chapter 6 also introduces FPGAs with subthreshold operation, further reducing the power consumption via the lower operating voltage. Finally, the potential development of high-performance computing by combining an FPGA and a CPU, which has recently attracted extensive interest, is discussed.

Chapter 7 presents an example of an image sensor that uses CAAC-IGZO FETs [20,21]. Many of the existing complementary metal–oxide semiconductor (CMOS) image sensors use a rolling shutter mode whereby sensor pixels sequentially capture imaging data row by row. However, this mode exhibits a delay between first and last capturing sensor pixels. Therefore, a fast-moving object yields a distorted image. This delay occurs because captured data get leaked over time and are required to be read out immediately after their capture. When CAAC-IGZO FETs are introduced in an image sensor, the extremely low off-state current of the FETs enables the implementation of a global shutter mode whereby all sensor pixels simultaneously capture data. This off-state current also allows sensor pixels to retain captured data until readout, regardless of any difference in readout timing. Using multiple retention nodes in each sensor pixel allows multiple capture with very short shutter times, an attractive feature in machine vision. Adding an image difference detection function to the sensor pixel gives a motion sensor that performs detection of changes with respect to a reference frame in addition to normal imaging.

Chapter 8 presents other examples of CAAC-IGZO FET applications, demonstrating the versatility of this device. These examples include radio-frequency devices, X-ray detectors, encoder–decoders (CODECs), DC–DC converters (DC denotes direct current), analog programmable devices, and neural networks that may find use in various environments. Further, memory-based computing and an ultra-efficient power gating mechanism are presented.

LSIs with CAAC-IGZO have characteristics of very low off-state current and the associated reduction in system power consumption suggests that CAAC-IGZO LSIs may entirely replace Si LSIs in some applications.

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