

CHAPTER 1

THE MAGIC OF DELTA-SIGMA MODULATION

The aim of this introductory chapter is to motivate the need for oversampling data converters, and to give a bird's-eye view of the topics covered in this book. Towards the end of the chapter, we give a brief overview of the origins of $\Delta\Sigma$ data conversion and trends in this exciting area.

1.1 The Need for Oversampling Converters

Computational and signal processing tasks are now performed predominantly by digital means, since digital circuits are robust and can be realized by extremely small and simple structures that can in turn be combined to obtain very complex, accurate, and fast systems. Every year, the speed and density (of transistors) of digital integrated circuits (ICs) increase, thereby enhancing the dominance of digital methods in almost all areas of communications and consumer products. Since the physical world nevertheless remains stubbornly analog, data converters are needed to interface with the digital signal processing (DSP) core. As the speed and capability of DSP cores increases, so too must the speed and accuracy of the converters associated with them. This presents a continual challenge to the lucky few engineers dedicated to the design of data converters!

Figure 1.1 illustrates the block diagram of a signal processing system with analog input and output signals, plus a central digital engine. As shown, the analog input signal (usually after some amplification and filtering) enters an analog-to-digital converter

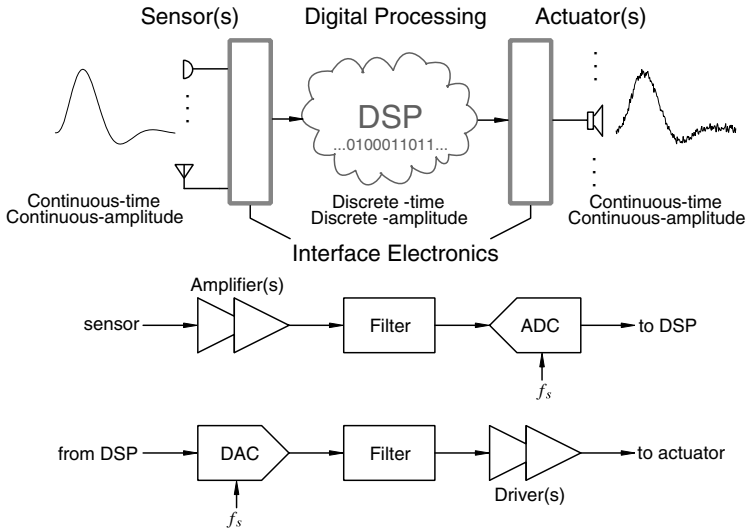


Figure 1.1 ADCs and DACs interface the real world to the virtual world.

(ADC), that transforms the input signal into a digital data stream. This stream is processed by the DSP core, and the resulting digital output signal is reconverted into analog form by a digital-to-analog converter (DAC). The DAC output is usually also filtered and amplified to obtain the final analog output signal.

Data converters (both ADCs and DACs) can be classified into two main categories: Nyquist-rate and oversampled converters. In the former category, there exists a one-to-one correspondence between the input and output samples. Each input sample is separately processed, regardless of the earlier input samples; in other words, the converter has no memory. Applying a digital input word containing bits b_1, b_2, \dots, b_N to a Nyquist-rate DAC ideally results in an analog output

$$V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \dots + b_N 2^{-N}), \quad (1.1)$$

where V_{ref} is the reference voltage, regardless of any previous input word. The accuracy of conversion can be evaluated by comparing the actual value of V_{out} with the ideal value given by (1.1).

As the name implies, the sampling rate f_s of a Nyquist-rate converter can be as low as Nyquist's criterion requires, i.e., twice the bandwidth B of the input signal. (For practical reasons, the actual rate is usually somewhat higher than this minimum value.)

In most cases, the linearity and precision of a Nyquist-rate converter is determined by the matching accuracy of the analog components (resistors, current sources, or capacitors) used in the implementation. For example, in the N -bit resistor-string DAC shown in Figure 1.2, the resistors must have a relative matching error less than 2^{-N} to guarantee an integral nonlinearity (INL)¹ less than 0.5 LSB. Similar matching requirements prevail for ADCs and DACs constructed from current sources or switched-capacitor (SC) branches.

¹INL is simply the difference between the actual output and the ideal output.

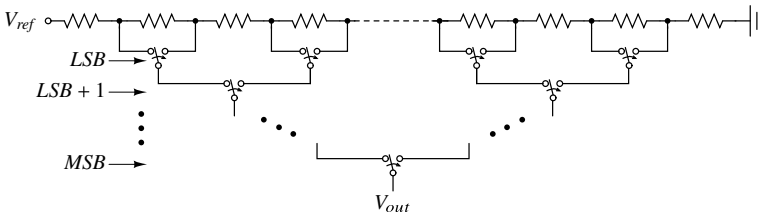


Figure 1.2 A resistor-string DAC. LSB denotes the least significant bit and MSB the most significant bit of the digital input.

Practical conditions restrict the matching accuracy to about 0.02%, and hence the effective number of bits (ENOB) to about 12, for such converters.

In many applications (e.g., digital audio), higher resolution and linearity are required, even as much as 18 or 20 bits. The only Nyquist-rate converters capable of such accuracy are the integrating or counting ones. These, however, require at least 2^N clock periods to convert a single sample, and hence, they are too slow for most signal processing applications.

Oversampling data converters are able to achieve over 20 ENOB resolution at reasonably high conversion speeds by relying on a trade-off. They use sampling rates much higher than the Nyquist rate, typically higher by a factor between 8 and 512, and generate each output utilizing numerous preceding input values. Thus, the converter incorporates memory elements in its structure. This property destroys the one-to-one relation between input and output samples. With oversampling converters, only a comparison of the complete input and output waveforms can be used to evaluate the converter’s accuracy, either in the time or in the frequency domain.

A common measure of a converter’s accuracy is the signal-to-noise ratio (SNR) for a sine-wave input. The relationship between ENOB and SNR (expressed in dB) for an ideal Nyquist converter with a full-scale sine-wave excitation is $SNR = 6.02 ENOB + 1.76$. The inverse relationship is often applied to oversampling converters to convert the SNR into an effective number of bits.

As will be shown in later chapters, the implementation of oversampling converters requires a considerable amount of digital circuitry, in addition to some analog stages. Both need to be operated faster than the Nyquist rate. However, the accuracy requirements on the analog components are relaxed compared to those associated with Nyquist-rate converters. The price paid for high accuracy thus includes faster operation and added digital circuitry; both of these are getting cheaper as digital IC technology advances. Hence, the trade-off offered by $\Delta\Sigma$ converters continues to improve. As a result, they are gradually taking over in many applications previously dominated by Nyquist-rate converters.

1.2 Nyquist and Oversampling Conversion by Example

To better understand the difference between Nyquist and oversampled analog-to-digital conversion, consider the following illustrative examples.

1.2.1 The Coffee Shop Problem

A student visits a coffee shop on campus every morning to get her fix of caffeine, so that she can get through the day. A coffee grande at the campus cafe costs \$3.47. What are the ways in which the student can pay this rather inconvenient sum? (The old-fashioned cafe does not accept credit cards). The “Nyquist” way of paying would be for the student to carry coins of the right denominations every day. She could, however, pay with a \$5 bill and expect to shop assistant to return \$1.53. The cafe, unfortunately, is severely short of small coins, and the shop assistant is not in a position to entertain this practice. Nevertheless, the shop assistant and the student come to an understanding that will allow the latter to pay with a \$5 bill, while at the same time not under or overpay the cafe. It exploits the fact that the student visits the cafe *every day*. This is the $\Delta\Sigma$ way, described below.

The agreement between the two parties is the following. On any day, if the student owes the cafe more than \$2.50, she hands a \$5 bill to the shop assistant. When instead, she owes less than \$2.50, she pays nothing. The student keeps track of how much she owes the cafe. The transactions for the first three days are shown in Figure 1.3.

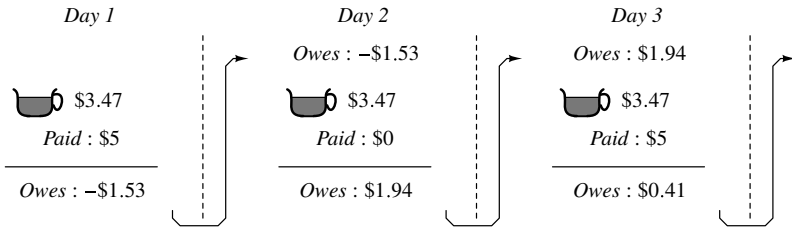


Figure 1.3 The $\Delta\Sigma$ way of paying \$3.47 for a coffee grande, with only \$5 bills.

On the first day, the student pays \$5, as agreed upon. She notes, at the end of the day, that she owes $-\$1.53$ to the cafe. The minus sign indicates that the student has overpaid.

While ordering at the cafe on the second day, the student reminds the shop assistant of the overpayment the previous day. The student needs to only pay $\$(3.47 - 1.53) = \1.94 . As agreed upon, she pays nothing, again noting that the cafe is owed \$1.94.

On the third day, the student needs to pay \$5.41, and as per the understanding with the shop assistant, hands over a \$5 bill. She notes that the cafe is owed \$0.41. This continues every day *ad infinitum*.

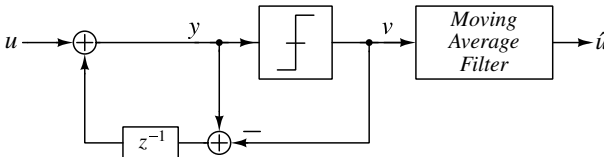


Figure 1.4 The algorithm of Figure 1.3. The u represents the cost of a coffee grande, and $v[n]$ is the payment made by the student on the n th day.

When the scheme above is cast into a signal flow diagram, Figure 1.4 results. In the figure, u presents the price of the coffee grande; $y[n]$, which is the input of the quantizer, represents the total amount owed by the student while ordering on the n th day; $v[n]$, which

is the quantizer output, represents the student's payment on the n th day, and takes the value 0 or 5. Therefore, $(y[n] - v[n])$ is the amount owed by the student to the cafe after making the payment on the n th day. The z^{-1} block in Figure 1.4 denotes a delay of one day.

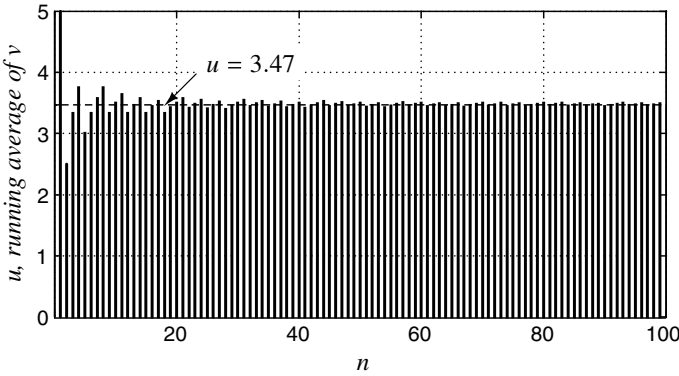


Figure 1.5 The running average of v approaches u for large n .

Figure 1.5 shows the running average of v , given by

$$\frac{1}{n} \sum_{k=1}^n v[k]. \tag{1.2}$$

The running average represents the price paid by the student per unit coffee grande, on average during the preceding days. As n becomes large, we see it approaches u , which is \$3.47.

In the beginning of this discussion, it might have seemed surprising that the student would be able to pay an inconvenient sum of \$3.47 with only \$5 bills. The $\Delta\Sigma$ way exploits the fact that u remains substantially the same from sample to sample. It uses feedback to make v approximate u on average. An individual sample of v has no meaning – one can determine u from v only by averaging many samples. Why does this scheme work? It is perhaps easier to see this by redrawing the diagram of Figure 1.4 as in Figure 1.6. We see that $y[n]$ is the total amount owed by the student (from the beginning of time) after grabbing her coffee for the day. As long as this is bounded, it must follow that the average of the accumulator's (Σ) input must be close to zero. Since the input to the accumulator is the difference (Δ) between the input and feedback sequence, it should follow that v and u would be equal, on average. Thus, by embedding a (very coarse) 2-level quantizer into a negative feedback loop, and sufficiently averaging the output sequence, the digital estimate \hat{u} can be a very good representation of u .

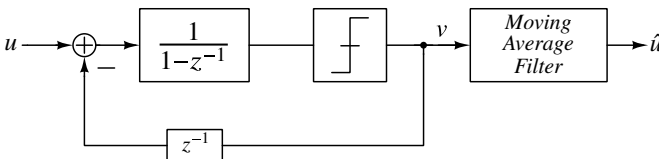


Figure 1.6 The system of Figure 1.4, redrawn.

The feedback loops of Figures. 1.4 and 1.6, both equivalent, represent a first-order $\Delta\Sigma$ modulator. The first structure is called the error-feedback structure, while the latter is the more traditional (and immediately recognizable) error accumulating structure.

1.2.2 The Dictionary Problem

A student visiting a bookstore begins to wonder about the thickness of that venerable tome, the *Webster's International Dictionary of the English Language*. An immediate way of finding the thickness is to get hold of a 6-inch ruler (this is a bookstore, after all) and measure the dictionary's thickness, as illustrated in Figure 1.7. Since the ruler has markings at every eighth of an inch, the worst-case error in measuring the thickness would amount to one-sixteenth of an inch. This is the "Nyquist" way, where the distance between successive marks on the ruler would correspond to the LSB. Measurement uncertainty (quantization error, in data-conversion parlance) can only be reduced by using a ruler with more finely spaced markings. The effort involved in making such a ruler is decidedly higher, not to mention the difficulty in discerning the marking that best corresponds to the height of the tome. Note, however, that the measurement is made in one shot – meaning that one use of the ruler is sufficient for measurement.

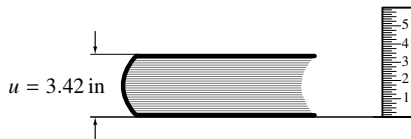


Figure 1.7 Measuring the thickness of *Webster's Dictionary* the Nyquist way.

The student finds focusing on the finely spaced levels a strain on the eyes, and he begins to wonder if it is at all possible to measure the book's thickness without having to look at the marks on the ruler at all. In other words, is it possible to find the thickness to within one-sixteenth of an inch (or even better) using only the fact that this is a 6-inch ruler? At first, this may seem like an impossible task – how is it possible to measure to within a fraction of an inch with a scale whose only "marking" is 6 in?

The student, being resourceful, exploits the fact that the bookstore has any number of copies of the *Webster's Dictionary* that he can put at his disposal. He contrives the following algorithm, which, he reasons, should allow him to determine the dictionary's thickness to arbitrary precision. The algorithm involves a sequence of operations, and proceeds as follows as illustrated in Figure 1.8.

Markings are made on the wall, from the floor up, at intervals of 6 inches using the (6-inch) ruler. The student places a copy of the *Webster's Dictionary* on the floor. The action of placing the book causes the level corresponding to the top of the stack of dictionaries (which contains just one instance at this time) to cross the lowest (6-inch) mark on the wall, which is at the floor level. The result of this experiment, denoted by v , is decreed to be 6 (corresponding to the 6-inch ticks on the wall).

A copy of *Webster's* is placed on the first, as shown in Figure 1.8(b). Since the action of adding the second copy causes the height of the stack to cross a marking on the wall, the result of this experiment is also deemed to be 6. This mode of operation continues *ad infinitum*. v at the end of every step, therefore, is 6 if the addition of a new copy causes

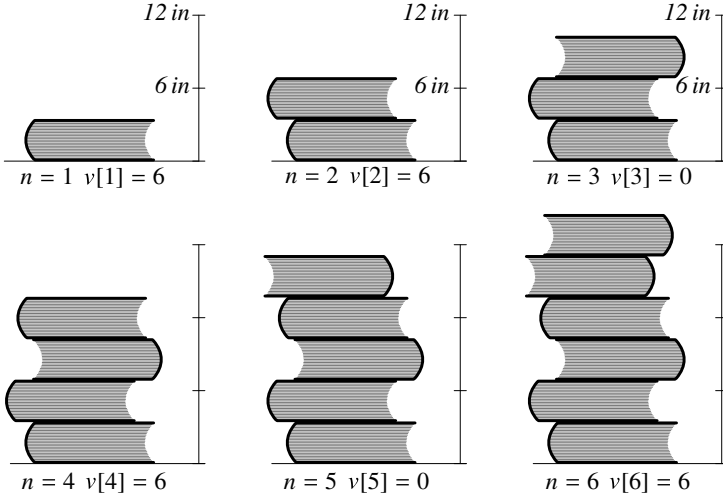


Figure 1.8 Measuring the thickness of *Webster's Dictionary* the $\Delta\Sigma$ way.

the stack to cross a new 6-inch mark, and zero otherwise. Denoting the thickness by u , the height of the stack in the n th instance is given by

$$\sum_{k=1}^n u = nu. \tag{1.3}$$

This is compared with the *next* 6-inch mark on the wall, whose height is given by

$$\sum_{k=1}^{n-1} v[k]. \tag{1.4}$$

Thus,

$$v[n] = \begin{cases} 6, & \sum_{k=1}^n u \geq \sum_{k=1}^{n-1} v[k], \\ 0, & \text{otherwise.} \end{cases}$$

The student argues that at the end of n operations,

$$0 < \sum_{k=1}^n v[k] - \sum_{k=1}^n u < 6, \tag{1.5}$$

since the height of the stack and the mark immediately above the top of the stack can differ by at most 6 inches. This means that

$$\frac{1}{n} \sum_{k=1}^n v[k] - \frac{6}{n} < u < \frac{1}{n} \sum_{k=1}^n v[k]. \tag{1.6}$$

An estimate of u can therefore be obtained by simply averaging the sequence $v[n]$. As n approaches infinity, the average of the output sequence approaches the true height of our venerable tome, which is about 3.42 inches.

When the student's scheme is translated into the language of electrical engineering, the diagram shown in Figure 1.9 results. The input u is summed in a delay-free integrator.

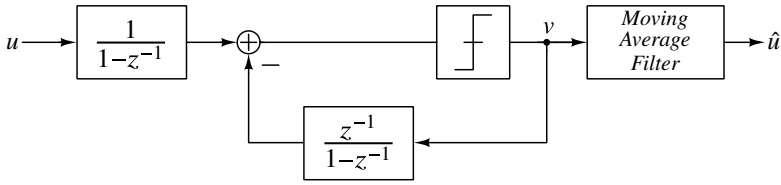


Figure 1.9 Equivalent representation of the algorithm in Figure 1.8.

The output sequence v is summed (Σ) using a delayed integrator, since the current decision depends on the sum of the previous decisions. The difference (Δ) between the two accumulated results is quantized to one of two levels (0 and 6 in our example). The resulting output sequence v is averaged (by a moving-average filter) to estimate the input u . The averaging filter acts on a digital input and is, therefore, a digital filter.

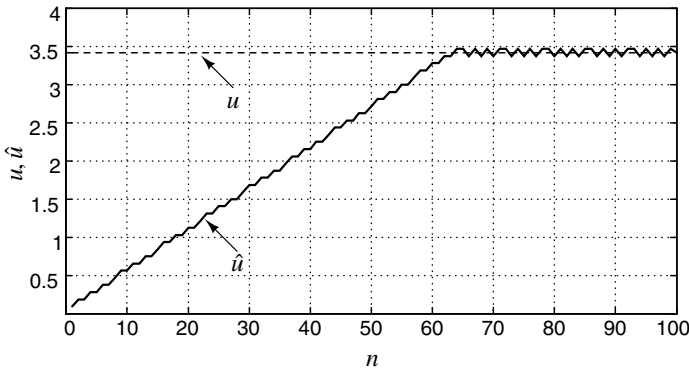


Figure 1.10 First 100 samples of the output of the moving average filter in Figure 1.11, for $u = 3.42$. A 64-tap filter (with all taps equal) is assumed.

Figure 1.10 shows the first hundred samples of \hat{u} at the output of a 64-tap moving-average filter. In steady state, \hat{u} happens to be within 0.05 inches of u . At first sight, it indeed seems remarkable that one can resolve to a small fraction of an inch with a scale marked only at 6 inches!

It is instructive to compare the Nyquist and $\Delta\Sigma$ ways of measurement. The former is a one-shot process, with the accuracy of measurement depending on the fineness and precision of the marks on the ruler. The latter, in contrast, is an iterative process. It involves feedback, since the outcome $v[n]$ of the n th iteration depends on the results of previous experiments. The $\Delta\Sigma$ method relies on the fact u does not change between successive iterations. This means that u is heavily *oversampled*. Moreover, $v[n]$ is not representative of u ; u can only be inferred by averaging the outcomes of a large number of iterations. Measurement accuracy generally improves as n is increased. Averaging 1000 samples reduces the error to 0.006 inches.

A practical problem with the realization of Figure 1.9 is that the outputs of both integrators keep increasing with n . In our bookstore example, the pile of dictionaries in Figure 1.8 would risk hitting the ceiling due to lack of headroom. Likewise, electronic integrators have limits on their maximum allowable output. This can be circumvented by

simply moving the integrators into the loop, as shown in Figure 1.11. In the figure, \hat{u} is a digital representation of u , and the system converts the continuous valued input u into a quantized output. This is achieved by embedding a coarse quantizer (which, in our example, has only two levels – 0 and 6 inches) in a negative feedback loop. The feedback loop of Figure 1.11 is called a $\Delta\Sigma$ modulator (or $\Delta\Sigma$ converter). More precisely, it represents a first-order, 2-level $\Delta\Sigma$ modulator. The integrator, whose output is quantized, is often referred to as the *loop filter*.

The discussion in this section was a (hopefully) gentle introduction to the basic idea behind $\Delta\Sigma$ modulation. A more detailed development of the first-order $\Delta\Sigma$ loop, its analysis and alternative ways of realizing the same functionality are given in Chapter 2.

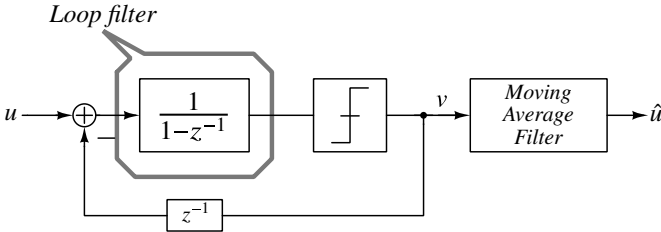


Figure 1.11 Addressing “headroom problems” of the system of Figure 1.9 by moving the integrators into the loop. Averaging v yields an estimate \hat{u} of u .

The reader might wonder why the measurement must proceed in the iterative fashion shown in Figure 1.8. Why not stack 64 dictionaries, and measure the height of the stack (to the nearest 6 inch mark) and divide by 64? To understand this, we denote the error introduced by the quantizer of Fig 1.11 in the n th iteration by $e[n]$. It is easy to see that

$$v[n] = u[n] + e[n] - e[n - 1]. \quad (1.7)$$

The output of the M -tap moving-average filter (with weights being equal) is given by

$$\hat{u} = \frac{1}{M} \sum_{k=r+1}^{M+r} v[k] = u + \frac{1}{M} (e[r + M + 1] - e[r]). \quad (1.8)$$

It is easy to see that \hat{u} is what one would obtain by stacking up M dictionaries, measuring the height of the stack to the nearest 6 inches, and dividing the result by M . From the equation above, we observe that the estimation error in \hat{u} is due to the e in the first and last of the 64 (assuming $M = 64$) samples being processed by the moving-average filter. This suggests that quantization error can be reduced by weighting $v[n]$ non-uniformly – that is, by attaching more importance to the middle set of samples than those toward the end. This intuition is confirmed by filtering the output sequence of the modulator with a 64-tap moving-average filter with a triangular impulse response. From Figure 1.12, we see that the peak-to-peak excursion of the output of such a filter is much smaller than that in the case where all the samples of $v[n]$ are equally weighted. Thus, there is merit to observing the height of the stack every time an additional dictionary is added, as this enables the use of arbitrary moving-average filters. Recall that measuring the height of a stack of 64 dictionaries (to the closest 6-inch mark) and dividing by 64 is equivalent to uniformly weighting the samples of v . To summarize, there is more to choosing the post-filter that processes the modulator’s output than simply averaging the output. To understand how

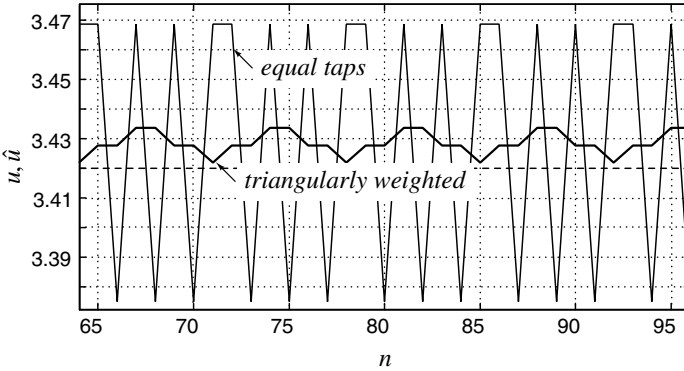


Figure 1.12 Outputs of moving-average filters with equal weights, and a triangularly weighted response.

one designs a post-filter, it is helpful to examine a $\Delta\Sigma$ modulator in the frequency domain, which we will do going forward. Before that, we wish to draw the reader’s attention to the following.

The example above considered the modulator’s input u to be constant. In practice, the input to be digitized has a nonzero bandwidth (which is much smaller than the sampling rate). Then, the output of the digital post-filter (which is a sequence at the sampling rate) can be downsampled, so that the output sample rate can equal the Nyquist rate corresponding to the input signal. Figure 1.13 shows the system model of an ADC employing

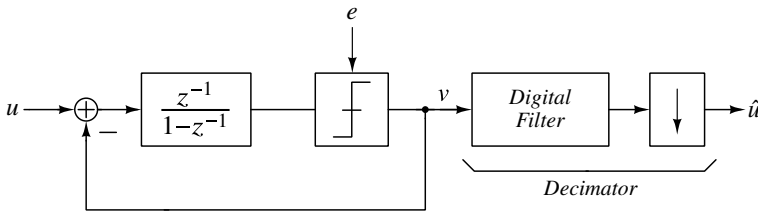


Figure 1.13 System model of an ADC with a first-order $\Delta\Sigma$ modulator.

a first-order $\Delta\Sigma$ modulator. The delay element in the feedback path of the modulator of Figure 1.11 has been pushed into the forward path. The (benign) consequence of this is to delay the input by one sample. The combination of the the digital post-filter and downsampler is called the *decimation filter* or decimator.

The output noise due to the quantization error in the $\Delta\Sigma$ modulator is $q[n] = e[n] - e[n-1]$. In the z -domain, this becomes $Q(z) = (1-z^{-1})E(z)$, and in the frequency domain, after z is replaced by $e^{j\omega}$, the power spectral density (PSD) of the output noise is found to be

$$S_q(\omega) = 4 \sin^2\left(\frac{\omega}{2}\right) S_e(\omega). \tag{1.9}$$

Here, $S_e(\omega)$ is the one-sided PSD of the quantization error (noise) of the internal ADC. For “busy” (i.e., rapidly and randomly varying) input signals, one may approximate e with white noise of mean-square value $\Delta^2/12$, where Δ is the step size of the quantizer, and thus

obtain

$$S_e(\omega) = \frac{\Delta^2}{12\pi}. \quad (1.10)$$

The filtering function $(1 - z^{-1})$ is called the noise transfer function (NTF). The squared magnitude of the NTF as a function of frequency is illustrated in Figure 1.14. As the

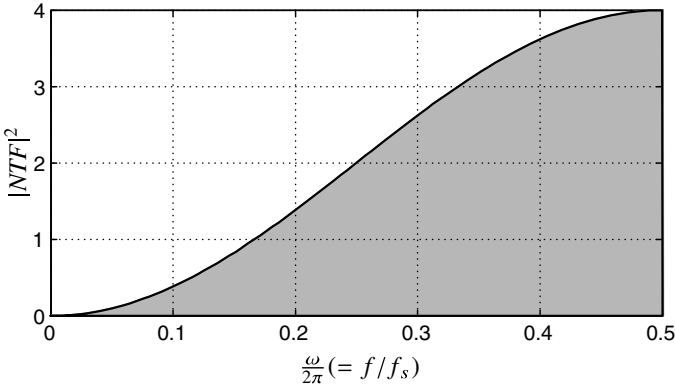


Figure 1.14 Noise-shaping function for the $\Delta\Sigma$ modulator shown in Figure 1.13.

figure shows, the NTF of the $\Delta\Sigma$ modulator is a highpass filter function. It suppresses e at frequencies around 0, but the NTF also enhances e at frequencies around $\omega = \pi$.

We introduce next the *oversampling ratio*

$$OSR = \frac{f_s}{2f_B}, \quad (1.11)$$

where f_B is the maximum signal frequency, which is the signal bandwidth. OSR defines how much faster we sample in the oversampled modulator than in a Nyquist-rate converter.

It turns out that the in-band component of quantization noise at the output of the modulator is given by

$$q_{rms}^2 = \frac{\pi^2}{3} \frac{e_{rms}^2}{OSR^3}. \quad (1.12)$$

As expected, the in-band noise decreases with increasing OSR . However, this decrease is relatively slow; doubling the OSR reduces the noise only by 9 dB, and hence it enhances the ENOB by only about 1.5 bits.

The discussion in this chapter is intended merely as an introduction, a whetting of the appetite – the topics of sampling, oversampling and the first-order $\Delta\Sigma$ modulator are covered in detail in Chapter 2.

1.3 Higher-Order Single-Stage Noise-Shaping Modulators

As the reader might have anticipated, a way to increase the resolution (i.e., the ENOB) of a $\Delta\Sigma$ modulator is to use a higher-order loop filter. By adding another integrator and feedback path to the modulator of Figure 1.13, the structure of Figure 1.15 results. Linearized

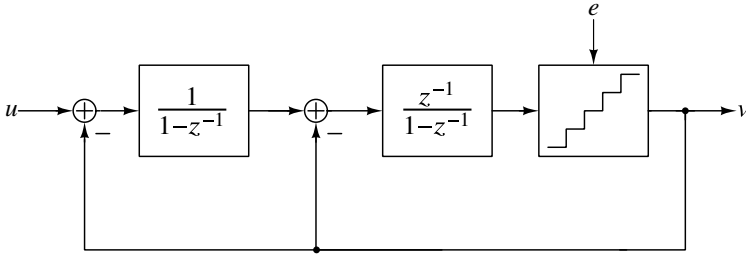


Figure 1.15 A second-order $\Delta\Sigma$ modulator.

analysis yields

$$V(z) = z^{-1}U(z) + (1 - z^{-1})^2E(z). \tag{1.13}$$

This indicates that the NTF is now $(1 - z^{-1})^2$ in the z -domain, which applies a shaping function of $(2 \sin(\omega/2))^4$ to the PSD of e . It follows that the in-band noise power is (to a good approximation for $OSR \gg 1$)

$$q_{rms}^2 = \frac{\pi^4 e_{rms}^2}{5 OSR^5}. \tag{1.14}$$

Doubling OSR, therefore, results in about 2.5 bits of additional resolution. This is a much more favorable trade-off than that of the first-order modulator. A more detailed analysis of second-order $\Delta\Sigma$ modulators, and alternative ways of realizing them, are discussed in Chapter 3.

In principle, by adding more integrators and feedback branches to the loop, even higher-order NTFs can be obtained. For an L th-order loop filter resulting in $NTF(z) = (1 - z^{-1})^L$, the in-band noise power is approximately

$$q_{rms}^2 = \frac{\pi^{2L} e_{rms}^2}{(2L + 1) OSR^{2L+1}}, \tag{1.15}$$

and the number of bits added to the resolution by doubling the OSR is given by $(L + 0.5)$.

From the discussion above, it appears as if using a $\Delta\Sigma$ loop with an appropriately chosen (very high-order) NTF can attain arbitrarily high SNRs, even for small OSR . This sounds too good to be true, and as the wise reader should suspect, something that *sounds* too good to be true is *probably* too good to be true. It turns out that for high-order loops, stability considerations, which have thus far been ignored, reduce the achievable resolution to a lower value than that given by the equations above. For high-order single-bit modulators, the difference is substantial, amounting to more than 60 dB for a fifth-order modulator. Higher-order $\Delta\Sigma$ modulators, their stability, trade-offs involved in their design, and various means of realizing them will be discussed in detail in Chapter 4.

1.4 Multi-Stage and Multi-Quantizer Delta-Sigma Modulators

The philosophy behind using a high-order loop to suppress in-band quantization noise is to *divide* noise by a large loop-gain, obtained by incorporating more integrators in the loop. An alternative strategy to accomplish the same objective is to *cancel* the quantization error

by measurement and subtraction. It turns out that this approach eases the stability problems associated with high-order modulators. The resulting structures are called cascade modulators, and also referred to as multi-stage or MASH (for Multi-stAge noise-SHaping) modulators. This, and other techniques based on this fundamental idea, form the subject of Chapter 5.

The basic concept behind a cascade modulator is illustrated in Figure 1.16. The output

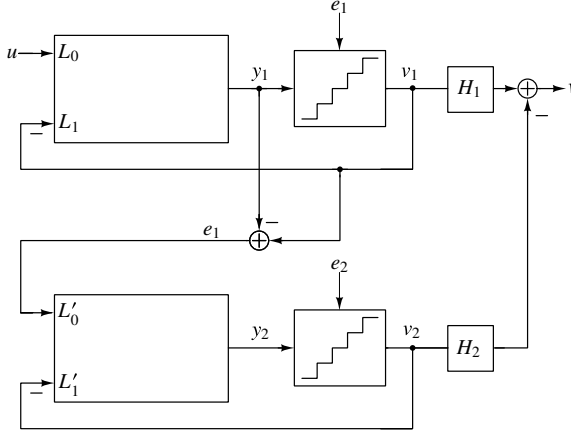


Figure 1.16 A multi-stage delta-sigma modulator.

signal of the first stage is given by

$$V_1(z) = STF_1(z)U(z) + NTF_1(z)E_1(z), \quad (1.16)$$

where STF_1 and NTF_1 are the signal and noise transfer functions, respectively, of the first stage. The second stage is added to improve the SNR beyond what NTF_1 can provide.

As shown in Figure 1.16, the quantization error e_1 of the input stage is found in analog form by subtracting the input to its internal quantizer from its output. e_1 is then fed to another $\Delta\Sigma$ loop forming the second stage of the modulator, and converted into digital form. Hence, the output signal of the second stage in the z -domain is given by

$$V_2(z) = STF_2(z)E_1(z) + NTF_2(z)E_2(z), \quad (1.17)$$

where STF_2 and NTF_2 are the signal and noise transfer functions, respectively, of the second stage. The digital filter stages H_1 and H_2 at the outputs of the two modulator loops are designed such that in the overall output v of the system, the first-stage error e_1 is canceled. By the equations above, this is achieved if the condition

$$H_1(z)NTF_1(z) = H_2(z)STF_2(z) \quad (1.18)$$

holds. The simplest (and usually most practical) choice for H_1 and H_2 that satisfies (1.18) is $H_1 = k \cdot STF_2$ and $H_2 = k \cdot NTF_1$, where k is constant chosen to give unity signal gain. Since STF_2 is often just a delay, H_1 is easily realized. The overall output is then given by

$$V(z) = k \cdot STF_1(z)STF_2(z)U(z) + k \cdot NTF_1(z)NTF_2(z)E_2(z). \quad (1.19)$$

In a typical case, both stages of the MASH modulator may contain a second-order loop, and their transfer functions may be given by $STF_1 = z^{-1}$, $STF_2 = 0.5z^{-2}$ and $NTF_1 = NTF_2 = (1 - z^{-1})^2$. Choosing $k = 2$, the output we obtain is then

$$V(z) = z^{-2}U(z) + 2(1 - z^{-1})^4 E_2(z). \quad (1.20)$$

Thus, the noise-shaping performance is essentially that of a fourth-order single-loop converter, but the stability behavior is that of a second-order one.

If the condition (1.18) is not exactly satisfied, for example, due to imperfections in the realization of the analog transfer functions, then $E_1(z)$ will appear at the output multiplied by $k \cdot [STF_2 NTF_{1a} - NTF_1 STF_{2a}]$, where the subscript a denotes the actual value of the analog transfer function. This is not surprising, since the efficacy of *any* technique based on cancellation is always degraded by mismatch. As will be shown in Chapter 5, mismatch can result in a serious deterioration of the noise performance of the converter.

1.5 Mismatch Shaping in Multi-Bit Delta-Sigma Modulators

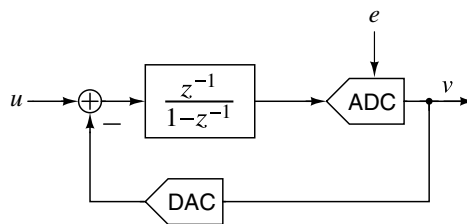


Figure 1.17 The quantizer in a $\Delta\Sigma$ modulator is implemented as a cascade of ADC and DAC.

A quantizer is implemented as a cascade of an ADC and DAC, as shown in Figure 1.17. The DAC appears in the feedback path of the $\Delta\Sigma$ modulator, and its nonlinearities result in comparable nonlinearities for the overall conversion. This occurs because the in-band part of the DAC output signal is forced by the feedback loop to follow the input signal u very accurately. Hence, if the DAC is nonlinear, its input will be distorted to give an accurate output. Since the DAC input is the output of the converter, the converter output is distorted.

It was this fact that forced early designers of $\Delta\Sigma$ modulators to use single-bit internal DACs in the $\Delta\Sigma$ loops. A single-bit DAC has the immensely important virtue of *inherent linearity*. Since the input to a one-bit DAC only takes on two values, the transfer characteristic of the DAC can be represented by two points in the input–output plane. Thus, a straight line that passes through those points models a 1-bit DAC exactly. In other words, the DAC is *exactly* described by an equation of the form $v_d = kv + offset$, where k and *offset* are constants. Since a system that obeys such a model does not introduce distortion, a 1-bit DAC is said to be *inherently linear*.

In contrast, single-bit ADCs (which are essentially comparators) have an ill-defined gain factor, as will be shown in Chapter 2. Also as Chapters 3 and 4 will show, loops containing one-bit quantizers must remain stable over a wide range of loop gains. This

consideration results in a reduction of the allowable input signal swing, and hence a reduction in the achievable SNR.

For a multi-bit quantizer, the loop is inherently more stable because the quantizer gain is well-defined, and its no-overload range is increased. In fact, linear analysis can be used to design the modulator so that its stability is guaranteed. Furthermore, since the quantization noise decreases by 6 dB for each bit added to the quantizer, and since aggressive high-order noise-shaping functions can be used, multi-bit modulators can have very high ENOB even at low OSR values. Hence, there is strong motivation to solve the problem of DAC nonlinearity inherent in the use of multi-bit quantization. While brute-force techniques, such as element trimming, have been used earlier, the techniques currently in favor use auxiliary digital circuitry to manipulate the elements of the DAC so as to reduce the in-band portion of the error signal introduced by DAC nonlinearities. These techniques are conceptually very similar to the noise shaping used in $\Delta\Sigma$ modulators, and are often described with the term *mismatch shaping*. As with noise shaping, the effectiveness of mismatch shaping increases with increasing OSR. For very low OSR values ($OSR < 8$), digital techniques can be used to determine and then correct the nonlinearities of the DAC.

The fundamental principles behind addressing DAC mismatch in multi-bit delta-sigma modulators will be covered in detail in Chapter 6.

1.6 Continuous-Time Delta-Sigma Modulation

At the beginning of this chapter, we saw that an ADC converts a continuous-time analog signal (which is continuous in time and amplitude) to a digital one (where time and amplitude are quantized). A discrete-time $\Delta\Sigma$ modulator acts on a sampled version of the analog signal, and its role is to quantize these samples. A continuous-time $\Delta\Sigma$ modulator (CT $\Delta\Sigma$ M), on the other hand, works with the continuous-time input $u(t)$. There are many ways of understanding a CT $\Delta\Sigma$ M – and the development below is appropriate for an introductory chapter such as this. A more general development, building on previous chapters discussing discrete-time $\Delta\Sigma$ design, is given in Chapter 8.

Figure 1.18(a) shows a first-order lowpass filter. The opamp is ideal. Regardless of the (continuous-time) input $u(t)$, the average capacitor current $\overline{i_c(t)}$ must be zero – otherwise, the voltage across the capacitor would become unbounded. Thus, $\overline{i_1(t)} = \overline{i_2(t)}$, which results in $\overline{u(t)} = -\overline{v(t)}$.

Next, the output of the opamp is sampled at a rate f_s , as shown in Figure 1.18(b). The resulting *sequence* $v[n]$ is zero-order held, before being fed back through the resistor. Assuming that the feedback loop is functional, the average capacitor current is still zero, meaning that the average of $\overline{u(t)}$ is still equal to the average of $\overline{v(t)}$. The latter now refers to the output of the ZOH. $\overline{v(t)}$, however, equals the average value of the *sequence* $v[n]$. By inserting a sampler into the loop, therefore, we are now in a position to relate the average of the input *waveform* $u(t)$ to the average of the output *sequence*. Now, if the input signal varies very slowly (in relation to the sampling period), $u(t)$ and its local average are largely the same. Under this circumstance, $u(t) \approx -v[n]$. Half the battle of analog-to-digital conversion has been won – we have accomplished discretization of time.

The next progression is to quantize $v[n]$ before feeding it back through the ZOH. Assuming the loop is still stable, and that $u(t)$ is slowly varying, $u(t)$ is still approximately

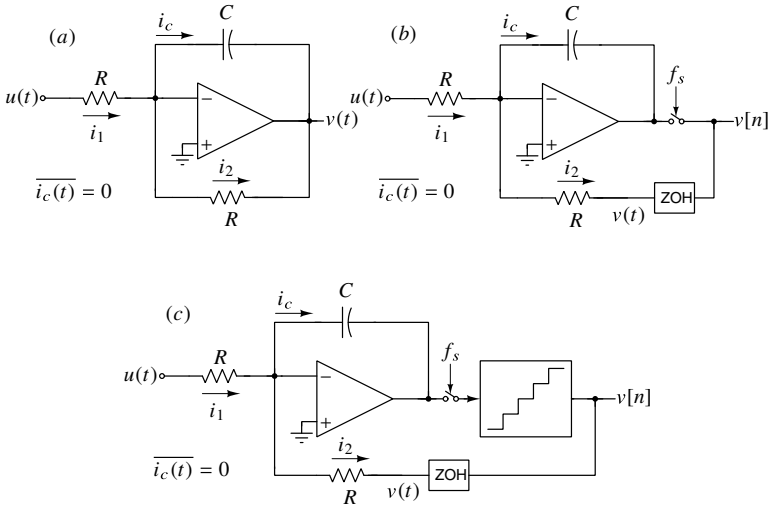


Figure 1.18 (a) A first-order lowpass filter. (b) Sampling the opamp’s output and feeding back the sampled sequence using a zero-order hold (ZOH). (c) Quantizing the output sequence before feeding it back.

equal to $-\overline{v[n]}$. $v[n]$ is now not only discrete in time, but also in amplitude. It can, therefore, be represented in digital form. Note that, as in the discrete-time case, it is only the *average* of $v[n]$ that approximates u ; the individual samples have no meaning in isolation. The system of Figure 1.18(c) is a first-order CTΔΣM – its output sequence has to be processed by an appropriately chosen digital filter, so as to properly average $v[n]$ and yield an estimate of $u(t)$. As in the discrete-time case, higher-order loop filters can better reject in-band quantization noise.

It is instructive to examine the output of the first-order CTΔΣM when $u(t) = \cos(2\pi f_s t)$, that is, for a sine wave whose frequency equals the sample rate². Since the virtual ground voltage is zero, and $\overline{u(t)} = 0$, it follows that $\overline{i_1(t)} = 0$. This means that $\overline{i_2(t)}$ has to be zero. This, in turn, implies that $\overline{v[n]} = 0$, indicating that the CTΔΣM does not respond to an input at its sampling frequency! This remarkable property of a CTΔΣM distinguishes it from all other ADC families, where an input at f_s cannot be distinguished from an input at dc. This ability of a CTΔΣM to respond differently to inputs at dc and f_s is referred to as *implicit anti-aliasing*. Chapter 8 gives a detailed discussion of the fundamentals of continuous-time ΔΣ modulation.

However, a CTΔΣM is the victim of many non-idealities – excess delay in the quantizer, time-constant variations in the loop filter, clock jitter and so forth. Chapter 9 analyzes the effects of these nonidealities and how they may be circumvented. Chapter 10 gives circuit design considerations for the blocks that make up a CTΔΣM.

The block diagram of a generic single-loop CTΔΣM is shown in Figure 1.19. It is a bag of contrasts. The loop filter processes $u(t)$ and $v(t)$, and it should be linear and time-invariant. The output of the filter is sampled and quantized. Sampling is a time-

²When a Nyquist converter without an anti-alias filter up front is subject to a sinusoidal input at its sampling frequency, the output is a dc sequence, indicating that the tone at f_s aliases to dc.

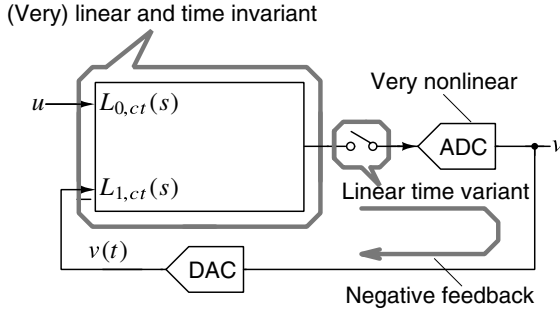


Figure 1.19 Block diagram of a generic single-loop CT $\Delta\Sigma$ M.

varying operation. The quantizer is nonlinear; in fact, it is extremely so, due to the abrupt steps in its transfer curve. To add to the excitement, all these blocks are enclosed in a negative-feedback loop. Thus, a CT $\Delta\Sigma$ M may be described as a part linear, part nonlinear, part time-invariant, part time-variant, part continuous-time, and part discrete-time system incorporating negative feedback. Understanding a CT $\Delta\Sigma$ M, therefore, exposes one to a variety of topics – from signal processing and systems theory to precision circuit design. Apart from its obvious pedagogical value, a CT $\Delta\Sigma$ M is also highly relevant in practice. It is what we would like to refer to as *a system for all seasons*.

1.7 Bandpass Delta-Sigma Modulators

Up to now, it was assumed that the signal energy was concentrated in a narrow band at low frequencies, centered at dc. In applications such as RF communication systems, the signal is concentrated in a narrow band of width f_B around a center frequency f_0 , where f_B is much smaller than f_s while f_0 is not. In such cases, $\Delta\Sigma$ modulation may still be effective, but now the noise transfer function NTF must have a bandstop, rather than highpass, character, with zeros located at or around f_0 .

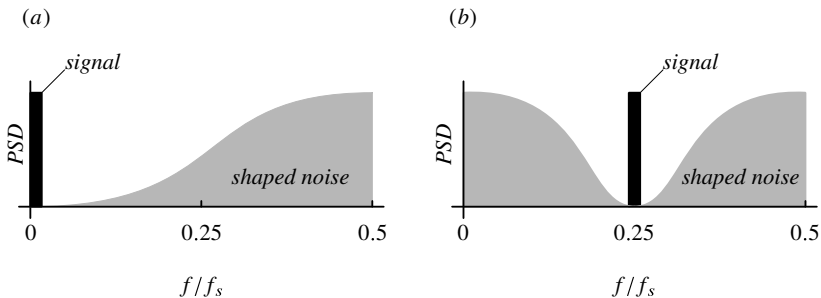


Figure 1.20 Conceptual output spectra for (a) lowpass and (b) $f_s/4$ bandpass modulators.

Figure 1.20 compares the conceptual output spectra of a lowpass and a bandpass $\Delta\Sigma$ modulator. A simple way to obtain the NTF of a bandpass $\Delta\Sigma$ modulator is to find first an appropriate lowpass NTF, and then perform a z -domain mapping on it. For example, the transformation $z \rightarrow -z^2$ maps the frequency range around dc (i.e., $z = 1$) to the

ranges around $\pm f_s/4$ (i.e., $z = \pm j$). Hence, the resulting NTF will have small values near $f_o = f_s/4$, and will suppress the quantization noise there. This bandstop noise-shaping makes it possible to achieve a high signal-to-noise ratio (SNR) for signals whose energy is restricted to frequencies near $f_s/4$.

Note that the mapping doubles the order of the lowpass NTF and transforms the zeros of the NTF from near $z = 1$ to the vicinity of the points $z = \pm j$, as illustrated in Figure 1.21. Other techniques for finding the NTF of bandpass $\Delta\Sigma$ modulators will be discussed in

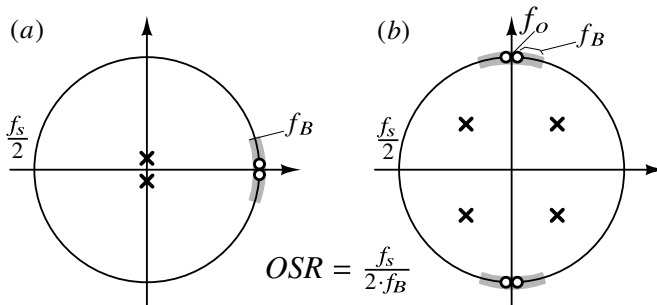


Figure 1.21 Pole-zero locations of (a) a lowpass NTF and (b) a bandpass NTF.

detail in Chapter 11 along with circuit design techniques for bandpass $\Delta\Sigma$ modulators.

1.8 Incremental Delta-Sigma Converters

In our discussions so far, we evaluated the in-band quantization noise of a delta-sigma modulator by integrating its spectral density over the signal bandwidth. This is justified only if the digital filter following the modulator has a brick-wall response. Such a requirement can only be approximated in practice, and like all sharp filters, the impulse response of the filter can be extremely long. This means that the $\Delta\Sigma$ modulator and accompanying post-filter have significant memory. This makes a conventional $\Delta\Sigma$ modulator unsuitable in applications where the ADC is multiplexed among multiple sensors, or when the ADC has to be operated in an intermittent fashion.

A different ADC scheme that applies the noise-shaping algorithm of $\Delta\Sigma$ ADCs, but only within the sample-by-sample operation of a Nyquist-rate ADC, is the *incremental* $\Delta\Sigma$ ADC. This family of ADCs is closely related to their conventional cousins, and it forms the subject of Chapter 12.

1.9 Delta-Sigma Digital-to-Analog Converters

The motivation for using $\Delta\Sigma$ modulation to realize high-performance DACs is the same as for ADCs: it is difficult, if not impossible, to reliably achieve an untrimmed linearity and accuracy better than about 14 bits for DACs operated at the Nyquist rate. With $\Delta\Sigma$ modulation, this task becomes feasible. A $\Delta\Sigma$ DAC system is illustrated in Figure 1.22. By operating a fully digital $\Delta\Sigma$ modulator loop at an oversampled clock rate, a data stream

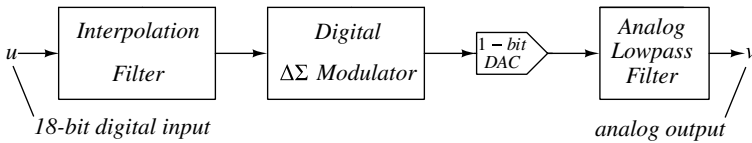


Figure 1.22 A $\Delta\Sigma$ DAC system.

with (say) 18-bit word length can be changed into a high-speed single-bit digital signal such that the baseband spectrum is preserved. The large amount of truncation noise generated in the loop is shaped in order to make the in-band noise negligible. The single-bit digital output signal can then be converted with high (ideally, perfect) linearity into an analog signal using a simple two-level DAC circuit. The out-of-band truncation noise can be subsequently removed using analog lowpass filters.

As in the case of analog $\Delta\Sigma$ loops, using single-bit truncation can lead to instability, and hence limits the effectiveness of the noise shaping. Using multi-bit (typically, 2–5 bit) truncation improves the noise shaping and makes the task of the analog post filter much easier. The linearity of the DAC for in-band signals can be achieved by using the same mismatch shaping techniques used in the internal DACs of analog multi-bit $\Delta\Sigma$ ADCs.

Also as in the case of ADCs, bandpass $\Delta\Sigma$ DACs can be designed. Noise-shaping now suppresses the truncation noise in a narrow band located around a nonzero center frequency f_0 , which need not be much smaller than the clock frequency f_s .

$\Delta\Sigma$ DACs will be discussed in detail in Chapter 13.

1.10 Decimation and Interpolation

The digital filter that follows the $\Delta\Sigma$ ADC has the crucial function of eliminating shaped noise. Assuming an ideal brick-wall filter, the filtered output of the modulator has a small bandwidth in relation to the sampling rate. This allows the output of the digital filter to be downsampled to yield an output sequence at the Nyquist rate. A brick-wall characteristic can only be approximated in practice, which means that the filter characteristic should be very sharp to prevent degradation of the in-band SQNR due to aliasing that occurs when samples are dropped. The combination of digital filtering and sample-dropping is performed by a *decimation filter*. In the same vein, a filter with similar requirements (called the interpolation filter) occurs in the beginning of a $\Delta\Sigma$ DAC signal chain.

Design considerations for decimation and interpolation filters are given in Chapter 14.

1.11 Specifications and Figures of Merit

The primary specifications of any ADC include its power consumption P , signal bandwidth (BW), and effective number of bits ($ENOB$). Clearly, there are combinations of $ENOB$, BW and P specifications that are hard, or even impossible, to satisfy, and others that are relatively easy. To quantify the degree of difficulty, it is common to compute a figure of merit (FoM) that reflects the power efficiency of the ADC. There are two commonly used

FoMs. The Walden FoM [1] is defined as

$$FoM_W = \frac{P}{2^{ENOB} \cdot f_N}. \tag{1.21}$$

Here P is the power needed by the ADC, $ENOB$ is the effective number of bits, and f_N is the Nyquist frequency. The dimension of FoM_W is Joules, and it gives the amount of energy needed for each conversion step (LSB step). Note that a smaller FoM_W indicates a more efficient ADC.

An alternative, proposed originally by Rabii and Wooley [2] and presented in a modified form in the first edition of this book, has been dubbed the Schreier FoM. It is defined as

$$FoM_S = \frac{DR \cdot BW}{P} \tag{1.22}$$

or

$$FoM_S (dB) = DR (dB) + 10 \cdot \log_{10} \left(\frac{BW}{P} \right), \tag{1.23}$$

where DR denotes the dynamic range of the ADC. A larger FoM_S indicates a more efficient ADC.

The motivation for the definition of the FoM_S is given next. We assume that the technology determines the full-scale signal power, and hence, the DR will be determined by the variable in-band noise power q_{rms}^2 . We also assume that the noise is white, so q_{rms}^2 is proportional to the signal bandwidth BW , and hence, DR is proportional to $1/BW$. As a consequence, for a given ADC with given P , the product $DR \cdot BW$ is a constant.

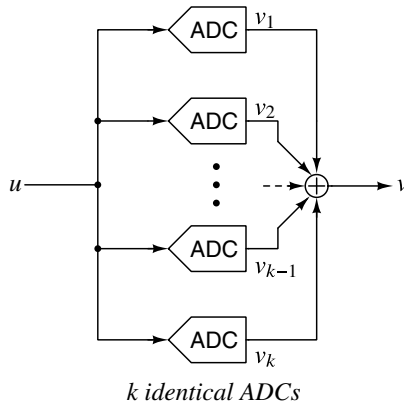


Figure 1.23 A multi-path $\Delta\Sigma$ ADC system.

For a fixed BW , the necessary power P is proportional to the required DR . To show this, assume that the ADC is realized in the multi-path configuration as shown in Figure 1.23. The component ADCs are identical, and ADC_i generates an output signal $v_i[n]$ and a noise output $q_i[n]$. The signals are fully correlated, and hence the output signal power will be $k^2 \cdot v_{rms}^2$. The noise outputs are uncorrelated, and hence the total noise output power will be $k \cdot q_{rms}^2$. The overall dynamic range of the ADC will hence be k times the DR of the individual component ADCs. If each ADC needs a power P , the total power used will be $k \cdot P$. Since both the DR and P are proportional to k , they must also be proportional to

each other. Note that this result agrees with the observation that the thermal noise power can be decreased by reducing the impedance level of the circuitry. Thus, increasing all C , g_m and $1/R$ values by a factor $k > 1$ will change DR into $k \cdot DR$, but it will increase all currents, and thus for fixed bias voltages P also, by the same factor k .

For a fixed DR , the power P needed is proportional to the required BW . To show this, assume initially that the power is kept constant, and the BW is increased by a factor l . Since, with fixed P , the product $DR \cdot BW$ is constant, the new dynamic range is DR/l . To restore DR to its original value, by the argument of the preceding paragraph, P must be replaced by $l \cdot P$. (An alternative derivation of the proportionality between BW and P can also be based on the structure of Figure 1.23, assuming that each ADC has a BW/l wide sub-band of the overall band.)

Finally, consider what happens if both DR and BW are changed. If DR is replaced by $k \cdot DR$, and BW by $l \cdot BW$, by the arguments presented above, the power P needs to be changed to $k \cdot l \cdot P$. This shows that $DR \cdot BW/P$ is a characteristic constant of a given converter, and hence can be used to compare the efficiencies of competing configurations and circuits.

The FoMs introduced above can be used for evaluating the energy efficiency of ADCs, but they do not tell the whole story about their practical usefulness. The key missing parameters are the cost and system impact of the chosen architecture. The cost aspects include the technology needed for their implementation, the silicon area occupied by the ADC, the number of pins required on the package, the production tests needed, and the fabrication yield. The system aspects include the prefiltering (anti-aliasing) needed, and the out-of-band signal transmission of the ADC. The latter determine how effectively the ADC can suppress large unwanted out-of-band “blockers” present in its input signal. For a meaningful comparison of the available ADC algorithms and configurations, these properties also need to be taken into account!

1.12 Early History, Performance, and Architectural Trends

The way $\Delta\Sigma$ modulation is developed in this book is not how it historically came about. The origins can be traced to Δ -modulation, which was a technique intended to be used to encode speech into digital form, so as to enable electronic switching in telephony. The prevalent technique at the time was to digitize speech at its Nyquist rate and quantize it to the required resolution of 8 bits. Since building an 8-bit ADC was a challenge, people began to wonder if using oversampling (so as to induce significant correlation between successive samples) could simplify the design of the quantizer.

The basic idea behind Δ -modulation is the following. If the input signal to be digitized is slowly varying in relation to the sampling rate, successive samples are so similar that one might as well transmit only the quantized *difference* (Δ) between successive samples. This way, the dynamic range of the transmitted signal can be significantly smaller than that of the signal itself, reducing the number of levels needed in the quantizer. In a Δ modulator, the quantizer is the simplest possible, namely the two-level one.

A naive attempt at transmitting the quantized difference is shown in Figure 1.24(a). The transmitter puts out a two-level sequence $\pm\Delta$, whose sign is dependent on the sign of the input slope. Since v contains the first difference of u , the receiver should be an inte-

grator. Figure 1.24(b) compares the sinusoidal input u and its estimate \hat{u} at the receiver's output, when $OSR = 512$. We see significant error between the two waveforms, since the low-frequency component of quantization noise is greatly amplified by the integrator in the receiver. Since v is a two-level sequence, it might be thought of as an ADC – however, as seen from Figure 1.24(b), its performance leaves a lot to be desired.

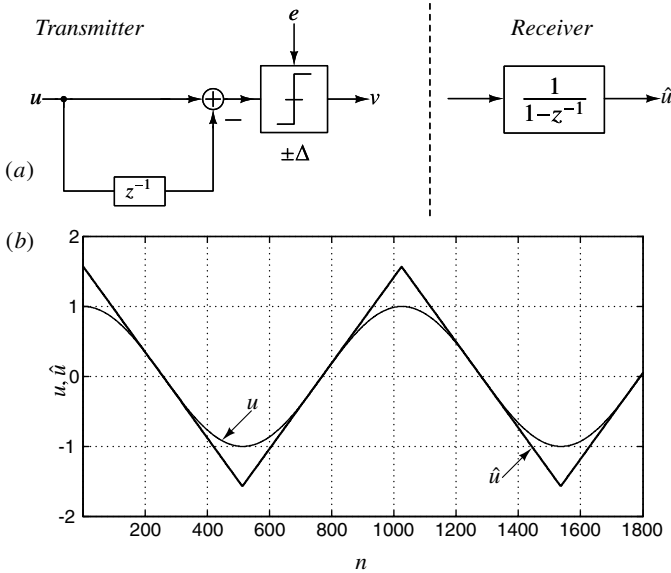


Figure 1.24 (a) A simple-minded attempt at quantizing the difference between successive samples of a highly oversampled signal. (b) Input and reconstructed waveforms. The reconstruction error has a large low-frequency component.

The Δ -modulator, which is a fundamental improvement over the idea discussed above, derives the delayed version of the input by integrating v , as shown in Figure 1.25(a). As a consequence, the quantization error e is in the feedback loop. It can be thought of as quantizing the difference between the input and its predicted value. In fact, the name Δ modulator is derived from the fact that the output is based on the difference (Δ) between a sample of the input and a predicted value of that sample. In the general case, the loop filter may be a higher-order circuit, which generates a more accurate prediction of the input sample $u[n]$, in order to subtract from the actual $u[n]$. This type of modulator is sometimes called a *predictive encoder*.

Referring to Figure 1.25,

$$v[n] = u[n] - u[n - 1] + e[n] - e[n - 1]. \tag{1.24}$$

We see that the quantization noise is also first-order shaped, and the reconstruction error at the receiver will therefore be much smaller. This is confirmed by the waveforms in Figure 1.25(b) – for the same input and step size, \hat{u} is a much better approximation to u when compared to the system of Figure 1.24(a). Since v is a two-level sequence from which u can be reconstructed, it follows that the Δ -modulator can also be thought of as an ADC. It, however, has several disadvantages. The loop filter (integrator for the first-order loop shown) is in the feedback path, and hence, its nonidealities limit the achievable

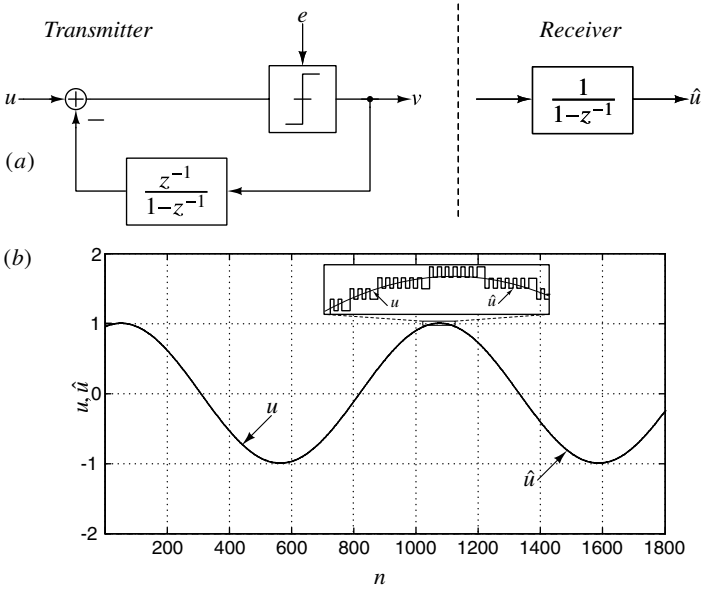


Figure 1.25 (a) The Δ -modulator. (b) Reconstruction error is greatly reduced due to noise-shaping of the quantizer’s error.

linearity and accuracy. The integrator in the receiver has a high gain in the signal band, and hence, it will amplify the nonlinear distortion of the transmitted waveform as well as any noise picked up by the signal between the modulator and demodulator. It can also produce an arbitrary dc offset in the output. A delta-modulator, therefore, does not work reliably with a dc input.

The Δ -modulator of Figure 1.25 is also called an error-feedback structure. It was proposed in 1952 by de Jager [3], and in a different form by Cutler [4].

The $\Delta\Sigma$ modulator of Figure 1.13 is an alternative oversampling structure that avoids the shortcomings of the Δ -modulator. It is again a feedback loop, containing a loop filter as well as an internal low-resolution quantizer, but the loop filter is now in the forward path of the loop. As seen earlier, the $\Delta\Sigma$ modulator’s output is given by

$$v[n] = u[n - 1] + e[n] - e[n - 1]. \tag{1.25}$$

Thus, the digital output contains a delayed, but otherwise unchanged, replica of the analog input signal u and a differentiated version of the quantization error e . Since the signal is not changed by the modulation process, the demodulation operation does not need an integrator as was the case for the delta modulator. Hence, the amplification of in-band noise and distortion at the receiver does not take place. Furthermore, the differentiation of the error e suppresses it at frequencies that are small compared to the sampling rate f_s . In general, if the loop filter has a high gain in the signal band, the in-band quantization “noise” is strongly attenuated, a process now commonly called noise shaping.

The $\Delta\Sigma$ modulator can be obtained from the Δ -modulator by cascading an integrator or summing block with the delta modulator. Hence, the structure of Figure 1.13 came to be called a sigma-delta ($\Sigma\Delta$) modulator. Alternatively, one can observe the differencing at

the input, followed by the summation in the loop filter, and hence call the structure a delta-sigma ($\Delta\Sigma$) modulator. Other systems with higher-order loop filters, multi-bit quantizers and the like are most properly called noise-shaping modulators, but it is common to extend the term $\Delta\Sigma$ modulator (or $\Sigma\Delta$ modulator) to these systems as well.

Although the basic idea of using feedback to improve the accuracy of data conversion has been around for about 50 years, the concept of noise-shaping was probably first proposed (along with the name delta-sigma modulation) in 1962 by Inose et al. [5]. They described a system containing a continuous-time integrator as the loop filter, and a Schmitt trigger as the ADC, that achieved (nearly) 40 dB SNR and had a signal bandwidth of about 5 kHz. Since the trade-off between analog accuracy and higher speed plus additional digital hardware was not particularly attractive at the time, further research on this topic was relatively sparse for a while.

Twelve years later, Ritchie proposed the use of higher-order loop filters [6]. Useful theory, as well as analysis and design techniques were developed by Candy and his collaborators at Bell Laboratories [7, 8, 9, 10, 11]. Candy and Huynh also proposed the MASH concept for the digital modulators used in $\Delta\Sigma$ DACs [12]. In 1986, Adams described an 18-bit $\Delta\Sigma$ ADC that used a third-order continuous-time loop filter, and a 4-bit quantizer with trimmed resistors performing as the DAC [13]. The MASH configuration was first applied in $\Delta\Sigma$ ADCs by Hayashi et al. [14] in 1986.

Using a multi-bit internal quantizer in a $\Delta\Sigma$ loop with digital linearity correction was proposed by Larson et al. [15] in 1988; the use of dynamic matching (randomization) was also introduced for the internal DAC of a $\Delta\Sigma$ ADC by Carley and Kenney in 1988 [16]. Various mismatch-shaping algorithms were suggested subsequently by Leung and Sutarja [17], Story [18], Redman-White and Bourner [19], Jackson [20], Adams and Kwan [21], Baird and Fiez [22], Schreier and Zhang [23], and Galton [24].

Bandpass $\Delta\Sigma$ modulators were motivated for their potential applications in wireless communications, and emerged in the late 1980s [25, 26, 27].

Current design trends in $\Delta\Sigma$ converters are aimed at extending the signal frequency range without any reduction in SNR. This will open up new applications in digital video, wireless and wired communications, radar and so on. Higher speed can often be achieved by using high-resolution (typically, 5-bit) internal quantizers, and a multistage (2- or 3-stage) MASH architecture. To correct for the nonlinearity of the internal DAC and for quantization noise leakage, digital correction algorithms have been proposed [28] for $\Delta\Sigma$ ADCs. A great deal of effort is also being applied to improving the performance of bandpass $\Delta\Sigma$ ADCs [29, 30, 31, 32, 33].

Over the last decade, there has been a significant wave of research, and commercial deployment of continuous-time $\Delta\Sigma$ ADCs. The benefits of such converters are many. As discussed earlier in this chapter, they feature the remarkable property of inherent anti-aliasing. It turns out that this makes them robust when they are part of a large digital chip with significant substrate noise. The input impedance of these ADCs is (usually) resistive, making them easy to drive. Reference generation circuitry is also generally simpler to design when compared to the corresponding effort needed in the case of a Nyquist ADC.

Technological trends (finer line widths, accompanied with lower breakdown voltages) stimulated research into $\Delta\Sigma$ modulators needing only low supply voltages [34]. Also applications opening up in portable devices motivated the development of low-power design techniques for $\Delta\Sigma$ data converters. Finally, applications in the instrumentation

and measurements area, including biomedical sensor interfaces motivated the development of low-frequency and very-high-accuracy ADCs, often realized by periodically reset $\Delta\Sigma$ modulators (which, as we discussed earlier, are called *incremental data converters*).

As noise-shaping theory and practice continue to mature, $\Delta\Sigma$ data converters can be expected to expand their range of application further.

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