CHAPTER 1

INTRODUCTION TO ΣΔ MODULATORS: FUNDAMENTALS, BASIC ARCHITECTURE AND PERFORMANCE METRICS

This chapter is conceived as an introduction to ΣΔ data converters. Their operating principle consists in combining oversampling, quantization error processing, and negative feedback for improving the effective resolution of a coarse quantizer. These basic concepts are presented in Section 1.1, putting especial emphasis on the two main processes involved in the analog-to-digital conversion, namely sampling and quantization. The errors associated with their inherent continuous-to-discrete transformations are analyzed and the way in which they can be mitigated by combining oversampling and noise shaping is presented. On the basis of these ingredients, the performance of ΣΔ converters is compared with Nyquist-rate converters in order to illustrate how to achieve the same specifications by trading circuit element accuracy for signal processing.

Section 1.2 shows the basic architecture, ideal behavior, and performance metrics of ΣΔ modulators and the simplest way to implement such an architecture is presented in Section 1.3, where the so-called first-order ΣΔ modulator is analyzed in detail. This simple architecture is used as an illustration to show the principles of operation behind ΣΔMs and to highlight the main drawbacks of the correlation between the quantization error and the input signal. System-level design parameters and strategies to enhance the performance of ΣΔ converters are discussed in Section 1.4, and the different types of ΣΔ topologies and their implementations are outlined. Everything is put together in Sections 1.5 and 1.6, where the different building blocks required to implement ADCs and DACs are described.

Sigma-Delta Converters: Practical Design Guide, Second Edition. José M. de la Rosa.

1.1 Basics of Analog-to-Digital Conversion

ADCs are electronic systems that perform the transformation of analog signals–which are continuous in time and in amplitude–into digital signals–which are discrete in both time and amplitude. Figure 1.1a illustrates the general block diagram of an ADC intended for the conversion of low-pass (LP) signals, It essentially consists of an *antialiasing filter* (AAF), a *sampler*, a *quantizer* and a *coder*.

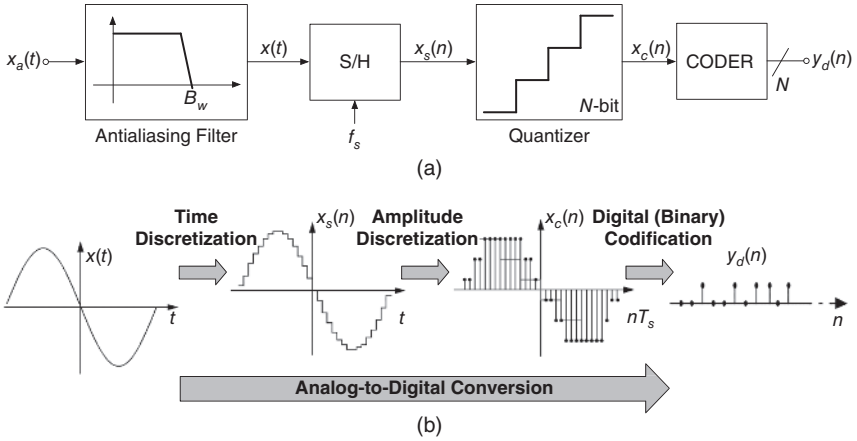

Figure 1.1 Analog-to-digital conversion: (a) conceptual block diagram; (b) signal processing. A Nyquist-rate ADC is assumed.

The operation of these blocks is illustrated in Figure 1.1b. First, the analog input signal $x_a(t)$ of the ADC passes through the AAF: an LP analog filter that prevents out-of-band components from folding over the signal bandwidth B_w during the subsequent sampling, which would corrupt the signal information according to the Nyquist sampling theorem. The resulting band-limited signal $x(t)$ is sampled at a rate f_s by the sampling and hold (S/H) circuit, thus yielding a discrete-time signal $x_s(n) = x(nT_s)$, where $T_s = 1/f_s$ stands for the sampling period. The continuous range of amplitudes of $x_s(n)$ are quantized using N bits, so that each continuous-valued input sample of the quantizer is mapped onto the closer discrete-valued level out of the 2^N that cover the input range. Finally, the digitization process is completed by assigning a unique digital code to each output level of the quantizer, normally using binary coding, which yields the N-bit digital output $y_d(n)$.

As conceptually shown in Figure 1.1b, the fundamental processes involved in A/D conversion are sampling and quantization. Both processes implement a continuous-to-discrete transformation, the former in time and the latter in amplitude. These two continuous-to-discrete transformations limit the performance of ADCs, defining their main specifications, in terms of the speed and accuracy, the latter also referred to as *resolution*[1] and measured in bits. It is therefore very common to compare the performance of different types of ADCs in the resolution-versus-speed plane, as illustrated in Figure 1.2. In this picture, the state-of-the-art performance of different digitization techniques – ΣΔ, Flash, two-step, folding, pipeline and SAR – are depicted. It can be seen that the so-called ΣΔ ADCs – the topic of this book – have the widest conversion region. This is one of the motivations for considering ΣΔ techniques for the implementation of ADCs, but it is not the only one. To understand

[1] As will be explained later in this book, the accuracy of an ADC is not only limited in practice by the quantization process, but also by a number of nonideal effects caused by the circuit and the physical implementation of the chip.

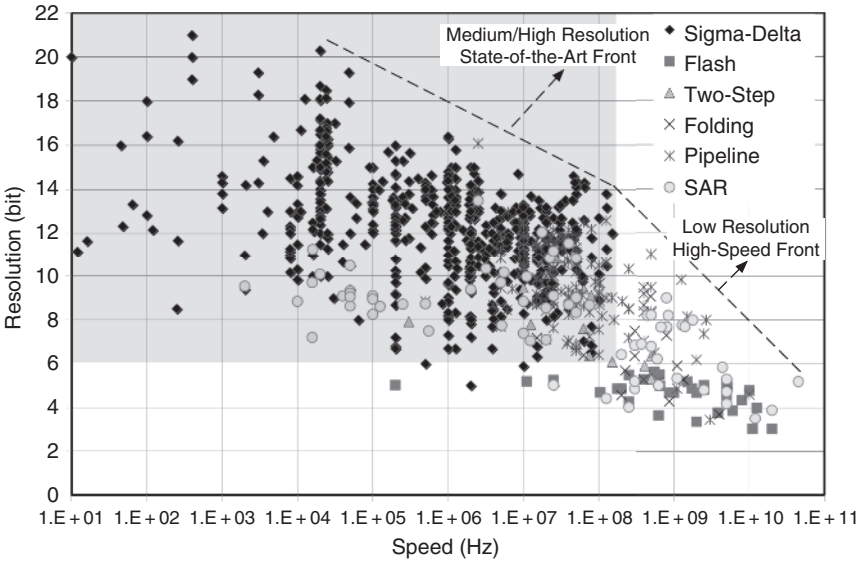

Figure 1.2 Resolution (accuracy) versus speed achieved by state-of-the-art ADCs.

the main benefits of ΣΔ ADCs it is important first to analyze in detail the processes involved in A/D conversion, namely sampling and quantization.

1.1.1 Sampling

As stated above, the sampling process performs the continuous-to-discrete transformation of the input signal in time and imposes a limit on the bandwidth of the analog input signal. According to the Nyquist theorem, to prevent information loss, $x(t)$ must be sampled at a minimum rate of $f_N = 2B_w$, often referred to as the Nyquist frequency. On the basis of this criterion, ADCs in which the analog input signal is sampled at the minimum rate ($f_s = f_N$) are called *Nyquist-rate ADCs*. Conversely, ADCs in which $f_s > f_N$ are called *oversampling ADCs*. How much faster than required the input signal is sampled is expressed in terms of the *oversampling ratio* (OSR), defined as:

$$\mathrm{OSR} = \frac{f_s}{2B_w} \tag{1.1}$$

Whether oversampling is used or not in an ADC has a noticeable influence on the requirements of its antialiasing filter. Since in Nyquist-rate ADCs the input signal bandwidth B_w coincides with $f_s/2$, aliasing will occur if $x_a(t)$ (as shown in Figure 1.1) contains frequency components above $f_s/2$. Higher-order analog AAFs are thus required to implement sharp transition bands capable of removing out-of-band components with no significant attenuation of the signal band, as illustrated in Figure 1.3a for the LP case. Conversely, since $f_s/2 > B_w$ in oversampling ADCs, the replicas of the input signal spectrum that are created by the sampling process are farther apart than in Nyquist-rate ADCs. As illustrated in Figure 1.3b, frequency components of the input signal in the range $[B_w, f_s - B_w]$ do not alias within the signal band, so that the filter transition band can be smoother; this greatly reduces the order required for the AAF and simplifies its design.

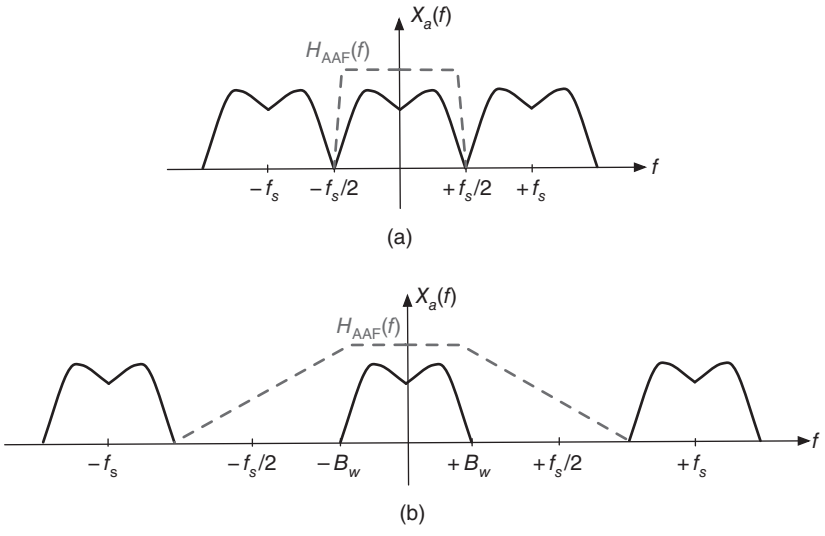

Figure 1.3 Antialiasing filter for: (a) Nyquist-rate ADCs; (b) oversampling ADCs.

1.1.2 Quantization

The quantization process also introduces a limitation on the performance of an ideal ADC, since an error is generated while performing the continuous-to-discrete transformation of the input signal in amplitude. This is commonly referred to as *quantization error*. The basic operation of quantizers is illustrated in Figure 1.4.

As an example, Figure 1.4c depicts the I/O characteristic of a quantizer with $N = 2$, although the results also apply to a generic N-bit quantizer. Input amplitudes within the full-scale input range $[-X_{FS}/2, +X_{FS}/2]$ are *rounded* to one out of the 2^N different output levels, which are usually encoded into a binary digital representation. If these levels are equally spaced, the quantizer is said to be *uniform* and the separation between adjacent output levels is defined as the *quantization step*,

$$\Delta = \frac{Y_{FS}}{2^N - 1} \tag{1.2}$$

where Y_{FS} stands for the full-scale output range. Since X_{FS} and Y_{FS} are not necessarily equal, the quantizer may exhibit a gain different from unity, as indicated in Figure 1.4c by the slope k_q. As shown in Figure 1.4e, the quantizer operation thus inherently generates a *rounding* error that is a nonlinear function of the input. Note that, if $q(n)$ is kept within the range $[-X_{FS}/2, +X_{FS}/2]$, the quantization error $e(n)$ is bounded within $[-\Delta/2, +\Delta/2]$. The former input range is known as the *nonoverload region* of the quantizer, as opposed to ranges with $|q(n)| > \Delta/2$, for which the magnitude of $e(n)$ grows monotonously. Figure 1.4 also shows the operation of a single-bit quantizer ($N = 1$). Note from Figure 1.4d that, compared to the multi-bit case, the output of a single-bit quantizer is determined by the input sign only, regardless its magnitude. Therefore, the gain k_q is undefined and can be arbitrarily chosen.

The quantization characteristics shown in Figure 1.4a correspond to those of so-called *midriser* quantizers. This term comes from what happens in the region around the zero value of the I/O characteristics, considering the analogy with a *staircase*. As a result, the number of levels is always an even number. Alternatively, there is another type of quantizer block called a *midtread* quantizer,

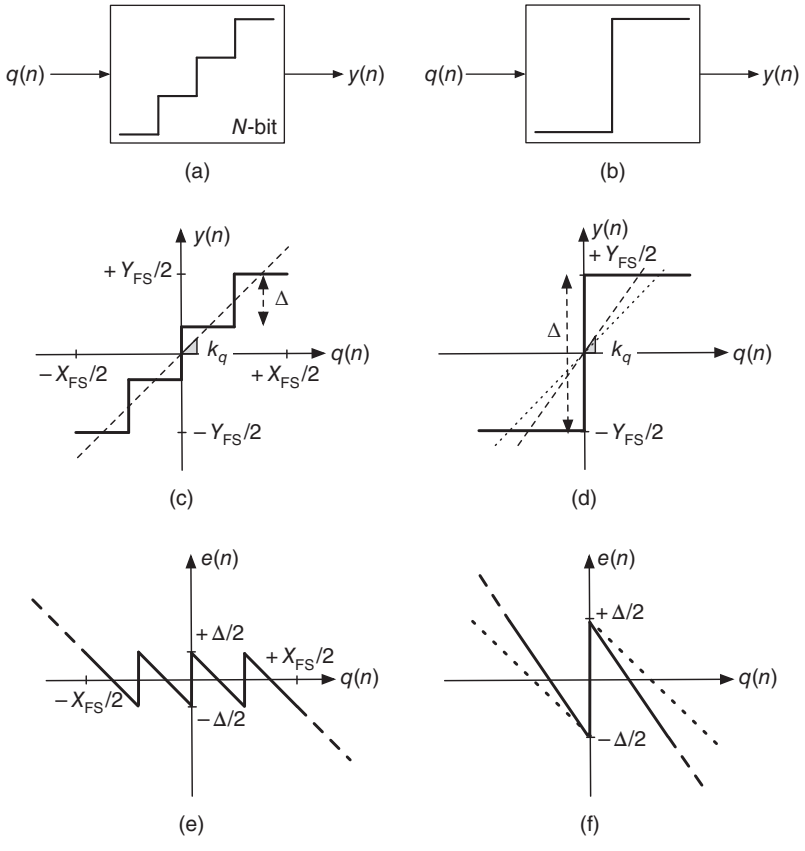

Figure 1.4 Quantization process: (a) multi-bit quantizer block; (b) single-bit quantizer block; (c) I/O characteristic of a multi-bit quantizer; (d) I/O characteristic of a single-bit quantizer; (e) multi-bit quantization error; (f) single-bit quantization error.

with a conceptual I/O characteristic like that shown in Figure 1.5a, in which the level corresponding to zero – like the tread of a staircase – is also considered a valid level for quantization purposes. These quantization I/O characteristics are usually exploited by fully-differential circuits, in which the zero value can be obtained by simply subtracting the characteristics of the two branches implementing the differential circuitry. For instance, Figure 1.5b illustrates how to obtain a three-level quantizer from two single-level quantizers; that is, comparator functions. In what follows, a midriser quantization will be considered, but without loss of generality.

1.1.3 Quantization White Noise Model

In practice, an ideal quantizer such as that shown in Figure 1.6a can often be modeled using the linear scheme in Figure 1.6b if several assumptions are made about the statistical properties of the quantization error [1–3]. As already shown in Figure 1.4e, the quantization error $e(n)$ is systematically determined by the quantizer input signal $q(n)$. Nevertheless, if $q(n)$ is assumed to change randomly from sample to sample within the range $[-\Delta/2, +\Delta/2]$, $e(n)$ will also be uncorrelated from sample to sample. This behavior is also seen if the number of quantizer levels increases. This is illustrated in

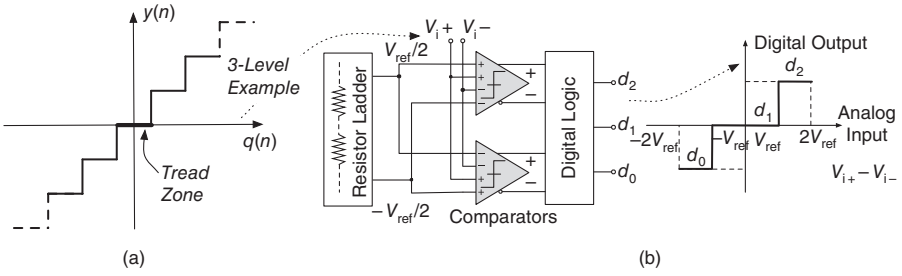

Figure 1.5 Midtread quantization: (a) conceptual I/O characteristic; (b) illustration of a three-level ADC made up of two single-bit quantizers (comparators).

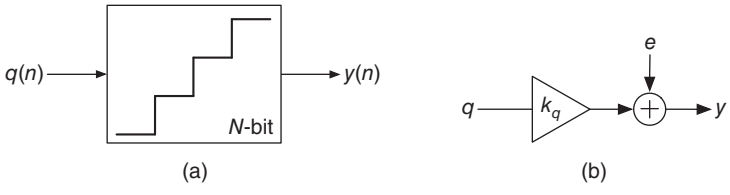

Figure 1.6 Quantization linear model: (a) multi-bit quantizer block; (b) equivalent model with additive white noise.

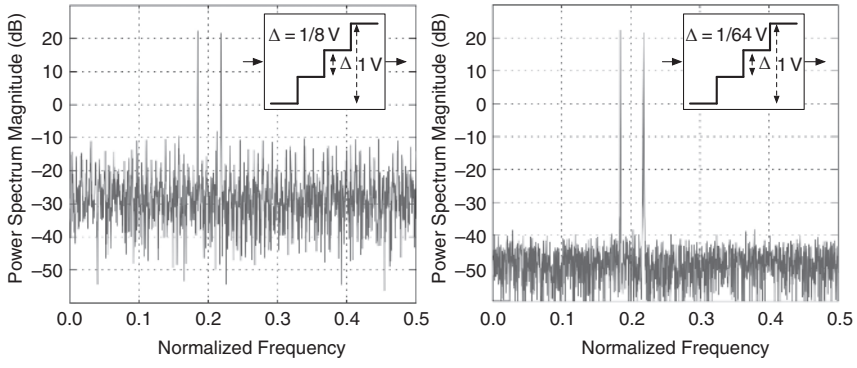

Figure 1.7 Illustrating the validity of the white-noise model for a quantizer when the number of levels of the quantizer is increased when a two-tone input signal is applied.

Figure 1.7, where a quantizer is excited by a two-tone signal. Note that a number of intermodulation tones can be observed in the output spectrum of the quantizer. These tones are caused by the strong correlation between the quantizer input and the quantization error, as conceptually depicted in Figure 1.4e. However, as the number of quantizer levels is increased (by decreasing Δ), the number of tones is drastically reduced, apart from the obvious reduction of the noise power.

Under these requirements, the quantization error can be viewed as a *random process with a uniform probability distribution* in the range $[-\Delta/2, +\Delta/2]$, as illustrated in Figure 1.8a. The power

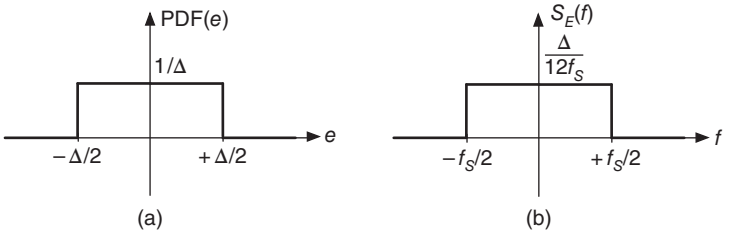

Figure 1.8 Quantization white noise: (a) probability density function (PDF); (b) power spectral density.

associated with the quantization error can thus be computed as:

$$\overline{e^2} = \sigma_e^2 = \int_{-\infty}^{+\infty} e^2 \mathrm{PDF}(e)\mathrm{d}e = \frac{1}{\Delta}\int_{-\Delta/2}^{+\Delta/2} e^2 \mathrm{d}e = \frac{\Delta^2}{12} \tag{1.3}$$

The former assumption implies that, as illustrated in Figure 1.8b, the power of the quantization error will be also *uniformly* distributed in the range $[-f_s/2, +f_s/2]$, yielding

$$\overline{e^2} = \int_{-\infty}^{+\infty} S_E(f)\mathrm{d}f = S_E \int_{-f_s/2}^{+f_s/2} \mathrm{d}f = \frac{\Delta^2}{12} \tag{1.4}$$

so that the power spectral density (PSD) of the quantization error in that range is:

$$S_E = \frac{\overline{e^2}}{f_s} = \frac{\Delta^2}{12f_s} \tag{1.5}$$

These assumptions are collectively known to as the *additive white noise approximation* of the quantization error and allow the representation of a quantizer that is deterministic and nonlinear with the random linear model in Figure 1.6b. Here $y(n) = k_q q(n) + e(n)$, with $e(n)$ being *quantization noise*.[2]

With the approximation of the quantization error as white noise, the performance of ideal ADCs can be easily evaluated. For a Nyquist ADC in which $f_s = 2B_w$, all the quantization noise power falls inside the signal band and passes to the ADC output as a part of the input signal itself, as illustrated in Figure 1.9a. Conversely, if an oversampled signal is quantized, since $f_s > 2B_w$, only a fraction of the total quantization noise power lies within the signal band, as illustrated in Figure 1.9b. The *in-band noise power* (IBN) caused by the quantization process in an ideal oversampling ADC is thus,

$$\mathrm{IBN} = \int_{-B_w}^{+B_w} S_E(f)\mathrm{d}f = \int_{-B_w}^{+B_w} \frac{\Delta^2}{12f_s}\mathrm{d}f = \frac{\Delta^2}{12\mathrm{OSR}} \tag{1.6}$$

so that the larger the oversampling ratio, the smaller the IBN.[3]

[2] Although the assumptions underlying the additive white noise approximation are rarely met in practice and are not strictly valid, it is commonly used in ADC design and usually yields good results – and better for a larger number of bits in the quantizer, as illustrated in Figure 1.7. Even though strictly speaking it is not valid for stand-alone single-bit quantizers, the assumption is also employed in the design of single-bit ΣΔ modulators [4].

[3] Note that Equation (1.6) for the IBN of oversampling ADCs also holds true for Nyquist ADCs, just considering OSR = 1. The same applies for subsequent expressions derived from Equation (1.6).

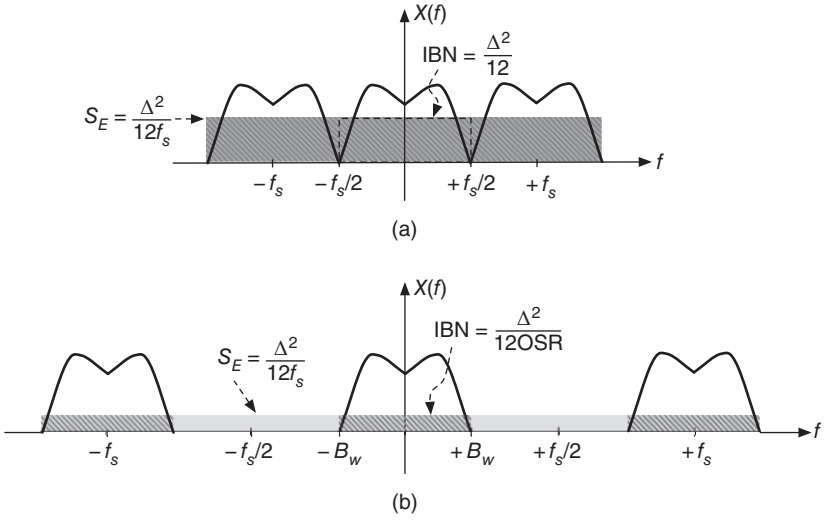

Figure 1.9 Quantization noise in: (a) Nyquist-rate ADCs; (b) oversampling ADCs.

The *dynamic range* (DR) of an ideal ADC can be determined as the ratio of the output power at the frequency of an input sinusoid with maximum amplitude to the in-band quantization noise power:

$$\text{DR (dB)} = 10\log_{10}\left(\frac{P_{\text{sig,out,max}}}{\text{IBN}}\right) \tag{1.7}$$

From Figure 1.4c, the maximum input amplitude in the nonoverload region of an N-bit quantizer is $X_{\text{FS}}/2$ and its corresponding output power can be approximated to [5]:

$$P_{\text{sig,out,max}} \approx \frac{(2^N\Delta/2)^2}{2} = 2^{2N-3}\Delta^2 \tag{1.8}$$

so that, using Equations (1.6) and (1.8), the DR of an ideal oversampling ADC yields:

$$\text{DR (dB)} \approx 6.02N + 1.76 + 10\log_{10}(\text{OSR}) \tag{1.9}$$

Note that, for a Nyquist ADC – that is, OSR = 1 in Equation (1.9) – each additional bit in the quantizer results in a DR increase of approximately 6 dB. For an oversampling ADC, the DR further increases with OSR by approximately 3 dB/octave, so that using, for instance, an OSR of 4 is similar to having one extra bit in the N-bit quantizer.

1.1.4 Noise Shaping

An approach to further increase the accuracy of an oversampling ADC is *shaping* the quantization white noise in the frequency domain – that is, filtering it – in such a way that most of its power lies outside the signal band. This is illustrated in Figure 1.10a, where the quantization noise is conceptually obtained by subtracting the quantizer input signal $q(n)$ from its output $y(n)$. It then passes through a filter transfer function, usually called *noise transfer function* (NTF).

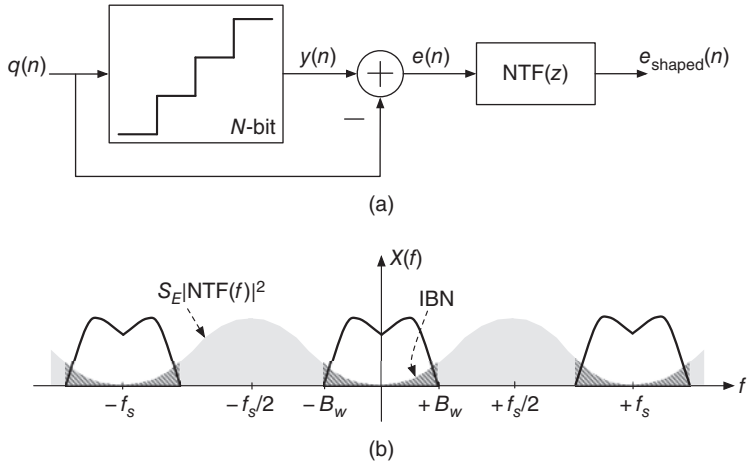

Figure 1.10 Quantization noise shaping: (a) conceptual block diagram; (b) effect on the in-band noise of an oversampling noise-shaping ADC.

For quantizers working on LP signals, NTF is of the high-pass type and can be easily obtained from a differentiator filter, with a Z-domain transfer function given by,

$$\mathrm{NTF}(z) = (1 - z^{-1})^L \tag{1.10}$$

where L stands for the filter order. Taking into account that $z = e^{sT_s} = e^{j2\pi f/f_s}$, the magnitude of the pure-differentiator NTF in Equation (1.10) can be approximated for low frequencies to

$$|\mathrm{NTF}(f)| = |1 - e^{-j2\pi f/f_s}|^L = \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^L \approx \left(\frac{2\pi f}{f_s}\right)^L, \quad \text{for } f \ll f_s \tag{1.11}$$

so that the power due to the shaped quantization noise that lies within the signal band yields:

$$\mathrm{IBN} = \int_{-B_w}^{+B_w} S_E(f)|\mathrm{NTF}(f)|^2 \mathrm{d}f \approx \frac{\Delta^2}{12}\frac{\pi^{2L}}{(2L+1)\mathrm{OSR}^{(2L+1)}} \tag{1.12}$$

Using Equations (1.8) and (1.12), the DR of an ideal oversampling noise-shaping ADC can be obtained as:

$$\mathrm{DR\ (dB)} \approx 6.02N + 1.76 + 10\log_{10}\left(\frac{2L+1}{\pi^{2L}}\right) + (2L+1)10\log_{10}(\mathrm{OSR}) \tag{1.13}$$

Note that, in comparison with Equation (1.9), if oversampling is used in combination with noise shaping, the DR increases with OSR by approximately $3(2L + 1)$ dB/octave.

1.2 Sigma-Delta Modulation

In contrast to the ADCs discussed so far, which are open-loop systems from a control perspective, ΣΔ ADCs rely on a feedback path to achieve closed-loop control of the quantization error. The fundamentals on how the shaping of quantization noise is implemented in practice, as well as the basic architecture, performance metrics, and ideal behavior of oversampling noise-shaping ADCs is presented in this section.

1.2.1 From Noise-shaped Systems to ΣΔ Modulators

The conceptual block diagram shown in Figure 1.10 only processes the quantization noise. In order to be used to digitize signals, the sampled input signal, $x_s(n)$, should be processed in parallel with the quantization noise, as conceptually depicted in Figure 1.11, where a *signal transfer function* (STF) is applied to the quantized version of $x_s(n)$. This, together with $e_{\text{shaped}}(n)$, yields a digital representation of the input signal, $y(n)$, which can be represented in the Z-domain as:

$$Y(z) = \text{STF}(z)X(z) + \text{NTF}(z)E(z) \tag{1.14}$$

There are many ways of implementing the system of Figure 1.11 in practice. One of the simplest forms is the so-called ΣΔ modulator (ΣΔM), which consists of a loop filter $H(z)$ and a B-bit quantizer in a feedback loop, as shown in Figure 1.12a [6]. Let us assume that the gain of the loop filter is large within the signal band and small outside it. Due to the action of the negative feedback, the analog input signal x and the analog version of the ΣΔM output y will coincide within the signal band, so that the error signal $x - y$ in this closed-loop system is very small within the signal band. Since the B-bit quantizer is uniform, most of the differences between the input and the output of the ΣΔM will be placed at higher frequencies, so that the quantization noise is shaped in the frequency domain and most of its power is pushed outside of the signal band.

Using the linear additive white noise model in Figure 1.6b for the embedded quantizer, the ΣΔM in Figure 1.12a can be modeled as the two-input (x and e) one-output (y) linear system shown in

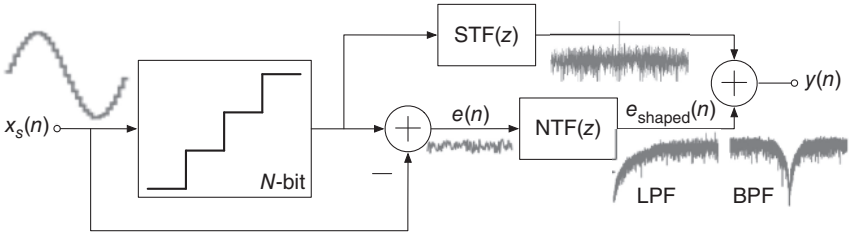

Figure 1.11 Conceptual block diagram of a noise-shaped ADC. Two different shaped noise output spectra are illustrated, for when the NTF is either a band-pass or a low-pass filter.

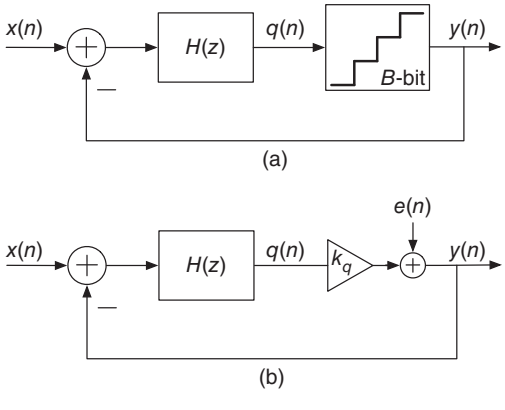

Figure 1.12 ΣΔ modulator: (a) block diagram; (b) ideal linear model.

Figure 1.12b, which is described in the Z-domain by Equation (1.14), where the STF and NTF are given by:

$$\mathrm{STF}(z) = \frac{k_q H(z)}{1 + k_q H(z)}, \quad \mathrm{NTF}(z) = \frac{1}{1 + k_q H(z)} \tag{1.15}$$

Note that, if the loop filter is designed such that $|H(f)| \gg 1$ within the signal band, then $|\mathrm{STF}(f)| \approx 1$ and $|\mathrm{NTF}(f)| \ll 1$; in other words, the quantization noise is ideally canceled while the input signal is perfectly transferred to the output.

1.2.2 Performance Metrics of ΣΔMs

In contrast to Nyquist-rate ADCs, whose performance is mainly characterized by static performance metrics – monotonicity, gain and offset errors, differential nonlinearity (DNL), and integral nonlinearity (INL) [5] – the characteristics of ΣΔ ADCs are typically measured using dynamic performance metrics, which are obtained from the frequency-domain representation of the time-domain digital output sequence. This therefore requires the computation of the fast Fourier transform (FFT) of a finite-length output sequence with a specific *windowing function*, as will be discussed in Chapter 5. From that power spectrum representation of a ΣΔM output sequence, various spectral metrics are directly measured and other noise and power metrics are derived.

Figure 1.13 illustrates an exemplary spectrum of a ΣΔM output sequence when a sinusoidal signal with frequency f_{in} is applied at the input. The main characteristics of the spectrum are highlighted: for example, the length of the digital sequence from which the FFT has been computed, the output signal peak at the frequency f_{in} corresponding to the converted signal, and so on. As will be discussed in Chapters 3 and 4, due to nonidealities of the circuitry used for implementing the ΣΔM, the output spectrum differs in practice from that from a *purely* shaped quantization noise. On the one hand, linear errors give rise to a noise floor, as well as to a degradation of the shaping order. On the other, nonlinear errors generate distortion, which is typically noticeable for large input amplitudes, but submerged under the noise floor for small input signal amplitudes. Spectral metrics such as the *spurious-free dynamic range* (SFDR) – the ratio of the signal power to the strongest spectral tone [5] – can be directly measured from the output modulator spectrum, as shown in Figure 1.13.

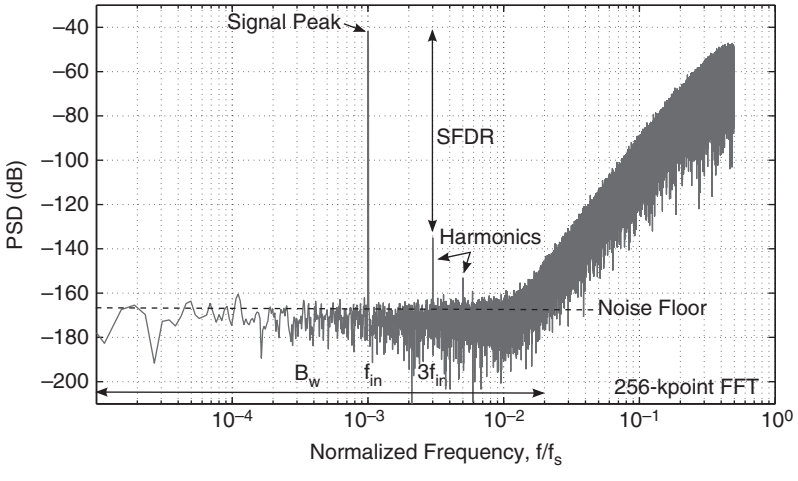

Figure 1.13 Illustration of a typical experimental output spectrum of a ΣΔ modulator and its main characteristics. An LP ΣΔM is assumed.

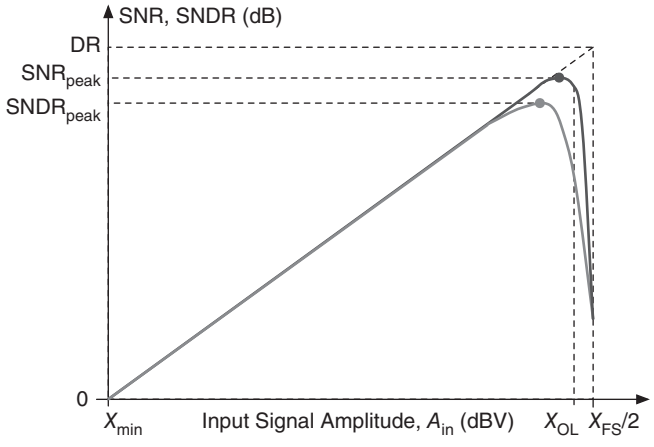

Figure 1.14 Illustration of the performance metrics of a ΣΔM on a typical SNR curve.

Noise and power metrics are derived from the ΣΔM output spectra by integration over the signal bandwidth. They are typically collected in a single plot, as shown in Figure 1.14. These metrics are usually the most important measures and comprise:

- **Signal-to-noise ratio (SNR)** is the ratio of the output power at the frequency of an input sinusoid to the *uncorrelated* in-band noise power:

$$\text{SNR (dB)} = 10\log_{10}\left(\frac{P_{\text{sig,out}}}{\text{IBN}}\right) \tag{1.16}$$

  This accounts for the modulator linear performance only, so that the in-band power associated with the harmonics of the input signal is not considered part of the IBN for SNR computations. If an ideal ΣΔM is considered and only the in-band quantization noise is accounted for in the IBN computation, the term *signal-to-quantization-noise ratio* (SQNR) is often employed.

- **Signal-to-noise-plus-distortion ratio (SNDR)** is defined as the ratio of the output power at the frequency of an input sinusoid to the total IBN power, also accounting for possible harmonics at the ΣΔM output. As illustrated in Figure 1.14, this makes a typical SNDR curve deviate from the SNR curve only for large input amplitudes, for which the generated distortion is noticeable. Therefore, the output spectra from which the SNDR curve is computed are typically obtained by applying an input signal at $f_{\text{in}} \leq B_w/3$ (for LP ΣΔMs), so that at least the second and third harmonics lie within the signal band.

- **Dynamic range (DR)** can be defined as the ratio of the output power at the frequency of an input sinusoid with maximum amplitude to the output power for a small input amplitude for which SNR = 0 dB; i.e., so it cannot be distinguished from the error. Ideally, a sinusoid with maximum amplitude at the modulator input will provide an output sinusoid sweeping the full-scale range Y_{FS} of the embedded quantizer, so that

$$\text{DR (dB)} = 10\log_{10}\left(\frac{P_{\text{sig,out,max}}}{\text{IBN}}\right) = 10\log_{10}\left[\frac{(Y_{\text{FS}}/2)^2}{2\text{IBN}}\right] \tag{1.17}$$

- **Effective number of bits (ENOB)**. Since the DR of an ideal N-bit Nyquist-rate converter is given by Equation (1.9) with OSR = 1, a similar expression can be established for ΣΔMs,

$$\text{ENOB(bit)} = \frac{\text{DR (dB)} - 1.76}{6.02} \tag{1.18}$$

  where ENOB can be defined as the number of bits needed for an ideal Nyquist-rate ADC to achieve the same DR as the ΣΔ ADC. The performance of oversampled ΣΔ converters and Nyquist-rate ADCs can thus be compared in simple way [7]. Instead of the DR, the peak SNDR is also often used in Equation (1.18) to express the accuracy of the A/D conversion in a ΣΔ modulator in bits.

- **Overload level (OL)**. As illustrated in Figure 1.14, the SNR of a ΣΔ modulator increases monotonously with the input signal amplitude (A_{in}), but sharply drops for input amplitudes close to half of the full-scale input range of the embedded quantizer ($X_{\text{FS}}/2$) due to its overload and the associated IBN increase. The overload level is considered to define the maximum input amplitude for which the ΣΔM still operates correctly, and can almost be arbitrarily defined, but it is typically chosen as the amplitude for which the SNR drops by 6 dB below the peak SNR [8].

1.3 The First-order ΣΔ Modulator

For the conversion of LP signals, the simplest loop filter $H(z)$ that exhibits the desired frequency performance defined in Equation 1.15 is an integrator, which has a Z-domain transfer function given by:

$$\text{ITF}(z) = \frac{1}{z-1} = \frac{z^{-1}}{1-z^{-1}} \tag{1.19}$$

The above transfer function can be realized using SC circuits, as illustrated in Figure 1.15. This circuit can be combined with an embedded quantizer, to implement a first-order ΣΔM. Note that the quantizer block is made up of an ADC in the feedforward path and a DAC in the feedback path. In this example, a single-comparator is used to implement the 1-bit ADC, whose output Y is the output of the modulator. This signal controls the feedback connection of reference voltages $V_{\text{ref+}}$ and $V_{\text{ref–}}$ to the integrator through an SC branch, which implements the required feedback 1-bit DAC. In this simple circuit example, both the modulator input and the DAC feedback signals are processed through the same sampling capacitor, C, in the integrator. Assuming a linear model for the quantizer with $k_q = 1$, the Z-transform of the modulator is given by:

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \tag{1.20}$$

This builds up a first-order high-pass shaping of the quantization noise – see Equation (1.10).

For the sake of illustration, Figure 1.16a shows the output waveform of a first-order ΣΔM with an embedded 3-bit (8-level) quantizer for a sinusoidal input signal. Note that, due to the combined action of oversampling and negative feedback, the modulator output is a pulse-density modulated (PDM) signal whose local average tracks the input signal value within adjacent code transitions.

Figure 1.16b plots the output *pulse stream*, often referred to as the *bitstream*, of a first-order ΣΔM with a 1-bit (2-level) quantizer, when a stair-waveform signal is applied at the input of the

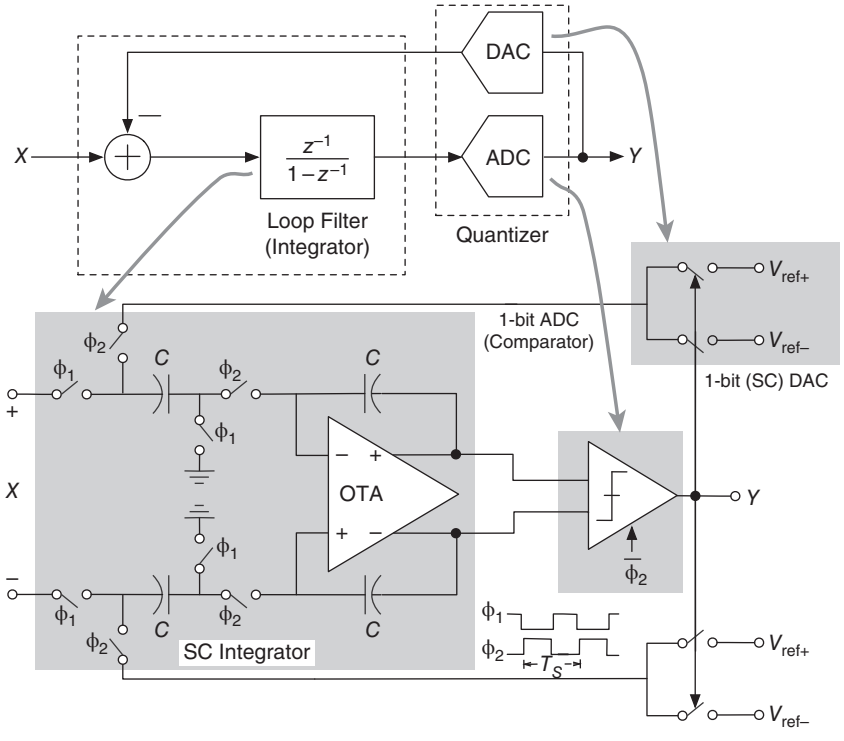

Figure 1.15 Block diagram of a first-order ΣΔM and its corresponding fully-differential SC circuit implementation with 1-bit quantization.

modulator. Note that the ΣΔM output pulse density is different for each input level, thus making the average of the feedback signal coincident with the corresponding stair step. The latter is better shown by considering an input DC signal and counting the number of positive (logic one) and negative (logic zero) pulses obtained at the output of the modulator. Table 1.1 illustrates the values of the input and output of a 1-bit quantizer in a first-order modulator by considering different cases of an input DC signal level measured by reference to the quantizer full-scale (FS) range, namely: 0, 1/3 and 2/3. It can be seen that there is always a repetitive pattern of output pulses – a digital representation of the input value – given by [9]:

$$\overline{Y} = \frac{P_{+1} - P_{-1}}{P_{+1} + P_{-1}} \cdot Y_{\text{FS}} \tag{1.21}$$

where P_{+1} and P_{-1} represent respectively the number of logic ones and logic zeroes included in the repetitive pattern (highlighted in Table 1.1). This behavior is the result of the action of the feedback in a ΣΔM, which forces the difference between the input and the output to be zero.

In spite of its simplicity, a negative effect of using a 1-bit quantizer in a first-order ΣΔM is the strong correlation between the input signal and the quantization error. This effect is illustrated in the so-called *noise pattern* [10] – depicted in Figure 1.17 – which represents the in-band quantization error power versus the DC value of the modulator input for OSR = 64. This strongly nonlinear behavior

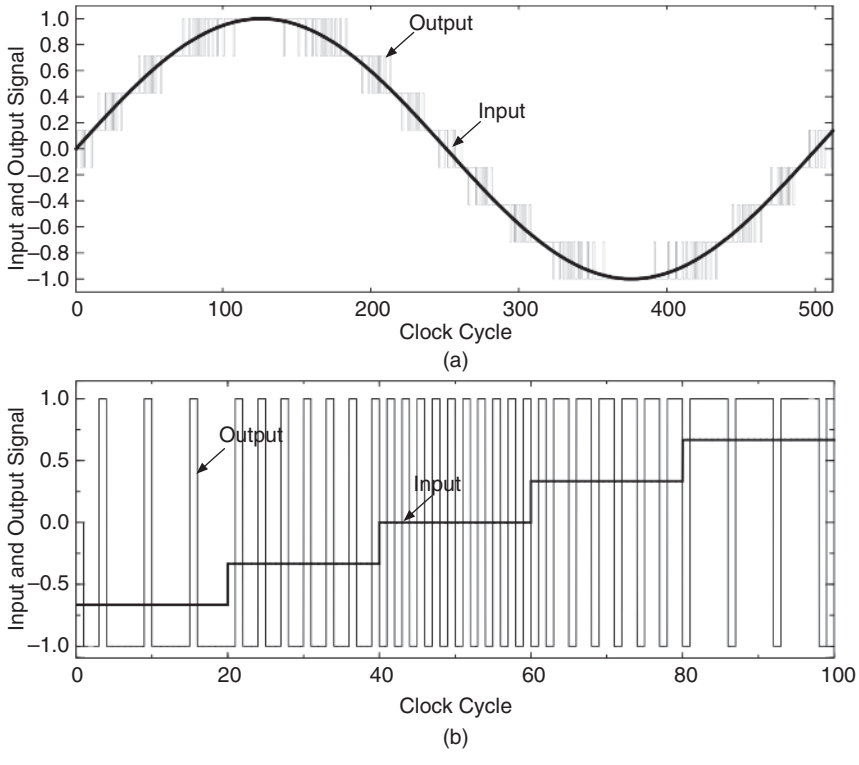

Figure 1.16 PDM output signal of a first-order ΣΔ modulator with a embedded (a) 3-bit quantizer for an input sinusoid and (b) 1-bit quantizer and an input stair waveform.

Table 1.1 Repetitive patterns in 1-bit ΣΔMs with DC inputs.

n	$q(n), y(n)$ $[\boldsymbol{x(n)=0}]$	$q(n), y(n)$ $[\boldsymbol{x(n)=1/3}]$	$q(n), y(n)$ $[\boldsymbol{x(n)=1/2}]$
0	$0, \mathbf{1}$	$0, \mathbf{1}$	$0, \mathbf{1}$
1	$-1, \mathbf{-1}$	$-2/3, \mathbf{-1}$	$-1/2, \mathbf{-1}$
2	$0, 1$	$2/3, \mathbf{1}$	$1, \mathbf{1}$
3	$-1, -1$	$0, 1$	$1/2, \mathbf{1}$
4	$0, 1$	$-2/3, -1$	$0, 1$
…	…	…	…

causes the linear model to be less valid and produces a number of discrete tones (often referred to as *idle tones* [9]) in the output spectrum, as illustrated in Figure 1.18. This tonal behavior disappears if the order of the loop filter, L, and/or the number of bits of the embedded quantizer, B, are increased, resulting in the white noise model being a better approximation for the quantizer. As an illustration, Figure 1.18 also shows the output spectrum of a first-order modulator with $B = 5$. It can be seen how, in addition a reduciton in the quantization noise power, the output spectrum tonality is drastically reduced as well.

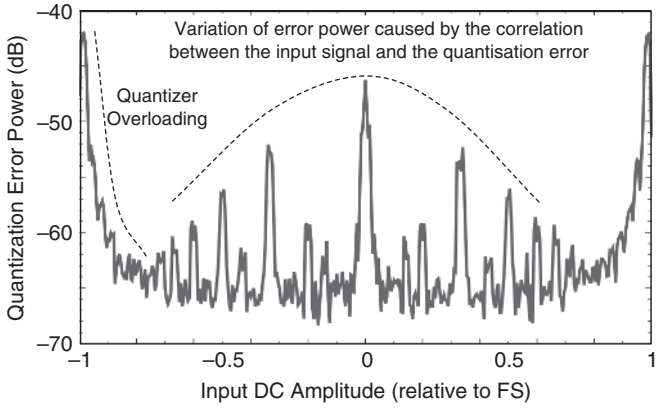

Figure 1.17 Noise pattern of a first-order ΣΔM with 1-bit quantizer.

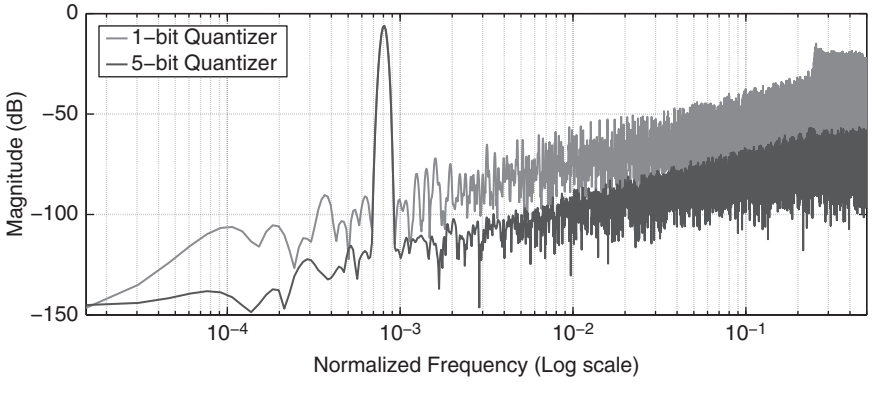

Figure 1.18 Output spectra of a first-order ΣΔM for a 1-bit and a 5-bit quantizer.

1.4 Performance Enhancement and Taxonomy of ΣΔMs

According to Equation 1.14, the output of an ideal LP Lth-order ΣΔM in the Z-domain can be considered to be

$$Y(z) = \mathrm{STF}(z)X(z) + \mathrm{NTF}(z)E(z) = z^{-L}X(z) + (1 - z^{-1})^{L}E(z) \tag{1.22}$$

where $|\mathrm{STF}(f)| = 1$ and the NTF builds up an Lth-order high-pass shaping of the quantization noise of the embedded quantizer. If a B-bit quantizer is employed, the dynamic range of the ΣΔM can be obtained from Equations (1.12) and (1.17) to ideally yield,

$$\mathrm{DR\ (dB)} = 10\log_{10}\left(\frac{P_{\mathrm{sig,out,max}}}{\mathrm{IBN}}\right) \approx 10\log_{10}\left[\frac{3}{2}(2^{B}-1)^{2}\frac{(2L+1)\mathrm{OSR}^{(2L+1)}}{\pi^{2L}}\right] \tag{1.23}$$

taking into account that $Y_{\mathrm{FS}} = (2^{B} - 1)\Delta$ – see Equation (1.2) – and considering quantization noise as the only contribution to the IBN.

1.4.1 ΣΔM System-level Design Parameters and Strategies

Note from Equation (1.23) that the dynamic range of a ΣΔ modulator is ideally determined by the values of L, OSR, and B, which can thus be considered as the three key parameters that define the ΣΔM at the top level. The pros and cons of increasing the DR of a ΣΔ modulator by increasing each of these parameters are briefly discussed next and will be analyzed in more detail in Chapter 2:

- **High-order ΣΔ modulators:** The accuracy of the A/D conversion can be considerably improved by increasing the noise-shaping order, since a larger fraction of the total quantization noise power will be pushed out of the signal band. Figure 1.19 illustrates the ideal noise-shaping functions of orders ranging from 1 to 5. The case $L = 0$ – no shaping – is also included for comparison purposes. The DR enhancement if L is increased by one for a given OSR can be obtained from Equation (1.23):

$$\Delta\text{DR (dB)} \approx 10\log_{10}\left[\frac{2L+3}{2L+1}\left(\frac{\text{OSR}}{\pi}\right)^2\right] \tag{1.24}$$

  This means that, for instance, the DR of a fourth-order ΣΔM with OSR = 32 is ideally 21.3 dB (3.5 bit) larger than that of a third-order ΣΔM. However, the use of high-order ($L > 2$) loop filters gives rise to stability problems in a ΣΔM. Although these problems can be circumvented, the dynamic range of a high-order ΣΔM will in practice be smaller than predicted by Equation (1.23).

- **High-OSR ΣΔ modulators:** Figure 1.20 shows the ideal dynamic range as a function of OSR for noise-shaping orders ranging from 0 (no shaping) to 5 and assuming a single-bit embedded quantizer ($B = 1$). As illustrated, the combination of oversampling and noise-shaping considerably enhances the ΣΔM performance for OSR > 4. Note from Equation (1.23) that the DR of an ideal L-order ΣΔM increases with OSR by $3(2L + 1)$ dB/octave. However, for a given conversion bandwidth B_w, the oversampling ratio cannot be arbitrarily increased, since it leads to a higher sampling frequency f_s for the operation of the ΣΔ circuitry. The latter, if achievable in practice for a given technological process, leads to larger power consumption.

- **Multibit ΣΔ modulators:** An increase in B leads to a decrease of the quantization step Δ and thus to a reduction of the quantization noise power. Each additional bit in the embedded quantizer of a ΣΔM is considered to typically yield a 6-dB (1-bit) improvement in the DR [11].

  However, a multi-bit embedded quantizer requires a multi-level DAC to close the negative feedback loop in the ΣΔM. In contrast to a two-level feedback DAC ($B = 1$), which is inherently

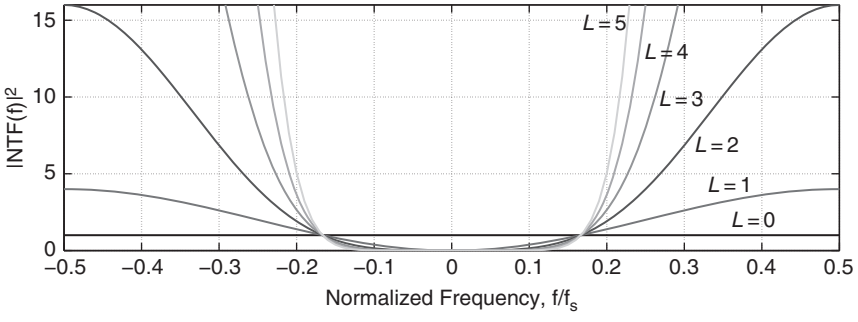

Figure 1.19 Illustration of the shaping of quantization noise as a function of frequency in a ΣΔM. NTF is given by Equation (1.10) and L is the noise-shaping order.

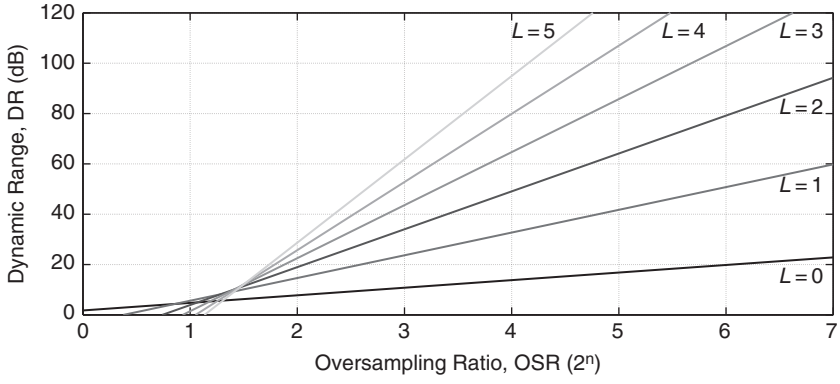

Figure 1.20 Ideal dynamic range of a ΣΔM as a function of the oversampling ratio for different noise-shaping orders (L). A single-bit internal quantizer ($B = 1$) is assumed.

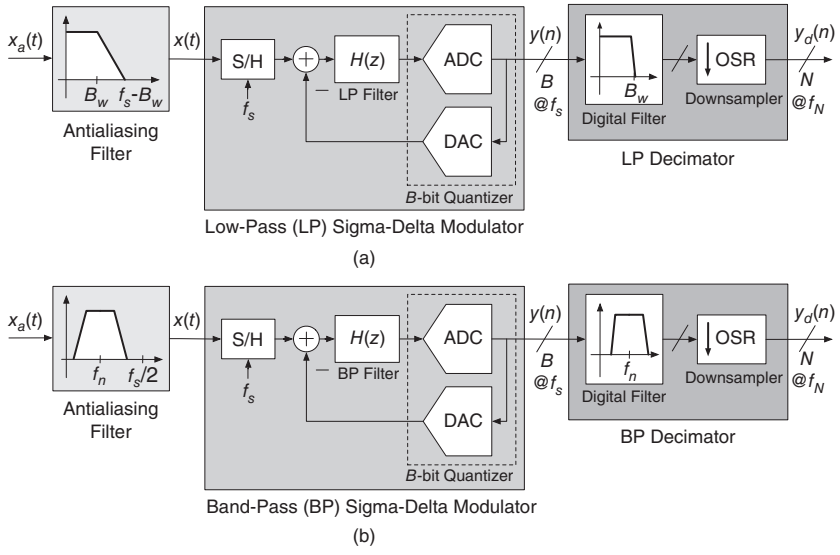

Figure 1.21 General block diagram of a ΣΔ ADC with: (a) LP signal; (b) BP signal.

linear, a multi-level DAC will in practice be nonlinear to some extent. As noticeable from Figure 1.21, the DAC nonlinearity will be directly added to the ΣΔM input and will thus appear at the output, since $|\mathrm{STF}(f)| \approx 1$ within the signal band. Therefore, the linearity required in a multi-bit DAC equals in practice that wanted for the ΣΔ modulator.

1.4.2 Classification of ΣΔMs

The strategies discussed above for improving the dynamic range of a ΣΔM may be combined in many different ways, giving rise to the huge number of ΣΔM topologies reported in literature, which can be grouped according to different classification criteria [12]:

- **Single-bit versus multi-bit ΣΔMs**, depending on the number of bits in the embedded quantizer.
- **Single-loop versus cascade ΣΔMs**, depending on the number of quantizers employed: ΣΔMs employing only one quantizer are called *single-loop* topologies, whereas those using several quantizers are often referred to as *cascade* or MASH ΣΔMs.
- **Low-pass versus band-pass ΣΔMs**, depending on the nature of the signals being converted. The A/D conversion of LP signals has been assumed in previous sections, but band-pass (BP) ΣΔMs can also be built.
- **Discrete-time versus continuous-time ΣΔMs**, depending on the nature of loop filter dynamics. The use of a discrete-time (DT) loop filter in the ΣΔM has been assumed in previous sections. However, continuous-time (CT) ΣΔMs can be also implemented in practice. According to this classification criteria, *hybrid* CT/DT ΣΔMs take advantage of the benefits of both DT and CT implementations.

Describing all possible ΣΔM architectures derived from these classification criteria goes beyond the scope of this book. A detailed analysis of them can be found in the vast quantity of papers and books available in the ΣΔ literature [4, 10, 11, 13–24]. Instead, this book will hereafter focus on the most representative families of ΣΔMs, and their benefits and drawbacks will be further discussed in Chapter 2. In the next sections, the different components required for use of ΣΔMs for the implementation of ADCs and DACs will be analyzed.

1.5 Putting All The Pieces Together: From ΣΔMs to ΣΔ ADCs

In order to use ΣΔMs for the implementation of ADCs, some additional building blocks are required to properly filter the input signal and remove the out-of-band quantization noise. Figure 1.21 illustrates the basic block diagram of a ΣΔ ADC, considering an LP signal (Figure 1.21a), and a BP signal (Figure 1.21b). In both cases, there are three main building blocks required to implement the ΣΔ ADC:

- **An antialiasing filter (AAF)** band limits the analog input signal to prevent aliasing during its subsequent sampling. As discussed in Section 1.1.1, oversampling can considerably relax the attenuation requirements of the AAF, so that smoother transition bands are usually sufficient, compared to Nyquist-rate ADCs. Typically, low-order (either first-order or second-order) filters are enough in the majority of applications. Moreover, in the case of CT-ΣΔMs, the ΣΔM implements an implicit AAF, as will be explained later in this book. This greatly simplifies this block in practice.
- **A sigma-delta modulator (ΣΔM)** is where the oversampling and quantization of the band-limited analog signal take place. The quantization noise of the embedded B-bit quantizer is shaped in the frequency domain by placing an appropriate loop filter $H(z)$ before it and closing a negative feedback loop around them both. As stated above, low-resolution quantizers, with B typically in the range 1–5 bits, are sufficient for obtaining small IBN and high accuracy in the A/D conversion.
- **A decimation filter** uses a high-selectivity digital filter to sharply remove the out-of-band spectral content of the ΣΔM output and thus most of the shaped quantization noise. The decimator also reduces the data rate from f_s down to the Nyquist frequency, while increasing the word length from B to N bits to preserve resolution.

The ΣΔ modulator is the block that has most influence on the performance metrics of the ADC, in essence because it is responsible for the sampling and quantization processes that ultimately limit the accuracy of the A/D conversion. This is the main reason why the majority of design efforts focus on the design of the modulator. In this book we will mainly focus on this block, although the reader should bear in mind that in order to build a complete ΣΔ ADC, the other blocks are always required.

1.5.1 Some Words about ΣΔ Decimators

Figure 1.22 depicts the signal processing of ΣΔ decimators considering both an LP-ΣΔ ADC and a BP-ΣΔ ADC. In this example, an single-tone input signal is used as a test signal, and hence the AAF does not have any action over the signal since it is band limited. The influence of the decimator is illustrated by firstly removing the out-of-band quantization noise and afterwards by downsampling the signal to the Nyquist rate. Note that the conceptual scheme shown in Figure 1.21b may require a highly selective digital BPF to implement decimation in BP-ΣΔ ADCs. However, as will be discussed in Section 2.5, this problem can be solved by mixing down the digital signal to baseband, where an LP decimator can be used.

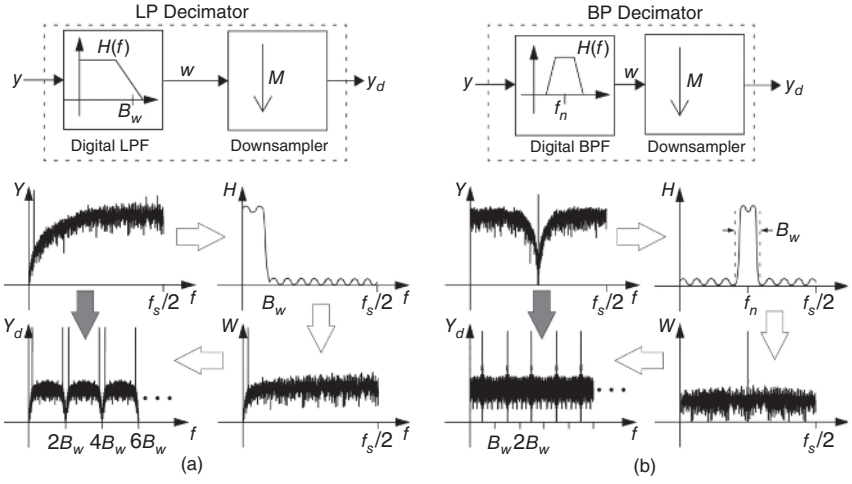

Figure 1.22 Illustrating the signal processing in ΣΔ decimators for: (a) LP ΣΔ ADCs, (b) BP ΣΔ ADCs.

As stated above, decimation filters reduce the oversampling frequency used by ΣΔMs down to the Nyquist rate, $f_s/2$, in order to process the signal more efficiently in the digital domain. The so-called cascaded-integrator-comb (CIC) structure – conceptually depicted in Figure 1.23 – is a compact way to implement decimation filters in ΣΔ ADCs, only requiring adders and delay elements for its implementation [25].

In the majority of practical situations, a multi-stage architecture is usually an efficient way to implement the filter and decimation stages in order to obtain a k-order decimation filter, as illustrated in Figure 1.23 [4]. The Z-domain transfer function of each stage is given by:

$$H_{\mathrm{CIC}}(z) = \frac{1}{M} \cdot \frac{1 - z^{-M}}{1 - z^{-1}} \tag{1.25}$$

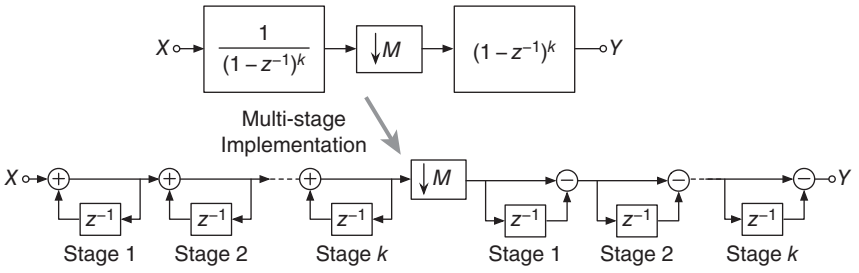

Figure 1.23 Block diagram of a k-order (sinc^k) CIC decimation filter.

which is also referred to as a *sinc* filter, whose frequency response is:

$$H_{\text{CIC}}(e^{j2\pi f}) = \frac{\text{sinc}(M\pi f)}{\text{sinc}(\pi f)} \tag{1.26}$$

where M is the decimation factor and $\text{sinc}(x) \equiv sin(x)/x$ stands for the *sinc* function. This function can be implemented at the logic level, as illustrated in Figure 1.24 [4].

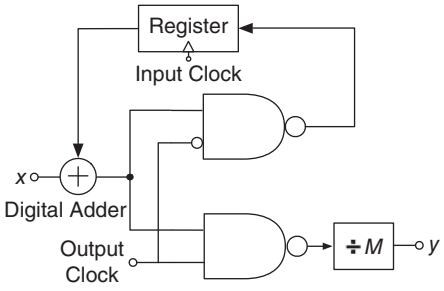

Figure 1.24 Decimation stage filter implementation [4].

It can be shown that a K-order CIC decimator produces a digital output with a word-length, b_{out}, given by [26]:

$$b_{\text{out}} = b_{\text{in}} + K \cdot \log_2 M \tag{1.27}$$

where b_{in} is the number of bits of the decimator input, i.e. the ΣΔM output. Note that if M is assumed to be a power of 2 – that is, $M = 2^p$ – then $b_{\text{out}} = b_{\text{in}} + p \cdot K$. For example, if a second-order decimator ($K = 2$), is used together with a 1-bit first-order ΣΔM with $M = 32$, an 11-bit word-length digital output is produced by the ΣΔ ADC.

It is important to note that a CIC decimator introduces a droop in the signal band, thus penalizing the resolution achieved by the ΣΔ ADC. Of course, a more accurate response can be obtained by increasing the decimator filter order, K, but at the price of increasing the circuit complexity and power consumption. As a rule of thumb, $K = L + 1$ is usually sufficient in most practical applications [19]. As an illustration, Figure 1.25 shows the time response of a ΣΔ ADC made up of a second-order ΣΔM and a third-order CIC decimator with $M = \text{OSR} = 128$ and $B = 1$, considering a half-scale input sine wave. It can be seen how, although the ΣΔM output is a PDM (single-bit) signal, the decimator output – the ADC output – is a multi-bit digital representation of the analog input signal (a sine wave in this example).

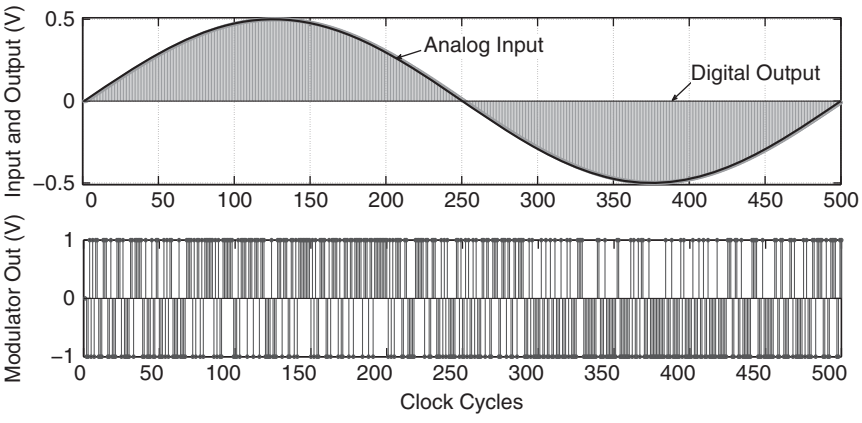

Figure 1.25 Signal waveforms in a ΣΔ ADC made up of a 1-bit second-order ΣΔM and a third-order CIC decimator.

Apart from CIC structures, other decimator topologies – such as recursive, multi-rate topologies, and so on – can be used to improve the efficiency in terms of silicon area and power consumption. This is especially so for high values of OSR, where the power increase is mostly due to the digital integrators, in which the adders operate at the highest sampling rate and with a full bit-width. A detailed analysis of different alternative decimation topologies is beyond the scope of this book and the interested reader can find a number of interesting publications related to this topic in the literature [26, 27].

1.6 ΣΔ DACs

DACs can take advantage of ΣΔ techniques to increase their performance by trading the accuracy of their analog components by digital signal processing. Figure 1.26 shows the block diagram of a ΣΔ DAC, which is made up of four main blocks: an interpolator, a digital ΣΔM, a DAC and an analog *reconstruction* filter. In this case, the ΣΔM is fully implemented in the digital domain, and combines oversampling and feedback to reduce the truncation error resulted from transforming a N_{in}-bit input signal into a N_{out}-bit output signal, with $N_{\text{in}} \ll N_{\text{out}}$. The ΣΔM input is provided by an interpolator filter, which generates the required oversampled N_{in}-bit data sequence sampled at $\text{OSR} \cdot f_N$. The truncation error that results from this transformation is shaped by the ΣΔM feedback loop, so that most of its power is pushed out of the signal band, where the ΣΔM digital output is converted into an analog signal by using a low-resolution highly-linear (typically $N_{\text{in}} = 1, 2$) DAC[4], and the out-of-band truncation noise can be subsequently removed using an analog filter.

1.6.1 System Design Trade-offs and Signal Processing in ΣΔ DACs

As illustrated in Figure 1.26, ΣΔ DACs are mostly-digital systems, except for the low-resolution DAC block and the reconstruction filter. However, the design of these blocks can be notably simplified

[4]The DAC building blocks used in ΣΔ DACs are typically implemented using current steering or SC circuit techniques, depending on the performance required in terms of speed and resolution. If high speed is required, current-steering circuits are usuaully the best approach, as will be discussed in Chapter 8.

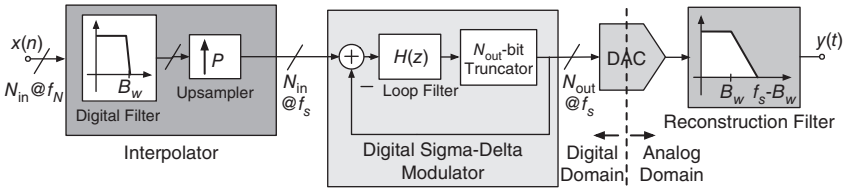

Figure 1.26 Conceptual block diagram of a ΣΔ DAC.

if OSR is high and $N_{out} = 1$. In this case, perfect linearity is guaranteed in the DAC and the filter specifications can be relaxed due to the action of OSR, in a similar way to what happens to the AAF in ΣΔ ADCs. Indeed, there are several design trade-offs involving the system-level parameters characterizing the performance of ΣΔ DACs, namely: N_{in}, N_{out}, OSR and L, with L being the ΣΔM loop-filter order.

On the one hand, using a low value of N_{out}, for instance $N_{out} = 1$, simplifies the design of the DAC circuit, and makes it more linear and robust against nonidealities. However, the stability of 1-bit ΣΔMs is more difficult to guarantee, specially for high values of L. Moreover, the high slew-rate of 1-bit DAC output (analog) signals and the large amount of out-of-band truncation noise, makes the design of the analog filter more complex. These design issues can be relaxed by using multi-bit ΣΔMs, but at the price of reducing the linearity of the DAC circuit [4].

Figure 1.27 shows the signal processing in ΣΔ DACs, where the operation of each building block is illustrated by the signal that results at its output. The role of the interpolator filter is the opposite of

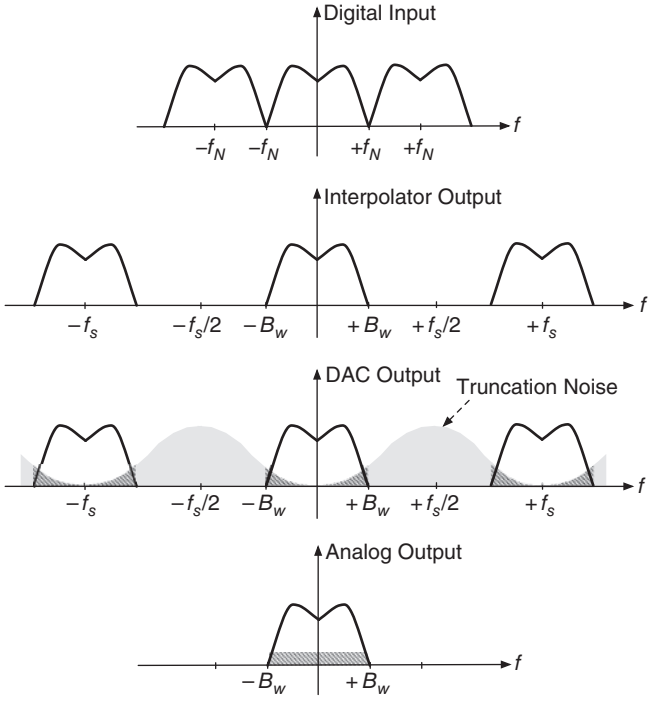

Figure 1.27 Illustration of signal processing in ΣΔ DACs.

a decimator: an interpolator oversamples the signal by increasing f_s from f_N to OSR $\cdot f_N$. One way of interpolating signals is to add OSR $-$ 1 zeroes between each sample of the input signal. This operation can be formulated in the discrete-time domain as:

$$y(n) = \begin{cases} x(n/\text{OSR}), & n = m \cdot \text{OSR} \\ 0, & \text{Otherwise} \end{cases} \tag{1.28}$$

where m is an integer number. Taking the Z-transform gives:

$$Y(z) = X(z^{\text{OSR}}) \tag{1.29}$$

The above function introduces spectral images or replicas at multiples of f_N, which must be suppressed by the interpolator filter, as depicted in Figure 1.27. To this end, a tap-based FIR filter can be used, although with this kind of filter topology, the chip area and the power consumption increase along with the number of taps included. A more efficient way of implementing interpolator filters is based on the use of multi-stage topologies – similar to those used in decimators – where the interpolation factor, $P \equiv$ OSR, is factorized in multiple steps, for example $P = P_1 \cdot P_2 \cdot P_3$..., where P_i is the interpolation factor of the ith stage.

An alternative interpolator implementation consists of repeating the signal samples at the oversampling rate; that is, without introducing zeroes between two consecutive input samples. In this case, the discrete-time response of the interpolator can be written as:

$$y(n) = x(n/P) \tag{1.30}$$

which can be represented in the frequency domain as a sinc function,

$$\frac{Y(f)}{X(f)} = \frac{\text{sinc}(\pi f)}{\text{sinc}(\pi f/P)} \tag{1.31}$$

As might be expected, the above transfer function is the inverse of that produced by decimator filters, as given in Equation (1.26). There are many ways of implementing interpolators. However, a detailed description is beyond the scope of this book and can be read in a number of references in the literature [28].

1.6.2 Implementation of Digital ΣΔMs used in DACs

As stated above, the operation of the ΣΔMs used to build DACs is similar to those used in ADCs. The main difference is related to the circuit implementation itself, since the ΣΔMs used in DACs are fully implemented in the digital domain, and hence, because all signals involved in the feedback systems are digital, no data conversion is required. Although their principle of operation is the same, and in theory similar architectures and system-level strategies can be applied to both ΣΔ ADCs and DACs, the digital implementation allows loop-filter solutions to be used, which are more robust against the effects of circuit nonidealities than the analog ones. Therefore, the loop-filter is implemented by digital accumulators – instead of analog integrators – and digital adders, delays and multipliers. They can be notably simplified in terms of hardware if the loop-filter coefficients are integer numbers, and even more so if they are powers of two.

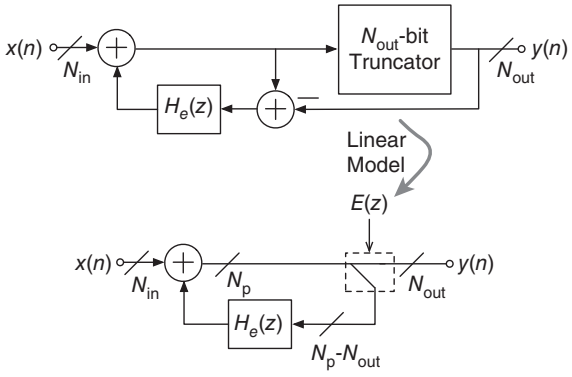

Figure 1.28 Conceptual block diagram of a digital ΣΔM typically used in ΣΔ DACs.

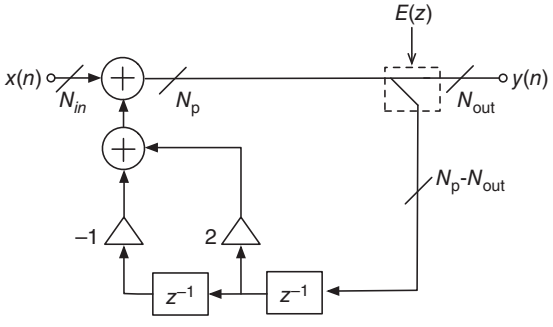

Figure 1.29 Block diagram of a second-order digital ΣΔM.

Figure 1.28 shows a system-level diagram of a highly efficient digital ΣΔM. Assuming a linear model for the truncator, it can be shown that the Z-domain transfer function of the ΣΔM output is given by:

$$Y(z) = X(z) + [1 - H_e(z)] \cdot E(z) \tag{1.32}$$

where $H_e(z)$ is the loop-filter transfer function, which – in contrast to analog ΣΔMs – is placed in the feedback path of the modulator. In the case of a first-order ΣΔM, $H_e(z) = z^{-1}$, and hence $STF(z) = 1$ and $NTF(z) = 1 - z^{-1}$. As an illustration, Figure 1.29 shows a second-order digital ΣΔM. In this case, $H_e(z) = 2z^{-1} - z^{-2}$, and hence $NTF(z) = (1 - z^{-1})^2$. As stated above, higher-order digital ΣΔMs can be implemented following the same philosophy as for their analog counterparts. Moreover, some state-of-the-art ΣΔ DACs use time-interleaving techniques in order to relax the speed specifications. This enables them to be used to handle signals in telecom applications operating in the gigahertz range, while keeping low values of the OSR [29].

1.7 Summary

This chapter has presented an introduction to ΣΔ converters. The benefits of employing oversampling and quantization noise shaping in the digitization of signals have been analyzed and compared to

the performance of Nyquist-rate ADCs. Among the blocks that build up a ΣΔ ADC, the chapter has focussed on the ΣΔ modulator, including its general architecture, ideal operation, and performance metrics.

The simplest topology of a ΣΔM – based on a first-order loop filter – was analyzed in detail to illustrate the principles of operation behind ΣΔ techniques that achieve high accuracy with low-resolution embedded quantization. The main limitations of first-order ΣΔMs – caused by the strong correlation between the quantization error and the input signal – were discussed and existing methods for increasing the effective resolution of ΣΔMs were highlighted as an introduction to the taxonomy of ΣΔM architectures; this will be discussed in more detail in Chapter 2.

The chapter concluded by showing how to build both ADCs and DACs using ΣΔMs. In both data-conversion systems, the core building block is the ΣΔM, which is implemented in the analog domain in ADCs and in the digital domain in DACs. The majority of system-level strategies – as will be discussed in Chapter 2 – can be applied to both analog and digital ΣΔMs. However, the former are more sensitive to nonideal-circuit effects, thus requiring more careful design and being in many cases the design bottleneck in very diverse electronic systems. Therefore, the rest of the book is mostly devoted to the practical design issues related to analog ΣΔMs, starting in next chapter with an analysis of their most representative system architectures.

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