1

Introduction

Current-mode control of pulse-width modulated (PWM) DC–DC converters has been one of the most challenging and interesting topics of study in the vast field of power electronics for almost two decades. Even to this day, rigorous research to establish a solid and systematic characterization of current-mode controlled DC–DC power converters is being performed. Continuing research in current-mode control is focused toward analysis, design, modeling, and efficient implementation in a wide variety of important applications such as power-factor correctors, battery chargers, and LED drivers. Chapters 2-5 seek to develop a complete characterization of the average current-mode control of basic DC–DC power converter topologies.

Current-mode control, particularly peak current-mode control, was first introduced by T. A. Froeschle in 1967 [1] and Cecil of Bell Labs/Western Electric in 1978 [2]. The invention mainly helped to balance the AC flux in a transformer of a push–pull converter to keep the core from walking off into saturation caused by a minor difference in the volt-sec balance. Core saturation generally occurred in converters with slightly asymmetric drive waveforms or was due to load transients. In view of the growing demand for DC–DC converters, especially in military, telecommunication, and aerospace industries, it became extremely necessary to develop static and dynamic models of power electronic systems. A significant advancement came when Dr. Slobodan Ćuk introduced the state-space averaging technique, where the circuit behavior in switching sub-intervals was mathematically represented in the form of state variables with the state variables being the inductor current and capacitor voltage. Another advancement that came via pioneering research, which realized the important aspects of closed-loop stability of peak current-mode controlled DC–DC converters, was conducted by Dr. David Middlebrook and Dr. F. D. Tan of California Institute of Technology in 1985. To this day, these works serve as a starting point for establishing stability criteria, especially in cascaded or multilevel power converters [3–6].

The concept of average current-mode control was reinstated by Lloyd Dixon from Unitrode Electronics in 1990 [7, 8]. In the following years, closed-loop modeling of the average current-mode controlled AC–DC and DC–C converters was performed by various researchers including Raymond B. Ridley *et al*. [9–11] and Jian Sun and

Average Current-Mode Control of DC-DC Power Converters, First Edition.
Marian K. Kazimierczuk, Dalvir K. Saini, and Agasthya Ayachit.

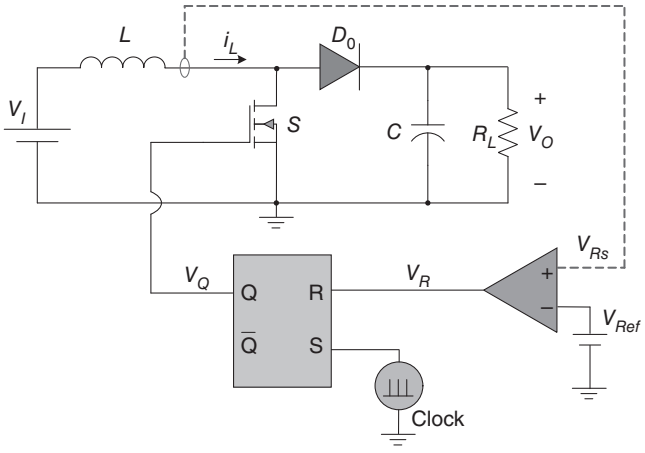

Figure 1.1 Boost DC–DC converter with a peak current-mode control, showing only the inner current loop.

R. M. Bass [12]. The peak current-mode control and the average current-mode control were also studied in [7–11, 13–35].

Before describing the principle of operation of the average current-mode control, it is imperative to discuss properties of peak current-mode control. Figure 1.1 depicts boost DC–DC converter with a peak current-mode control, showing only the inner current loop. In the peak current-mode control, the peak of the inductor current waveform is tracked and controlled [53]. The peak inductor current is compared with the reference current set by the outer-voltage loop of the DC–DC converter (not shown in Figure 1.1). As the peak value of the sensed inductor current becomes equal to the reference current, the comparator outputs a logic low at the instant of comparison and a logic high for all other values. The comparator output is connected to the reset pin R of the RS latch, whereas the set pin S is connected to a clock tuned to operate at the switching frequency. Initially, the set pin S enables the latch output Q to the switch ON state. Eventually, as the reset pin receives a logic high, the output of latch resets the switch to the OFF position and remains in this state until the clock sets it back to high position. The clock determines the beginning of the cycle, and the crossing of the inductor current waveform with the reference current determines the end of the high level of the gate-source voltage. The following operational disadvantages are observed as a consequence of peak current-mode control:

- Switching is highly susceptible to noise. At the instant of comparison of the peak inductor current and the current reference, a noise spike is created. The noise signal can create false triggering of the logic gates, resulting in the undesirable switching events.
- Slope compensation is required. The peak current-mode control needs slope compensation circuitry for duty cycles higher than 0.5 to avoid instability. The fixed compensation ramp provides adequate compensation; however, it will overcompensate much of the time, resulting in the performance degradation and increased distortion [7].

- Peak-to-average current ratio is high. The inductor current peak-to-average ratio is high. Therefore, the outer-voltage loop cannot completely eliminate the error between the peak and average values. This is a problem, especially in power-factor corrector converters, and causes distortion in the input current waveform.
- Uncompensated current loop gain is low. In the classical peak current-mode control, the uncompensated loop gain is very low. Therefore, higher-order compensation schemes such as Type-II and Type-III voltage error amplifiers are needed to boost the loop gain at DC.

1.1 Principle of Operation of Conventional Average Current-Mode Control Technique

In the conventional average current-mode control, the time-varying average value of the sensed inductor current is regulated. Figure 1.2 shows the circuit of a buck DC–DC converter using the conventional average current-mode control scheme. The reference to the current loop is set by the outer loop. The current reference generated by the outer-voltage loop is set to be equal to the desired inductor current average. A high-gain integrating amplifier in the current loop attempts to track the average value of the inductor current and sends the amplified current error to a PWM. The amplified current error is compared with a large amplitude sawtooth waveform oscillating at the switching frequency at the PWM comparator inputs.

Unlike peak current-mode control, the current loop gain can be modified for optimum performance by the compensation network in the current loop. For example, it is possible to have equal loop-gain crossover frequencies in both peak current-mode and average current-mode control schemes, but the gain will be much greater in average current-mode control at lower frequencies. This is essential to reduce the steady-state error significantly.

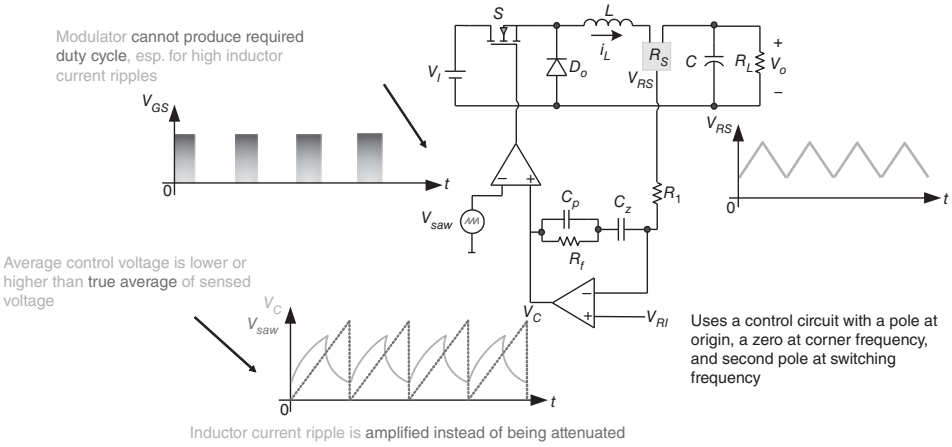

Figure 1.2 Circuit of a buck DC–DC converter with the conventional average current-mode control scheme [7]. Based on L. H. Dixon, 1990.

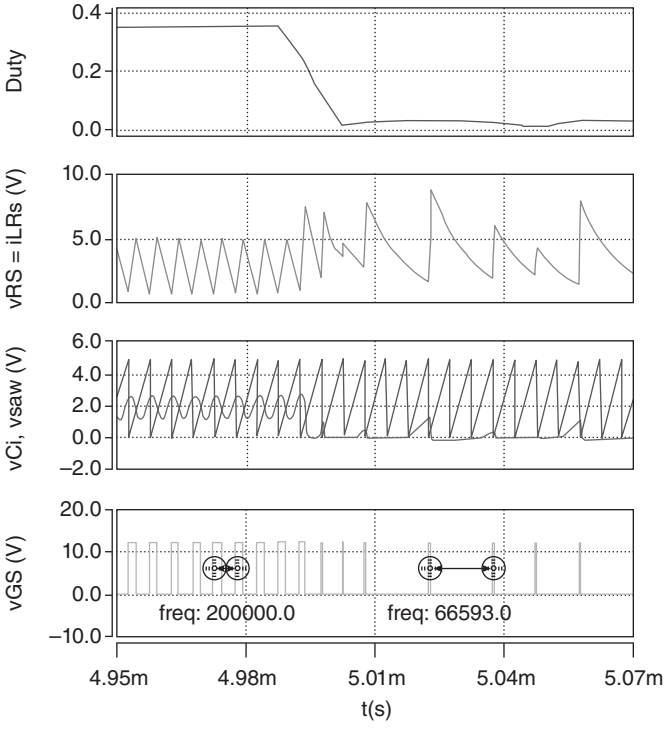

Figure 1.3 Waveforms showing the challenges encountered using conventional average current-mode control.

Although the conventional average current-mode control has unique advantages over peak current-mode, a few challenges are encountered. Figure 1.3 shows the waveforms of duty cycle d, sensed inductor current υ_{RS}, output voltage of current error amplifier υ_{Ci}, sawtooth voltage υ_{saw}, and gate-to-source voltage υ_{GS} relevant to a buck DC–DC converter. As the input voltage increases, the duty cycle must reduce. At low duty cycles, the inductor current ripple increases in magnitude. Since the error amplifier basically amplifies the error between the sensed inductor current and the current reference, the large inductor current ripple is also amplified. Therefore, the comparison between the sawtooth waveform and the amplified error output takes place more than once in each switching period resulting in subharmonic oscillations. This drawback cannot be ignored especially in converters used as power-factor correctors. Also, this method limits the designer from implementing switch current sensing due to larger current magnitudes. Moreover, even under normal operating conditions, the current-loop error amplifier must filter the switching frequency component in the sensed inductor current and perform normal compensation functions. In this technique, the inductor current is sensed and converted into sensed voltage by a current-to-voltage transducer. The sensed voltage comprises both DC and switching frequency ripple and is supplied to the control circuit. An integral single-lead (or Type-II) control circuit is used in this technique and performs two tasks:

1. Provides the required compensation for the inner loop.
2. Acts as a low-pass filter to reduce the switching frequency ripple in the sensed voltage. The control circuit comprises a pole at origin and a single pole-zero pair located at high frequencies. The pole at the origin provides a high DC gain to reduce the steady-state error, the high-frequency zero extends the current loop crossover frequency, and the high-frequency pole must filter the switching frequency ripple in the sensed signal [12].

A few evident shortcomings of this technique are as follows:

- The control circuit has a limited degree of freedom. For example, tuning its components for a desired phase margin will compromise the low-pass filter requirements and *vice versa*.
- At a high input voltage, the duty cycle is low and the inductor current ripple is high. This yields a large ripple at the control voltage supplied to the PWM. The slope of the control voltage exceeds the slope of the carrier voltage, causing switching instability [7, 12, 14].
- Due to the above two drawbacks, pulsating or discontinuous currents such as the switch current or diode current in the converter cannot be effectively sensed.
- Since the inductor current is sampled per switching period, the sampling gain needs to be taken into account.
- The location of the high-frequency pole is close to the switching frequency. Therefore, its contribution in reducing the switching frequency ripple and providing any compensation for the inner loop at high frequencies is limited.

Therefore, a modified average current-mode control scheme is developed and is shown in Figure 1.4. Here, the compensation circuit and the low-pass filter are decoupled, and they function independently. The sensed voltage that is dependent on the inductor current is provided to a low-pass filter dedicated only to cancel its switching frequency component. The output voltage of the low-pass filter with

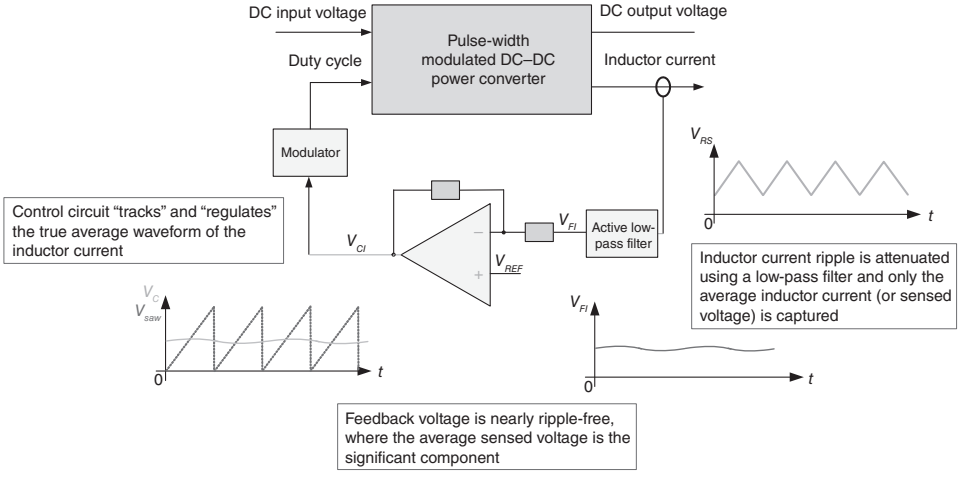

Figure 1.4 Block diagram of the average current-mode controlled DC–DC power converter.

a reduced switching frequency ripple component is then provided to the control circuit. Thus, the control voltage also exhibits a reduced ripple [52]. A detailed operation of the modified average current-mode control scheme is discussed in Section 1.2.

1.2 Principle of Operation of Modified Average Current-Mode Control Technique

Figure 1.4 shows the block diagram of the modified average current-mode controlled DC–DC converter. Figure 1.5 illustrates the key waveforms related to the sensing and feedback path. The sense resistor or current sensor is placed in the inductor branch to sense the inductor current. The sensed voltage is v_{RS}. The sensed voltage is provided to a low-pass filter composed of a resistor and capacitor network. The switching frequency component is eliminated by the low-pass filter. Therefore, the filter output voltage is DC with negligible ripple. The effective feedback voltage to the inner loop is v_{FI}. The reference voltage to the inner-current loop v_{RI} is governed by the outer-voltage loop. Based on the desired parameters such as high bandwidth and high DC gain of the inner-current loop, an appropriate control circuit with forward path impedance Z_{ii} and the feedback path impedance Z_{fi} will be derived and is a topic of discussion in Chapters 2–5. The control voltage v_{CI} at the output of the controller is compared with a sawtooth waveform v_{saw}, which generates the duty cycle d_T. By virtue of circuit operation, the exact average value of the inductor current (or any branch current) is sensed and controlled by the inner-current loop.

The major advantages of using the modified average current-mode control technique are as follows:

1. The compensation and filtering processes are performed independently. A good selection of the filter cutoff frequency assists the dynamic response and will be discussed in Chapters 2–5.

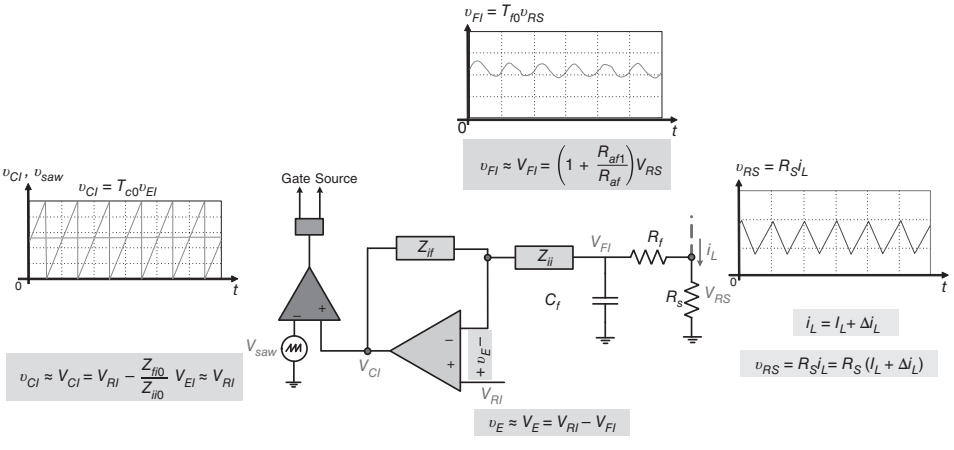

Figure 1.5 Circuit and key waveforms related to the feedback path in the average current-mode control.

2. The feedback voltage to the control circuit primarily contains the average value of the sensed current, and the switching frequency component is negligible. Therefore, a discontinuous switch or diode current with a large amplitude, a continuous or discontinuous inductor current of any amplitude, or the load current can be sensed by placing the current sensor in the corresponding branch.
3. The low-pass filter can be placed in either the feedback path or the forward path to reduce the ripple in the control voltage.
4. Due to the presence of the low-pass filter, the current loop does not behave as a sampling system. Thus, the effect of sampling gain is eliminated.
5. The problems due to the switching instability are completely avoided as the control voltage intersects the carrier voltage only once during each switching period.

This book endeavors to present a complete inner-loop analysis of different power converters whose average branch current such as inductor current, switch current, etc. is regulated by the modified current-mode control scheme. The steady-state large-signal operation, open and closed-loop transfer functions, and transient characteristics are presented.

1.3 Steady-State Operation

The inductor current comprises switching frequency component Δi_L superimposed on DC value I_L. From Figure 1.5, the potential difference across the sensed resistor R_S is given as

$$v_{RS} = R_s i_L = R_s(I_L + \Delta i_L). \tag{1.1}$$

The filter eliminates the switching frequency component of v_{RS}. By selecting appropriate sense resistance R_s, V_{RS} can be made equal to V_{RI}, where V_{RI} is the current reference voltage. The output voltage of the active filter is then compared with the reference voltage V_{RI}. The error signal is given as

$$V_{EI} = V_{RI} - V_{FI}. \tag{1.2}$$

The error signal is the input to the controller. The output of the controller is

$$V_{CI} = V_{RI} + T_{cio} V_{EI}, \tag{1.3}$$

where T_{cio} is the DC gain of the controller. The pulse-width modulator circuit is an inverting op-amp comparator. The control voltage is applied to the non-inverting input, and the sawtooth voltage signal v_{saw} is applied to the inverting input of the comparator. For any change in the control voltage v_C from V_C to $V_C + v_c$, the duty cycle d_T also changes from D to $D + d$. The control voltage-to-duty cycle transfer function of the PWM is expressed as

$$T_m = \frac{D}{V_{CI}} = \frac{1}{V_{Tm}}, \tag{1.4}$$

where V_{Tm} is the amplitude of the sawtooth waveform. In steady state, $V_{EI} \approx 0$, which yields

$$V_{CI} = V_{RI} = DV_{Tm}. \tag{1.5}$$

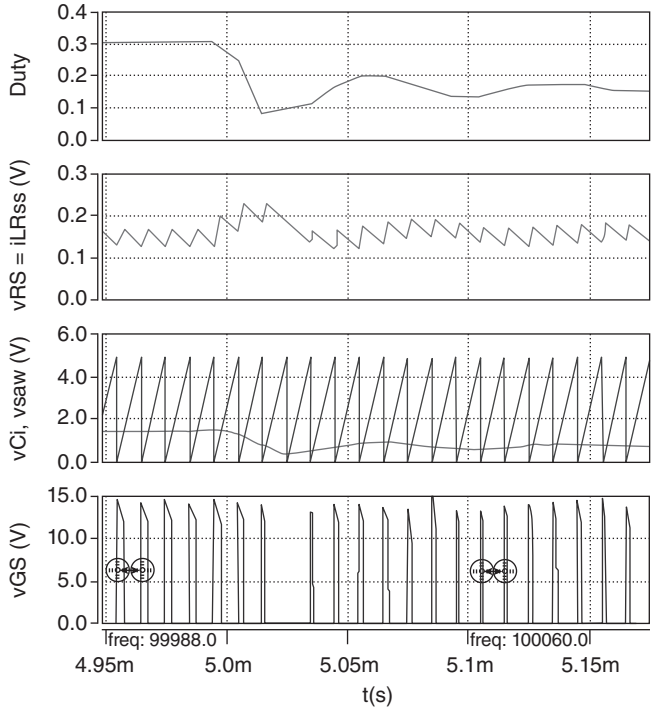

Figure 1.6 Waveforms related to the average current-mode controlled DC–DC buck converter with modified average current-mode control technique.

A buck DC–DC converter circuit with the modified average current-mode control was simulated, and the waveforms of duty cycle d, sensed inductor current v_{RS}, output of current error amplifier v_{CI}, sawtooth waveform v_{saw}, and gate-to-source voltage v_{GS} are shown in Figure 1.6. It can be seen that as the duty cycle decreases, the inductor current ripple stays unchanged. The comparator is able to track the amplified error voltage and produce gate-to-source voltage oscillating at the required switching frequency.

Chapters 2–5 discuss the closed-loop small-signal analysis of closed-loop buck, boost, and buck-boost PWM DC–DC converter with the modified average current-mode control technique. The DC large-signal and AC small-signal models are derived using circuit averaging technique [36–44]. The open-loop and closed-loop small-signal transfer functions are derived for the DC–DC converters with modified average current-mode control. Block diagrams are developed for each converter to characterize the inner-current loop for the power stage and the outer-voltage loop. Techniques to design the inner current-loop and outer voltage-loop are provided, and the responses of open loop, closed inner-current loop, and closed outer-voltage loop are compared. Through the step-by-step approach presented in this book, the readers can gain a deeper insight into the steady-state and small-signal operation of the fundamental DC–DC converters used today in various electronic applications.