Microwave and Wireless Synthesizers: Theory and Design, Second Edition.
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LOOP FUNDAMENTALS

1-1 INTRODUCTION TO LINEAR LOOPS

The majority of frequency synthesizers utilize the phase-locked loop (PLL). Indeed, it was the realization of the PLL in an integrated circuit that led to the inexpensive frequency synthesizer. Because an understanding of PLLs is necessary for the design of frequency synthesizers, they are discussed in detail in this chapter. The emphasis here is on the PLL as used in a frequency synthesizer rather than for signal detection. For the latter problem, the PLL input is a relatively low-level signal embedded in noise, and the PLL serves to detect the noisy signal. For PLL applications in frequency synthesizers, the input signal-to-noise ratio is high, and the PLL serves to lock out the output frequency on a multiple of the input frequency.

Although the PLL is a nonlinear device, it can be modeled as a linear device over most of its operating range. This chapter first presents the linearized analysis of the PLL, including its stability characteristics. The design of compensating filters to improve PLL performance is then discussed.

A PLL includes a phase detector, low-pass filter, and voltage-controlled oscillator (VCO), as illustrated in Figure 1-1. The phase detector is a nonlinear device, and its characteristics determine loop performance. The various types of phase detectors are described in Chapter 3. The loop transient performance is discussed in Section 1-10. No generalized results are available for transient performance, but the discussion illustrates one analysis approach that can be used.

Several books have been published on this matter, and for those involved in research or have interest in a more theoretical approach of the PLL principle, the following classic books are recommended:

Best, Roland E., *Phase Locked Loops*: *Design, Simulation, and Applications*, 6th Edition, McGraw-Hill, New York, NY, 2007.

Crawford, James A., *Frequency Synthesizer Design Handbook*, Artech House, Boston-London, 1994.

Egan, William F., *Frequency Synthesis by Phase Lock*, Wiley, New York, NY, 2007. ISBN 978-0-470-17871-3.

Gardner, Floyd M., *Phaselock Techniques*, 3rd edition, Wiley, New York, NY, 2005. ISBN 978-0-471-43063-6.

Gorsky-Popiel, Jerzy, *Frequency Synthesis Techniques and Applications*, IEEE Press, New York, NY, 1975.

Kroupa, Venceslav F, *Phase Lock Loops and Frequency Synthesis*, Griffin, London, 2003, ISBN 978-0-470-86512-5.

Lindsey, William C, and Chie, Chak M., *Phase-Locked Loops and Their Applications*, IEEE Press, New York, NY, 1985.

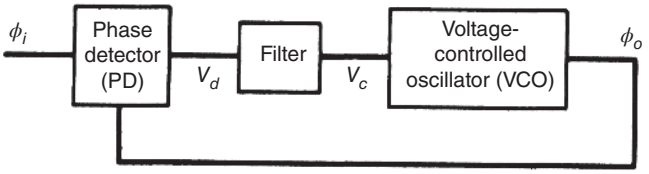


Figure 1-1 Block diagram of a PLL.

Manassewitsch, Vadim, *Frequency Synthesizers Theory and Design*, 3rd edition, Wiley, New York, NY, 2005, ISBN 978-0-471-77263-7.

Robert Bogdan Staszewski and Poras T. Balsara, *All-Digital Frequency Synthesizer in Deep-Submicron CMOS*, September 2006, ISBN 978-0-471-77255-2.

The term *phase-locked* loop refers to a feedback loop in which the input and feedback parameters of interest are the relative phases of the waveforms. The function of a PLL is to track small differences in phase between the input and feedback signal. The phase detector measures the phase difference between its two inputs. The phase detector output is then filtered by the low-pass filter and applied to VCO. The VCO input voltage changes the VCO frequency in a direction that reduces the phase difference between the input signal and the local oscillator (LO). The loop is said to be in *phase lock or locked* when the phase difference is reduced to zero.

Although the PLL is nonlinear since the phase detector is nonlinear, it can accurately be modeled as a linear device when the loop is in lock. When the loop is locked, it is assumed that the phase detector output voltage is proportional to the difference in phase between its inputs; that is,

$$V_d = K_\theta(\theta_t - \theta_o) \tag{1-1}$$

where θ_t and θ_o are the phases of the input and VCO output signals, respectively.

K_θ is the phase detector gain factor and has the dimensions of volts per radian. It will also be assured that the VCO can be modeled as a linear device whose output frequency deviates from its free-running frequency by an increment of frequency,

$$\Delta\omega = K_o V_e \tag{1-2}$$

where V_e is the voltage at the output of the low-pass filter and K_o is the VCO gain factor, with the dimensions of rad/s per volt. Since frequency is the time derivative of phase, the VCO operation can be described as

$$\Delta\omega = \frac{d\theta_o}{dt} = K_o V_e \tag{1-3}$$

With these assumptions, the PLL can be represented by the linear model shown in Figure 1-2. $F(s)$ is the transfer function of the low-pass filter. The linear transfer function relating $\theta_o(s)$ and $\theta_t(s)$ is

$$B(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_\theta K_o F(s)/s}{1 + K_\theta K_o F(s)/s} \tag{1-4}$$

If no low-pass filter is used, the transfer function is

$$B(s) = \frac{\theta_o}{\theta_i} = \frac{K_\theta K_o}{s + K_\theta K_o} = \frac{K}{s + K} \tag{1-5}$$

which is equivalent to the transfer function of a simple low-pass filter with unity dc gain and bandwidth equal to K.

This is really the minimum configuration of a PLL. Since there is no divider in the chain, the output frequency and the reference frequency are the same. The first PLL built probably used a ring modulator as a phase detector.

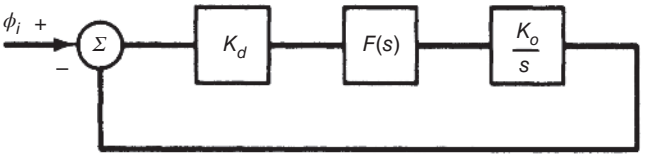


Figure 1-2 Block diagram of a PLL using a linearized model.

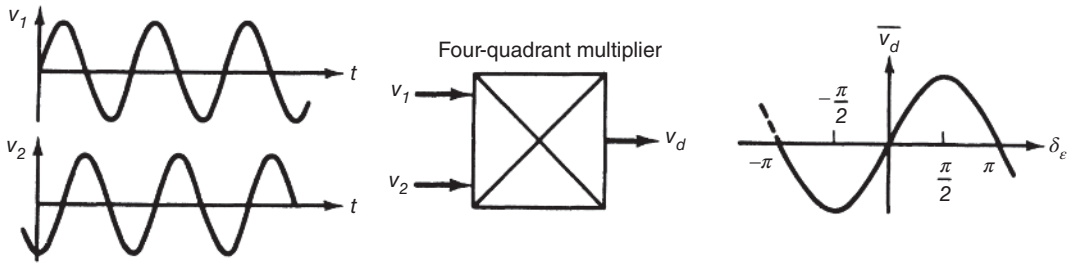


Figure 1-3 Waveform and transient characteristic of a linear phase detector.

The ring modulator or diode bridge is electrically the same as a four-quadrant multiplier and operates from $-\pi$ to $+\pi$ of phase range.

Since the VCO probably has a sine-wave output and the reference frequency also has a sine wave, it is referred to as a *sinusoidal phase detector*. This does not really mean that the phase detector is sinusoidal; it means that the waves applied to the phase detector are sinusoidal.

Since there are no digital components in this basic loop, it is correctly called an *analog phase-locked loop* and, as stated earlier, is the minimum form of a PLL. To model it correctly, a number of assumptions are required.

We have already stated that, for our initial consideration, the loop is locked and that the transfer characteristic of the phase/frequency detector is linear in the area of operation. A four-quadrant multiplier or diode quad has a sinusoidal output voltage, as shown in Figure 1-3, and is only piecewise linear for $\theta = 0$ or in the center of operation.

This minimum configuration of a PLL has several drawbacks. The absence of a filter does not allow one to choose parameters for optimized performance; the diode ring has only several hundred millivolts output, and an additional loop amplifier will add noise to the system. Therefore, for frequency synthesizer applications, a simple analog loop without any filter is rarely used. Such a loop would be called a first-order type 1 loop, and we will deal with it later.

There are some applications for a 1:1 loop, as we will see. The 1:1 loop is used to clean up an existing frequency, whereby the loop bandwidth is kept narrow enough to allow fast locking, and wide enough to permit fast acquisition. However, the loop bandwidth is narrower than the spurious frequencies present at the reference input. The attenuation of the loop filter of such a loop, which should be a second-order loop, will clean up the output signal relative to the reference.

1-2 CHARACTERISTICS OF A LOOP

We have met the minimum-configuration analog PLL and already learned that there are several limitations to this loop. The first step in increasing the output voltage delivered from the diode quad and avoiding an operational amplifier is to use a different phase detector.

If the diode bridge arrangement is changed and the diodes are overdriven by the reference signal and the input signal from the VCO remains sufficiently small relative to the reference, the phase detector is still in a linear operation mode, and the output signal of the phase detector is no longer a sinusoidal curve but rather has a linear

sawtooth form. The range over which the phase detector operates is still from $-\pi$ to $+\pi$, and the circuit is called *quasi-digital*. Later, when dealing with ring modulators, we will learn that it is a major requirement that the reference or LO signal must have a specified range, with a minimum typically 0.5 V for hot carrier diodes, and the VCO voltage should be substantially smaller for linear operation.

As the amplitude of the VCO signal is increased, the diode bridge or double-balanced modulator is overdriven, and a large number of harmonics occur. In a 1:1 loop, this is not very dangerous because all harmonics are phase and frequency coherent and do not generate unwanted signals. If a double-balanced mixer is used in a conversion scheme inside a loop, as we will see later, it is of utmost importance to operate the double-balanced mixer in its linear range and use a double-balanced mixer that has sufficient isolation between all ports.

In the case of the double-balanced mixer, whether overdriven from the LO or not, we refer to it as an analog linear PLL. If the VCO signal also overdrives the double-balanced mixer, we call it quasi-digital.

The digital equivalent of a double-balanced mixer is the exclusive-OR gate. The exclusive-OR gate, when built in CMOS logic, can be operated at 12 V, and therefore the dc output voltage can now be from almost 0 to +12 V, obtained from the integrator. We now have found a way to increase our dc control voltage without the noise sacrifice of an additional operational amplifier.

Both the double-balanced mixer and the exclusive-OR gate are only phase sensitive. The exclusive-OR gate also operates from $-\pi$ to $+\pi$, and the VCO has to be pretuned to be within the capture range.

Both phase detectors can be used for harmonic locking.

When we analyze the various loop components in Chapter 4, we will find some drawbacks that limit the use of the exclusive-OR gate.

The edge-triggered JK master/slave flip-flop can be used as a phase/frequency comparator. It operates from -2π to $+2\pi$. The edge-triggered JK master/slave flip-flop has two outputs. One output supplies pulses to charge a capacitor, and the other can be used to discharge a capacitor.

To use this phase/frequency detector requires an active loop filter or active integrator, commonly referred to as a *charge pump*. This type of phase detector generates a beat frequency at the output, and the average dc voltage generated in the integrator is either negative or positive, relative to half the power supply voltage, depending on whether the signal frequency is higher or lower than the reference. This is a useful feature and explains why we can state that this circuit is not only phase sensitive but also frequency sensitive. Unfortunately, the frequency sensitivity for this type of phase/frequency discriminator is useful only for large differences. For very small differences in frequency, there is very little advantage in choosing this circuit over the exclusive-OR gate or the double-balanced mixer. We will learn more about this circuit in Chapter 4.

The most important circuit for phase/frequency comparators is probably an arrangement of two flip-flops and several gates. This particular circuit will be called a *tri-state phase/frequency comparator*, for reasons we will see later. It has several advantages:

(1) The operating range is linear, from -2π to $+2\pi$.

(2) It has the best possible locking performance and best frequency and phase difference detection.

(3) Regardless of the amount of frequency error, the average output voltage is always above or below half the operating voltage. This results in good locking.

The last two types of phase/frequency detectors, because of their charge/discharge capability, require active filters or summation circuits. It is theoretically possible to avoid the amplifier and use purely resistive circuits, but as we will soon learn, this has disadvantages. So far, we still have only used a loop that has no frequency divider.

The introduction of a frequency divider requires that the input to the divider be a square wave (transistor–transistor logic (TTL)), and we will now define all loops that use digital dividers and phase/frequency comparators as digital loops. This should not be confused with digital synthesizers. A digital frequency synthesizer is most likely a direct synthesizer in which the output frequency is digitally generated with the help of a processor and is not available anywhere in analog or sine wave form. The output frequency is then the summation of several digital signals in a quasi-sine wave at the output generated only by means of digital circuitry. There are several methods besides the one currently used, which employs a lookup table for sine or cosine functions. For very low-frequency application, a complicated arrangement of diodes can be used to generate sine waves out of triangular waveshapes. Table 1-1 shows a comparison of the various phase/frequency detectors.

Table 1-1 Comparison of Various Phase/frequency Comparators

Type	Operating range	Sensitivity
Diode ring	$-\pi$ to π	Phase only
Exclusive-OR gate	$-\pi$ to π	Phase only
Edge-triggered JK flip-flop	-2π to 2π ($-\pi$ to π); See Table 1-2	Phase frequency; undefined for small errors
Tri-state phase/frequency	-2π to 2π	Phase frequency comparator

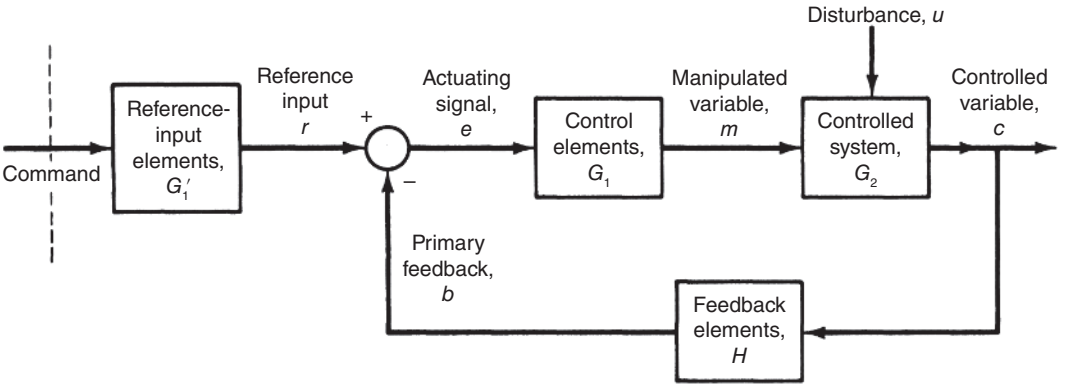


Figure 1-4 Equivalent diagram of a PLL using feedback control system analogy.

We have learned that because of its wider operating range, the PLL using digital phase/frequency comparators offers significant advantages over the analog PLL, and that is the main reason it is used in frequency synthesizers.

A closed loop is really a feedback system, and the various rules for feedback systems apply. We have already written down without further justification the formula that applies for a closed loop:

$$B(s) = \frac{\text{forward gain}}{1 + (\text{open-loop gain})} \tag{1-6}$$

Before we continue, let us take a look at some of the abbreviations and definitions that are used in feedback control systems. Figure 1-4 shows the equivalent block diagram of a feedback system. The gain is equal to the multiplication of the VCO gain K_o times the phase/frequency comparator K_θ and will be abbreviated by K:

$$K = K_o K_\theta \frac{\text{rad/s}}{\text{V}} \frac{\text{V}}{\text{rad}} \tag{1-7}$$

The feedforward function

$$G(s) = \frac{K}{s} F(s) \tag{1-8}$$

takes a filter function $F(s)$ into consideration, and the fact that the VCO itself is a perfect integrator is also taken into consideration.

To close the loop, we have to describe the feedback transfer function

$$H(s) = \frac{1}{N} \tag{1-9}$$

which will describe the divider ratio N and assumes that there is no delay in the divider. If there is delay in the divider, $H(s)$ is expressed in the form

$$H(s)^* = \frac{e^{-T_n s}}{N} \tag{1-10}$$

Therefore, the open-loop gain of the system is written

$$A(s) = G(s)H(s) \tag{1-11}$$

This definition of open-loop gain must not be confused with the open-loop gain K or the feedforward gain. From our definition earlier, the closed-loop gain is

$$\begin{aligned} B(s) &= \frac{\text{forward gain}}{1 + (\text{open-loop gain})} \\ &= \frac{\theta_o(s)}{\theta_i(s)} \\ &= \frac{G(s)}{1 + G(s)H(s)} \\ &= \frac{K(s)F(s)}{s + K(s)F(s)/N} \end{aligned} \tag{1-12}$$

It has become customary to incorporate the divider ratio N in the K, which means that K in most cases can be said to equal

$$\frac{K_o K_\theta}{N}$$

If this substitution is made, the formulas are generally valid, provided that the correct factor of K is selected, and the formulas are generally usable regardless of the actual division ratio. In synthesizer design it is interesting to determine the system's noise bandwidth, B_n, which is defined as

$$B_n = \frac{1}{2\pi} \int_0^\infty B(j\omega)\, d\omega \tag{1-13}$$

The 3-dB bandwidth can be determined by solving the equation substituting

$$|B_n(j\omega)| = 0.707$$

the resulting j_θ would then be the 3-dB bandwidth, the complex variable j deleted. Another important piece of information in feedback control system performance is the *steady-state error*, that is, the error remaining after all transients have died out. The equation for the error function is

$$E(s) = \frac{\theta_e}{\theta_i} = 1 - B(s) = \frac{1}{1 + G(s)H(s)} \tag{1-14}$$

We will compute the steady-state error as a function of the various systems in Section 1-10 and make some predictions on loops of various orders. As previously mentioned, we have classified the loops to be either analog or digital, referring to the phase/frequency detector, and in writing the initial equations, we have already indicated that the loop may or may not have a filter incorporated.

In analyzing the loop, we will find that to describe a loop, we can express it in terms of both the order of the loop and the type of loop. The expression "type of loop" refers to the number of integrators used. A PLL using no active integrator can really only be a type 1 loop. The term "order" refers to the order of the polynomial that is required to express the loop transfer characteristic.

The absolute minimum in a loop is a phase/frequency detector, a VCO, and no filter. By this definition, this would be a first-order type 1 loop. Another way of explaining this is by saying that the *type* of a system refers to the number of poles of the loop transfer function locked at the origin. The *order* of a system refers to the highest degree of the polynomial expression of the denominator that can be expanded into a polynomial expression. In this book we deal with loops of types 1 and 2 from first order up to fifth.

We have now learned that there are two classifications for loops:

(1) Classification by phase detector, characterizing the loop to be analog or digital.

(2) Characterizing the loop by the type of loop filter and number of integrators.

1-3 DIGITAL LOOPS

Using our previous definition, a digital PLL is a PLL system in which the phase/frequency comparator is built from digital components such as gates or flip-flops to form either an exclusive-OR gate, an edge-triggered JK master/slave flip-flop, or what we call a tri-state phase/frequency comparator. In addition, digital PLLs use frequency dividers, and although some circuits using the principle of subharmonic locking for dividers are known, this generally refers to the use of asynchronous or synchronous dividers. Asynchronous dividers are usually ripple counters, and synchronous dividers are counters that are being clocked by a common reset line.

The basic difference between an analog and a digital phase/frequency loop is in the possible delay introduced by the frequency divider and the nonlinear effects of the phase/frequency comparator, and the question of ultimate resolution of the phase/frequency comparator. The phase/frequency comparator using active filters shows some highly nonlinear performance during zero crossings at the output or under perfectly locked conditions. As there is no output from a tri-state phase/frequency comparator under locked conditions, the gain of the loop is zero until there is a requirement to send correcting pulses from the digital phase/frequency comparator, which then results in a jump of loop gain.

We will demonstrate that digital phase/frequency comparators, especially tri-state phase/frequency comparators, have two ranges for acquisition. One is called *pull-in* range, and the other is called *lock-in* range. The acquisition time is the time for both. This total time to acquire both frequency and phase lock is sometimes called the *capture time* or *digital acquisition time*. Depending on the loop filter and the phase/frequency comparator, we will have different time constants.

For reasons of convenience and linearity, we have, so far, assumed that the loop is in the locked condition. Initially, when the loop is switched on for the first time, it is far from being locked, and the VCO frequency can be anywhere within tuning range. *Tuning range* is defined as the frequency range over which the VCO can be tuned with the available control voltage.

There are, however, limitations because of the tuning diodes. The minimum voltage that can be applied is determined by the threshold voltage of the diode itself before it becomes conductive. This voltage is typically 0.7 V, and the maximum voltage is the potential determined by the breakdown voltage of the tuning diode. Even in the case where the familiar back-to-back diode arrangement is used, these are the two limits for the voltage range. In practice, however, this range is even narrower because the voltage sensitivity of the tuning diode is excessive at the very low end and very small at the extreme high end. Even before the breakdown voltage is reached, the noise contribution from the diode already increases because of some zener effects.

As the loop currently is not in locked condition, we have to help it to acquire lock. Very few loops acquire locking by themselves, a process called *self-acquisition*. Generally, the tuning range is larger than the acquisition range. Self-acquisition is a slow, unreliable process. If the loop is closed for the first time, the process called "pull-in" will occur. The oscillator frequency, together with the reference frequency, will generate a beat note and a dc control voltage of such phases that the VCO is pulled in a direction of frequency lock. As the oscillator itself generates noise in the form of a residual frequency modulation (FM), the oscillator is constantly trying to break out of lock, and the loop is constantly monitoring the state and reassuring lock. This results, under normal circumstances, in constant charging and discharging of the holding capacitor responsible for the averaging process.

There is one other phase/frequency comparator that is really more a switch than anything else; it is called a *sample/hold comparator*. The sample/hold comparator, which we will deal with later, has the advantage of very

good reference frequency suppression, introduces a phase shift that reduces the phase margin, and is really useful only up to several hundred kilohertz of frequency. For frequencies higher than this, there is too much leakage. The sample/hold comparator, which has been popular for a number of years, is described in Chapter 4. Modern frequency synthesizers, however, prefer digital phase/frequency comparators because the sample/hold comparator is only a phase comparator and does not recognize frequency offsets. It is too slow to be used for harmonic sampling and, in our opinion, has only limited use.

The sample/hold comparator is used mostly with T networks for additional reference suppression, and although these circuits provide good reference suppression, the phase margin has to be so high that the loops are generally slow in their response.

The switching speed of the loop and its general performance to noise are covered in detail in Section 1-10.

Now let us take a look at a numerical example. Consider a frequency synthesizer using a PLL to synthesize a 1-MHz signal from a 25-kHz reference frequency. To realize an output frequency of 1 MHz, a division of 1 MHz/25 kHz = 40 is necessary.

Let us assume that there is no filtering included, and therefore the closed-loop transfer function will be

$$B(s) = \frac{K}{s + K/N} \tag{1-15}$$

A typical value for K_θ is 2 V/rad and a typical value for the VCO gain factor K_o is 1000 Hz/V. With these values the closed-loop transfer function is

$$B(s) = \frac{K_\theta K_o}{s + K_\theta K_o/N} = \frac{1000 \times 2\pi \times 2}{s + [(1000 \times 2\pi \times 2)/40]} = \frac{4000\pi}{s + 100\pi} \tag{1-16}$$

The 3-dB frequency of the system by definition is

$$\omega_{3\text{dB}} = \frac{K_\theta K_o}{N} \tag{1-17}$$

and therefore

$$\omega_n = 100\pi$$

If this is solved to determine f, we obtain $f = 50$ Hz.

As the reference frequency is 25 kHz, the reference suppression of the simple system can be determined from

$$A = 20\log_{10}\left(\frac{25{,}000}{50}\right) = 20\log_{10}(500)$$

$$= 54 \text{ dB}$$

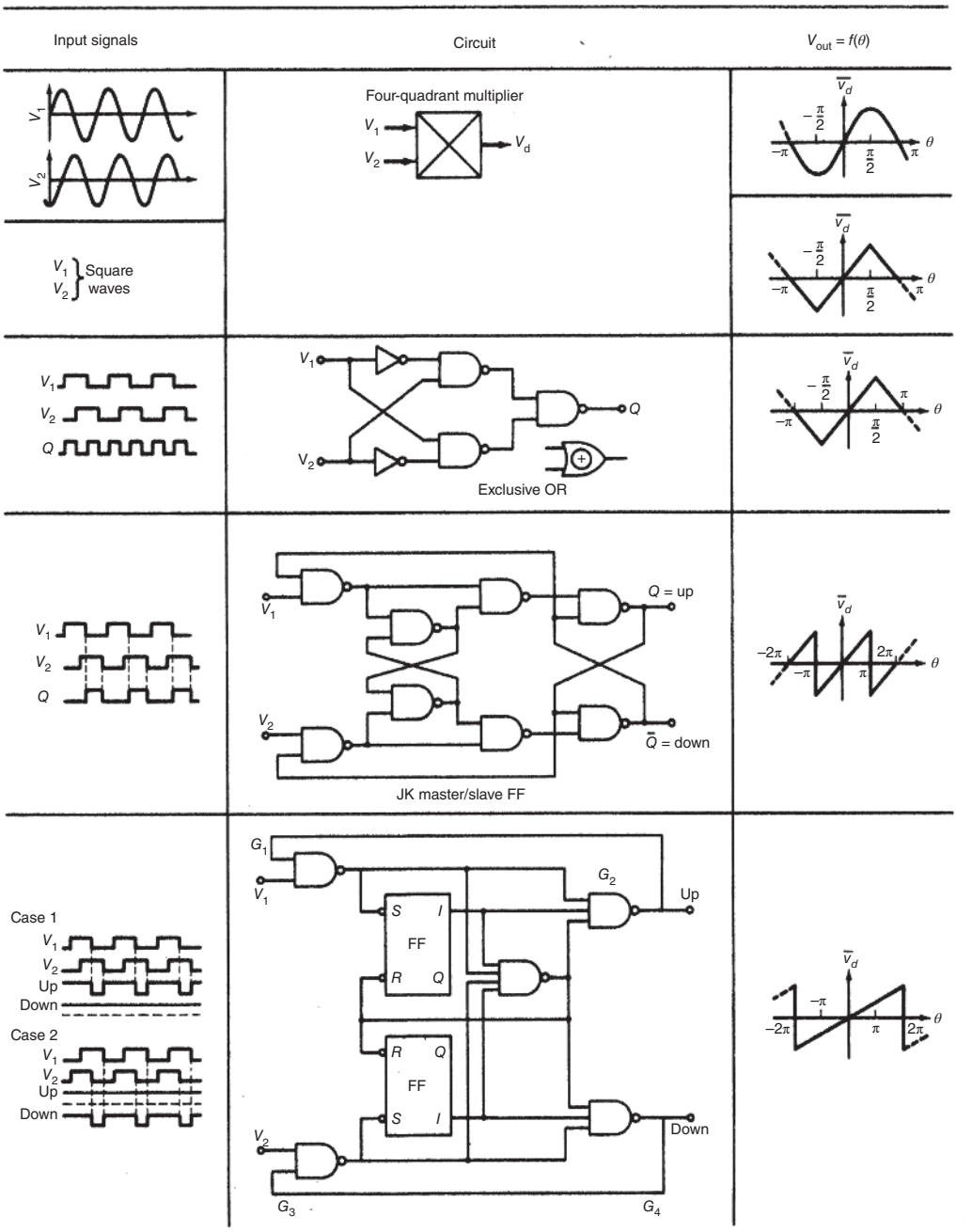
The loop bandwidth of the system by itself is 50 Hz.

We have, with very little effort, calculated a first-order type 1 loop. We deal more with these loops in Chapter 2.

Table 1-2 shows the input waveforms and the output average voltage of:

(1) A four-quadrant multiplier or double-balanced mixer being driven either by a sine wave or a square wave.
(2) The input and output voltages for an exclusive-OR gate.
(3) The input and output voltages after the integrator of an edge-triggered JK master/slave flip-flop.
(4) The input and output voltages of a tri-state phase/frequency comparator after the integrator. Notice that the extended operating range is linear from -2π to $+2\pi$.

Table 1-2 Circuit Diagrams and Input and Output Waveforms of Various Phase/frequency Comparators



Source: Courtesy of Fachschriftenverlag, Aargauer Tagblatt AG, Aarau, Switzerland.

1-4 TYPE 1 FIRST-ORDER LOOP

The type 1 first-order loop contains a digital phase/frequency comparator and a digital divider, and throughout the rest of this book, we will deal only with digital loops. This is done on the assumption that the phase/frequency comparator can be modeled as a linear device over the operating range, which is certainly not true. However, as most of the formulas and deviations that deal with PLLs have certain assumptions that have finite accuracy, it is permissible to do so. We realize that a purist will be offended by this statement. However, as many PLLs have been designed by rule of thumb and the final results were within a few percent accurate, we assume that the reader will permit this simplification.

The analog loop, as mentioned earlier, does not provide enough dc output, and for reasons of sideband noise, there is no advantage in using the linear loop in digital frequency synthesizers. Therefore, the PLL without a loop filter, $F(s) = 1$, is called a type 1 first-order loop because it has only one integrator, and the highest power (s) in the denominator of the system transfer function is 1.

The open-loop gain of a type 1 first-order PLL is equal to the forward gain divided by N, $(K_\theta K_o/s)/N$. The transfer function is

$$B(s) = \frac{N}{1 + s[1/(K_\theta K_o/N)]} \tag{1-18}$$

The loop noise bandwidth can be determined from the integration to be

$$B_n = \frac{K_\theta K_o}{4N} \tag{1-19}$$

It should be noted that the noise bandwidth changes as a function of the division ratio N. If there is a large change in the division ratio, the noise bandwidth will change substantially. This is another reason why the type 1 first-order loop is not very popular.

Let us assume that the loop is not in locked condition. The phase/frequency comparator receives two different frequencies at the two inputs. For digital phase/frequency comparators, we will use an exclusive-OR gate, which requires an active integrator.

Because of the limits of the operating range, presteering is required for the VCO to be within the range $-\pi$ to $+\pi$ for a locking condition. It is known that the maximum difference between the VCO free-running frequency and the desired final frequency at which phase lock is possible can be equal to

$$\Delta\omega_{\text{capture}} = \Delta\omega_H = \frac{K_\theta K_o}{N} \text{ rad/s} \tag{1-20}$$

It is important to keep the steady-state phase error small; therefore, high dc loop gain is required. As the increase in loop gain would require an amplifier, this makes the loop noisy and eventually unstable.

We have explained previously that the VCO gain is limited because of the tuning range of the diodes, and we will learn later that it is desirable to keep the VCO gain as low as possible. The input line to the VCO is a high-impedance, and pick-up on this line will result in spurious output at the VCO. To keep the spurious frequencies small, the VCO gain must be kept as small as possible.

The phase detector sensitivity depends mainly on the operating voltage. We recall that the double-balanced modulator with four diodes supplies only several hundred millivolts; instead, the exclusive-OR gate was chosen, as this can be operated from 12 V or even higher if CMOS logic is used.

There are several estimates regarding the acquisition time for the type 1 first-order PLL. Using the exclusive-OR gate, the acquisition time is approximately

$$T_A = \frac{2}{K_\theta K_o/N} \ln \frac{2}{\theta_\varepsilon} \tag{1-21}$$

where ln refers to the natural logarithm and θ_ε refers to the final phase error in radians.

From our previous example, the acquisition time T_A would be determined to be

$$T_A = \frac{2}{50} \ln \frac{2}{0.2}$$
$$= 9.2 \times 10^{-2} \text{ s}$$

Assuming that the initial offset was less than 50 Hz, the loop locks in frequency without skipping cycles. In practice, it is impossible to presteer the loop within 50 Hz; therefore, this formula has only limited use.

We have just determined the acquisition time, but we have to ask ourselves: What does it really mean? Does it mean that the frequency from the initial offset is now the same as the reference frequency? Does it mean that we have reached a certain percentage of final frequency or gotten very close to the final frequency or final phase? Will we ever reach the final value, or is there a residual error?

The *error function*, which we met earlier, provides us with information and insight.

$$E(s) = \frac{\theta_\varepsilon}{\theta_i} = 1 - B(s) = \frac{1}{1 - G(s)H(s)} \tag{1-14}$$

It has been shown that, depending on the type of change of input, we get different results. These results are determined by the use of a transformation from the frequency into the time domain. Section A-4 presents the mathematical background for the Laplace transform and discusses how it is applied. Here, we use only the results. Inserting the known factors into Eq. (1-14), we obtain

$$E(s) = \frac{s\theta_\varepsilon(s)}{s + K} \tag{1-22}$$

with $K = K_\theta K_o/N$. It is customary to analyze the performance of the loop for three different conditions:

(1) To apply a step to the input and see what the output response is.
(2) A ramp voltage.
(3) A parabolic input.

Case 1, the step input, means an instantaneous jump with zero rise time to which the output will respond with a delay. The steady-state phase error resulting from this step change of input phase of magnitude $\Delta\theta$ for a ramp,

$$\theta(s) = \frac{\Delta\theta}{s} \tag{1-23}$$

is

$$\varepsilon = \lim_{s \to 0} \frac{\Delta\omega}{s + K} = \frac{\Delta\theta}{K} \tag{1-24}$$

Case 2, the steady-state error resulting from a ramp of input phase that is the same as a step change in reference frequency in the amount $\Delta\omega[\theta(s) \times \Delta\omega/s^2]$, is

$$\varepsilon = \lim_{s \to 0} \frac{\Delta\omega}{s + K} = \frac{\Delta\omega}{K} \tag{1-25}$$

It is apparent from these two equations that after a certain time, a type 1 first-order loop will track out any step change in input phase within the system hold-in range and will follow a step change in frequency with a phase error that is proportional to the magnitude of the frequency steps and inversely proportional to the dc loop gain. The loop will show the same performance if phase or frequency of the VCO changes rather than the reference.

In case 3, for the type 1 first-order PLL, it is of interest to examine a ramp change in frequency, the case in which the reference frequency is linearly changed with a time rate of $\Delta\omega/dt$ rad/s^2 and $\theta(s) = (2\Delta\omega/dt)/s^3$. Why

is this so important? Let us assume that we sweep a PLL at a constant rate, as is done in some modern spectrum analyzers, and we have to find the final condition for the steady-state phase error. The final phase error is

$$\varepsilon = \lim_{s\to 0} \frac{2\Delta\omega/dt}{s^2 + sK} = \infty \tag{1-26}$$

What does this mean for us? It means that, as there is no infinite value for K in a type 1 first-order loop, this loop is not very attractive for tracking, and it also means that above a certain and critical rate of change of reference frequency or VCO frequency, the loop will no longer stay in locked condition. Therefore, if the loop is swept above a certain rate, it will not maintain lock.

1-5 TYPE 1 SECOND-ORDER LOOP

A type 1 second-order loop is shown in Figure 1-5.

If we insert in our PLL a simple low-pass filter

$$F(s) = \frac{1}{\tau_s + 1} \tag{1-27}$$

the closed-loop transfer function using

$$K = \frac{K_o K_\theta}{N}$$

is

$$B(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{NK}{s(\tau s + 1) + K} = \frac{N}{(s^2/\omega_n^2) + (2\zeta/\omega_n)s + 1} \tag{1-28}$$

where

$$\omega_n = \sqrt{\frac{K}{\tau}} \tag{1-29}$$

and

$$2\xi = \frac{\omega_n}{K} = \sqrt{\frac{1}{\tau K}} \tag{1-30}$$

The magnitude of the steady-state frequency response is

$$|B(s)| = \left|\frac{\theta_o}{\theta_i}(j\omega)\right| = \frac{1}{[(1 - \omega^2/\omega_n^2)^2 + (2\zeta\omega/\omega_n)^2]^{1/2}} \tag{1-31}$$

and the phase shift is

$$\arg \frac{\theta_o}{\theta_i}(j\omega) = \arctan \frac{2\zeta\omega}{\omega_n(1 - \omega^2/\omega_n^2)^2} \tag{1-32}$$

The frequency response of this second-order transfer function determined in Eq. (1-28) is plotted in Figure 1-6 for selected values of ζ. For $\zeta = 0.07$, the transfer function becomes the second-order "maximally flat" Butterworth response. For values of $\zeta < 0.07$, the gain exhibits peaking in the frequency domain. The maximum value of the frequency response M_P can be found by differentiating the magnitude of Eq. (1-28) (with $s = j\omega$). M_P is found to be

$$M_P = \frac{1}{2\zeta\sqrt{1 - \zeta^2}} \tag{1-33}$$

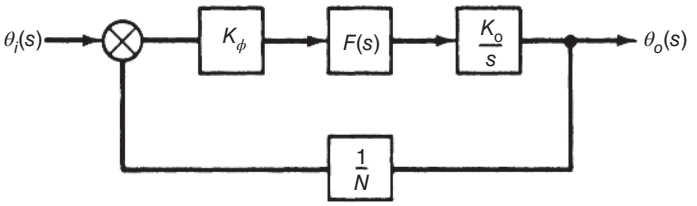


Figure 1-5 Block diagram of the second-order PLL.

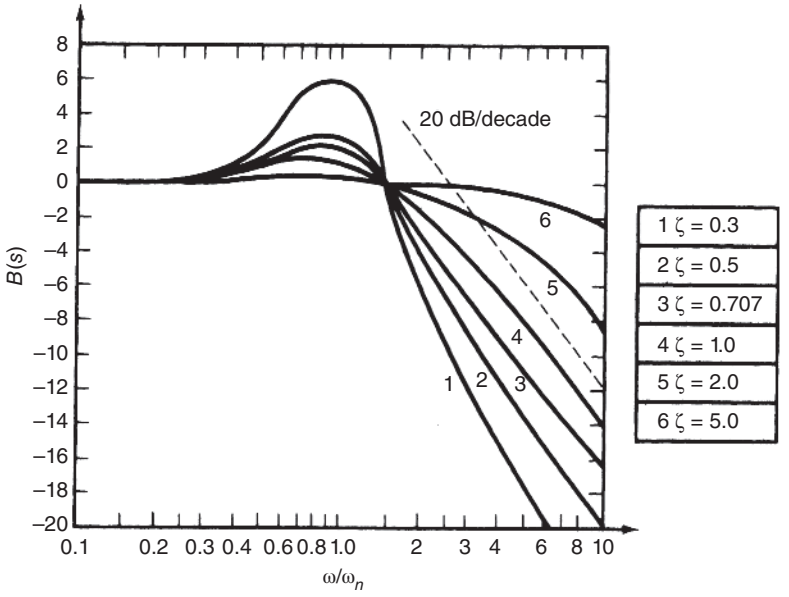


Figure 1-6 Frequency response of the type 1 second-order loop as a function of ζ.

and the frequency ω_p at which the maximum occurs is

$$\omega_p = \omega_n\sqrt{1-2\zeta^2} \tag{1-34}$$

The 3-dB bandwidth B can be derived by solving for the frequency ω_h at which the magnitude of Eq. (1-28) (with $s = j\omega$) is equal to 0.707. B is found to be

$$B = \omega_n(1-2\zeta^2+\sqrt{2-4\zeta^2+4\zeta^4})^{1/2} \tag{1-35}$$

The time it takes for the output to rise from 10% to 90% of its final value is called the *rise time* t_r. Rise time is approximately related to the system bandwidth by the relation

$$t_r = \frac{2.2}{B} \tag{1-36}$$

which is exact only for the first-order system described by Eq. (1-5).

The error signal θ_ε, defined as $\theta_i - \theta_o$, can be expressed (in unity feedback systems) as

$$\theta_\varepsilon(s) = \frac{\theta_i(s)}{1 + KG(s)} = \frac{\theta_i(s)}{1 + KF(s)/s} \tag{1-37}$$

If the system is stable, the steady-state error for polynomial inputs $\theta_i(t) = t^n$ can be obtained from the final value theorem,

$$\begin{aligned} \lim_{t\to\infty} \theta_\varepsilon(t) &= \lim_{s\to 0} s\theta_\varepsilon(s) \\ &= \lim_{s\to 0} \frac{2\theta_i}{KF(s)} \end{aligned} \tag{1-38}$$

If $\theta_i(t)$ is a step function representing a sudden increase in phase, $\theta_i(s) = 1/s$ and

$$\lim_{t\to\infty} \theta_\varepsilon(t) = \lim_{s\to 0} \frac{s}{KF(s)} \tag{1-39}$$

$F(s)$ is either a constant or a low-pass filter that may include poles at the origin. That is,

$$\lim_{s\to 0} F(s) = \frac{K^*}{s^n} \neq 0 \tag{1-40}$$

Therefore, Eq. (1-39) can be written

$$\lim_{t\to\infty} \theta_\varepsilon(t) = \lim_{s\to 0} \frac{s^{n+1}K^*}{KK^*} = 0 \tag{1-41}$$

That is, a PLL will track step changes in phase with zero steady-state error.

If there is a constant-amplitude change in the input frequency of A rad/s,

$$\theta_i(s) = \frac{A}{S^2} \tag{1-42}$$

Equation (1-39) becomes

$$\lim_{t\to\infty} \theta_\varepsilon(y) = \lim_{s\to 0} \frac{A}{KF(s)} = \frac{A}{KF(0)} \tag{1-43}$$

If $F(0) = 1$, the steady-state phase error will be inversely proportional to the loop gain K. Recall that the larger K is, the larger will be the closed-loop bandwidth and thus the faster the loop response. To increase the response speed and reduce the tracking error, the loop gain should be as large as possible. If $F(0)$ is finite, there will be a finite steady-state phase error. The frequency error,

$$f_\varepsilon(t) = \frac{d}{dt}\theta_\varepsilon(t) \tag{1-44}$$

will be zero in the steady state. That is, the input and VCO frequencies will be equal ($\omega_i = \omega_o$).

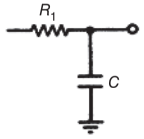
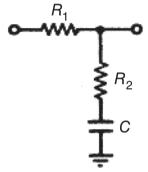
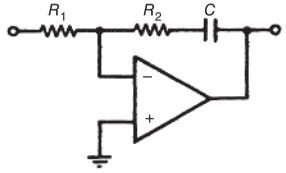
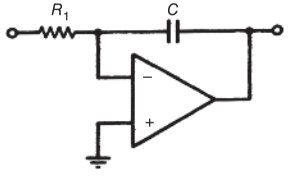
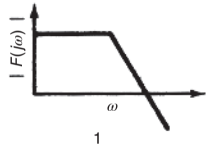
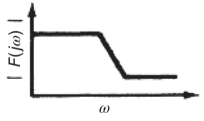
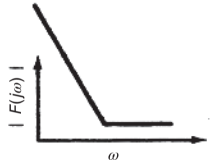
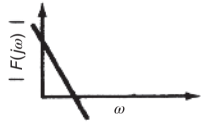
Table 1-3 shows the popular loop filters for the type 2 second-order loop. We have now dealt with case 1, a simple resistor-capacitor (RC) filter. The performance obtained with this loop filter is relatively restricted, mainly because the advantage over the loop with no filter was that we only got one additional parameter, a time constant τ_1.

Let us look at the table and the various filters. The passive filter type 2 uses two resistors and one capacitor, which allows compensation of phase.

The active filter, with which we will be dealing shortly, will add an additional integrator and therefore change this loop from a type 1 second-order to a type 2 second-order. The second-order loops we are currently dealing with are of type 1 because there is only one integrator involved, the VCO.

As we have only the time constant available as the additional parameter, which as we saw previously determines both the natural loop frequency ω_n and the damping factor ζ, we have not made much progress toward improving

Table 1-3 Circuit and Transfer Characteristics of Several PLL Filters

Type	Passive		Active	
	1	2	3	4
Circuit				
Transfer characteristic				
$F(j\omega) =$	$\frac{1}{1 + j\omega\tau_1}$	$\frac{1 + j\omega\,\tau_2}{1 + j\omega(\tau_1 + \tau_2)}$	$\frac{1 + j\omega\,\tau_2}{j\omega\,\tau_1}$	$\frac{1}{j\omega\tau_1}$
	$\tau_1 = R_1\,C$	$\tau_2 = R_2\,C$		

the loop and choosing independent parameters. If we add a resistor in series with the capacitor and obtain the loop filter shown in Table 1-3, type 2, the transfer function $F(s)$ is

$$F(s) = \frac{1 + \tau_2 s}{1 + \tau_1 s} \tag{1-45}$$

or as it is sometimes defined,

$$F(s) = \frac{1 + j\omega\tau_2}{1 + j\omega(\tau_1 + \tau_2)} \tag{1-46}$$

What is the difference? In the first case, we use the abbreviations

$$\tau_1 = (R_1 + R_2)C \tag{1-47}$$

and

$$\tau_2 = R_2 C \tag{1-48}$$

whereas in the second case, and as listed in Table 1-3,

$$\tau_1 = R_1 C \tag{1-49}$$

and

$$\tau_2 = R_2 C \tag{1-50}$$

This fact should be pointed out, as it may cause confusion to the reader. This results in the transfer function of the type 1 second-order PLL using the first-case definition,

$$\begin{aligned} B(s) &= \frac{K(1 + \tau_2 s/1 + \tau_1 s)}{s + K(1 + \tau_2 s/1 + \tau_1 s)} \\ &= \frac{K(1/\tau_1)(1 + \tau_2 s)}{s^2 + (1/\tau_1)(1 + K\tau_2)s + (K/\tau_1)} \end{aligned} \tag{1-51}$$

To be consistent with our previous abbreviations, we now insert the terms of the loop damping factor ζ and the natural frequency ω_n and obtain

$$B(s) = \frac{s\omega_n(2\zeta - \omega_n/K) + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{1-52}$$

where

$$\omega_n = \sqrt{\frac{K}{\tau_1}} \text{ rad/s} \tag{1-53}$$

and

$$\zeta = \frac{1}{2}\sqrt{\frac{1}{\tau_1 K}(1 + \tau_2 K)} \tag{1-54}$$

We remember our abbreviation used previously, ω_n. The magnitude of the transfer function of the phase-lag filter magnitude is

$$|F(j\omega)| = \sqrt{\frac{1 + (\omega R_2 C)^2}{1 + [\omega C(R_1 + R_2)]^2}} \tag{1-55}$$

and the phase is

$$\theta(j\omega) = \arctan(\omega\tau_2) - \arctan(\omega\tau_1)$$

When we use the other definition of τ_1 and τ_2 insert the abbreviations

$$\omega_n = \sqrt{\frac{K}{\tau_1 + \tau_2}} \tag{1-56}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{K}{\tau_1 + \tau_2}}\left(\tau_2 + \frac{1}{K}\right) \tag{1-57}$$

we obtain the expression

$$B(s) = \frac{s\omega_n(2\zeta - \omega_n/K) + \omega_n^2}{s^2 + 2\zeta(\omega_n^s + \omega_n^2)} \tag{1-58}$$

which turns out to give the same result.

As we were interested in the 3-dB bandwidth of the type 1 first-order loop, we now determine the 3-dB bandwidth of the type 1 second-order loop to be

$$B_{3\text{dB}} = \frac{\omega_n}{2\pi}(a + \sqrt{a^2 + 1})^{1/2}\ \text{Hz} \tag{1-59}$$

with the substitution

$$a = 2\zeta^2 + 1 - \frac{\omega_n}{K}\left(4\zeta - \frac{\omega_n}{K}\right) \tag{1-60}$$

The noise bandwidth of the type 1 second-order loop is

$$B_n = \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right)\ \text{Hz} \tag{1-61}$$

Again, we are interested in the final phase error and information we can gain from the phase error function

$$E(s) = \frac{s(1 + \tau_1 s)\theta(s)}{\tau_1 s^2 + (1 + K\tau_2)s + K} \tag{1-62}$$

As we are still dealing with a type 1 system, we obtain zero steady phase error, for a step in phase, and constant error for a ramp input in phase. One of these cases is shown in Figure 1-7, where the transient phase error due to a step in phase is plotted.

For the loop to stay in lock, the following critical values have to be considered. The maximum rate of change of reference frequency $d\Delta\omega/dt$ should satisfy the equation

$$\left(\frac{d\Delta\omega}{dt}\right)_{\max} = \omega_n^2 \tag{1-63}$$

The maximum rate at which the VCO can be swept must satisfy the condition

$$\left(\frac{d\Delta\omega}{dt}\right)_{\max} < \frac{\omega_n^2}{2} \tag{1-64}$$

to achieve lock. The hold-in range of this loop is

$$\Delta\omega_H = K\ \text{rad/s}$$

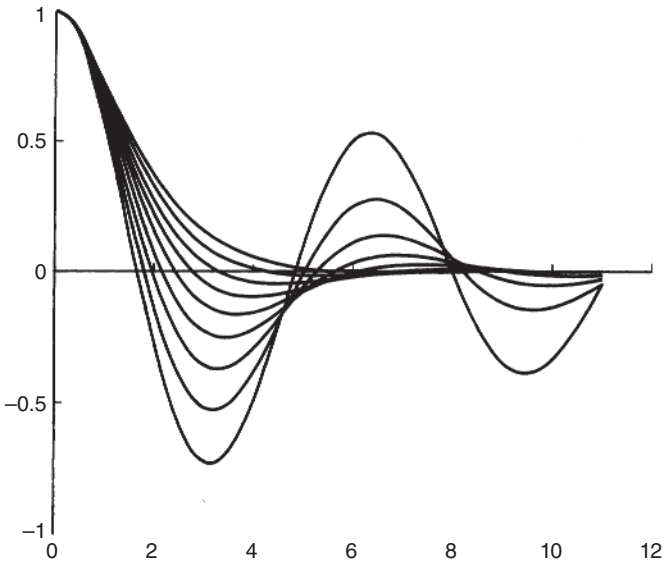


Figure 1-7 Transient phase step response for type 1 second-order loop.

and the capture range is

$$\Delta\omega_C = K\left(\frac{\tau_1}{\tau_2}\right) \text{ rad/s} \tag{1-65}$$

An approximate time required for this type 1 second-order loop to obtain frequency lock is

$$T_{\text{acq}} \simeq \frac{4(\Delta f)^2}{B_n^3} \text{ s} \tag{1-66}$$

A simple numerical example may give some additional insight. Let us assume that we have an oscillator operating at 45 MHz, using a reference frequency of 1 kHz. The tuning range of the oscillator is 5 MHz, which means that the frequency of the VCO in the beginning can be at either 40 or 50 MHz, as an extreme value. If we take the Δf offset worst-case condition of 5 MHz, and to get adequate reference suppression, we use a 50-Hz natural loop frequency and a damping factor ζ of 0.7, the noise bandwidth is

$$\begin{aligned} B_n &= \frac{50}{2}\left(0.7 + \frac{1}{0.7 \times 4}\right) \\ &= 25(0.7 + 0.3571) \\ &= 25 \times 1.0571 \\ &= 26.4 \text{ Hz} \end{aligned}$$

For a 5-MHz offset,

$$T_{\text{acq}} = \frac{4(5 \times 10^6)^2}{26.4^3} = 5.4 \times 10^9 \text{ s}$$

This is a ridiculous value. Unless the loop gets acquisition help, we would lose patience before it has ever acquired lock. Let us assume for a moment that we have a Δf of only 1 kHz or one step size. This still results in an acquisition time of 380 s, much too long for practical values. In Section 1-10 we will learn some acquisition

aids that can speed up the otherwise lengthy procedure. For now, it is sufficient to know that in cases where we do not use a phase/frequency comparator, it generates a beat note that is capable of switching and, therefore, aiding acquisition. Externally switched oscillators can be used, or automatic circuits can be incorporated that change the loop bandwidth before acquisition occurs and therefore can speed up the circuit substantially.

We end our discussion of the type 1 second-order loop here and concentrate on the more popular type 2 second-order loop. Why is the type 2 second-order loop so much more popular?

We found out previously that the freedom of choice of parameters was limited.

(1) In the type 1 first-order loop with no filter, K determined everything.

(2) In the type 1 second-order loop, we had one time constant (τ_1) available, which restricted us in the choice of ω_n and ζ, as these values were related. The type 1 second-order loop has finite dc gain and therefore it is questionable whether the term "PLL" is really justified. By this definition we really should not call it a true PLL system because, from the assumptions made previously, zero phase error requires infinite dc gain.

How do we accomplish the infinite dc gain, and how do we accomplish zero phase error?

If it is necessary to have zero phase error in response to step changes in the input frequency, $\lim_{s\to 0} F(s)$ must be infinite. That is, the dc gain of the low-pass filter must be infinite. This can be realized by including in $F(s)$ a pole at the origin. In this case $F(s)$ will be of the form

$$F(s) = \frac{1}{s}\frac{\tau_2 s + 1}{\tau_1} \tag{1-67}$$

The addition of the pole at the origin creates difficulties with the loop stability. In fact, the system will now be unstable unless a lead network is included in $F(s)$. With a passive filter, therefore resulting in a type 1 second-order loop, the condition is generally that we start with specified values for ω_n and ζ and we want to determine the time constants τ_1 and τ_2. This has rarely been shown in the literature, and for those interested, here is the result. We start off with $K_\theta K_o/N = K$ and

$$\omega_n = \sqrt{\frac{K}{\tau_1 + \tau_2}} \tag{1.56}$$

$$\zeta = \frac{1}{2}\left(K + \frac{1}{\tau_1 + \tau_2}\right)^{1/2}\left(\tau_2 + \frac{1}{K}\right) \tag{1-68}$$

By squaring ζ and inserting the value for ω_n, after some manipulation we obtain

$$\tau_2^2 K^2 + \tau_2 2K + 1 - 4\zeta^2\frac{K^2}{\omega_n^2} = 0 \tag{1-69}$$

This equation can be solved with

$$\tau_1 = \frac{K}{\omega_n^2} - \tau_2 \tag{1-70}$$

$$\tau_2 = \frac{-2K + \sqrt{4K^2 - 4K^2[1 - 4\zeta^2(K^2/\omega_n^2)]}}{2K^2} \tag{1-71}$$

and

$$R_1 = \frac{\tau_1}{C} \tag{1-72}$$

and

$$R_2 = \frac{\tau_2}{C} \tag{1-73}$$

1-6 TYPE 2 SECOND-ORDER LOOP

The type 2 second-order loop uses a loop filter in the form

$$F(s) = \frac{1}{s}\frac{\tau_2 s + 1}{\tau_1} \tag{1-67}$$

The multiplier $1/s$ indicates a second integrator, which is generated by the active amplifier. In Table 1-3, this is the type 3 filter. The type 4 filter is mentioned there as a possible configuration but is not recommended because, as stated previously, the addition of the pole of the origin creates difficulties with loop stability and, in most cases, requires a change from the type 4 to the type 3 filter. One can consider the type 4 filter as a special case of the type 3 filter, and therefore it does not have to be treated separately. Another possible transfer function is

$$F(s) = \frac{1}{R_1 C}\frac{1 + \tau_2 s}{s} \tag{1-74}$$

with

$$\tau_2 = R_2 C \tag{1-50}$$

Under these conditions, the magnitude of the transfer function is

$$|F(j\omega)| = \frac{1}{R_1 C\omega}\sqrt{1 + (\omega R_2 C)^2} \tag{1-75}$$

and the phase is

$$\theta = \arctan(\omega\tau_2) - 90^\circ$$

Again, as if for a practical case, we start off with the design values ω_n and ζ, and we have to determine τ_1 and τ_2. Taking an approach similar to that for the type 1 second-order loop, the results are

$$\tau_1 = \frac{K}{\omega_n} \tag{1-76}$$

and

$$\tau_2 = \frac{2\zeta}{\omega_n} \tag{1-77}$$

and

$$R_1 = \frac{\tau_1}{C} \tag{1.72}$$

and

$$R_2 = \frac{\tau_2}{C} \tag{1.73}$$

The closed-loop transfer function of a type 2 second-order PLL with a perfect integrator is

$$B(s) = \frac{K(R_2/R_1)[s + (1/\tau_2)]}{s^2 + K(R_2/R_1)s + (K/\tau_2)(R_2/R_1)} \tag{1-78}$$

By introducing the terms ζ and ω_n, the transfer function now becomes

$$B(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{1-79}$$

with the abbreviations

$$\omega_n = \left(\frac{K}{\tau_2}\frac{R_2}{R_1}\right)^{1/2} \text{ rad/s} \tag{1-80}$$

and

$$\zeta = \frac{1}{2}\left(K\tau_2\frac{R_2}{R_1}\right)^{1/2} \tag{1-81}$$

and $K = K_\theta K_o/N$.

The 3-dB bandwidth of the type 2 second-order loop is

$$B_{3\text{dB}} = \frac{\omega_n}{2\pi}[2\zeta^2 + 1 + \sqrt{(2\zeta^2+1)^2+1}]^{1/2} \text{ Hz} \tag{1-82}$$

and the noise bandwidth is

$$B_n = \frac{K(R_2/R_1) + 1/\tau_2}{4} \tag{1-83}$$

Again, we ask the question of the final error and use the previous error function,

$$E(s) = \frac{s\theta(s)}{s + K(R_2/R_1)\{[s + (1/\tau_2)]/s\}} \tag{1-84}$$

or

$$E(s) = \frac{s^2\theta(s)}{s^2 + K(R_2/R_1)s + (K/\tau_2)(R_2/R_1)} \tag{1-85}$$

As a result of the perfect integrator, the steady-state error resulting from a step change in input phase or change of magnitude of frequency is zero.

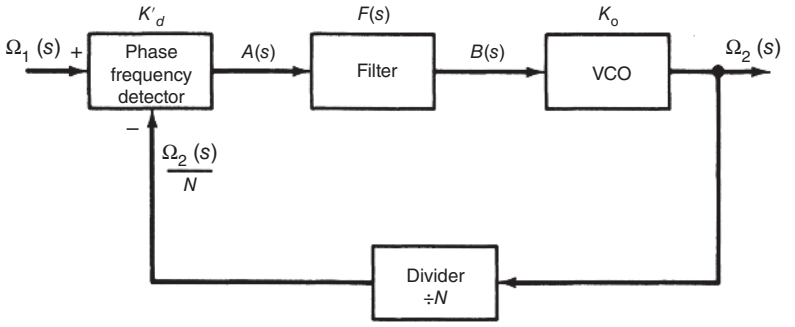
If the input frequency is swept with a constant range change of input frequency ($\Delta\omega/dt$) for $\theta(s) = (2\Delta\omega/dt)/s^3$, the steady-state phase error is

$$E(s) = \frac{R_1}{R_2}\frac{\tau_2(2\Delta\omega/dt)}{K} \text{ rad} \tag{1-86}$$

The maximum rate at which the VCO frequency can be swept for maintaining lock is

$$\frac{2\Delta\omega}{dt} = \frac{N}{2\tau_2}\left(4B_n - \frac{1}{\tau_2}\right) \text{ rad/s} \tag{1-87}$$

The introduction of N indicates that this is referred to the VCO rather than to the phase/frequency comparator. In the previous example of the type 1 first-order loop, we referred it only to the phase/frequency comparator rather than the VCO.



Note: The frequency transfer const. of the VCO = K_o
(not $\frac{K_o}{s}$, which is valid for phase transfer only.)

Figure 1-8 Block diagram of a digital PLL before lock is acquired.

1-6-1 Transient Behavior of Digital Loops Using Tri-state Phase Detectors

Pull-in Characteristic

The type 2 second-order loop is used with either a sample/hold comparator or a tri-state phase/frequency comparator. We will now determine the transient behavior of this loop. Figure 1-8 shows the block diagram.

Very rarely in literature is a clear distinction between pull-in and lock-in characteristics or frequency and phase acquisition made as a function of the digital phase/frequency detector. Somehow, all the approximations or linearizations refer to a sinusoidal phase/frequency comparator or its digital equivalent, the exclusive-OR gate.

The tri-state phase/frequency comparator (which will be explored in greater detail in Chapter 4) follows slightly different mathematical principles.

The phase detector gain

$$K'_d = \frac{V_d}{\omega_0} = \frac{\text{phase detector supply voltage}}{\text{loop idling frequency}}$$

is explained fully in Chapter 4, and we only use the result here. This phase detector gain is valid only in the out-of-lock state and is a somewhat coarse approximation to the real gain, which, due to nonlinear differential equations, is very difficult to calculate. However, practical tests show that this approximation is still fairly accurate.

Definitions:

$$\Omega_1(s) = l[\Delta\omega_1(t)] \quad \text{Reference input to } \delta/\omega \text{ detector}$$

$$\Omega_2(s) = l[\Delta\omega_2(t)] \quad \text{Signal VCO output frequency}$$

$$\Omega_e(s) = l[\Delta\omega_e(t)] \quad \text{Error frequency at } \delta/\omega \text{ detector}$$

$$\Omega_e(s) = \Omega_1(s) - \frac{\Omega_2(s)}{N}$$

$$\Omega_2(s) = [\Omega_1(s) - \Omega_e(s)]/N$$

From the circuit earlier,

$$A(s) = \Omega_e(s)K'_d$$

$$B(s) = A(s)F(s)$$

$$\Omega_2(s) = B(s)K_o$$

The error frequency at the detector is

$$\Omega_e(s) = \Omega_1(s)N\frac{1}{N + K_oK_d'F(s)} \tag{1-88}$$

The signal is stepped in frequency:

$$\Omega_1(s) = \frac{\Delta\omega_1}{s} \quad (\Delta\omega_1 = \text{magnitude of frequency step}) \tag{1-89}$$

Active Filter of First Order

If we use an active filter

$$F(s) = \frac{1 + s\tau_2}{s\tau_1} \tag{1-90}$$

and insert this in Eq. (1-88), the error frequency is

$$\Omega_e(s) = \frac{1}{s\left(N + K_oK_d'\frac{\tau_2}{\tau_1}\right) + \frac{K_oK_d'}{\tau_1}} \tag{1-91}$$

Utilizing the Laplace transformation, we obtain

$$\omega_e(t) = \Delta\omega_1\frac{1}{1 + K_oK_d'(\tau_2/\tau_1)(1/N)}\exp\left[-\frac{1}{(\tau_1N/K_oK_d') + \tau_2}\right] \tag{1-92}$$

and

$$\lim_{t\to 0}\omega_e(t) = \frac{\Delta\omega_1 N}{N + K_oK_d'(\tau_2/\tau_1)} \tag{1-93}$$

$$\lim_{t\to\infty}\omega_e(t) = 0 \tag{1-94}$$

Passive Filter of First Order

If we use a passive filter

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \tag{1-95}$$

for the frequency step

$$\Omega_1(s) = \frac{\Delta\omega_1}{s} \tag{1-96}$$

the error frequency at the input becomes

$$\Omega_e(s) = \Delta\omega_1 N\left\{\frac{1}{s}\frac{1}{s[N(\tau_1 + \tau_2) + K_oK_d'\tau_2] + (N + K_oK_d')} + \frac{\tau_1 + \tau_2}{s[N(\tau_1 + \tau_2) + K_oK_d'\tau_2] + (N + K_oK_d')}\right\} \tag{1-97}$$

For the first term we will use the abbreviation A, and for the second term we will use the abbreviation B.

$$A = \frac{1/[N(\tau_1 + \tau_2) + K_o K_d' \tau_2]}{s\left[s + \frac{N + K_o K_d'}{N(\tau_1+\tau_2)+K_o K_d' \tau_2}\right]} \tag{1-98}$$

$$B = \frac{\frac{\tau_1+\tau_2}{N(\tau_1+\tau_2)+K_o K_d' \tau_2}}{s + \frac{N+K_o K_d'}{N(\tau_1+\tau_2)+K_o K_d' \tau_2}} \tag{1-99}$$

After the inverse Laplace transformation, our final result becomes

$$\mathscr{L}^{-1}(A) = \frac{1}{N + K_o K_d'}\left\{1 - \exp\left[-t\frac{N + K_o K_d'}{N(\tau_1 + \tau_2) + K_o K_d' \tau_2}\right]\right\} \tag{1-100}$$

$$\mathscr{L}^{-1}(B) = \frac{\tau_1 + \tau_2}{N(\tau_1 + \tau_2) + K_o K_d' \tau_2} \exp\left(-t\frac{N + K_o K_d'}{N(\tau_1 + \tau_2) + K_o K_d' \tau_2}\right) \tag{1-101}$$

and finally

$$\omega_e(t) = \omega_1 N[\mathscr{L}^{-1}(A) + (\tau_1 + \tau_2)\mathscr{L}^{-1}(B)] \tag{1-102}$$

What does the equation mean? We really want to know how long it takes to pull the VCO frequency to the reference. Therefore, we want to know the value of t, the time it takes to be within 2π or less of lock-in range.

The PLL can, at the beginning, have a phase error from -2π to $+2\pi$, and the loop, by accomplishing lock, then takes care of this phase error.

We can make the reverse assumption for a moment and ask ourselves, as we have done earlier, how long the loop stays in phase lock. This is called the *pull-out* range. Again, we apply signals to the input of the PLL as long as the loop can follow and the phase error does not become larger than 2π. Once the error is larger than 2π, the loop jumps out of lock.

We will learn more about this in Section 1-10, but as already mentioned with regard to the condition where the loop is out of lock, a beat note occurs at the output of the loop filter following the phase/frequency detector.

The tri-state phase/frequency comparator, however, works on a different principle, and the pulses generated and supplied to the charge pump do not allow the generation of an ac voltage. The output of such a phase/frequency detector is always unipolar, but, relative to the value of $V_{\text{batt}}/2$, the integrator voltage can be either positive or negative. If we assume for a moment that this voltage should be the final voltage under a locked condition, we will observe that the resulting dc voltage is either more negative or more positive relative to this value, and because of this, the VCO will be "pulled in" to this final frequency rather than swept in, which had been mentioned previously. The swept-in technique applies only in cases of phase/frequency comparators, where this beat note is being generated. A typical case would be the exclusive-OR gate or even a sample/hold comparator. This phenomenon is rarely covered in the literature and was probably discussed in detail for the first time in the book by Roland Best [1].

Let us assume now that the VCO has been pulled in to final frequency to be within 2π of the final frequency, and the time t is known. The next step is to determine the lock-in characteristic.

Lock-in Characteristic

We will now determine lock-in characteristic, and this requires the use of a different block diagram. Figure 1-8 shows the familiar block diagram of the PLL, and we will use the following definitions:

$\theta_1(s) = \mathscr{L}[\Delta\delta_1(t)]$ Reference input to δ/ω detector

$\theta_2(s) = \mathscr{L}[\Delta\delta_2(t)]$ Signal VCO output phase

$$\theta_e(s) = \mathcal{L}[\delta_e(t)] \qquad \text{Phase error at } \delta/\omega \text{ detector}$$

$$\theta_e(s) = \theta_1(s) - \frac{\theta_2(s)}{N}$$

From the block diagram, the following is apparent:

$$A(s) = \theta_e(s)K_d$$

$$B(s) = A(s)F(s)$$

$$\theta_2(s) = B(s)\frac{K_o}{s}$$

The phase error at the detector is

$$\theta_e(s) = \theta_1(s)\frac{sN}{K_oK_dF(s) + sN} \tag{1-103}$$

In Section A-4 we will see that a step in phase at the input, with the worst-case error being 2π, results in

$$\theta_1(s) = 2\pi\frac{1}{s} \tag{1-104}$$

We will now treat the two cases using an active or a passive filter.

Active Filter

The transfer characteristic of the active filter is

$$F(s) = \frac{1 + s\tau_2}{s\tau_1} \tag{1.90}$$

This results in the formula for the phase error at the detector,

$$\theta_e(s) = 2\pi\frac{s}{s^2 + (sK_oK_d\tau_2/\tau_1)/N + (K_oK_d/\tau_1)/N} \tag{1-105}$$

The polynomial coefficients for the denominator are

$$a_2 = 1$$

$$a_1 = (K_oK_d\tau_2/\tau_1)/N$$

$$a_0 = (K_oK_d/\tau_1)/N$$

and we have to find the roots W_1 and W_2. Expressed in the form of a polynomial coefficient, the phase error is

$$\theta_e(s) = 2\pi\frac{s}{(s + W_1)(s + W_2)} \tag{1-106}$$

After the Laplace transformation has been performed, the result can be written in the form

$$\delta_e(t) = 2\pi\frac{W_1e^{-W_1t} - W_2e^{-W_2t}}{W_1 - W_2} \tag{1-107}$$

with

$$\lim_{t\to 0}\delta_e(t) = 2\pi$$

and

$$\lim_{t\to\infty} \delta_e(t) = 0$$

The same can be done using a passive filter.

Passive Filter

The transfer function of the passive filter is

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \tag{1.95}$$

If we apply the same phase step of 2π as before, the resulting phase error is

$$\theta_e(s) = 2\pi \frac{[1/(\tau_1 + \tau_2)] + s}{s^2 + s\frac{N + K_o K_d \tau_2}{N(\tau_1 + \tau_2)} + \frac{K_o K_d}{N(\tau_1 + \tau_2)}} \tag{1-108}$$

Again, we have to find the polynomial coefficients, which are

$$a_2 = 1$$
$$a_1 = \frac{N + K_o K_d \tau_2}{N(\tau_1 + \tau_2)}$$
$$a_0 = \frac{K_o K_d}{N(\tau_1 + \tau_2)}$$

and finally find the roots for W_1 and W_2. This can be written in the form

$$\theta_e(s) = 2\pi \left[\frac{1}{\tau_1 + \tau_2} \frac{1}{(s + W_1)(s + W_2)} + \frac{s}{(s + W_1)(s + W_2)} \right] \tag{1-109}$$

Now we perform the Laplace transformation and obtain our result:

$$\delta_e(t) = 2\pi \left(\frac{1}{\tau_1 + \tau_2} \frac{e^{-W_1 t} - e^{-W_2 t}}{W_1 - W_2} + \frac{W_1 e^{-W_1 t} - W_2 e^{-W_2 t}}{W_1 - W_2} \right) \tag{1-110}$$

with

$$\lim_{t\to 0} \delta_e(t) = 2\pi$$

and

$$\lim_{t\to\infty 0} \delta_e(t) = 0$$

We will show with the type 2 third-order loop how these roots are being determined, as the roots are going to be fifth order. We assume that determining the roots of a cubic equation is known and easy.

As a result of the last equation for the active as well as for the passive filter, Eqs. (1-107) and (1-110) have the dimension of radians. Although mathematically speaking it is not strictly accurate, it is permissible to multiply these values with the division ratio N and the reference frequency to obtain a final error in the dimension frequency. It has been shown in practical experiments that, if this final error is less than 0.1 Hz, the time (t) it takes to get there can be taken as the lock-in time. In Chapter 2, we will learn that any VCO has a certain residual FM. This means that even under locked condition, the output frequency moves within certain boundaries. Medium-quality synthesizers show a residual FM of 3 Hz, whereas a loop with dividers at the output and low division ratio can have a residual

FM as low as 0.1 Hz or better. This is, at times, also called *incidental FM*, and similar expressions have been found in the literature.

In Table 1-2 we indicated that the exclusive-OR gate and the edge-triggered JK master/slave flip-flop have a different operation mode than that of the tri-state phase/frequency comparator.

We will go into the details in Section 1-10, since the tri-state phase/frequency comparator does not require any acquisition aid.

Let us take a look at a numerical example. We have a PLL with the following parameters:

Reference frequency	5000 Hz
K_o	$2\pi \times 1$ MHz
K_θ	2.1 V/rad
N	1000
ω_n	500 Hz
Phase margin	45°
ζ	0.7
R_1	1336 Ω
R_2	445 Ω
C_1	1E-6 F
Reference suppression	20 dB
Lockup time	8 ms

These values were determined for the type 2 second-order loop with a program.

In Section 1-7 we will find that the type 2 third-order loop, although initially somewhat more difficult to treat mathematically, will show better reference suppression, faster lockup time, and really is better as far as reproducibility is concerned. This is due to the fact that there are always stray capacitors and some other elements in the circuit, which can be incorporated in the type 2 third-order loop, whereas the type 2 second-order loop really does not exist in its pure form.

Some of the dynamics of the type 2 second-order loop and of the type 2 third-order loop are dealt with in Section 1-10. For reasons of consistency, however, the transient behavior of the type 2 second-order loop has already been treated, and the equivalent performance of the type 2 third-order loop will be discussed on the following pages.

1-7 TYPE 2 THIRD-ORDER LOOP

We have stated several times previously that low-order loops really do not exist. The reasons for this are the introduction of phase shift by the operational amplifier, stray capacitors, and other things in the loop.

The type 2 third-order loop is a very good approximation of what is actually happening and can easily be developed from the type 2 second-order loop by adding one more *RC* filter at the output. Most likely, the operational amplifier as part of the active filter has to drive a feed-through capacitor, and for reasons of spike decoupling or additional filtering, one resistor is put in series.

Figure 1-9 shows a loop filter for a type 2 third-order loop. Just a reminder: this loop has two integrators, one being the VCO and one being the operational amplifier and three time constants.

This filter can be redrawn as shown in Figure 1-10. The transfer function for this filter is

$$F(s) = -\frac{1}{s\tau_1}\frac{1 + s\tau_2}{1 + s\tau_3} \tag{1-111}$$

with

$$\tau_1 = C_1 R_1 \tag{1-112}$$

$$\tau_2 = R_2(C_1 + C_2) \tag{1-113}$$

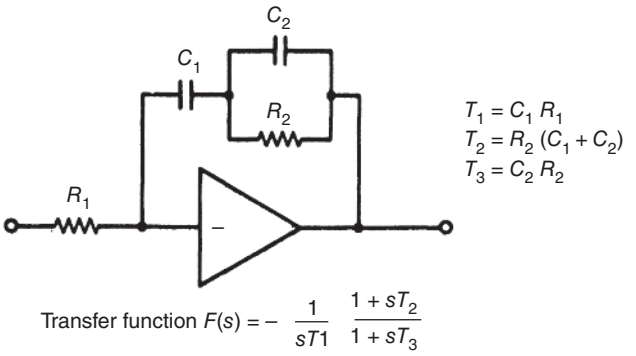


Figure 1-9 Circuit diagram of loop filter for the third-order loop.

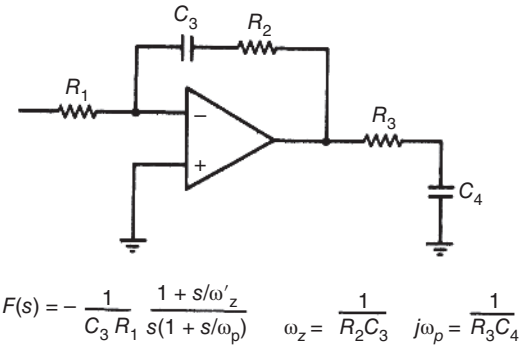


Figure 1-10 Circuit diagram of redrawn Figure 1-9. Note that this is the same type of loop filter as in the type 2 second-order loop with an additional *RC* time constant.

$$\tau_3 = C_2 R_2 \tag{1-114}$$

Let us now determine the transfer function for the type 2 third-order loop.

1-7-1 Transfer Function of Type 2 Third-Order Loop

The forward gain is

$$K = K_\theta F(s)\frac{K_o}{s} \tag{1-115}$$

and for

$$H(s) = \frac{1}{N} \quad N = \text{division ratio} \tag{1-116}$$

the open-loop gain is

$$A(s) = K_\theta F(s)\frac{K_o}{s}\frac{1}{N} \tag{1-117}$$

and the system transfer function is

$$\begin{aligned} B(s) = \frac{\theta_o(s)}{\theta_i(s)} &= \frac{\text{forward gain}}{1 + (\text{open-loop gain})} \\ &= \frac{K_\theta F(s)(K_o/s)}{1 + \frac{K_\theta F(s)(K_o/s)}{N}} \\ &= \frac{K_\theta F(s) K_o}{s + \frac{K_\theta F(s) K_o}{N}} \end{aligned} \tag{1-118}$$

If we insert our time constants τ_1, τ_2, and τ_3, we obtain

$$B(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{1 + s\tau_2}{s\tau_1 + s^2\tau_1\tau_3} \frac{K_\theta K_o}{s + \frac{K_\theta K_o}{N} \frac{1+s\tau_2}{s\tau_1 + s^2\tau_1\tau_2}} \tag{1-119}$$

and

$$B(s) = NK_\theta K_o(1 + s\tau_2) \frac{1}{s^3 N\tau_1\tau_3 + s^2 N\tau_1 + sK_\theta K_o\tau_2 + K_\theta K_o} \tag{1-120}$$

$$\text{polynominal } P = s^3 N\tau_1\tau_3 + s^2 N\tau_1 + sK_\theta K_o\tau_2 + K_\theta K_o \tag{1-121}$$

As we have done before, we have to determine the roots:

$$\frac{P}{N\tau_1\tau_3} = s^3 + s^2\frac{1}{\tau_3} sK_\theta K_o \frac{\tau_2}{N\tau_1\tau_3} + K_\theta K_o \frac{1}{n\tau_1\tau_3} = 0 \tag{1-122}$$

Therefore, the coefficients are

$$a_4 = 1 \tag{1-123}$$

$$a_3 = \frac{1}{\tau_3} \tag{1-124}$$

$$a_2 = K_\theta K_o \frac{\tau_2}{N\tau_1\tau_3} \tag{1-125}$$

$$a_1 = K_\theta K_o \frac{1}{N\tau_1\tau_3 = \frac{a_2}{\tau_2}} \tag{1-126}$$

The polynomial is of the order of 3, and we can use a calculator routine to find the roots b_1, b_2, and b_3; finally,

$$s_1 = 0 \tag{1-127}$$

$$s_2 = -b_1 \tag{1-128}$$

$$s_3 = -b_2 \tag{1-129}$$

$$s_4 = -b_3 \tag{1-130}$$

The next step is partial fraction forming:

$$\begin{aligned} \frac{1}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s} &= \frac{1}{a_4 s(s + b_1)(s + b_2)(s + b_3)} \\ &= \left(\frac{c_1}{s + b_1} \frac{c_2}{s + b_2} \frac{c_3}{s + b_3} \frac{c_4}{s} \right) \frac{1}{a_4} \end{aligned} \tag{1-131}$$

Now we have to determine C_i, for $i = 1$–4, and multiply the equation previously,

$$\frac{c_1(s+b_2)(s+b_3)s + c_2(s+b_1)(s+b_3)s + c_3(s+b_1)(s+b_2)s + c_4(s+b_1)(s+b_2)(s+b_3)}{(s+b_1)(s+b_2)(s+b_3)s}$$

which is equal to

$$\frac{1}{(s+b_1)(s+b_2)(s+b_3)s} \quad \text{(numerator = 1)}$$

Rearranging yields

$$\begin{aligned} &s^3(c_1 + c_2 + c_3 + c_4) \\ &\quad + s^2[c_1(b_2 + b_3) + c_2(b_1 + b_3) + c_3(b_1 + b_2) + c_4(b_1 + b_2 + b_3)] \\ &\quad + s[c_1b_2b_3 + c_2b_1b_3 + c_3b_1b_2 + c_3b_1b_2 + c_4(b_1b_2 + b_1b_3 + b_2b_3)] \\ &\quad + c_4b_1b_2b_3 \end{aligned}$$

and since

$$c_1 + c_2 + c_3 = 0 \tag{1-132}$$

$$c_1(b_2 + b_3) + c_2(b_1 + b_3) + c_3(b_1 + b_2) = 0 \tag{1-133}$$

$$c_1b_2b_3 + c_2b_1b_3 + c_3b_1b_2 = \frac{1}{N\tau_1\tau_3} \tag{1-134}$$

our final results are

$$c_3 = -c_1 - c_2 \tag{1-135}$$

$$c_2 = -c_1\frac{b_3 - b_1}{b_3 - b_2} \tag{1-136}$$

$$c_1 = \frac{1}{N\tau_1\tau_3}\frac{1}{(b_3 - b_1)(b_2 - b_1)} \tag{1-137}$$

Let us test this equation with a step function

$$\theta_1(s) = \frac{1}{s} \tag{1-138}$$

We obtain

$$-13\ \text{dBm}$$

$$\begin{aligned} \theta_o(s) &= NK_\theta K_o\frac{1 + s\tau_2}{s}\frac{1/N\tau_1\tau_3}{s^3 + \frac{1}{\tau_3}s^2 + \frac{\tau_2K_\theta K_o}{N\tau_1\tau_3}s + \frac{K_\theta K_o}{N\tau_2\tau_3}} \\ &= NK_\theta K_o\left[\tau_2\left(\frac{c_1}{s+b_1} + \frac{c_2}{s+b_2} + \frac{c_3}{s+b_3}\right) + \frac{c_1}{b_1}\left(\frac{1}{s} - \frac{1}{s+b_1}\right) + \frac{c_2}{b_2}\left(\frac{1}{s} - \frac{1}{s+b_2}\right) + \frac{c_3}{b_3}\left(\frac{1}{s} - \frac{1}{s+b_3}\right)\right] \\ &= NK_\theta K_o\left[\frac{(\tau_2 - 1/b_1)c_1}{s+b_1} + \frac{(\tau_2 - 1/b_2)c_2}{s+b_2} + \frac{(\tau_2 - 1/b_3)c_3}{s+b_3} + \frac{(c_1/b_1) + (c_2/b_2) + (c_3/b_3)}{s}\right] \end{aligned} \tag{1-139}$$

If we perform a Laplace transformation, our final result is

$$\theta_o(t) = NK_\theta K_o\left[\left(\tau_2 - \frac{1}{b_1}\right)c_1e^{-b_1t} + \left(\tau_2 - \frac{1}{b_2}\right)c_2e^{-b_2t} + \left(\tau_2 - \frac{1}{b_3}\right)c_3e^{-b_3t} + \left(\frac{c_1}{b_1} + \frac{c_2}{b_2} + \frac{c_3}{b_3}\right)\right] \tag{1-140}$$

To plot the Bode diagram, the open-loop gain equation for $A(j\omega)$ determined and plotted in magnitude and phase. We obtain

$$\begin{aligned} A(j\omega) &= -\frac{K_\theta K_o}{Nj\omega}\left(\frac{1}{j\omega\tau_1}\right)\frac{1+j\omega\tau_2}{1+j\omega\tau_3} \\ &= \frac{K_\theta K_o}{N\omega^2}\left(\frac{1+j\omega\tau_2}{1+j\omega\tau_3}\right)\frac{1}{\tau_1} \end{aligned} \tag{1-141}$$

We will then abbreviate

$$\frac{K_\theta K_o}{N\omega^2}\tau_9 \tag{1-142}$$

The phase is determined from

$$\frac{(1+j\omega\tau_2)(1-j\omega\tau_3)}{1+\omega^2\tau_3^2} = \frac{1+\omega^2\tau_2\tau_3+j\omega(\tau_2-\tau_3)}{1+\omega^2\tau_3^2} \tag{1-143}$$

and

$$\tan\phi = \frac{\omega\tau_2}{1+\omega^2\tau_2\tau_3} - \frac{\omega\tau_3}{1+\omega^2\tau_2\tau_3} \tag{1-144}$$

The magnitude is

$$|A(j\omega)| = \frac{\tau_9}{\tau_1}\frac{\sqrt{1+\omega^2\tau_2^2}}{\sqrt{1+\omega^2\tau_3^2}} \tag{1-145}$$

with

$$|A(j\omega)| = 1 \quad \text{(crossover point)} \tag{1-146}$$

We finally obtain

$$\tau_1 = \tau_9\sqrt{\frac{1+\omega^2\tau_2^2}{1+\omega^2\tau_3^2}} \tag{1-147}$$

and

$$A_1 = 1+\omega^2\tau_2^2 \tag{1-148}$$

$$A_2 = 1+\omega^2\tau_3^2 \tag{1-149}$$

The phase margin is

$$\phi = \arctan\omega\tau_2 - \arctan\omega\tau_3 + \pi \tag{1-150}$$

assuming that

$$\omega^2\tau_2\tau_3 \ll 1$$

Let us determine the natural loop frequency ω_o from the point of zero slope of the phase response,

$$\frac{d\phi(\omega)}{d\omega} = 0 \tag{1-151}$$

$$\frac{d\phi}{d\omega} = \frac{\tau_2}{1+(\omega\tau_2)^2} - \frac{\tau_3}{1+(\omega\tau_3)^2} = 0 \tag{1-152}$$

and therefore

$$\omega_o = \sqrt{\frac{1}{\tau_2 \tau_3}} \tag{1-153}$$

If we set

$$\alpha = \arctan \omega\tau_2 \tag{1-154}$$

$$\beta = \arctan \omega\tau_3 \tag{1-155}$$

$$\phi = \alpha - \beta + \pi \tag{1-156}$$

and

$$\begin{aligned} \tan\phi &= \tan[(\alpha - \beta) + \pi] \\ &= \frac{\tan(\alpha - \beta) + 0}{1 - 0} = \tan(\alpha - \beta) \end{aligned} \tag{1-157}$$

then

$$\tan(\alpha - \beta) = \frac{\tan\alpha - \tan\beta}{1 + \tan\alpha \tan\beta} = \frac{\omega\tau_2 - \omega\tau_3}{1 + \omega^2\tau_2\tau_3} = \tan\phi \tag{1-158}$$

If we set

$$\omega = \omega_o = \sqrt{\frac{1}{\tau_2 \tau_3}} \tag{1-159}$$

then

$$\tan\phi_o = \frac{(1/\sqrt{\tau_2\tau_3})(\tau_2 - \tau_3)}{1 = 1} = \frac{\tau_2 - \tau_3}{2\sqrt{\tau_2\tau_3}} \tag{1-160}$$

and

$$\sqrt{\tau_2\tau_3} = \frac{1}{\omega_o} \tag{1-161}$$

$$\omega_o^2\tau_2\tau_3 = 1 \tag{1-162}$$

$$\tau_2 = \frac{1}{\omega_o^2\tau_3} \tag{1-163}$$

Using this value, we can determine the time constant τ_3 from

$$\tan\phi_o = \frac{(1/\omega_o^2\tau_3) - \tau_3}{2(1/\omega_o)} = \frac{(1/\omega_o^2\tau_3) - \omega_o\tau_3}{2} \tag{1-164}$$

and

$$2\tan\phi_o\omega_o\tau_3 = 1 - \omega_o^2\tau_3^2 \tag{1-165}$$

$$\omega_o^2\tau_3^2 + 2\tan\phi_o\omega_o\tau_3 - 1 = 0 \tag{1-166}$$

The time constant τ_3 is determined from

$$\begin{aligned}\tau_3 &= \frac{-2\tan\phi_o\omega_o + \sqrt{4\tan^2\phi_o\omega_o^2 + 4\omega_o^2}}{2\omega_o^2} \\ &= \frac{-2\tan\phi_o\omega_o + 2\omega_o\sqrt{\tan^2\phi_o + 1}}{2\omega_o^2} \\ &= \frac{\tan\phi_o + \sqrt{(\cos^2\phi_o + \sin^2\phi_o)/\cos^2\phi_o}}{\omega_o} \\ &= \frac{-\tan\phi_o + 1/\cos\phi_o}{\omega_o}\end{aligned} \tag{1-167}$$

τ_3 is now determined independent of the other parameters, τ_1 and τ_2, by setting the value for ω_o and the phase margin ϕ to begin with. Once τ_3 is determined, the values for τ_1 and τ_2 can be computed by inserting them in the necessary equations.

These equations were somewhat lengthy, but they were spelled out in great detail to show the approach taken. A computer program based on these equations is presented in Section A-3 and can be used for Bode diagram plotting.

It may be useful to compare the normalized output response of the different types of loops. Figure 1-11a shows the step response for a phase margin of 10° and 45° and a type 2 third-order loop. Figure 1-11b shows the result for a type 1 second-order loop similar to the normalized output response for a damping factor of 0.1 and 0.45. Figure 1-11c shows the normalized output response for the same damping factors, 0.1 and 0.45.

These responses can be plotted in the Bode diagram. Figure 1-11d shows the integrated response $F(s)$ of the second- and third-order loops.

The closed-loop response of the type 2, second- and third-order loops is somewhat similar; but as Figure 1-11e shows, we obtain a much better suspension from the type 2 third-order loop than from the type 2 second-order loop.

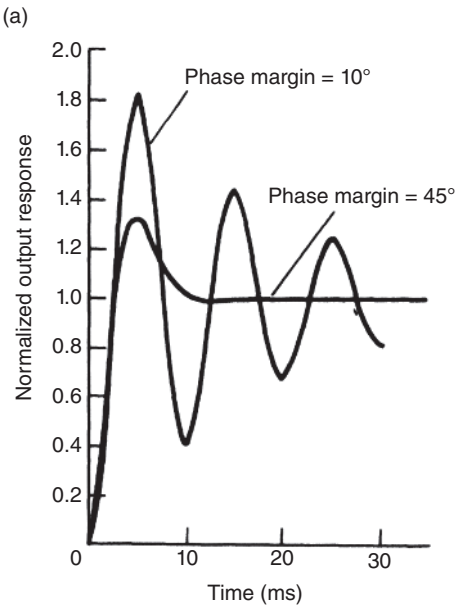


Figure 1-11a Normalized output response of a type 2 third-order loop with a phase margin of 10° and 45°.

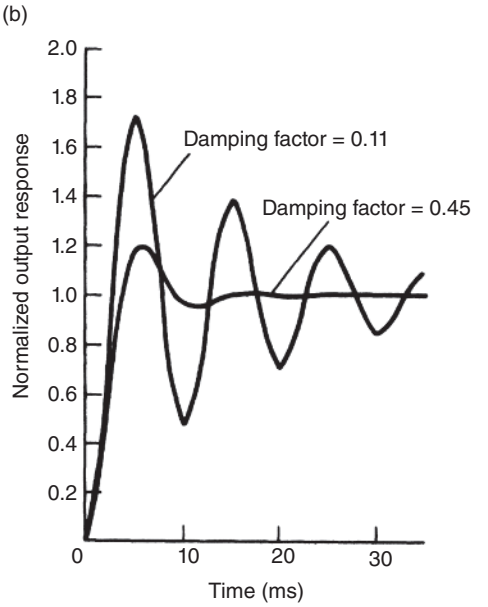


Figure 1-11b Normalized output response of a type 1 second-order loop having a damping factor of 0.1 and 0.45.

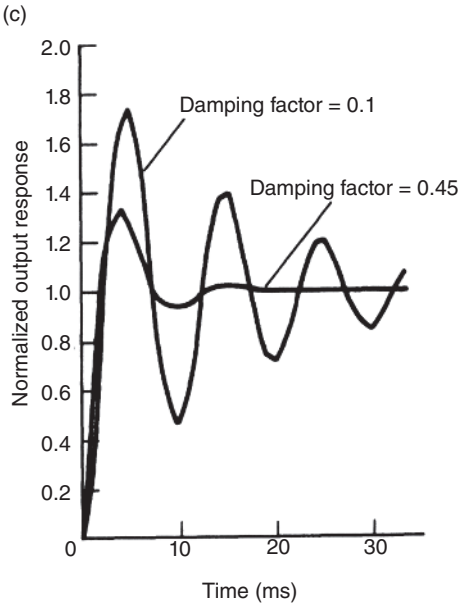


Figure 1-11c Normalized output response of a type 2 second-order loop with a damping factor of 0.1 and 0.05 for $\Omega_n = 0.631$.

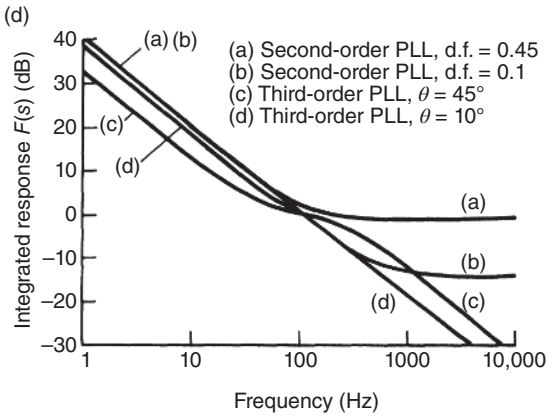


Figure 1-11d Integrated response for various loops as a function of the phase margin.

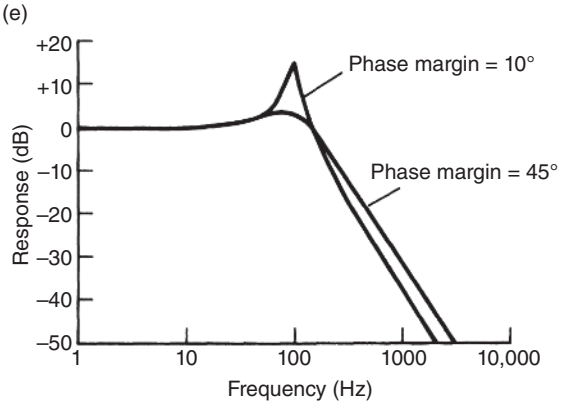


Figure 1-11e Closed-loop response of a type 2 third-order PLL having a phase margin of 10° and 45°.

If the phase margins of the damping factor chosen are inappropriate, we obtain an overshoot that translates into discrete spurious noise at the appropriate offset from the carrier.

1-7-2 FM Noise Suppression

In drawing the Bode plot, it is also convenient to show the suppression of noise of the VCO that is provided by the PLL. Using

$$E_n = \text{VCO noise voltage}$$

and

$$E = \text{noise voltage with loop closed}$$

we can write

$$E(s) = E_n(s)\frac{1}{1 + (\text{open-loop gain})}$$

$$= \frac{1}{1 + G(s)H(s)}$$
$$= \frac{1}{1 + A(s)} \tag{1-168}$$

or

$$\left| \frac{E(\omega)}{E_n(\omega)} \right| = \frac{1}{\frac{K_\theta K_o}{N\omega^2 \tau_1} \left| \frac{1+j\omega\tau_2}{1+j\omega\tau_3} \right| + 1} \tag{1-169}$$

The type 2 third-order loop is really the most important but was not used that often in the past. This may be a lack of understanding or not realizing that, by proper combination of the time constants, the unavoidable feed-through capacitors and some series capacitors can be incorporated to obtain this type of loop. The advantages of the third-order loop over the second-order loop are in the higher reference suppression for a given loop frequency, or if a certain loop frequency has to be chosen because of lockup time, the reference suppression is higher than we would find in the case of a type 2 second-order loop.

Let us take a case where we have the following parameters:

Reference frequency	5000 Hz
K_o	$2\pi \times 1$ MHz
K_θ	2.1
Division ratio N	10,000
ω_n	500 Hz
Phase margin	45°

The resulting values for the loop filter are determined from the computer program:

R_1	5600 Ω
R_2	1105 Ω
C_1	5.7E-7 F
C_2	1.19E-7 F
Reference suppression	32 dB
Lockup time	3 ms

The same loop in a type 2 second-order system would show reference suppression of 20 dB for the same loop bandwidth and 8-ms lockup time. These last two figures clearly indicate the advantage of the type 2 third-order loop.

Many applications require an even higher reference suppression. In the following analysis, we will deal with higher-order loops that are capable of additional suppression. However, the lockup time and the phase stability now may become a trade-off, as we will soon find out.

1-8 HIGHER-ORDER LOOPS

1-8-1 Fifth-Order Loop Transient Response

The fifth-order loop consists of a type 2 third-order loop with a second-order low-pass filter. The integrator is described by

$$F(s) = -\frac{1}{s\tau_1} \frac{1 + s\tau_2}{1 + s\tau_3} \tag{1.111}$$

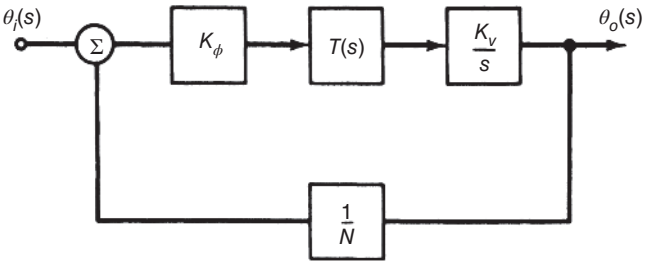


Figure 1-12 Noise contributing block in a type 2 fifth-order loop.

and the second-order low-pass filter is described by

$$K(s) = \frac{1}{s^2(1/\omega_n^2) + s(2d/\omega_n) + 1} \tag{1-170}$$

The transfer function of the filters is

$$\begin{aligned} T(s) &= \frac{-(1+s\tau_2)}{s^2\tau_1\tau_3 + s\tau_1} \frac{1}{s^2(1/\omega_n^2) + s(2d/\omega_n) + 1} \\ &= \frac{1+s\tau_2}{s^4\frac{\tau_1\tau_3}{\omega_n^2} + s^3\frac{\tau_1}{\omega_n}\left(2d\tau_3 + \frac{1}{\omega_n}\right) + s^2\tau_1\left(\tau_3\frac{2d}{\omega_n}\right) + s\tau_1} \end{aligned} \tag{1-171}$$

We use the familiar block diagram, Figure 1-12, which shows the phase detector, the low-pass filter, the active integrator [both condensed in $T(s)$], the VCO, and the divider. The forward gain now becomes $(K_\theta K_o/s)T(s)$, and the open-loop gain is

$$A(s) = \frac{K_\theta K_o}{s}\frac{T(s)}{N} \tag{1-172}$$

The closed-loop transfer function is

$$B(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{\text{forward gain}}{1 + (\text{open-loop gain})} \tag{1-173}$$

or

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{(K_\theta K_o/s)\,T(s)}{1 + (K_\theta K_o/Ns)\,T(s)} = \frac{K_\theta K_o T(s)}{s + K_\theta K_o T(s)/N} \tag{1-174}$$

Rearranging yields

$$\theta_o(s) = \theta_i(s) K_\theta K_o \frac{T(s)}{S + K_\theta K_o T(s)/N} \tag{1-175}$$

The output phase, which is the same as the VCO phase, is now assumed to be disturbed by a step of magnitude S_v. The amount S_v would be in the maximum case $N \times 2\pi$, using phase detector operating ranges of $\pm 2\pi$.

If this step is referred to the input of the phase detector, it has to be divided by N, and in Laplace notation, we have

$$\theta_i(s) = \frac{S_v}{Ns} \tag{1-176}$$

from which results

$$\theta_o(s) = \frac{S_v K_\theta K_o}{N} \frac{T(s)}{s^2 + (K_\theta K_o/N)sT(s)} \tag{1-177}$$

with $K_\theta K_o/N = U$. Applying a partial fraction, we obtain

$$\theta_o(s) = \frac{S_v}{s} - \frac{S_v s}{s^2 + UsT(s)} = \frac{S_v}{s} - \frac{S_v}{s + UT(s)} \tag{1-178}$$

After some manipulations, which are deleted, it can be shown that

$$\Delta\theta_o(s) = -S_v \frac{s^4 + s^3\frac{2d\tau_3\omega_n+1}{\tau_3} + s^2\left(\omega_n^2\frac{2d\omega_n}{\tau_3}\right) + s\frac{\omega_n^2}{\tau_3}}{s^5 + s^4\frac{2d\tau_3\omega_n+1}{\tau_3} + s^3\left(\omega_n^2\frac{2d\omega_n}{\tau_3}\right) + s^2\frac{\omega_n^2}{\tau_3} + s\frac{U\tau_2\omega_n^2}{\tau_1\tau_3}\ \frac{U\omega_n^2}{\tau_1\tau_3}} \tag{1-179}$$

We now factorize a denominator polynomial of the form

$$s^5 a_5 + s^4 a_4 + s^3 a_3 + s^2 a_2 + s a_1 + a_o$$

and therefore obtain the following coefficients:

$$a_5 = 1 \tag{1-180}$$

$$a_4 = \frac{2d\tau_3\omega_n + 1}{\tau_3} \tag{1-181}$$

$$a_3 = \omega_n^2 + \frac{2d\omega_n}{\tau_3} \tag{1-182}$$

$$a_2 = \frac{\omega_n^2}{\tau_3} \tag{1-183}$$

$$a_1 = U\tau_2\frac{\omega_n^2}{\tau_1\tau_3} \tag{1-184}$$

$$a_o = U\frac{\omega_n^2}{\tau_1\tau_3} \tag{1-185}$$

The next task is to determine the roots W_i and rewrite the denominator polynomial in the form

$$P_{\text{demoninator}} = (s - W_5)(s - W_4)(s - W_3)(s - W_2)(s - W_1) \tag{1-186}$$

For the Laplace transform, we need the residues

$$K_s = W_i = e^{ts}\frac{\text{numerator}}{\text{demoninator without containing } W_i} \tag{1-187}$$

The next step is to calculate the binomial residues:

$$K_k = e^{tPk}\frac{A_{k1} + A_{k2} + A_{k3} + A_{k4}}{B_{k1}B_{k2}B_{k3}B_{k4}} \tag{1-188}$$

$$K_1 = e^{tP_1}\frac{A_{16} + A_{15} + A_{14} + A_{13}}{B_{12}B_{13}B_{14}B_{15}} \tag{1-189}$$

$$K_2 = e^{tP_2}\frac{A_{26} + A_{25} + A_{24} + A_{23}}{B_{21}B_{23}B_{24}B_{25}} \tag{1-190}$$

$$K_3 = e^{tP_3}\frac{A_{36} + A_{35} + A_{34} + A_{33}}{B_{31}B_{32}B_{34}B_{35}} \tag{1-191}$$

$$K_4 = e^{tP_4}\frac{A_{46} + A_{45} + A_{44} + A_{43}}{B_{41}B_{42}B_{43}B_{45}} \tag{1-192}$$

$$K_5 = e^{tP_5}\frac{A_{56} + A_{55} + A_{54} + A_{53}}{B_{51}B_{52}B_{53}B_{54}} \tag{1-193}$$

As

$$A_{ij} = P_i \uparrow (j-2)Q\,j \tag{1-194}$$

$$i = 1,\ 2,\ 3,\ N_2 \tag{1-195}$$

$$j = 3,\ 4,\ 5,\ N_2 + 1 \tag{1-196}$$

and

$$B_{ij} = P_i - P_j \tag{1-197}$$

$$i = 1, 2, 3, \ \ldots\ , N_2 \tag{1-198}$$

$$j = 1, 2, 3, \ \ldots\ , N_2 \tag{1-199}$$

it is apparent that

$$A_{1ij} \triangleq \text{real}\, A_{ij} \tag{1-200}$$

$$A_{2ij} \triangleq \text{imaginary}\, A_{ij} \tag{1-201}$$

$$B_{1ij} \triangleq \text{real}\, B_{ij} \tag{1-202}$$

$$B_{2ij} \triangleq \text{imaginary}\ \ B_{ij} \tag{1-203}$$

$$K_{1i} \triangleq \text{real}\ \ K_i \tag{1-204}$$

$$K_{2i} \triangleq \text{imaginary}\ \ K_i \tag{1-205}$$

Using the results, we can rewrite

$$\Delta\theta_o(s) = \frac{s^4Q_6 + s^3Q_5 + s^2Q_4 + sQ_3}{s^5Q_6 + s^4Q_5 + s^3Q_4 + s^2Q_3 + sQ_2 + Q_1} \tag{1-206}$$

Finally, we obtain the roots P_1 to P_5 in terms of Q_1 to Q_6; then the partial fraction expansion gives the residues:

$$\underset{s=P_1}{K_1} = e^{tP_1}\frac{P_1^4Q_6 + P_1^3Q_5 + P_1^2Q_4 + P_1Q_3}{(P_1 - P_2)(P_1 - P_3)(P_1 - P_4)(P_1 - P_5)} \tag{1-207}$$

$$\underset{s=P_2}{K_2} = e^{tP_2}\frac{P_2^4Q_6 + P_2^3Q_5 + P_2^2Q_4 + P_2Q_3}{(P_2 - P_1)\,(P_2 - P_3)\,(P_2 - P_4)\,(P_2 - P_5)} \tag{1-208}$$

$$\underset{s=P_3}{K_3} = e^{tP_3}\frac{P_3^4Q_6 + P_3^3Q_5 + P_3^2Q_4 + P_3Q_3}{(P_3 - P_1)(P_3 - P_2)(P_3 - P_4)(P_3 - P_5)} \tag{1-209}$$

$$\underset{s=P_4}{K_4} = e^{tP_4} \frac{P_4^4 Q_6 + P_4^3 Q_5 + P_4^2 Q_4 + P_4 Q_3}{(P_4 - P_1)(P_4 - P_2)(P_4 - P_3)(P_4 - P_5)} \tag{1-210}$$

$$\underset{s=P_5}{K_5} = e^{tP_5} \frac{P_5^4 Q_6 + P_5^3 Q_5 + P_5^2 Q_4 + P_5 Q_3}{(P_5 - P_1)(P_5 - P_2)(P_5 - P_3)(P_5 - P_4)} \tag{1-211}$$

$$\Delta\theta(t) = \left[\sum_{n=1}^{5} K_n\right] \tag{1-212}$$

What is the practical use of higher-order loops? Higher-order loops are really useful only in frequency synthesizers if the reference frequency is substantially higher than the loop frequency. A typical example would be a reference frequency of as high as 5 or 10 MHz down to as low as 25 kHz, which has to be suppressed more than 90 dB. The phase shift introduced by the additional filtering, as can be seen by the computer program in the Appendix B and the example shown here, can be allowed only if the cutoff frequency of the loop is small relative to the additional poles of the filter. What is a typical example? Let us assume that we have a reference frequency of 25 kHz, and our loop frequency is set at 1 or 2 kHz. The resulting reference suppression with the simple loop filter would be approximately 20 times log(25 kHz/2 kHz), or roughly 20 dB. This is totally insufficient, of course.

The third-order loop, because of its deeper filtering, will increase this to roughly 33 dB, but this is still not enough. The insertion of a steep filter, such as an active filter or an inductor-capacitor (*LC*) elliptic filter, with poles at 25 kHz, will have very little phase shift at 2 kHz, the cutoff frequency of the loop filter, and a substantial suppression of the reference becomes possible. However, these high-order systems are useful only if there is enough difference between the reference frequency and the loop frequency. The higher the ratio between the two values, the easier it becomes to design a high-order system.

To get high suppression and not too much phase shift and to be able to work close to the reference frequency, special detectors are generally required. The phase shift introduced by using a sample/hold comparator is fairly small, and it is possible to set the loop filter at about half of the reference. If properly designed, the dual sampler combines good reference suppression with low noise. The phase shift can be adjusted and compensated. The drawback of the sample/hold comparator, as we will see in Chapter 4, is its limits as to what is the highest frequency of operation.

If properly designed, the tri-state phase/frequency comparator, also discussed in Chapter 4, may have 60–70 dB inherent reference suppression without the filter and may ease the requirement on the loop filter. Only techniques that compensate the spikes at the output of the tri-state phase/frequency comparator, as will be described later, will reduce the phase jitter and incidental FM introduced by this somewhat noisy discriminator. As the tri-state comparator is somewhat noisier than the sample/hold, the particular loop with its cutoff frequency and its noise requirements will determine which sample to use.

It may be useful to do some comparison between the different loops based on their performance. Figure 1-13a shows a simple block diagram of a PLL loop with a 15-MHz reference oscillator and 300-MHz output frequency. The division ratio is therefore 20. An active integrator with the time constant $T_1, \ldots, T_4$ and the open-loop gain A_0 is selected.

The plot of Figure 1-13b shows the phase noise of the VCO, the phase noise of the reference oscillator of 15 MHz, and the resulting phase noise when the loop is closed. The overshot is due to the loop bandwidth and the damping factor. In this case, the reduction of the loop and width would have reduced the phase noise as the VCO had better noise properties than the closed loop.

1-9 DIGITAL LOOPS WITH MIXERS

The single-loop synthesizer has a number of restrictions. One immediate restriction is the fact that the step size is the same as the reference frequency, unless special techniques are used, which are described in Chapter 3.

In addition, as we have frequency dividers that work "only" up to about 2 GHz, it becomes difficult, if not impossible, to build a PLL at a much higher frequency unless some mixing techniques are used. These techniques

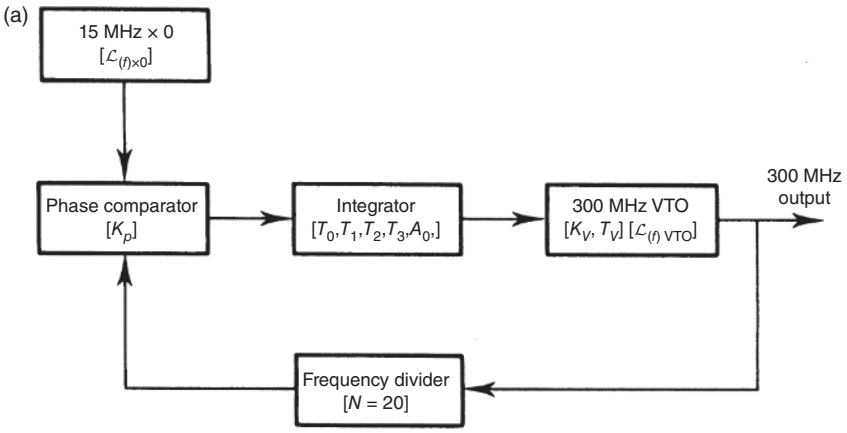


Figure 1-13a Simple block diagram of fifth-order PLL.

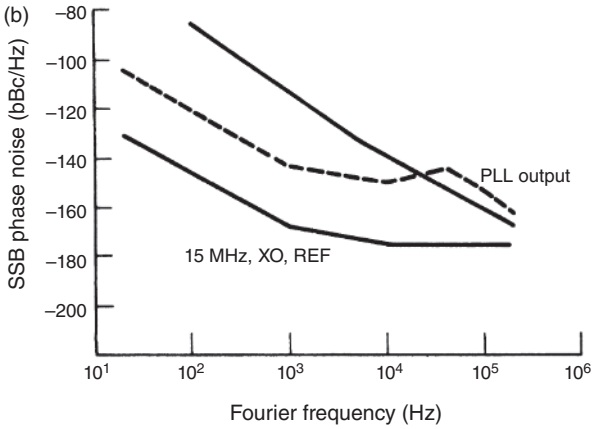


Figure 1-13b Single sideband (SSB) phase noise in dBc/Hz for the 15-MHz crystal oscillator (solid line) 300 MHz L_c VCO (solid line above) and PLL output of total system (curve).

are also sometimes referred to as *heterodyning techniques*. Figure 1-14 shows a single-loop synthesizer that has a mixer incorporated, which heterodynes the VCO frequency down to a lower frequency at which we have dividers available. The auxiliary frequency that is injected in the loop for down-conversion is generated from the reference oscillator and may be a direct-digital synthesis (DDS). Today we can get a DDS system up to 6 GHz, to be driven at 12 GHz or higher. Theoretically we could omit the divide by N stage, but the penalty would be the internal spurious of the DDS, so it is advisable to operate the DDS at less the 1/10 or less of the sampling frequency. For now we are mostly concerned only with the question of loop stability as a function of the introduction of this mixer, and its possible effects as far as unwanted sidebands are concerned.

Let us assume the numerical example shown in Figure 1-15. This synthesizer is intended for use in an amateur transceiver operating from 144 to 148 MHz, a frequency range that is well within the capabilities of current dividers. However, since we want to minimize power consumption, we find that it requires less power to generate an auxiliary frequency of 140 MHz from our 5-MHz standard (synchronizing a 70-MHz crystal and doubling it). The output frequency of this mixer then is 4–8 MHz, and this frequency range can be handled by a programmable divider in CMOS. Between the mixer and the divider, we will insert a bandpass filter of 4-MHz bandwidth. The divider in

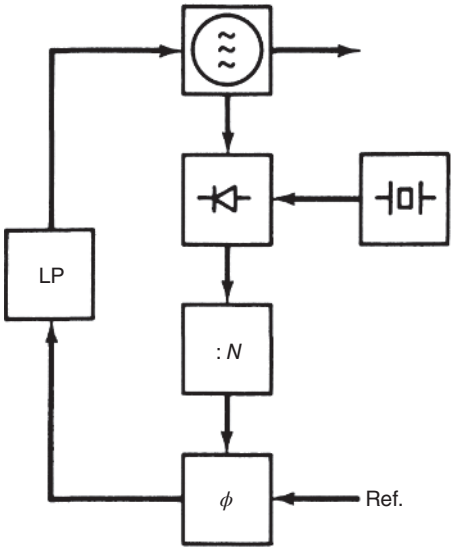


Figure 1-14 Block diagram of a digital PLL using the heterodyne technique.

CMOS now has to operate between 4 and 8 MHz. For such amateur applications it is frequently required that the same synthesizer be used to transmit and receive.

For transmit applications, frequency modulating the synthesizer is required, and the modulation can be inserted in the loop filter, as the loop bandwidth probably is restricted to a few hundred hertz, while the step size will be 5 kHz, in accordance with the channels available. The modulation could also be done if the 140 MHz was generated from a free-running 70-MHz crystal, which is then modulated.

At 70 MHz we will probably have to use a third- or fifth-overtone crystal, which cannot be pulled very well, probably not enough to accommodate a maximum of 3-kHz deviation. More information on pulling of crystals is presented in Chapter 4.

What does the insertion of the mixer do to our system? The division ratio without mixing would have been 28,800–29,600, or a ratio of 1:1.0278. After inserting the mixing stage, the division ratio now is 800–1600, and the absolute ratio is 1:2.

The loop gain, assuming that the VCO gain is constant over the tuning range, is now changing by the amount 1:2. In some loops we will find that the introduction of such a mixer results in a much larger change of division ratios, and if the frequencies are not selected properly, a change of 1:10 will occur. This will cause two difficulties:

(1) If the multiplication changes too much, the sideband of the reference being multiplied at the output will change substantially as a function of frequency setting, while the percentage change of the frequency at the output is very small. Therefore, at the higher frequency, in our case 148 MHz, the noise sideband inside the loop bandwidth will be twice as high as the 144 MHz. In a case where the loop gain changes more dramatically, such as 1:10, the noise will change by this amount.

(2) If the loop gain changes with all other parameters remaining constant, this may cause a stability problem. The net result is that, in the case of a type 2 second-order loop, our damping factor ζ can range from 0.1 to 1, and the transient performance of the loop will vary substantially; therefore, stability will become an issue. We have to find a method to compensate for the change of loop gain, and we will show a method of dealing with this phenomenon in Section 1-10. Right now it is only important to know that it does occur and that it can present a problem.

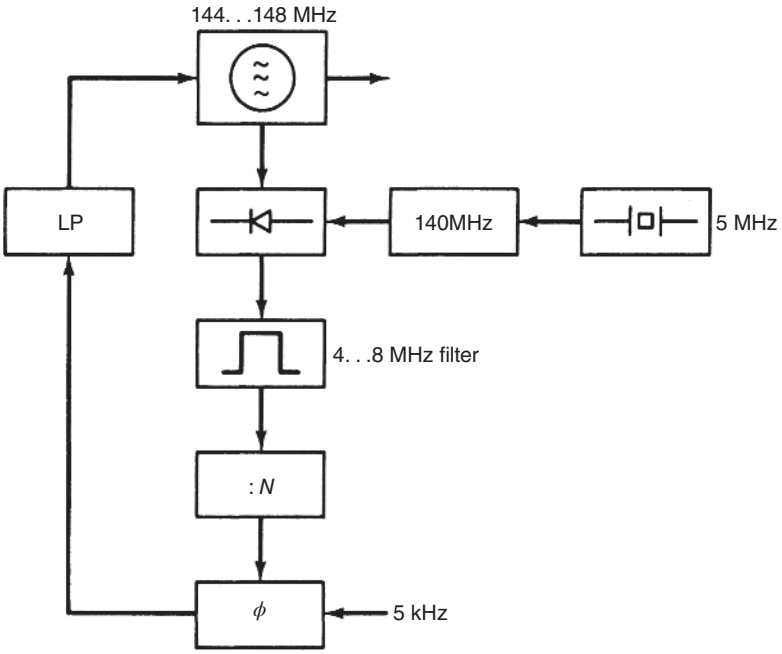


Figure 1-15 Block diagram of a 144- to 148-MHz synthesizer using the heterodyne technique, resulting in an internal IF of 4–8 MHz.

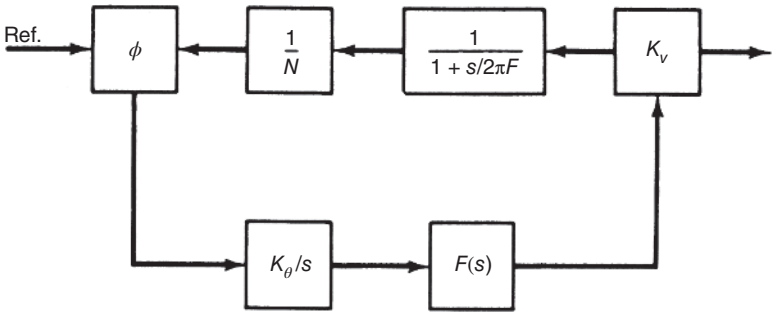


Figure 1-16 Linearized equivalent circuit of a PLL with the heterodyne technique, including delay information introduced by the IF filter.

The next effect the mixer produces is the consequence of phase shift of the IF filter following the mixer, in our case a filter ranging from 4 to 8 MHz. As a result, we have to modify our block diagram of the loop, as shown in Figure 1-16. The additional box represents the low-pass equivalent of the bandpass filter, and the delay of this filter has to be determined. There are a number of good books available that provide the necessary computation aids for these filters and information about the delay. One book, which is by Anatol I. Zverev [2], will be mentioned herein several times and is really an absolute must for the library of any design engineer who handles radio frequency (RF) and filter design.

The phase shift of the equivalent low-pass filter of the IF filter is

$$\theta_{\text{low pass}} = \arctan \frac{G_1(f_m)\sin\theta(f_m) - G_1(-f_m)\sin\theta(-f_m)}{G_1(f_m)\cos\theta(f_m) - G_1(-f_m)\cos\theta(-f_m)} \tag{1-213}$$

In some cases, we will have to use loops with conversions, where the resulting IF filter is very narrow. The use of a crystal filter will introduce a group delay in addition to the phase shift. These delays have to be added to the block diagram and added or subtracted from the actual phase. Since this can be done fairly easily and has a substantial impact on the stability, it is recommended that the interested reader analyze such an example mathematically, where it is assumed that the loop bandwidth is 2 kHz, the IF bandwidth is 100 kHz, and the loop bandwidth is increased to 50 kHz. We also have to take into consideration the effect of the phase shift of the low-pass filter equivalent of the bandpass filter. As the output signal from the mixer is passing the IF filter, which will be assumed to be symmetrical, the amplitude of the carrier G_1 (f_m) will change relative to the input signal. The losses of the filter and the sidebands will be shifted in phase equal to the phase shift generated by the filter. As is known from the literature, it is possible to convert the bandpass performance of this filter into an equivalent low-pass filter and deal with it. These details and examples are beyond the scope of this book and should be studied in the literature, such as in the book by Zverev already mentioned.

There are a number of unpleasant effects in addition to the one mentioned, such as ringing, as a result of non-equalized group delay, and if the IF filter bandpass is not symmetrical relative to the carrier frequency, AM-to-FM conversion occurs and has to be calculated. These special effects are an interesting topic, and the reader not only should be made aware of them but is also encouraged to calculate some numerical examples. In the rest of the book, we will assume that we know how to deal with these effects. The result of the calculations will be that a higher phase margin than the 45° recommended for higher-order loops has to be allowed to compensate for the additional delay. As a result of this higher phase margin, the settling time of the loop will become larger. In analyzing loops and in determining what frequency arrangements to use, one has to be aware of these trade-offs and optimize the loop by calculating a number of examples and finding the best solution by iteration.

The next effect we will analyze is the number of spurious signals introduced by the mixer. The double-balanced mixer, the best for such application, is still a highly nonlinear device that generates harmonics of the two frequencies applied, and those frequencies will mix with each other, resulting in a wide spectrum at the output. To keep the number of unwanted frequencies at the output at an acceptable level, we should observe two design rules:

(1) To obtain an IF, the two input frequencies should be as high and as close together as possible; the lower image is then used. A fairly simple low-pass filter at the output minimizes the possibility of feed-through and unwanted products.

(2) The power ratio between the RF and the LO should meet certain requirements. A design engineer is well advised to have about a 30-dB difference in level. Let us assume that the LO drive is +17 dB, a typical drive level for a medium-level double-balanced mixer; the RF input should then be −13 dBm or less. A further reduction in RF input may have the disadvantage of requiring too many amplifiers following at the output of the mixer and therefore generating additional noise from the post-amplifiers.

In cases such as that of our previous example, where we are mixing a fixed frequency of 140 MHz with a 144- to 148-MHz band, this requirement may be relaxed, and a drive level of 5 or 6 dBm may still be permissible. A decision on this matter depends on the particular case, and the best way of solving it is to take measurements in an actual circuit.

A spectrum analyzer connected at the output of the mixer operating at the range of interest with enough dynamic range should provide the necessary information. If these theoretical guidelines are followed, the design should be fairly trouble-free.

In Chapter 6 you will find several examples where double-balanced mixers are incorporated and IF frequencies inside the synthesizer are being used. In many cases, we have provided level information, and the particular synthesizers shown are spurious-free, at least 90 dB down relative to the carrier.

1-10 ACQUISITION

In order to understand the acquisition performance of the digital PLL, we must first look at the linearized model. As mentioned previously, we have several ranges in which the loop can operate, and Figure 1-17 shows a plot of these

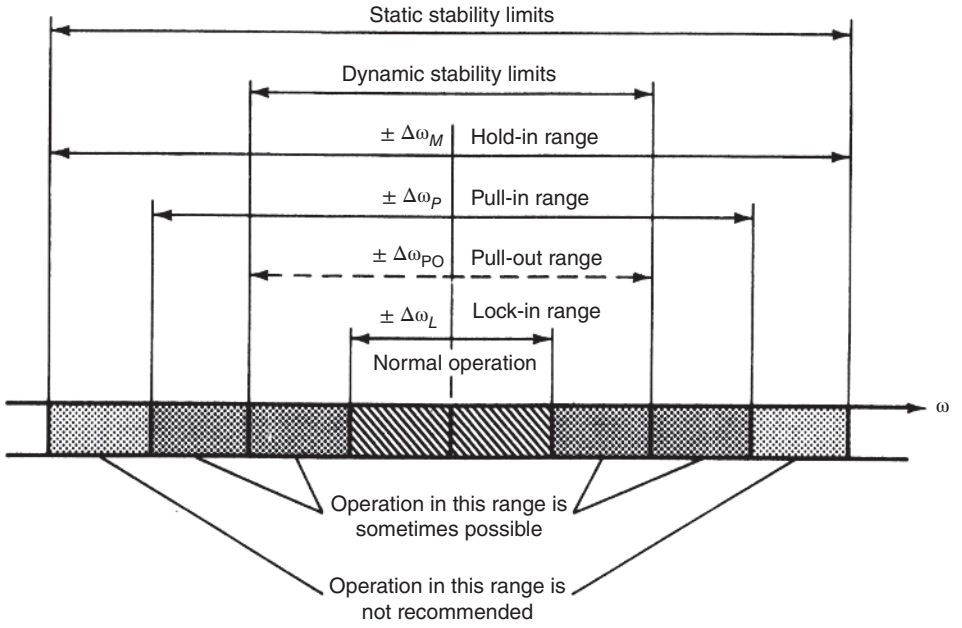


Figure 1-17 Possible operating ranges of a PLL.

ranges. The closest range around the center is the normal operating range and also the capture range, frequently called the *lock-in range*. Once a PLL has acquired lock, it maintains the locked condition within the hold-in range, and the borderline between the hold-in range and instability is fairly narrow. From our previous calculation and Laplace transform, applying

$$\theta_1(s) = \frac{\Delta\omega}{s^2} \tag{1-214}$$

to the input of the PLL, we can determine the maximum error using the final value theorem,

$$\lim_{t\to\infty} \theta_e(t) = \lim_{s\to 0} s\,\theta_e(s) = \frac{\Delta\omega}{K_o K_\theta f(o)} \tag{1-215}$$

With the assumption $\theta \approx \sin\theta$, the maximum amount this can be is 1 and therefore

$$\Delta\omega_H = K_o K_\theta F(o) \tag{1-216}$$

For the active filter $F(o)$ is infinite and therefore

$$\Delta\theta_H = \infty \tag{1-217}$$

and for the passive filter $F(o) = 1$ and

$$\Delta\omega_H = K_o K_\theta = \langle\langle \text{loop gain} \rangle\rangle \tag{1-218}$$

We have just calculated the hold-in range of the analog linear PLL. It is apparent that the use of an active loop filter guarantees a wider hold-in range.

Now let us go back and assume that the loop has not yet acquired lock. In the beginning we have two different frequencies applied to the phase detector. It is important to understand that, as the loop will acquire lock, we have

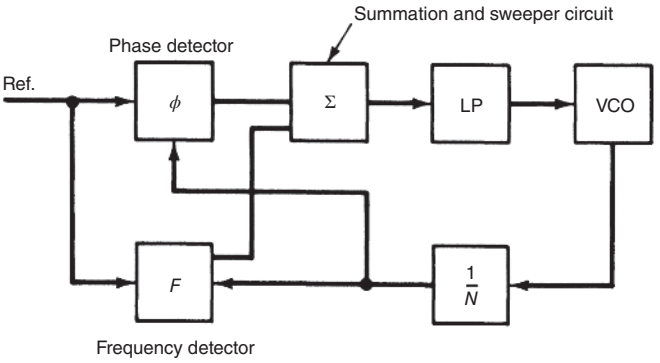


Figure 1-18 Block diagram of a PLL using a phase detector and frequency detector for acquisition aids in addition to the sweeper circuit.

to deal with two different ranges. One is the area in which we acquire frequency lock, and only after frequency lock has been accomplished can phase lock occur. There are several requirements necessary to make frequency lock possible.

(1) The tuning range of the VCO has to be wide enough to cover the desired range of operation.
(2) The VCO itself has to be able to oscillate through this required range without disruption of oscillation, a jump phenomenon frequently called "discontinuities."
(3) The tuning diodes have to be operated in a range where they do not become conductive (see Chapter 4) since leakage current from the diodes into the phase detector causes difficulty.
(4) Depending on the phase detector used, we either have a pull-in phenomenon, which we will discuss later, or sweeping, where the generated beat note at the output will sweep the oscillator from one end of the range to the other as an aid to acquire lock. In some instances, especially with pure phase detectors, an external frequency lock device may be necessary.

Figure 1-18 shows the two popular techniques used to help obtain frequency lock. The first one is the use of an additional frequency comparator, and an electronic device switches over from this to the phase detector. This technique is also used in the Philips HEF4750/51 large-scale integration (LSI) PLL integrated circuits. To obtain frequency lock, we first use a digital tri-state phase/frequency comparator that has a dead zone in the middle of its operating range where it is locked, and the system then switches over to a sample/hold comparator offering low-noise operation.

Another technique used in the past is an external sweeping device. Figure 1-19 shows the schematic of such an arrangement. We find a phase detector that operates into an NPN transistor. The loop filter is at the output of the phase detector, and the gain of the following dc amplifier is defined as the ratio of R_L/R_E.

A unijunction, or double-base transistor, is used to generate a sweeping signal. As the dc output voltage from this circuit reaches a certain level, the unijunction transistor ignites and starts its sweeping action. The frequency of oscillation of this circuit can be determined with the equation

$$f = \frac{1}{R_T C_T \log 2} \tag{1-219}$$

Note that R_T has to be derived from adding $R_{T1} + R_{T2} + R_{T3}$ in the starting condition, whereby we can assume that the amplifier draws no current. For the values taken here, we obtain a frequency of

$$f = \frac{1}{(18\,\text{k}\Omega + 10\,\text{k}\Omega + 220\,\Omega)10^{-6} \log 2} = 118\,\text{Hz}$$

The circuit will be swept with this particular frequency.

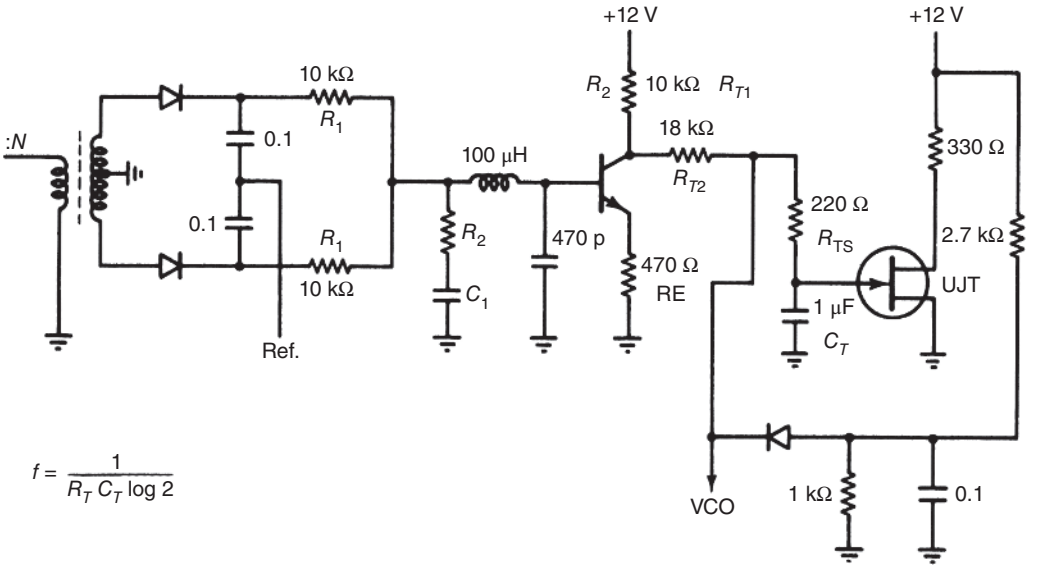


Figure 1-19 Schematic of the phase detector section of a PLL including a dc amplifier and a sweeping circuit.

We must now remember that there is a maximum frequency with which we can sweep the circuit to acquire lock. This is called the *pull-out range*. Pull-out range, defined $\Delta\omega_{PO}$, is determined by the equation

$$\Delta\omega_{PO} = 1.8\,\omega_n(\zeta + 1) \tag{1-220}$$

which is an approximation that can be applied in most cases. In our particular case with the unijunction transistor, the maximum sweep rate for $\zeta = 0.7$ and $\omega_{PO} = 118\,(2\pi)$ results in 38 Hz for the loop frequency ω_n.

However, our system is currently not yet in lock; we still have to calculate the lock-in range. A similar formula can be found as a function of the type of filter. For the simple *RC* filter with no phase compensation, as shown previously, the lock-in range is

$$\Delta\omega_L \approx \omega_n \tag{1-221}$$

and for the filter with phase compensation

$$\Delta\omega_L = 2\zeta\omega_n \tag{1-222}$$

We are interested in determining how long it takes to acquire lock. The following relation gives a good approximation of the lock-in time:

$$T_L \approx \frac{1}{\omega_n} \tag{1-223}$$

This is valid for all type 2 second-order linear PLLs. The calculation that we have just made referred to the phase lock. It becomes apparent from these equations that for $\zeta = 0.7$, the lock-in range is only equal to or slightly larger than the loop bandwidth. To move the VCO frequency within these limits, additional functions are required. This area is called *frequency lock*. We are now dealing with the pull-in range.

The pull-in range is the first range we have to deal with, as the PLL is about to acquire frequency, and later, phase lock. The explanation given here is somewhat backward, but it is easier to understand if one considers the ranges in this sequence, as the equations indicate the limitations. Pull-in is probably best understood by remembering that the system starts off with an offset in frequencies, and therefore a beat note appears at the output of the phase detector and of the loop filter. In the schematic using the sweeping technique shown previously, the loop bandwidth remains

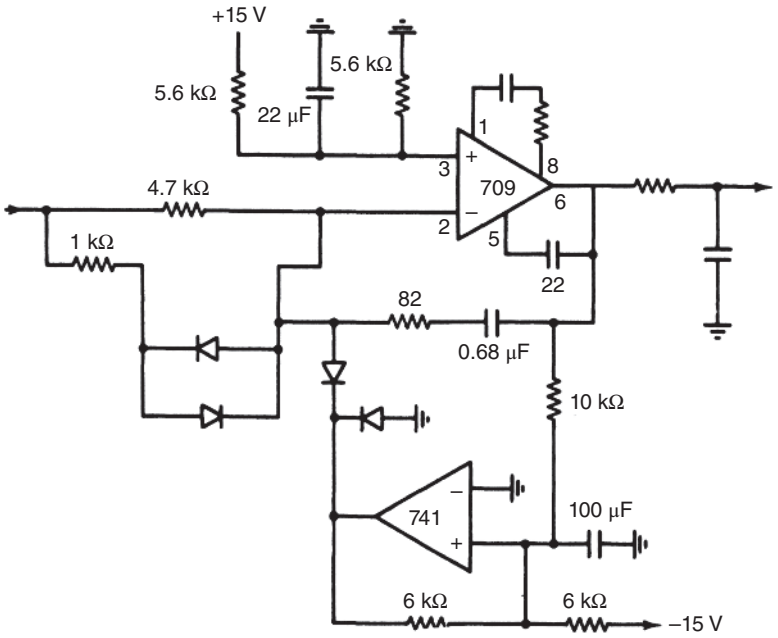


Figure 1-20 Schematic of a loop filter/integrator where the time constant is changed with the help of antiparallel diodes in the loop.

constant. Another way of helping the loop to acquire frequency lock is to widen the bandwidth of the loop filter, enabling phase lock with a larger frequency offset.

Figure 1-20 shows the schematic of a dual-time-constant loop filter, which can be used to explain the pull-in effect. Let us assume that initially we have a difference of several kilohertz between the two frequencies at the phase detector and are currently not considering the effect of a frequency divider.

The beat note generated at the output of the phase detector is an ac voltage together with a dc component. We also have to assume that in the initial condition the beat note is much larger in frequency than the bandwidth of the loop filter. As the output voltage of the loop filter sweeps the oscillator to either a higher or lower frequency, we have to see what the magnitude of the beat note as a function of sweeping is doing. It turns out that the difference in frequency becomes smaller if the VCO is swept toward higher values and becomes larger if the VCO is swept toward smaller frequency values. The output sweep frequency or beat note, therefore, is nonlinear and nonharmonic, and the average frequency at the output is no longer zero. The loop filter acting as an integrator will average the sweep.

The mathematical model for this pull-in is somewhat complicated. The *pull-in time*, defined as the time required for the average frequency error to decay from the initial condition to the locked limit, is

$$T_P = \frac{(\Delta\omega)^2 \tau_2}{K^2} = \frac{(\Delta\omega)^2}{2\zeta\omega_n^3} \tag{1-224}$$

This formula is valid only for the linear type 2 second-order loop. A model for the digital PLL will follow.

Example 1

Let us assume that our initial frequency offset is 1 MHz and that the loop bandwidth ω_n is 10 Hz. The time it requires for the pull-in range is

$$T_P = \frac{(2\pi \times 10^6)^2}{2\zeta(2\pi \times 10)^3} = 113.68 \times 10^6 \text{ s}$$

or 3.6 years. If we use the system that automatically increases the loop bandwidth with the two antiparallel diodes as previously shown, which results in a new loop bandwidth of 10 kHz prior to lock, the formula changes to

$$T_P = \frac{(2\pi \times 10^6)^2}{2\zeta(2\pi \times 10^4)^3} = 0.113 \text{ s}$$

The difference between both is dramatic, and with the simple trick of changing the loop bandwidth, we have speeded up the pull-in substantially.

Immediately after frequency lock has occurred, the switching diodes are no longer conductive. The remaining phase offset is handled by the lock-in function and the time it will now take to phase-lock the loop:

$$T_L = \frac{1}{\omega_n} = \frac{1}{10\,(2\pi)} = 16 \text{ ms}$$

The time required for phase lock, therefore, is much smaller than the time required for frequency lock, and the total lock time would be 0.1296 s.

Lock-in performance of the digital PLL system that uses a tri-state digital phase/frequency comparator as shown in Chapter 4 can no longer be calculated using the linearized model as is frequently done in the literature. The output of the tri-state phase/frequency comparator behaves totally different from the linearized models.

We have to take a look at two different examples. First, we will look at a tri-state phase/frequency comparator where the loop filter is placed after the summation stage, and Motorola CD4046 fits this description. When the system is switched on, first the two pulses that are combined through the CMOS switches will jam the output voltage up to the power supply voltage and the loop filter will delay this action, depending on the integration time constant. The dc voltage to the VCO, therefore, will slowly rise, the VCO will be swept, and pull-in will be accomplished.

It turns out that this particular example practically behaves as the linear analog phase detector version.

Now let us consider a phase/frequency comparator equal to the MC4044, which has two outputs, where pulses are available to charge or discharge a capacitor.

If the loop filter combination shown in Figure 1-21 is used, whereby each output of the phase/frequency comparator is applied to one input of an operational amplifier provided that the amplifier is fast enough to follow the input frequency, we now have to analyze the statistical average and determine from there what the output of the operational amplifier is showing.

The following mathematical mode, to the best of our knowledge, is the only one that ever assessed this effect correctly and was published by Roland Best in his book *Theory and Application of Phase-Locked Loops* [1]. The following discussion is published here with Dr. Best's permission.

1-10-1 Pull-in Performance of the Digital Loop

In the beginning of this chapter, when we were discussing the differences between the analog and digital PLL, we started with the digital phase/frequency comparators. The flip-flop-based digital phase/frequency comparators work on the principle that they analyze the rising edges of the input signals, edge-triggered flip-flops, and are insensitive to the duty cycle.

The output can be used to charge or discharge a capacitor and has to be combined with an active filter to take full advantage of its capabilities. Figure 1-21 showed the typical arrangement using this type of phase/frequency comparator.

Initially, when the loop is not in lock, we can assume that frequencies f_1 and f_2 have a random relation to each other, the phase of one to the other is random, and the next edge of the following signal within the time interval $0 \le t \le T$ can occur with the same probability in any given time. We define $w(t)dt$ as the probability that the next rising edge of the signal f_2 will occur in the time $t \cdot \cdot \cdot t + dt$. Therefore, we can write

$$w(t) = \frac{1}{T^2} \quad (t \le T_2) \tag{1-225}$$

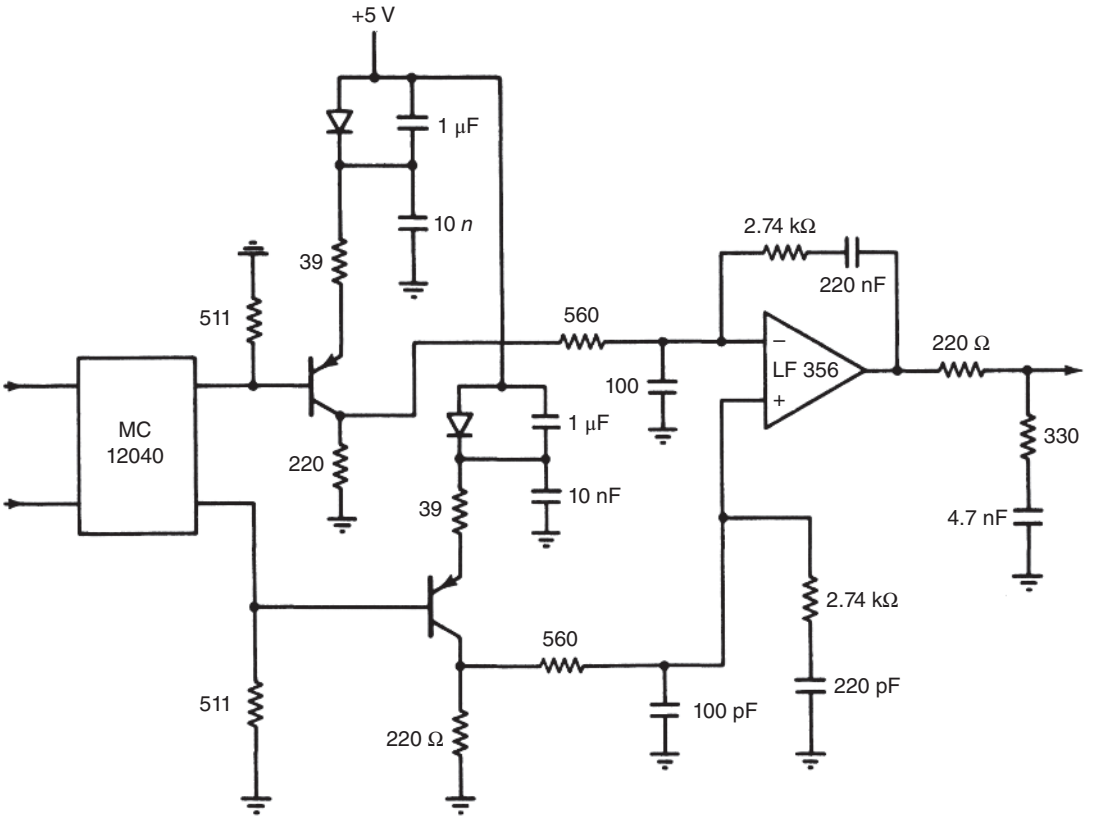


Figure 1-21 Schematic of an ECL phase/frequency comparator driving a high-frequency operational amplifier. The outputs to the inverting and noninverting input of the operational amplifiers are pulses, which are charging and discharging the loop capacitor of 220 nF. Note the additional output filter following the operational amplifier.

$$w(t) = 0 \quad (t > T_2) \tag{1-226}$$

We now may have two principal cases:

(1) f_2 is smaller than f_1 or $T_2 > T_1 = 1/f_1$, and the negative edge will occur: *case 1*, in the time interval $0 \le t \le T_1$; *case* 2, in the time interval $T_1 \le t \le T_2$.
(2) In the case of f_1 being smaller than f_2, these conditions are reversed.

As the output signal of the phase/frequency comparator is a chain of pulses that are combined, the duty cycle $\delta(t)$ will change. The average duty cycle $\bar{\delta}$, according to probability theory, can be determined from

$$\bar{\delta} = \int_0^{T_2} w(t)\delta(t)dt \tag{1-227}$$

The integration of this can be done in two steps:

$$\bar{\delta} = \int_0^{T_1} w(t)\frac{t}{T_1}dt + \int_{T_1}^{T_2} w(t)\frac{t}{2T_1}dt \tag{1-228}$$

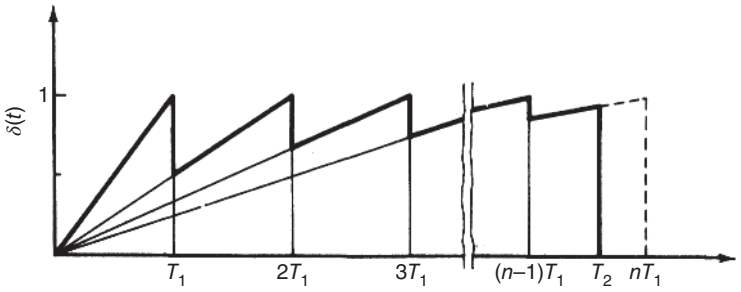


Figure 1-22 Change of duty cycle $\Delta(t)$ as a function of T.

with

$$\delta(t) = \frac{t}{T_1} \quad \text{and} \quad \frac{t}{2T_1}$$

depending on the time area, as discussed previously.

In reality, the time interval is not going to lie between T_1 and $2T_1$ but can be between T_1 and ∞. Therefore, our average duty cycle has to be written in the form of several integrals and

$$\bar{\delta} = \int_0^{T_1} w(t)\frac{1}{T_1}dt + \int_1^{T_1} w(t)\frac{1}{2T_1}dt + \cdots + \int_{T_1}^{T_2} w(t)\frac{1}{nT_1}dt \tag{1-229}$$

This can be converted into the final equation based on $f_1 > f_2$, and we obtain

$$\bar{\delta} = \frac{f_2}{2f_1}n - \sum_{i=1}^{n}\frac{1}{i} + \frac{f_1}{2nf_2} \tag{1-230}$$

with $n = \text{Int}(f_1/f_2) + 1$. Figure 1-22 shows the duty cycle for any combinations of $n\tau_1$, and Figure 1-23 shows the average duty cycle $\bar{\delta}$ as a function of the frequency ratio f_2/f_1. The straight-line approximation in this curve can be used to simplify the formula, as the lock-in will occur for the case $f_1 = f_2$. We will then obtain for the average duty cycle

$$\bar{\delta} = \frac{f_1 - f_2}{f_1} = \frac{\omega_1 - \omega_2}{\omega_1} \tag{1-231}$$

In this case, the average output voltage is

$$\bar{v}_d = \bar{\delta}V_B = \frac{V_B}{\omega_o}(\omega_1 - \omega_2) \tag{1-232}$$

since

$$\bar{v}_d = K_d'(\omega_1 - \omega_2) \tag{1-233}$$

We finally obtain the previously used gain constant of the phase comparator of this particular type in the out-of-lock condition to be

$$K_d' \approx \frac{V_B}{\omega_o} \tag{1-234}$$

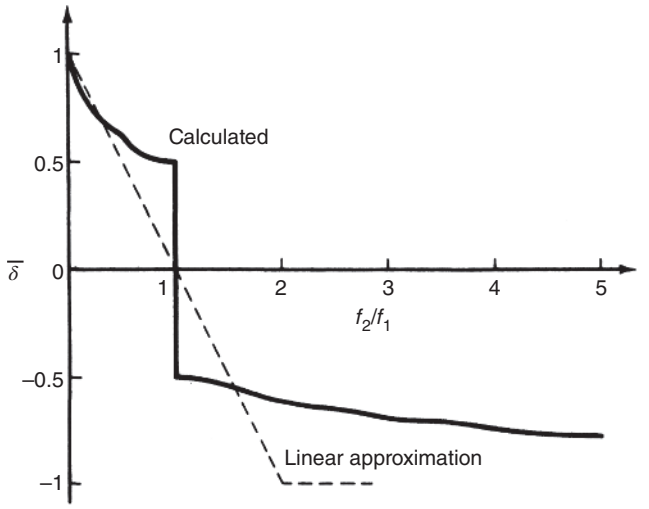


Figure 1-23 Average duty cycle $\bar{\delta}$ as a function of the frequency ratio f_2/f_1.

1-10-2 Coarse Steering of the VCO as an Acquisition Aid

We have learned so far that we can use a frequency detector or a sweep oscillator to steer or sweep the oscillator close to its final frequency.

In the case of sweeping, we have to make sure that the sweeping speed is not too fast, because if it is, the oscillator will never acquire lock or it will skip cycles several times before its acquires lock. The phenomenon of cycle skipping is explained in Gardner's book [5], but generally not enough information is available about the particular loop to take full advantage of the theoretical evaluation.

Once the transfer characteristic of the VCO is known, it is possible to use a read-only memory (ROM) that receives frequency information and, with the help of a digital-to-analog (D/A) converter within very fine resolution, to coarse steer the oscillator toward its desired final frequency. This method avoids the necessity of the additional external frequency comparator and the sweeping technique. The drawback is that if diodes are changed or the characteristic of the tuning diode as a function of age changes, the lookup table will become incorrect. This is true for extremely fine resolution. Let us assume the case where we have an oscillator operating from 70 to 80 MHz, which we want to coarse steer. If we assume for a moment that the tuning diodes do not produce additional noise or that, under certain circumstances, the additional noise contribution of the coarse-steering tuning diodes can be neglected, it is possible to take an 8-bit D/A converter, as shown in Figure 1-24, that is getting its frequency information from the binary-coded decimal (BCD) commands to the frequency divider, and generate within 100-kHz resolution an output that can be used to coarse steer the tuning diodes. Now the tuning diodes responsible for the fine tuning only have to work over a fairly narrow range, and as a result of this, the VCO gain is very small.

The output impedance of the D/A converter can be made very low, and because the coarse-tuning diodes are being driven from a low-impedance point rather than the typical high impedance the dc control line has, there is no pickup on the coarse-steering line from hum of any significant amount. As the fine-control loop now has a voltage gain of 30–100 kHz/V at most, the pickup is reduced by at least 20 dB, if not more. Therefore, the amount of spurious signal because of pickup and hum is reduced by the same amount.

This technique has the advantage also that the loop gain for this narrow window remains fairly constant, regardless of the VCO's curvature, as the transfer characteristic in this narrow window does not change very much.

The D/A converter has to generate a dc voltage that is not only nonlinear but rather is the opposite of the transfer characteristic of the tuning diodes used for the wide tuning range. A larger voltage swing will be needed at the higher frequency, whereas less voltage is required at the low end of the VCO. A practical schematic where this technique is used is given in Chapter 6.

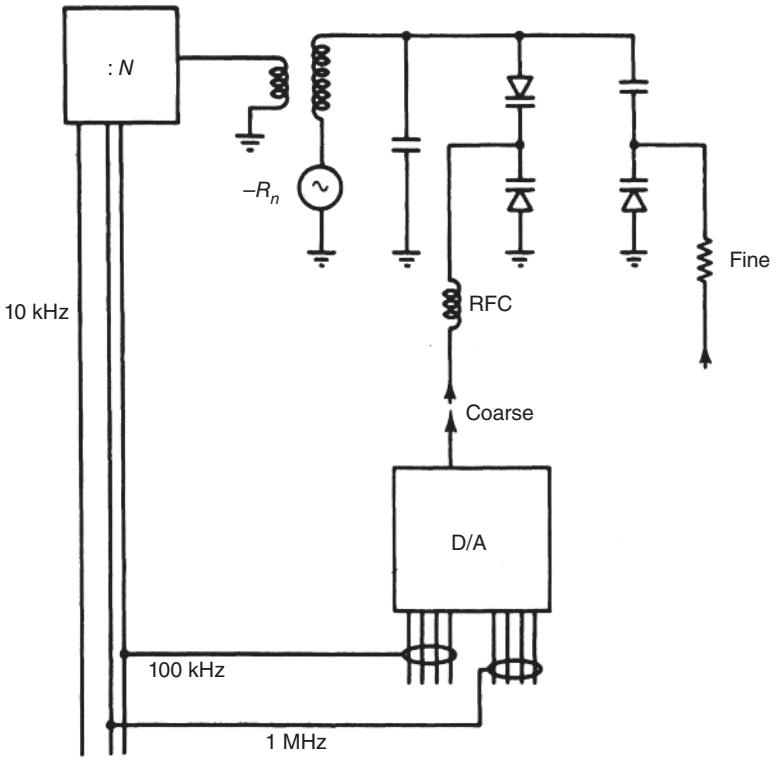


Figure 1-24 VCO coarse steering using a D/A converter.

In dealing with mixers, we have learned that one of the drawbacks of a heterodyne loop is that the open-loop gain changes more dramatically as the division ratio required becomes much larger. A typical loop without a heterodyne technique may have 30% or 40% variation of loop gain due to change of N, and we have seen cases where the division factor N, as a result of heterodyne technique, has changed by 20:1. How do we cope with this problem? The best way of handling this is either to use a coarse-steering technique with either tuning diodes or switching diodes and allow a very narrow window in which the oscillator will operate or change the loop filter dc control gain. Figure 1-25 shows an arrangement where, depending on the frequency setting of the dividers, several CMOS switches change the dc loop gain following the loop filter and, therefore, linearize the loop. The introduction of this amplifier after the loop filter has the drawback that the noise is no longer limited by a following filter, or if such an RC low-pass filter is used after the amplifier, the technique of analyzing high-order loops has to be used, and inside the loop bandwidth, we still find the additional noise contribution.

This approach is typically used in wideband loops where the output oscillator operates from 200 to 300 MHz, as an example, and the reference frequency is between 100 kHz and several megahertz. The loop gain, because of the small division ratio, is fairly high, while the loop gain variation due to some heterodyning may also be very high. In an effort to linearize, either the operational amplifiers are offset with a dc control voltage, or the loop filter is modified with additional capacitors in parallel, or a dc amplifier following the loop filter is used, which changes the dc gain. In some instances, all three techniques are used simultaneously, and it becomes very tricky to avoid additional noise being brought into the loop and to make all systems track without difficulty. Figure 1-26 shows a combination of all these techniques. Table 1-4 shows the most important formulas for digital PLLs. See also [3] and [4].

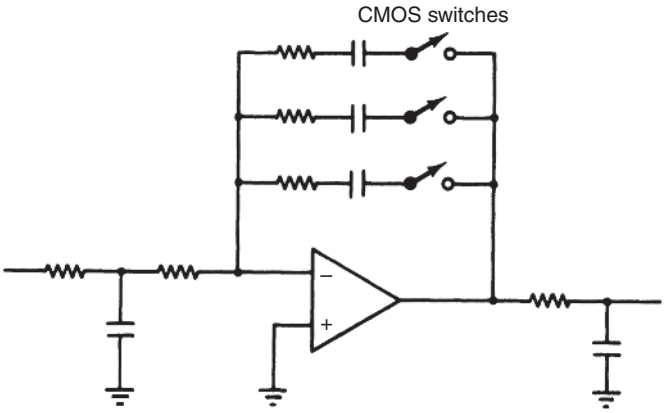


Figure 1-25 Linearizing of loop gain by changing loop components.

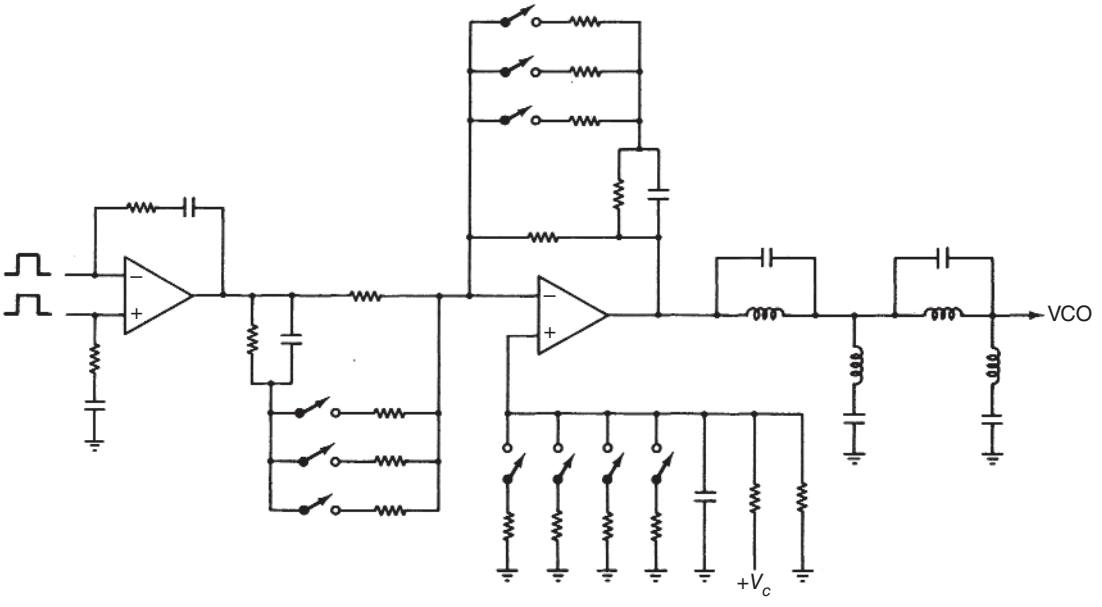


Figure 1-26 Circuit diagram of the loop filter dc amplifier arrangement of a PLL, where the loop gain and dc offset are controlled by CMOS switches to linearize and coarse steer the VCO.

1-10-3 Loop Stability

The easiest way to analyze the loop stability is to plot the magnitude and phase of the open-loop transfer function $K_v F(s)/s$ as a function of frequency. First, consider the case where $F(s)$ is a simple low-pass filter described by Eq. (1-27). For this case the open-loop frequency response is

$$K_v G(j\omega) = \frac{K_v}{j\omega(j\omega\tau + 1)} \tag{1-235}$$

Table 1-4 Most important formulas for digital PLLs (second-order only)

	Exclusive-OR gate		Edge-triggered JK master/slave flip-flop	
Phase/frequency comparator	Active filter	Passive filter	Active filter	Passive filter
Hold-in range	$\Delta\omega_H \to \infty$	$\Delta\omega_H = \frac{\pi}{2}\frac{K_o K_d}{N}$	$\Delta\omega_H \to \infty$	$\Delta\omega_H = \pi\frac{K_o K_d}{N}$
Capture range				
$\tau_2 \neq 0$	$\Delta\omega_L \approx \pi\zeta\omega_n$		$\Delta\omega_L \approx 2\pi\zeta\omega_n$	
$\tau_2 = 0$	$\Delta\omega_L \approx \frac{\pi}{\sqrt{8}}\omega_n$		$\Delta\omega_L \approx \frac{\pi}{\sqrt{3}}\omega_n$	
Pull-in range	$\Delta\omega_P \approx \frac{\pi}{2}\sqrt{\frac{2\zeta\omega_n K_o K_d}{N}}$	$\Delta\omega_P \approx \frac{\pi}{2}\sqrt{\frac{2\zeta\omega_n K_o K_d}{N} - \omega_n^2}$	$\Delta\omega_P \approx \pi\sqrt{\frac{2\zeta\omega_n K_o K_d}{N}}$	$\Delta\omega_P \approx \pi\sqrt{\frac{2\zeta\omega_n K_o K_d}{N} - \omega_n^2}$
Pull-in time	$T_P \approx \frac{4}{\pi^2}\frac{\Delta\omega_o^2}{\zeta\omega_n^3}$		$T_P \approx \frac{\Delta\omega_o^2}{\pi^2\zeta\omega_n^3}$	
Pull-out range				
$\zeta < 1$	$\Delta\omega_{PO} \approx 1.8\,\omega_n(\zeta + 1)$		$\Delta\omega_{PO} = \pi\,\omega_n \exp\left(\frac{\zeta}{\sqrt{1-\zeta^2}}\arctan\frac{\sqrt{1-\zeta^2}}{\zeta}\right)$	
$\zeta > 1$			$\Delta\omega_{PO} = \pi\,\omega_n \exp\left(\frac{\zeta}{\sqrt{\zeta^2-1}}\arctan\frac{\sqrt{\zeta^2-1}}{\zeta}\right)$	

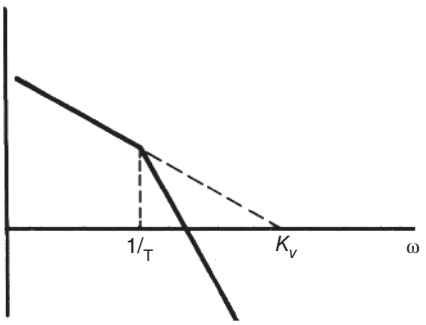


Figure 1-27 Magnitude of the open-loop gain of a PLL system.

The straight-line approximation of the magnitude of this open-loop transfer function is plotted in Figure 1-27. The magnitude of the response decreases at the rate of 6 dB/octave until the frequency is equal to the −3-dB frequency of the low-pass filter (1/2); for higher frequencies the magnitude decreases at a rate of −12 dB/octave.

Several rules of thumb, developed by Bode for feedback amplifiers, are useful in selecting the loop parameters. The first has to do with selecting the filter bandwidth $\omega_L = 1/\tau$. The approximation is: If the open-loop frequency response crosses the 0-dB line with a slope of −6 dB/octave, the system is stable; if the slope is −12 dB/octave or greater, the system is unstable. The second-order system under consideration is inherently stable, but the model is an approximation to a higher-order system. If the open-loop second-order model crosses the 0-dB line at −12 dB/octave, there is little room left for error. Additional phase shift from the VCO or phase detector could cause the loop to go unstable.

To have the open-loop gain cross the 0-dB line at −6 dB/octave, it is necessary that $\omega_L > K_v$. The larger ω_L is, the better will be the loop stability. From the filtering viewpoint, the smaller ω_L, the smaller the loop bandwidth and the less noise that will reach the VCO. K_v should be as small as possible to minimize the bandwidth. The larger the K_v, the smaller the steady-state error and the faster the loop response. Hence, in PLL design, compromises among noise performance, loop stability, steady-state error, and transient performance must be made.

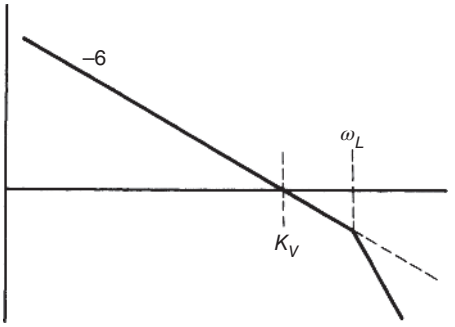


Figure 1-28 Open-loop frequency response in the case $\omega_L = K_v$.

Another rule of thumb that is helpful in PLL design is that the frequency ω_c at which the magnitude of the open-loop transfer function is unity,

$$\frac{K_v F(j\omega)}{j\omega_c} = 1 \tag{1-236}$$

is approximately the closed-loop 3-dB bandwidth. This relation is exact for the case where $F(j\omega) =$ constant.

If $F(s)$ is a simple low-pass filter response and $\omega_L > K_v$, the open-loop frequency response will be as shown in Figure 1-28. In this case, the loop bandwidth is approximately equal to K_v.

If $\omega_L < K_v$, the straight-line approximation will cross the 0-dB line with a slope of -12 dB/octave, which is not good from the standpoint of loop stability. Thus the filter bandwidth should be greater than the open-loop crossover frequency ω_c; ω_c will be approximately equal to the closed-loop bandwidth. Therefore, the filter bandwidth, for good loop stability, should be greater than the loop bandwidth for the simple type 1 system under discussion.

Another parameter that is useful in evaluating the response of second-order and higher systems is the phase margin, which is defined as

$$180^\circ + \arg KG(j\omega_c) \tag{1-237}$$

That is, the phase margin is equal to 180° plus the phase shift of the open-loop gain (a negative number) at the open-loop crossover frequency ω_c. The greater the phase margin, the more stable the system and the more phase lag from parasitic effects that can be tolerated.

Example 2

Consider a PLL that has $K_v = 10$ rad/s and that contains a low-pass filter with a corner frequency of 20 rad/s. The magnitude and phase of the open-loop transfer function are plotted in Figure 1-29. The system crossover frequency is approximately 10 rad/s. At this frequency, the phase shift of the open-loop transfer function is $-112.5°$, so the phase margin is 67.5°.

In this example, the complete phase plot was presented, but once one is familiar with phase plots, they no longer need to be included. One can simply calculate the phase shift after determining the open-loop crossover frequency from the magnitude plot.

Example 3

In Example 2, if the filter corner frequency had been 2 rad/s rather than 20 rad/s, what would have been the system phase margin?

Solution: To determine the phase margin, first plot the magnitude of the open-loop gain and determine the crossover frequency. The straight-line approximation of the magnitude is plotted in Figure 1-30. ω_c is found to be

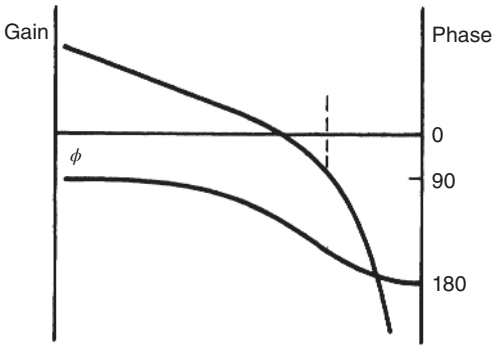


Figure 1-29 Magnitude and phase of the open-loop transfer function for $K_v = 19$ rad/s and $\omega_L = 20$ rad/s.

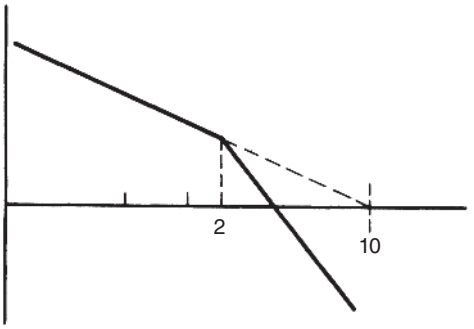


Figure 1-30 Magnitude of the open-loop gain of Example 3.

approximately 4.4 rad/s. Thus, the system phase margin is

$$180^\circ - (90^\circ + \arctan 2.2) = 23.40^\circ$$

which is too small for good loop stability. This is in agreement with the rule of thumb, which states that if the magnitude of the open-loop response described crosses the 0-dB line with a slope of -12 dB/octave, the system is unstable. In this example, the straight-line approximation for the gain decreases at -12 dB/octave, but the actual response crosses the 0-dB line with a slope slightly more positive than -12 dB/octave: hence, the small phase margin.

Although the most important frequency-domain design parameters are the closed-loop bandwidth ω_h and the peak value M_P of the closed-loop frequency response, no design techniques exist that allow easy specification of B and M_P. It is relatively easy to design for specified open-loop parameters ω_c and ϕ_m. There are approximations that relate ω_c and ϕ_m to ω_n, M_P, and ζ, and thus to the system rise time and overshoot. Fortunately, the conditions under which these approximations are valid are satisfied by most PLLs.

For the open-loop system (second-order loop),

$$K_v G(s) = \frac{K_v}{s(s/\omega_L + 1)} \tag{1-238}$$

Used with unity feedback, the closed-loop transfer function is given by Eq. (1-28), with

$$\omega_n^2 = K_v \omega_L \tag{1-239}$$

and

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_L}{K_v}} \tag{1-240}$$

The open-loop unity gain frequency is easily shown to be

$$\omega_c = \omega_L \left[\frac{\sqrt{1 + 4(K_v/\omega_L)^2} - 1}{2} \right]^{1/2} \tag{1-241}$$

Once ω_c is known, the phase margin

$$\phi_m = 90^\circ - \arctan \frac{\omega_c}{\omega_L} = 90^\circ - \arctan \left[\frac{\sqrt{1 + (1/2\zeta)^2} - 1}{2} \right]^{1/2} \tag{1-242}$$

can be calculated. This equation is plotted in Figure 1-31. The closed-loop system parameters of most importance are adequate stability (which is related to phase margin), system bandwidth (which determines the speed of the transient response), and system transient response (rise time and overshoot). For a low-pass transfer function, the bandwidth ω_n is defined as the frequency at which the gain is equal to 0.707 of its dc value. The bandwidth of the system represented by Eq. (1-28) is

$$\omega_h = \omega_n(1 - 2\zeta^2 + \sqrt{2 - 4\zeta^2 + 4\zeta^4})^{1/2} \tag{1-243}$$

which can be calculated using Eqs. (1-35), (1-239), and (1-240). For the underdamped second-order system given by Eq. (1-28) ($\zeta < 1$), the peak value of the time response to a unit step input can be shown to be

$$P_o = 1 + e^{-n\,\zeta/\sqrt{1-\zeta^2}} \tag{1-244}$$

The overshoot is determined solely by ζ. P_o as a function of ζ is plotted in Figure 1-32.

For high-order systems, the overshoot and bandwidth are not readily related to the open-loop system parameters, but a good first approximation is that Eq. (1-241) holds for higher-order systems. It is relatively easy to design a system to have a given phase margin. A design can then be evaluated using computer simulation. If the simulation indicates that the overshoot is too high (or too low), the phase margin can be increased (reduced), but the relations among phase margin, damping, and overshoot are amazingly accurate for higher-order systems. This implies that the response of most feedback systems can be described by a second-order model. Also, the closed-loop bandwidth can be related to the open-loop crossover frequency ω_c and the damping ratio, but it usually suffices to use the rule of thumb that the closed-loop bandwidth of underdamped systems is approximately 50% greater than the open-loop crossover frequency ω_c.

If it is desired to design for a peak transient overshoot, Eq. (1-240) can be used to determine the damping and then Eq. (1-241) is used to determine the required phase margin.

Example 4

For the PLL with open-loop transfer function

$$\frac{K_v}{s(s/\omega_L + 1)}$$

($K_v = 1000$), determine the low-pass filter corner frequency ω_L so that the system peak overshoot in response to a step input will be less than 20%.

Solution: Equation (1-242) or Figure 1-32 indicates that for $P_o < 1.2$, the damping ratio ζ must be greater than 0.45. For a ζ of 0.45, the corresponding phase margin is found [using Eq. (1-242)] to be about 50.

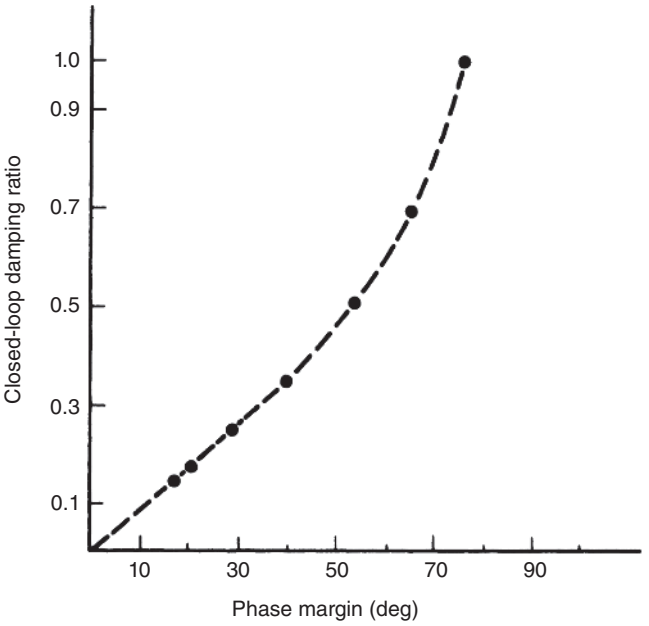


Figure 1-31 Closed-circuit damping ratio and phase margin relationship.

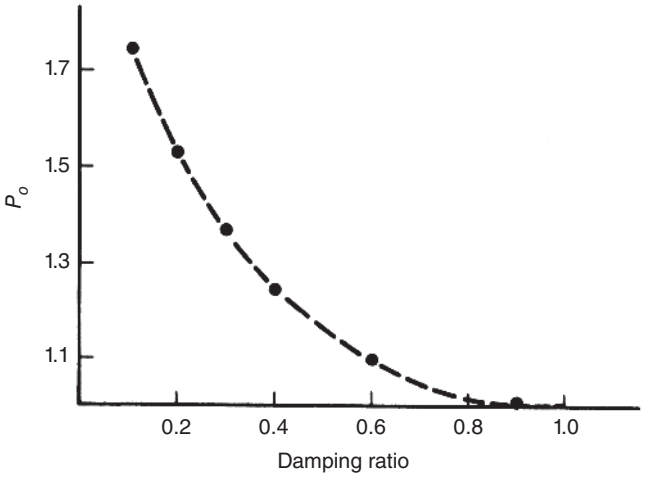


Figure 1-32 Peak overshoot as a function of damping ratio.

The low-pass filter can contribute −40° phase lag 1 and the phase margin will be equal to 50%. Therefore, ω_L must be greater than ω_c (if $\omega_L = \omega_c$, the phase margin would be 45°), so ω_c is approximately 1000 rad/s = K_v. Thus, arctan $1000/\omega_L = 40°$ or $\omega_L = 1192$. (This is somewhat of an approximation, since adding the low-pass filter will slightly reduce the crossover frequency.) The desired open-loop transfer function becomes

$$\frac{1000}{s\left(\frac{s}{1.10\times10^3}+1\right)} = KG(s) \tag{1-245}$$

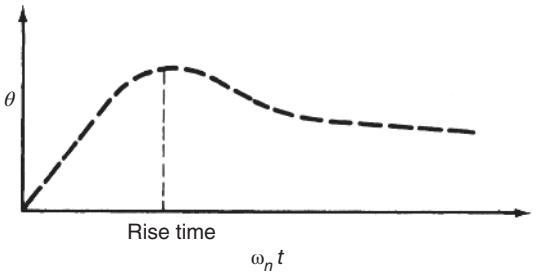


Figure 1-33 Overshoot and rise time of our example.

The step response is plotted in Figure 1-33. The overshoot is 13% and the rise time is 2.1 ms. The overshoot is considerably less than the specified maximum of 20% because of the straight-line approximations used to estimate the gain and crossover frequency. Note that this second-order system is simple enough to be solved analytically since

$$\frac{K_v G}{1 + K_v G} = \frac{1}{(s^2/1000\omega_L) + (s/1000) + 1} = \frac{1}{(s^2/\omega_n^2) + (2\,\zeta s/\omega_n) + 1}$$

where $\omega_n^2 = 1000\omega_L$ and $2\zeta/\omega_n = 1/1000$, or

$$\zeta = \frac{\omega_n}{2000} = \frac{\sqrt{1000\omega_L}}{2000}$$

For $\zeta = 0.45$ (the design value),

$$\omega_L = \frac{(900)^2}{1000} = 810$$

The straight-line approximations resulted in a 32% error in the calculation of the low-pass corner frequency and the overshoot was 13% rather than 20% (for $\omega_L = 810$, the rise time is 2.28 ms). The differences between the two methods could have been reduced by accounting for the fact that the pole of the low-pass filter reduces the crossover frequencies and thus increases the actual phase margin over that estimated with the straight-line approximation.

In some instances it is also necessary to specify the loop bandwidth. In order to control both the loop damping and bandwidth, an amplifier can be added in series with the low-pass filter. If the filter is implemented using active components, the additional gain can be obtained without any additional components.

Example 5

Consider Example 4 with the additional specification that the rise time in response to a unit step input be less than 1 ms. Since the overshoot is to be less than 20%, the phase margin must be approximately 50°. To design for the rise-time specification, it is easiest to use the approximation

$$t_r = \frac{2.2}{B}$$

which is exact only for first-order systems but provides a good design guideline for higher-order systems. Thus, ω_c should be greater than $2.2/t_r = 2.2 \times 10^3$ rad/s.

The previous discussion has shown that

$$\omega_c = K_\theta K_o K = 1000K$$

Thus, for $\omega_c = 2.2 \times 10^3$ rad/s, an additional amplifier with a gain $K = 2.2$ needs to be added. With the increased ω_c, ω_L will have to be increased from Example 4 in order to meet the phase margin specification. For the second-order systems under discussion,

$$\frac{2\zeta}{\omega_n} = \frac{1}{K_v} \tag{1-246}$$

The damping ζ is to be approximately 0.45 to meet the overshoot specification. It suffices to estimate the closed-loop bandwidth by assuming that it is approximately equal to ω_n, which is also approximately equal to the open-loop crossover frequency. Therefore, for $\zeta = 0.45$ and 1 ms rise time,

$$\omega_n = \frac{2.2}{10^{-3}} = 2.2 \times 10^{-3} = 2\,\zeta K_v = \sqrt{K_v \omega_L}$$

Therefore,

$$K_v = \frac{2.2 \times 10^3}{2 \times 0.45} = 2.44 \times 10^3$$

and

$$\omega_L = \frac{(2.2 \times 10^3)^2}{2.44 \times 10^3} = 1.98 \times 10^3$$

An additional gain K required is

$$K = 2.44$$

The complete open transfer function is then

$$K_v G(s) = \frac{2.44 \times 10^3}{s\left(\frac{s}{1.98 \times 10^3} + 1\right)}$$

and the closed-loop transfer function is

$$\frac{K_v G}{1 + K_v G} = \frac{1}{\frac{s^2}{(2.2 \times 10^2)^2} + \frac{s}{2.33 \times 10^3} + 1}$$

A plot of the step response is shown in Figure 1-34. The peak overshoot is 10% and the rise time is 0.7 ms. The two specifications are now met. In general, two adjustable parameters, such as loop gain and filter bandwidth, are needed to independently specify overshoot and rise time.

An operational amplifier circuit to realize the low-pass filter with a gain of 2.4 is shown in Figure 1-35. Since the feedback impedance is

$$Z_f = \frac{R_f}{R_f C_f s + 1} \tag{1-247}$$

the ideal voltage gain is

$$A_v = \frac{-Z_f}{Z_t} = \frac{-R_f / R_i}{R_f C_f s + 1} \tag{1-248}$$

which realizes the desired gain and filter provided that

$$\frac{R_f}{R_t} = 2.44 \quad \text{and} \quad \mathrm{R}_f C_f = \frac{1}{1.98 \times 10^3}$$

If the phase inversion resulting from this circuit is undesirable, phase inverting at the phase/frequency discriminator can be performed.

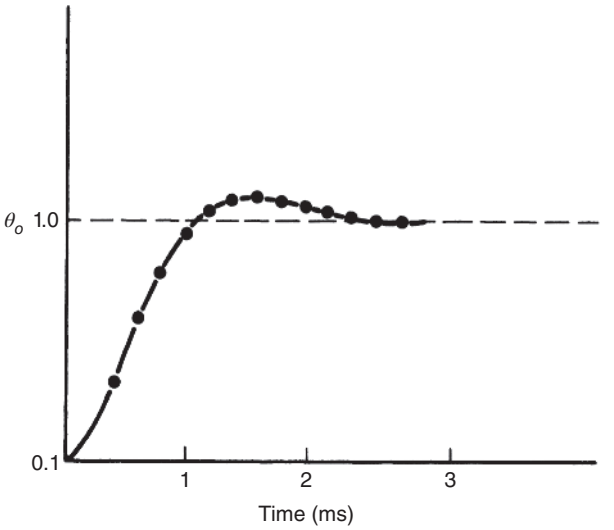


Figure 1-34 Plot of the step response of a 10% overshoot and 0.7-ms rise time.

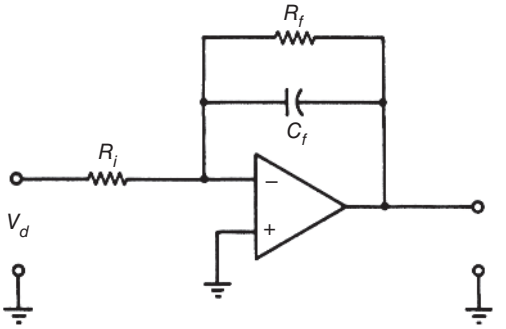


Figure 1-35 Loop filter with a gain of 2.2.

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SUGGESTED READING

Some of the references listed in this section are not very recent but we found them very helpful.

The following search of the IEEE data base gives more than 5000 useful references with continuous updates: http://ieeexplore.ieee.org/search/searchresult.jsp?queryText=Pll%20circuits&newsearch=true.

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