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Why ESD?

1.1 A Historical Perspective

Sure, this book means to discuss about electrostatic discharge (ESD) protection designs for integrated circuits (ICs). Yet nothing would prohibit our free minds from wandering around a bit before the show starts.

Imagine a world without electricity? The answer is no-brainer – impossible and scary!

To solve any problem, it is important to know where does it come from. Human curiosity in electricity dates back to our ancient ancestor era. Let us take a flash cyber-trip traveling through the time tunnel back to the ancient past. Around 600 BC, the Greek scientific philosopher, Thales of Miletus, discovered that a piece of amber rubbed with fur can magically attract light things, such as leaves, ash, or dust, because the amber was considered to have gained static *charges*, or, *electrostatic charge* as we call it these days. This *amber effect* is what is called *static electricity* today. Indeed, the loveliness of amber goes well beyond its natural beauty as shown in Figure 1.1. In fact, the English word *electron* came from the Greek word *elektron* for amber. Later, William Gilbert conducted serious studies on the attraction associated with rubbing materials, such as amber, and named it *electric* attraction, which led to the publication of *DeMagnete* in 1600 [1]. The word *electricity* was derived subsequently. The two types of electricity, i.e., vitreous (glass) and resinous (amber) was documented by Charles François de Cisternay DuFay in 1733 [2]. In 1751, Benjamin Franklin gave the terms of “positive” and “negative” for the two types of electrostatic charges in his publication of “Experiments and Observations on Electricity” [3], albeit a reverse definition might have made the life of college freshman students a little easier in understanding the current flowing direction versus the electron flowing direction. Obviously, when Franklin enjoyed his leisure time flying a kite, as shown in Figure 1.2, his brain never stopped roaming in the scientific wonderland. During 1800s, it became evident that electric charge may not be further divided, and Johnstone Stoney gave it the name “electron.” Later, Joseph John Thomson’s experiments led to the conclusion of the existence of light particles carrying negative charge, and the word “electron” was used for it in 1897. The hard-working Thomson (Figure 1.3) was rewarded with the Nobel Prize in Physics in 1906 “in recognition of the great merits of his theoretical and experimental investigations on the conduction of electricity by gases.”

The magic charges have brought in unlimited amount of amazing applications, which have dramatically changed our life today. In a conductor, electric charges can move freely to form the electric current, which fire up an electric lightbulb and light up our life, mostly thanks to Humphry Davy who invented the first electric light in 1809 and Thomas Edison who demonstrated the first carbon filament bulb in 1897, as shown in Figure 1.4. Equally amazing and important are the electric charges at rest, i.e., static charges or electrostatic charges, which when discharge through an air



Figure 1.1 Elektron in Greek word means Amber that is beautiful both aesthetically and scientifically. (Courtesy of Custom Crystal.)



Figure 1.2 Benjamin Franklin's thought about electricity: (1) the lightning is electricity; (2) the two types of electrical charge are positive (vitreous) and negative (resinous). (Courtesy of Chris Wang.)



Figure 1.3 J. J. Thomson discovered the electron in experiment to study “cathode rays” in 1897. He found that cathode rays consist of charged particles (electrons) that can conduct electricity. (Courtesy of Cavendish Laboratory, University of Cambridge.)

gap, being one version of the ESD phenomena, will produce electromagnetic waves that eventually led to radio-frequency (RF) wireless communications. The ESD-based radio waves were first observed by Heinrich Rudolf Hertz in experiments conducted during 1886–1889 using amazingly simple spark-gap radio transmitter as shown in Figure 1.5 [4]. At the time, Hertz did not realize the importance of his spark-gap radio wave experiments. In his own words, Hertz said *it's of no use whatsoever* and describes his work was *just an experiment that proves Maestro Maxwell was right*. As Hertz stated, *we just have these mysterious electromagnetic waves that we cannot see with the*

Figure 1.4 Thomas Edison debuted the first incandescent lightbulb on 21 October 1897, which burned for about 13 hours. (Courtesy of ThoughtCo.)

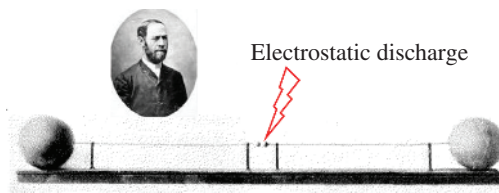
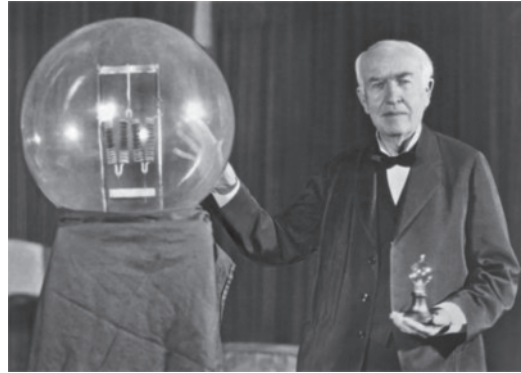


Figure 1.5 Hertz's first spark-gap radio transmitter, which can be called an ESD discharging device, is a capacitor-type dipole resonator comprising a pair of 1-m copper wires separated by a spark gap of about 7.5 mm. When a high voltage is applied through an inductor coil, the spark gap fires up the air and generates standing waves of roughly 50 MHz. (Heinrich Rudolf Hertz/Wikipedia Commons/Public domain.)

naked eye, but they are there, his experiments proved that the airborne electromagnetic waves, initially called Hertzian waves and later named radio waves, exist as predicted by Maxwell.

1.2 ESD and the Dangers

While Hertz's spark-gap transmitter may be regarded as an original ESD discharging device that is *useful*, the ESD phenomena that we are concerned about today are more *harmful* than *useful*, which is the topic of this book.

Electric charge is a fundamental physical property of a matter, which makes it feel a force in an electromagnetic field. There are two types of electric charges. Per Franklin's convention, the electric charges gained by a glass rod rubbing a silk cloth are positive charges (vitreous), while the electric charges obtained by a piece of amber rubbed by a piece of fur are negative charges (resinous). Charge is quantized, meaning a charge carrier can only contain integer number of elementary charges. The SI unit for charge is Coulomb. An elementary charge (denoted as e) is indivisible. Elementary charge is a fundamental physical constant given as $e = 1.602\,176\,634 \times 10^{-19}$ C exactly [5]. One electron has one charge of $-e$.

Electric charge experiences a *force* through an electrostatic field. In modern physics, there exist four fundamental forces: weak force, strong force, electromagnetic force, and gravitational force. Weak force and strong force apply in "short" distance (microscale), while electromagnetic and gravitational forces act in "long" distance (macroscale). These fundamental forces, also referred to as fundamental interactions, can be mathematically described as a field. Electromagnetic force has two components: the electrostatic force that applies to electrically charged particles at rest, and the

combined electric and magnetic forces that act on charged particles in motion. Due to the electrostatic force, *like* charges repel each other, while *unlike* charges attract each other. The electrostatic force acting on charges follows the Coulomb's Law as depicted below



$$F = \kappa \frac{Q_1 Q_2}{r} \quad (1.1)$$

where F is the Coulomb's Force, Q_1 and Q_2 are the amount of electrostatic charges contained by the two charge-carrying objects involved, r is the distance in between, and κ is a constant. Therefore, it requires certain amount of energy, defined as *work*, to move a charge in an electric field, which is characterized by the electrostatic potential at related points in the electric field.

Electrostatic charges are created when two objects, at least one of them has to be an electrical insulator or of high electrical resistivity in nature, are brought into contact and then separate from each other. Static electricity reflects an imbalance of electric charges (net positive or negative) inside a charged object. In physics, an isolated system follows the Law of Conservation of Charge, which states that the net charges, the difference of positive and negative charges, are preserved in the universe. Charge conservation does not prohibit static charges from being generated or destroyed. But any gain in charges somewhere at a time will accompany with the loss of the same amount of charges somewhere else. Static charges are associated with electric *charging* and *discharging* for an object. Electric charging puts static charges into an object, while electric discharging removes static charges from an object. Electric charging and discharging are two opposite phenomena associated with static charges, which involve separation and neutralization of positive and negative charges of materials. Electric charging leads to static electricity. Static charge generation requires separation of positive and negative charges through electric charging procedure. Normally, materials are electrically neutral because the atoms have same number of positive and negative charges. When two objects are in contact, electrons may move in between, which causes imbalance of positive or negative charges within each object. Then, when the two objects are separated thereafter, they may retain the charge imbalance, i.e., containing net positive or negative charges. This completes a charging procedure. Therefore, the static electricity phenomena involve contact and separation of materials. There are many electric charging mechanisms. The most common electrostatic charging phenomena observed in our daily life is the *triboelectricity* phenomena, which follow a contact-induced charge separation mechanism. When two objects with different electrical resistivity are in contact, electrons will exchange in between due to different binding force. Upon separation of the two objects, each object will be electrically charged containing either net positive or negative charges. Many magic and fun static electricity phenomena observed in our life follow the contact-induced charge separation procedure. For example, amber rubbed by fur can attract leaves; a plastic comb combing through hair can attract paper scraps; or you feel your hair raising when taking off a hat in a dry day. The triboelectric effect is considered to be related to the materials adhesion phenomenon and dominated by the atomic-scale electron transfer mechanism [6]. Triboelectric effect is generally unpredictable and depends heavily on many factors, such as materials, surfaces, temperature, pressure, and humidity. The Triboelectric series, as given in Table 1.1, is a reference for the tendency of contact-induced electrostatic charge generation based upon the materials properties. Different materials are friendly to either positive or negative charges at varying levels. The farther apart the two involved materials in the Triboelectric series table, the stronger the triboelectric effect, i.e., the easier the two materials will exchange charges. Materials very close to each other may not exchange charges, i.e., triboelectrification may not occur. Figure 1.6 presents a quantified Triboelectric series [7].

Charge-induced charge separation is another electrostatic charging phenomenon commonly observed also referred to as *electrostatic induction*. In an electrically neutral materials, it has equal

Table 1.1 Triboelectric series.

Materials	Most Positive (+)
Air	
Human hands. skin	
Asbestos	
Rabbit fur	
Glass	
Human hair	
Mica	
Nylon	
Wool	
Lead	
Cat fur	
Silk	
Aluminum	
Paper	
Cotton.	
Steel	
Wood	
Lucite	
Sealing wax	
Amber	
Rubber balloon	
Hard rubber	
Mylar	0
Nickel	
Copper	
Silver	
UV resist	
Brass	
Synthetic rubber	
Gold, platinum	
Sulfur	
Acetate, rayon	
Polyester	
Celluloid	
Polystyrene	
Orion, acrylic	
Cellophane tape	
Polyvinylidene chloride (Saran)	
Polyurethane	
Polyethylene	
Polypropylene	
Polyvinylchloride (Vinyl)	
Kel-F (PCTFE)	
Silicon	
Teflon	
Silicone rubber	
	Most negative (-)

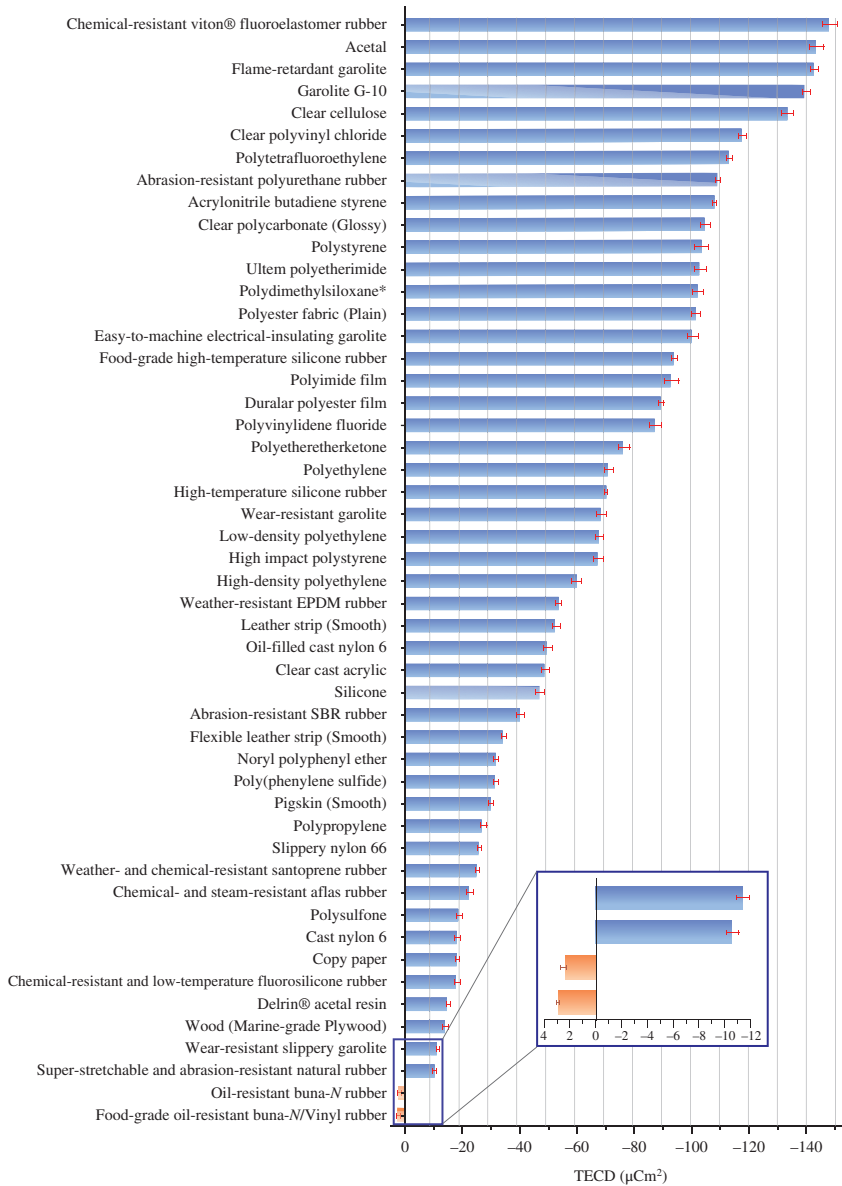


Figure 1.6 The quantified triboelectric series. The error bar indicates the range within a standard deviation. (Zou et al. [7]. Licensed under CC BY 4.0.)

amount of positive and negative charges in it with the electrons carry the negative charges and atomic nuclei hold the positive charges. Since the positive and negative charges are very close to each other in the microatomic scale, the neutral materials do not have locally lumped net charges, therefore, people do not get electric shock when touching an uncharged object in our daily life. In a conductor, like metal, electrons are “free” to move around, while in an insulator, such as

amber, electrons are “bound” locally, so they cannot move freely. This makes electrostatic charging very different for conductors and nonconductors. In the scenario involving conductive materials, such as metal rods, if a charged object A, assuming positive, is placed near an electrically neutral conductor B, for example a copper rod without net charge, the electric field generated by the positive charges of A will act on the free electrons in B per the Coulomb’s Law. Some free electrons in object B will be attracted to the end closer to object A, effectively leaving positive charges on the far end of the copper rod. Hence, redistribution of electric charges inside the object B occurs. If the copper rod is then grounded, the positive charges on the far end of the copper rod will flow into the ground, leaving the object B negatively charged with net electrons. In the scenario involving nonconductive materials, i.e., dielectric objects such as glass, amber, or rubber, the charge separation procedure is different. Assume a positive-charged object A is placed close to an electrically neutral glass rod B, the electric field produced by the positive charges of A will be experienced by the charges in object B. However, since the electrons inside the dielectric object are not free and bound to atoms or molecules locally, the electrons cannot move to the end close to the object A. Instead, in microscale of a molecule, electrons are attracted closer to the object A, while the positive nuclei are repelled to farther from the object A. This is called *polarization*, which results in electrical *dipoles* at atomic or molecular level. Hence, charge separation or dielectric polarization occurs for the glass rod as governed by the Coulomb’s Law. Many everyday electrostatic magics can be explained by the dielectric polarization effect. For example, moving a silk-rubbed glass bar to close to small paper scraps, polarization occurs for the paper scraps where tons of molecular dipoles are created within the paper scraps with the bound electrons being closer to the glass bar. Collectively, the electrostatic force from the positive-charged glass bar will be able to attract these small lightweight paper scraps per the Coulomb’s Law. Other induction-based charge separation mechanisms are pressure induction and heat induction. In pressure-induced charge separation, the mechanical stress applied to certain materials will separate positive and negative charges of the materials, which is referred to as piezoelectric effect or *piezoelectricity*. Piezoelectric effect exists in certain crystals and ceramics, such as quartz and zinc oxide (ZnO). Heat-induced charge separation is also called pyroelectric effect or *pyroelectricity*. For certain materials, temperature variation, being heated or cooled, will cause polarization of charges in microscale. The widely used pyroelectric materials are gallium nitride (GaN).

The opposite of static charge generation is the removal (or, *neutralization*) of static charge. Correspondingly, there are electrostatic charging (or static charging) and electrostatic discharging (or static discharging) procedures. With typical electrostatic charging phenomena, through charge separation, explained, let us understand the opposite phenomena – electrostatic discharging, or broadly called ESD. *ESD is a charge neutralization procedure*. In principle, when two objects with different electrostatic potentials are brought into close proximity, either in direct contact or having a small gap in between, transfer of electrostatic charges between the two objects occurs. This process is broadly called ESD. In general, ESD phenomenon is a sudden flow of electric current with a short duration between two differently charged objects. Triggering of ESD discharging may be direct contact of the two objects or dielectric breakdown in between in case of a small gap (air or other dielectrics) separating the two objects. The most common and dangerous everyday ESD discharging phenomenon is *lightning*. In natural atmosphere, electrostatic charges can accumulate in thunderstorm clouds, which may be neutralized between two clouds of different electrostatic potentials, or, from a cloud to the ground, resulting in a sudden transfer of static charges with an

instantaneous release of energy of gigajoule scale. The air breakdown voltage causing lightning is around 10 000 V/cm (10 kV/cm) [8]. The lightning will zap-heat the air leading to light emission through incandescence, producing a flash, and shock waves of radiation, generating thunders. More commonly and often the fun side, an ESD phenomenon is accompanied by a spectacular spark, which is triggered by abrupt air breakdown at an electric field density exceeding around 4–30 kV/cm, making the air electrical conducting in a sudden. However, most ESD phenomena are invisible to human eyes. While everyday ESD phenomena may typically cause discomfort to human only, such as feeling an electric shock when opening a car door, ESD discharging can pose serious dangers to the industry, causing life hazards in certain environments. For example, movement of fine powders (e.g., granulated grain in a grain silo) and dust clouds in manufacturing plants or flowing of flammable liquids (e.g., gasoline and crude oils) in pipelines can accumulate electrostatic charges, which may be ignited by a tiny ESD spark, causing explosion.

On the other hand, ESD phenomena are extremely harmful to electronic components, particularly for semiconductor ICs [9], which is the concern of this book. The ESD failure problem became a real concern since World War II when highly insulating polymeric materials started to find widespread usage. Electrostatic charges can be easily generated and accumulated in those insulating materials and ESD discharge may shut down machinery in manufacturing plants, causing ESD damages and losses. Yet it was the birth and prosperity of the modern semiconductor microelectronics industry that made people realize the seriousness of ESD failures to the microelectronics industry, the economy, and the society. The invisible ESD phenomena, with a transient level lower than 1000 V, or even as low as 10 V, can cause ESD failures to modern electronics. In the past 70+ years, the microelectronics industry has gained unprecedented successes, which has entirely changed the human life. Germanium (Ge) transistor was invented at the Bell Lab in 1947 [10], which broke the dawn of the microelectronics era. ICs in Germanium and Silicon (Si) were invented in 1958 and 1959, respectively [11, 12]. Si complementary metal-oxide-semiconductor (CMOS) IC technology was invented in 1963 [13]. For more than seven decades, semiconductor IC technologies have been continuously advancing at the pace of the Moore's Law [14]. *Performance* and *Reliability* are the two key aspects for ICs. ESD failure is a main part of IC reliability problems. Every piece of IC may be subjected to ESD failure during its life cycle. As the IC technology reaches to 5 nm node for mass production today, ESD failure is becoming much more serious to the micro/nanoelectronics industry. This is due to the fact that the natural ESD phenomena remain the same as time flies, regardless worse global warming, better ESD awareness, and stricter ESD control measures; while CMOS technology scaling makes tiny ICs more susceptible to ESD transients of the same scale or even lower level. In other word, the ESD phenomena never shrank as the IC technologies have been going through for decades. In fact, as consumer electronics become dominant today, such as smartphones, tablets, and wearable devices, the ESD risks are getting much higher simply because people are touching tiny electronic devices every second. It is obvious that the ESD failure is becoming much bigger an IC reliability concern and challenge today than ever before. Industrial data suggest that up to 30% of all IC field failures are somewhat associated with ESD events of all kinds, which costs the microelectronics industry billions of US dollars in revenue losses annually. ESD failures can be either catastrophic (*hard* ESD failure) or latent (*soft* ESD failure) in nature. Hard ESD failures cause outright damages to ICs, showing immediate IC malfunction or burn out. Soft ESD failures may cause undetectable deterioration of IC performance and future malfunction within the life cycle, i.e., a lifetime issue. In principle, ESD failures are attributed to either high energy associated with large ESD current transients, which causes thermal damages to semiconductors and metal interconnects, or high electric field density associated with large ESD voltage transients, which may breakdown the IC materials,

such as a CMOS gate oxide. Therefore, regardless of the origins and phenomena of ESD failures, effective protective measures are needed to protect ICs against ESD failures, which is the topic of this book.

1.3 ESD Protection: The Principles

Obviously, the ESD dangers to semiconductors and ICs are anywhere anytime during the entire lifespan of any microelectronics product, including manufacturing, packaging, shipping, installment to field applications. The ESD risks are unavoidable to ICs because, first of all, electrostatic charge generation occurs any moment during the processes of handling ICs. For example, in typical microelectronics manufacturing settings, as an engineer walks across a floor, triboelectric generation can readily produce static electricity reaching to anywhere from 800 V on a rubber floor to 35 000 V on a carpet. Therefore, it is a no-brainer that one can never decorate an electronic workshop with any fancy carpet as in your bedroom. Sliding electronic devices out of a container can generate triboelectricity easily from 2000 V (plastic tube) to 14 500 V (foam). Relative humidity has strong impact on triboelectricity generation. Lower relative humidity increases triboelectricity. Higher humidity reduces static charging because a thin moisture film on a surface helps to dissipate static charges. Humidity control is therefore important for ESD prevention. Table 1.2 summarizes typical triboelectric charge generation in common workplaces.

Practically, it is impossible to imagine a life without any static electricity. The ESD experience, good or bad, is really an integral part of our everyday life. Therefore, the ESD consequences should never be overlooked. In the industry, electronic devices that are sensitive to ESD failure are called *electrostatic discharge sensitive (ESDS) device*, often being referred to as *ESDS* devices. The survivability of ESDS devices against ESD failures is a property referred to as the *ESD sensitivity* in the field. Since ESD phenomena always exist, which can damage electronic products including ICs, proper ESD protective measures must be used for electronics, called *ESD protection*. In the real world, the counter-ESD measures can be roughly classified as *ESD Prevention* and *ESD Protection*. The rationale for ESD prevention is to eliminate, more practically, to minimize, as much as possible, electrostatic charge generation, i.e., preventing static electricity from occurring in the first place. ESD prevention includes several measures. First, different materials have different sensitivity to the charge separation and generation processes. Certain materials are extremely sensitive to the triboelectric effect. Hence, it is a good idea to select the materials that are insensitive to static electricity, e.g., per the Triboelectric Series, to make the products “immune” to static electricity. Such a principle is fundamental because it would prevent generation of electrostatic charges, hence, no further ESD issues to worry about. However, this is practically not much of a solution because choice of ESD-insensitive materials for given products and applications are not much at all in the first place. Materials selection may be easier for certain applications, for example better using anti-static floor instead of carpet in a workplace. However, for the semiconductor industry, silicon is the main materials to use and we have to deal with it, anyway, in terms of static charge generation. Second, proper ESD control measures should be established in workplaces and at user ends to eliminate, or more practically, to reduce static charge generation and accumulation in products. A good *ESD Control (Static Control)* program has many principles and measures to follow. *Grounding* and *Neutralization* are important concepts for ESD Control. Grounding means to connect all concerned items, including devices, equipment, and personnel, to the same electrical potential level within a working or usage space. Equalizing electrical potential prevents static charge generation and accumulation. Neutralization is a process where excess positive or negative static charges on an object

Table 1.2 Common triboelectric generation at varying humidity related to ICs.

Occurrences	Electrostatic potential at relative humidity (R.H.)	
	10%	55%
Walking across rubber floor	800 V	200 V
Removing DIP devices from plastics	2 000 V	400 V
Moving on bench	6 000 V	400 V
Removing DIP devices from vinyl tray	11 500 V	2 000 V
Walking across vinyl floor	12 000 V	3 000 V
Removing DIP devices from polystyrene foam	14 500 V	3 500 V
Removing PWB parts from bubble wrap	26 000 V	5 500 V
Walking across carpet	35 000 V	7 500 V

DIP, dual-in-line package; PWB, printed wire board.

will be removed through cancellation with the same amount of static charges of opposite polarity. Many specific ESD control means have been widely used in the industry. Wrist and/or ankle straps are commonly used personnel grounding tools, which remove excess static charges from a human body before touching an ESDS item, hence avoiding ESD failures to ESDS devices. ESD protective flooring is extremely critical to preventing static-charging electronic products, such as in IC foundry cleanroom facilities, testing lines, and packaging and assembly plants. In workplaces, an *ESD protected area* (EPA) must be established, which can be a small workstation or workspace, or a large manufacturing floor, where ESD grounding is properly set. EPA area uses static-insensitive materials to prevent static charge generation, and grounded conductive and dissipative materials to avoid static charge accumulation. Figure 1.7 depicts a typical EPA-enabled workstation where everything is connected to the *ESD Common Point Ground*, which is connected to the system/universal ground [15, 16]. Another important ESD control measure is to promote ESD awareness by widely using *ESD Awareness Symbols*. Figure 1.8 shows three commonly used ESD awareness symbols suggested by the EOS/ESD association [16, 17]. The ESD common point ground symbol (Figure 1.8a) indicates the grounding point to ground everything in an EPA area to ensure equal electrical potential, hence, preventing static charge generation. The ESD susceptibility symbol (Figure 1.8b) is used to clearly identify an ESDS item, which must be handled with ESD caution. This symbol basically says “ESD sensitive, do not touch!” The ESD protective symbol (Figure 1.8c) is used to indicate that proper ESD prevention and protection measures are provided to workplaces, tools, and devices. The basic philosophy for ESD prevention may be understood as follows: No Charges – No Discharge. Nevertheless, while various ESD prevention methods can significantly reduce the potential of ESD problems, ESD prevention itself cannot completely eliminate all ESD dangers. ESD protection is therefore required for all electronics. Broadly, ESD protection for anything, not limited to ICs, has a long history and many formats. Back to the fifteenth century, military entities in Europe started to use various ESD protection methods to safely handle munitions. The lightning rod invented by

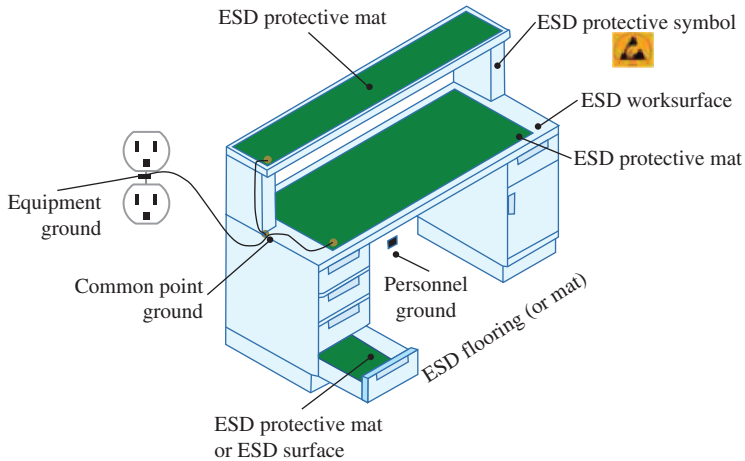


Figure 1.7 Illustration of a typical ESD workstation providing an EPA area. (Reprinted with permission from EOS/ESD Association, Inc.; www.esda.org.)

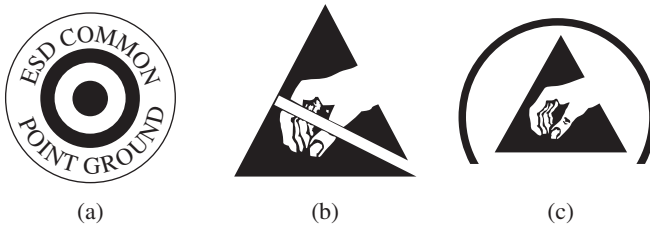


Figure 1.8 Commonly used ESD awareness symbols: (a) ESD common point ground symbol, (b) ESD susceptibility symbol, and (c) ESD protective symbol. (Reprinted with permission from EOS/ESD Association, Inc.; www.esda.org.)

Franklin is still in use for all buildings and high-rises today (Figure 1.9). Precipitation static dischargers are installed on the trailing edges of aircraft to safely discharge the accumulated static electricity into surrounding air as an aircraft flies through rain or snow. Dryer sheets are commonly used in a cloth dryer to prevent and dissipate static charges. For electronics, ESD protection can be at materials, IC, packaging, printed circuit board (PCB), and system levels often in a combination to guarantee ESD safety as much as possible. For example, ESD dissipative materials, high-resistive conducting materials, may be applied to IC packaging to slowly and safely dissipate any static charges accumulated without causing charged device model (CDM) type ESD failures. Standalone ESD protection devices are widely used at system board level for electronic products, e.g., smartphones, which are called *transient voltage suppressors* (TVS). Nevertheless, on-chip ESD protection is always required for ICs, as long as not prohibited by extreme IC performance specifications (Specs). Obviously, one cannot add a lightning rod on an IC chip for ESD protection. ESD phenomena relevant to semiconductors and ICs are unique in that the ESD transients are extremely

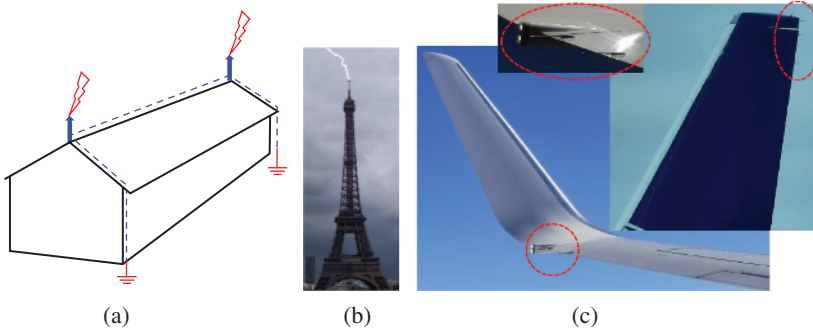


Figure 1.9 ESD protection in real life: (a) a house has a lightning rod system, (b) Eiffel Tower has a lightning rod on the top, and (c) static dischargers (static wicks) are installed at trailing edges of commercial aircraft to protect onboard electronics.

short, typically about 150 ns or less, yet they can easily generate transient current and voltage surges up to a few tens of amperes (A) and kilovolts (kV). Therefore, on-chip ESD protection designs for ICs are unique and challenging. The ESD protection performance, also called *ESD robustness*, for ESD-protected chips is typically evaluated by the *ESD failure threshold voltage* of ICs, normally in units of volts or kilovolts (kV) and referred to as *ESD failure threshold voltage (ESDV)*. To characterize ICs for ESD robustness, i.e., ESDV specs that are given in the product datasheet of an IC, ESD measurements are conducted for the chips, also referred to as the *devices under test (DUT)*, which involves applying ESD transient waveforms to the DUT devices, an ESD testing procedure called *ESD zapping*. From the early days all the way to today, diodes, in both forward and reverse conducting fashions (i.e., Zener diodes), have been widely used for on-chip ESD protection for ICs [9]. Over the past seven decades, as semiconductor technologies continuously advance and IC reliability requirements constantly increase, various ESD protection structures have been developed, such as bipolar junction transistor (BJT) ESD protection devices, metal-oxide-semiconductor field-effect transistor (MOSFET) ESD protection devices and silicon controlled rectifier (SCR) ESD protection structures, and their derivatives of all kinds. Various ESD sub-circuits have also been developed for advanced ESD protection for mixed-signal ICs and system-on-a-chip (SoC) chips. As IC technologies rapidly advance from micrometer nodes to nanometer nodes, novel ESD protection structures have been developed to address the emerging design challenges, such as very large-scale integration (VLSI) chips, high-speed and high-throughput mixed-signal ICs, and high-frequency and broadband RF ICs. Notable design examples include dual-directional and multiple-mode SCR ESD protection structures, diode-triggered silicon controlled rectifier (DTSCR) ESD protection structures, and ultralow parasitic ESD protection structures [18–21]. Particularly, the complex interactions between ESD protection structures and the core circuits under ESD protection have been intensively studied that led to novel ESD-IC codesign techniques [22]. Parallely, high-triggering-voltage and latch-up-immune ESD protection structures have been developed for high-voltage, high-power ICs. Critically, ESD protection design philosophy has gradually shifted from device-centric ESD protection designs to full-chip-oriented ESD protection designs [22, 23]. Over decades since 1960s, the field of on-chip ESD protection has never been settled, and today, ESD protection research is becoming more and more active.

1.4 ESD Protection: More or Less?

From the previous discussions, it is clear that ESD is everyday phenomenon that nobody can avoid. On-chip ESD protection is therefore required for all ICs. Practically, the strategy for developing ESD protection solutions has two aspects to consider: Science and Marketing. First, there are obviously scientific and technical needs of ESD protection for electronics. On the one hand, it is straightforward that engineers must understand the scientific fundamentals of ESD phenomena and ESD protection mechanisms including the WHYs and HOWs. ESD events involve fast and large current and voltage transients, when applied to electronics, causing unbearable internal heating and electric field stressing that result in thermal failures and/or dielectric breakdown. Therefore, on-chip ESD protection is required to provide a low-resistance (low- R) conducting path to discharge the electrostatic charges without overheating and/or electric field over-stressing to ICs. For a given ESD transient, the ESD energy is there, which must be discharged safely into the ground without overheating ICs. Similarly, the substantial electric field induced by an ESD surge must be defused safely through low-resistive conduction. Therefore, there are clearly hard-core science and technical concerns for on-chip ESD protection. On the other hand, any product designs must consider economic impacts, marketing competition, and consumer psychology. Electronic products are made to sell. If any key function does not “look” good or makes customers “feel” better and “worth” the dollars compared to competitive alternatives on the market, your products cannot be sold. Also, time-to-market is an important consideration for new IC product development today. At the time when averaging costs reached to one hundred million U.S. dollars and beyond in developing a new smartphone SoC chip at 10 nm node, a possible ESD failure, quite often in IC designs, will require lengthy and painful debug and redesign efforts, hence, seriously delaying new product release and missing the narrow market window. It would not only result in significant revenue losses but also put the fate of a company in jeopardy. The above discussions naturally lead to typical engineering questions: for ESD protection designs, how high is too high, how low is too low, and what is adequate? In deciding on *More* or *Less* for ESD protection, the following factors should be considered on a big picture as a good ESD protection design strategy. First, one has to meet the basic ESD protection target, for example 2 kV human body model (HBM) ESD protection is commonly accepted as a basis bar for most ICs. Without providing adequate ESD protection, your ICs may not be sold well, or, even if being sold, you may expect substantial field returns from the customers later. Second, more ESD protection is better only IF it would not adversely affect the IC specs. There are many negative impacts of ESD protection on ICs: Almost all ESD protection are based on PN junctions, which inherently introduce parasitic capacitance, leakage, and noises. These ESD-induced parasitic effects can seriously affect performance of core IC under ESD protection. ESD protection structures also take substantial die area on a chip. ESD protection device layout is often irregular. Hence, overall, more ESD protection using a given ESD structure type means more negative impacts on IC performance and chip density. Particularly, the ESD-induced parasitic effects may have deadly impacts on high-speed, high-through, high-frequency, and broadband ICs, for example, >10 Gbps or >10 GHz. Consequently, you often see much lower ESD protection for high-data-rate I/O pads of high-speed datalink chips or high-frequency pins of RF ICs. Third, one must balance the needs for core IC performance and ESD robustness by excising thorough ESD-IC co-design in order to simultaneously achieve both IC specs and ESD protection. Careful IC-ESD

design trade-off is critical in practical designs. Fourth, IC designers should always keep the customer's needs in mind and consider the marketing. Given similar or little better IC specs, higher ESD protection would offer your IC products a critical advantage over competitors on the market. The common user psychology is to buy better things using same dollars, and ESD protection is a considering factor when consumers shop for ICs. Keep in mind that what you think about ESD protection as a product designer is much less important compared to what the customers think they would want for ESD protection. To this end, there is often no rocket science for ESD protection. System vendors and end users want a peace in mind in terms of reliability. In recent years, as IC technologies advanced into sub-28 nm nodes, and IC performance and chip complexity continuously increased, ESD protection for advanced ICs becomes extremely challenging. One key reason is that ESD protection never followed the Moore's Law to shrink in sizes. The negative factors for ESD protection, including ESD-induced parasitic effects, ESD layout, and size issues (collectively called *ESD-induced design overhead*), make it extremely difficult to maintain the usual ESD protection targets for advanced CMOS ICs. Accordingly, an industrial ESD workgroup of ESD engineers, "the Industry Council on ESD Target Levels," was established in 2006 with a mission "to review the ESD robustness requirements of modern IC products for allowing safe handling and mounting in an *ESD protected area*." The Industrial Council recognized that the current industry ESD qualification target levels are "unsupportable" and released several White Papers to recommend "suitable" (lower) ESD target levels [24–27]. The White Paper believes that the common ESD targets are unnecessary on manufacturing sites with basic ESD control management, for example the common 2 kV ESD target in HBM ESD protection is too high because 500 V would be ESD safe. Hence, it recommends significant reduction of ESD qualification target level to 1 kV HBM (down from the common target of 2 kV) [24] and 250 V CDM (down from commonly 500 V) for modern ICs [25]. The key rationale of the White Papers is that ESD "awareness" is common now and ESD "control" is comprehensive in manufacturing sites today, hence, the ESD danger is much "lower." The White Papers further promote ESD protection at system board level as an alternative solution to the "unsupportable" on-chip ESD protection requirements [26, 27]. However, one must never forget that any ICs are to be used by the customers, being system vendors to make electronic products including smartphones and touch pads, and the consumers who use smartphones or wear smart watches. For the everyday consumers in a real world, the ESD phenomena stay the *same* today compared to ten years ago, hence, the ESD dangers never shrank today. Further, consumer electronics are more touch-based today that essentially increases the likelihood and level of ESD dangers, while the advanced IC technologies are much more vulnerable at 7 nm node compared to at 180 nm node. Also, since the new product development costs increase exponentially for today's microelectronics products, e.g., iPhones and Tesla cars, hence, the system vendors actually require extra ESD protection at both IC and board levels to minimize return losses from customers. Asking the system vendors to increase system-level ESD protection while dramatically reducing on-chip ESD protection will not fly. Therefore, regardless of what perfect and strict ESD control program are in place on manufacturing sites, never imagine to ask the consumers (e.g., grandparents) in the street to think about ESD control before using a smartphone. This is a classic example to argue that IC designers must keep the end-users in minds in terms of ESD protection designs when designing IC products. Product designers and manufacturers must take care of the product reliability and not try to shift the reliability burden to users. It is indeed that ESD protection design is becoming more and more challenging for advanced IC technologies. It is important to keep up the research and development efforts to continuously explore novel and transformative ESD protection solutions for advanced IC technologies.

1.5 ESD Protection: Evolution to Revolution

The previous discussions cover a long and interesting history of ESD research and development spanning around seven decades and the preceding section clearly states the needs for novel ESD protection solutions for advanced IC technologies. Since 1970s, significant R&D efforts have been devoted to continuously improve ESD protection for ICs, from simple PN junction diodes to more sophisticated gated and shallow trench isolation (STI) diode ESD protection structures in advanced technologies; from ESD diodes to BJT and MOSFET ESD protection structures; from single diode to diode-string ESD protection structures for less ESD-induced parasitic capacitance; from grounded-gate MOSFET (ggMOS) to gate-coupled MOS (gcMOS) for lower triggering voltage; from single-device to subcircuits for ESD triggering assistance; from single-finger ESD device to multiple-finger ESD protection structures for improved ESD discharging uniformity; from MOSFET ESD to SCR ESD structures for high-voltage ICs; from regular SCR to DTSCR for lower ESD-induced parasitic capacitance and lower ESD triggering voltage; from single-stage ESD structure to two-stage ESD protection for improved CDM ESD protection; and so on. ESD protection design principles gradually shifted from device-centric individual/standalone ESD protection structure designs to circuit-oriented full-chip ESD protection designs. ESD design practices have been evolving from experience-based trial-and-error design, to CAD-based ESD protection design for design optimization and predication, and to full-chip ESD protection circuit design verification by CAD. ESD protection design goal also changes from focusing on ESD protection level to balancing both ESD protection and core IC performance for advanced ICs. On the other hand, almost all-traditional ESD protection structures rely on PN junction-based structures for ESD discharging, except for a few inductor-based ESD protection subcircuits that are inherently narrow band in nature. As IC technologies march into sub-10 nm regime, the traditional PN junction-based ESD structures have fundamental disadvantages. For example, the ESD-induced parasitic effects, including ESD-induced parasitic capacitance (C_{ESD}), leakages (I_{leak}), and noises, are quickly becoming relatively more significant and unbearable to high-performance ICs. In the meantime, complete whole-chip ESD protection requires too many ESD protection structures that are consuming relatively too much Si area for complex ICs with hundreds to thousands of pads. Further, simply imagine future chips comprising non-CMOS non-Si devices, such as various nano devices, micro/nano-electromechanical systems (MEMS/NEMS) devices, bioinspired devices, etc., it is naturally to expect that the traditional inside-Si PN-junction-based ESD structures will not be acceptable for future chips. Hence, it is important to think abnormally about ESD protection and imperative to explore truly disruptive ESD protection methods, from ESD protection mechanisms to structures. For example, a backend-based above-IC graphene-based mechanical switch structure concept and graphene-based ESD interconnects were reported, which are fundamentally different from any traditional in-Si PN-based ESD protection solutions [28, 29]. In other words, ESD protection designs have been advancing since 1970s, yet the progresses have been incremental and evolutionary so far. Revolution in on-chip ESD protection is needed for future chips.

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