1

Modular Multilevel Converters

1.1 Introduction

Power converters have been widely used in electric power conversion systems that can convert electric power with high conversion efficiency and economic benefits. In the past few decades, several power converters have been developed and commercialized in the industrial community. They can be classified into current source converters (CSCs) and voltage source converters (VSCs).

The modular multilevel converter (MMC), as a kind of VSC, has been considered one of the most promising converters for medium/high-voltage and high-power applications, with the superiority such as excellent output power quality, high efficiency, modularity, and scalability [1–3]. Compared with traditional two-level and multilevel converters, the MMC has prominent advantages such as high efficiency and low power losses. What is more, high modularity enables the MMC to easily expand capacity. Recently, the MMC has become attractive for high-voltage direct-current (HVDC) transmission [4], renewable energy generation [5], electric railway supplies [6], micro power grid [7], etc.

This chapter deals with the fundamental principles of the MMC. The configuration of the MMC is presented in Section 1.2. Section 1.2 gives an introduction of the converter configuration and the submodule (SM) configuration. The operation principles of the SM and the converter are shown in Section 1.3. Section 1.4 demonstrates the modulation schemes, including phase-disposition (PD) pulse width modulation (PWM), phase-shifted (PS) PWM, and nearest level modulation (NLM). Afterward, mathematical models of the SM, the arm, and the MMC are introduced in Section 1.5. Then, Section 1.6 introduces the parameter design methods of power devices, capacitor, and arm inductor in the MMC. An overview of the MMC faults is given in Section 1.7.

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Fujin Deng, Chengkai Liu, and Zhe Chen.

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1.2 MMC Configuration

1.2.1 Converter Configuration

A three-phase MMC topology is shown in Figure 1.1, which consists of three phase-legs, each composed of an upper arm and a lower arm. Each arm contains n identical SMs and an arm inductor L_s. The upper and lower arm currents are i_{ju} and i_{jl}, respectively, in phase j ($j = a, b, c$). The AC side of the MMC is equipped with the filter inductor L_f. The MMC links the DC side and the three-phase AC side. Electric power can flow from the DC side to the AC side or from the AC side to the DC side through changing the operation mode of the MMC. The number of SMs can affect the output voltage level and thus power quality. A multilevel voltage would be synthesized at the AC side of the MMC, and output harmonic contents would be reduced with the cascading of SMs [8].

1.2.2 Submodule Configuration

The SM unit is the fundamental component of the MMC. Figure 1.2 shows the typical half-bridge (HB) SM configuration, which is widely used in power

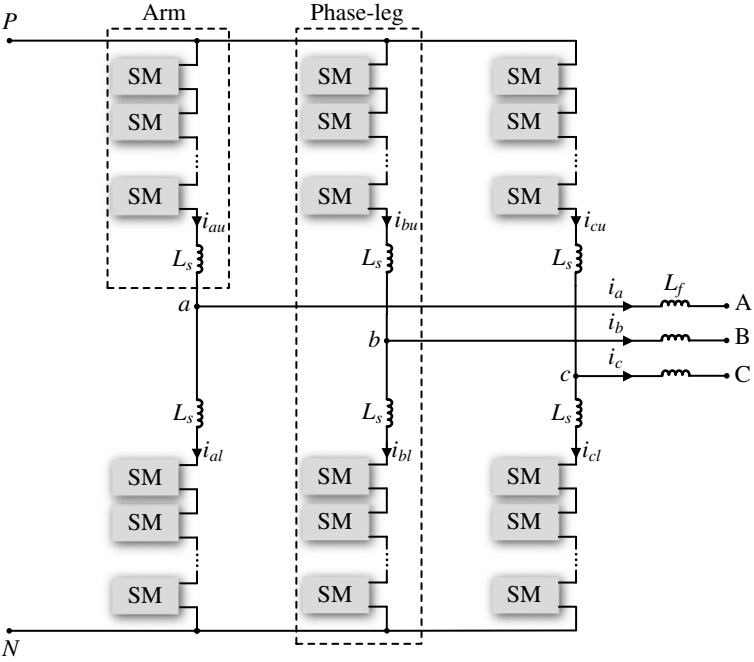
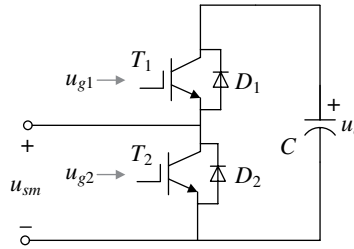


Figure 1.1 Three-phase MMC configuration.

Figure 1.2 Half-bridge SM.



applications. The HB SM consists of two switches/diodes T_1/D_1 and T_2/D_2 and a DC capacitor C. Through the switching of the power switches T_1 and T_2, the HB SM can output two voltage levels, including the capacitor voltage u_c and 0 [8].

1.3 Operation Principles

1.3.1 Submodule Normal Operation

In the normal operation of the MMC, the operation state of the SM is controlled by the switching function S, which is defined as

$$S = \begin{cases} 1, & u_{g1} \text{ is high-level and } u_{g2} \text{ is low-level} \\ 0, & u_{g1} \text{ is low-level and } u_{g2} \text{ is high-level} \end{cases} \tag{1.1}$$

where u_{g1} and u_{g2} are the drive voltages of switches T_1 and T_2, respectively, as shown in Figure 1.2. The switching modes of the HB SM are listed in Table 1.1.

- The T is turned on when the u_g is high-level
- The T is turned off when the u_g is low-level.

The relationship between the SM's output voltage u_{sm} and the SM's capacitor voltage u_c is

$$u_{sm} = S \cdot u_c \tag{1.2}$$

The normal operation of the HB SM has four operation modes, as shown in Table 1.2 and Figure 1.3, which are decided by the switching function S and the direction of the arm current i_{arm}, as follows:

Table 1.1 Switching modes of the HB SM.

S	u_{g1}	u_{g2}	T_1	T_2
1	High-level	Low-level	On	Off
0	Low-level	High-level	Off	On

Table 1.2 Four normal operation modes of the HB SM.

Mode	S	i_{arm}	Circuit state	SM state	T_1	T_2	u_{sm}	C	u_c
1	1	>0	Inserted	On	On	Off	u_c	Charged	Increased
2		<0	Inserted	On	On	Off	u_c	Discharged	Reduced
3	0	>0	Bypassed	Off	Off	On	0	Bypassed	Unchanged
4		<0	Bypassed	Off	Off	On	0	Bypassed	Unchanged

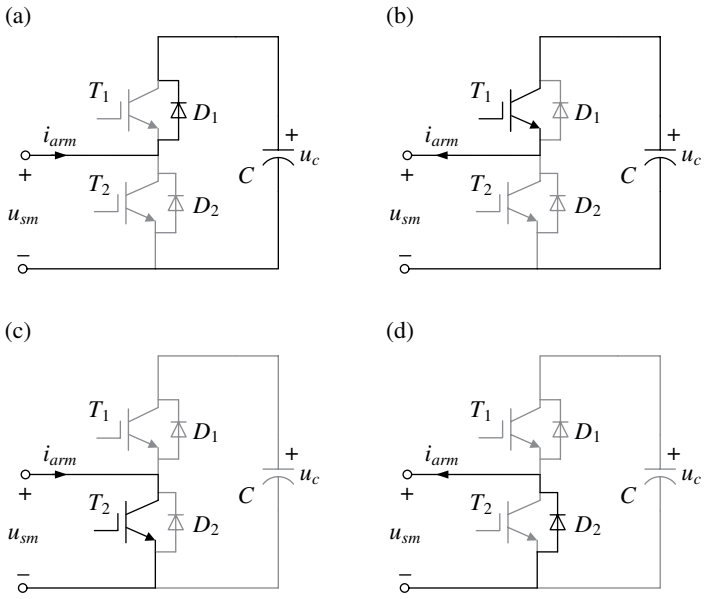


Figure 1.3 Four normal operation modes of the HB SM. (a) Mode 1 (normal operation). (b) Mode 2 (normal operation). (c) Mode 3 (normal operation). (d) Mode 4 (normal operation).

- *Mode 1 (normal operation)*: When $S = 1$ and $i_{arm} > 0$, as shown in Figure 1.3a, the T_1 is turned on, the T_2 is turned off, the SM is inserted into the arm circuit, the SM state is on, and the SM output voltage u_{sm} is equal to the SM capacitor voltage u_c. In this case, the SM capacitor C is charged by i_{arm}, and the capacitor voltage u_c is increased.
- *Mode 2 (normal operation)*: When $S = 1$ and $i_{arm} < 0$, as shown in Figure 1.3b, the T_1 is turned on, the T_2 is turned off, the SM is inserted into the arm circuit, the SM state is on, and the SM output voltage u_{sm} is equal to the SM capacitor

voltage u_c. In this case, the SM capacitor C is discharged by i_{arm}, and the capacitor voltage u_c is reduced.

- *Mode 3 (normal operation)*: When $S = 0$ and $i_{arm} > 0$, as shown in Figure 1.3c, the T_1 is turned off, the T_2 is turned on, the SM is bypassed from the arm circuit, the SM state is off, and the SM output voltage u_{sm} is equal to 0. In this case, the SM capacitor C is bypassed, and the capacitor voltage u_c is unchanged.
- *Mode 4 (normal operation)*: When $S = 0$ and $i_{arm} < 0$, as shown in Figure 1.3d, the T_1 is turned off, the T_2 is turned on, the SM is bypassed from the arm circuit, the SM state is off, and the SM output voltage u_{sm} is equal to 0. In this case, the SM capacitor C is bypassed, and the capacitor voltage u_c is unchanged.

1.3.2 Submodule Blocking Operation

In the blocking operation of the HB SM, the drive voltages u_{g1} and u_{g2} are both low-level and the switches T_1 and T_2 are both turned off, which has two operation modes and is decided by the arm current i_{arm}, as shown in Table 1.3 and Figure 1.4, as follows:

- *Mode 1 (blocking operation)*: When T_1 and T_2 are both turned off and $i_{arm} > 0$, as shown in Figure 1.4a, the SM is inserted into the arm circuit, the SM state is on, and the SM's output voltage u_{sm} is u_c. In this case, the capacitor C is charged by i_{arm}, and the capacitor voltage u_c is increased.

Table 1.3 Two blocking operation modes of the HB SM.

Mode	i_{arm}	Circuit state	SM state	T_1	T_2	u_{sm}	C	u_c
1	>0	Inserted	On	Off	Off	u_c	Charged	Increased
2	<0	Bypassed	Off	Off	Off	0	Bypassed	Unchanged

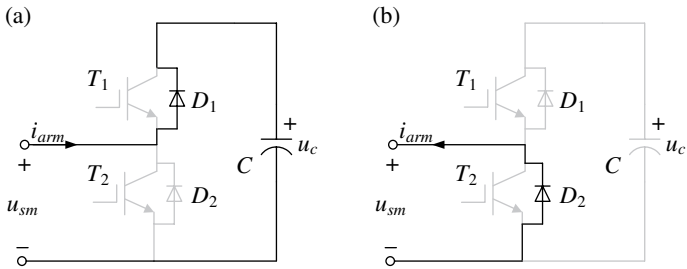


Figure 1.4 Two blocking operation modes of the HB SM. (a) Mode 1 (blocking operation). (b) Mode 2 (blocking operation).

- *Mode 2 (blocking operation)*: When T_1 and T_2 are both turned off and $i_{arm} < 0$, as shown in Figure 1.4b, the SM is bypassed from the arm circuit, the SM state is off, and the SM's output voltage u_{sm} is 0. In this case, the capacitor C is bypassed, and the capacitor voltage u_c is unchanged.

1.3.3 Converter Operation

The MMC generates the multilevel stepped waveform at its AC side by controlling the number of inserted SMs in the arm. To get an intuitive understanding of the operation principle of the MMC, Figure 1.5a shows an example of the upper arm of phase A, where four HB SMs (SM1–SM4) per arm are considered for the MMC. Here, all SMs' capacitor voltages are supposed to be the same as u_c, and the output voltages of the SM1–SM4 are u_{sm_au1}, u_{sm_au2}, u_{sm_au3}, and u_{sm_au4}, respectively. The waveform of the upper arm voltage u_{au} in phase A in one fundamental period is shown in Figure 1.5b, which is the sum of all SMs' output voltages u_{sm_au1}, u_{sm_au2}, u_{sm_au3}, and u_{sm_au4} in the upper arm of phase A. The switching functions of the SM1–SM4 and the corresponding output voltages of the SM1–SM4 are shown in Table 1.4, where the switching functions of

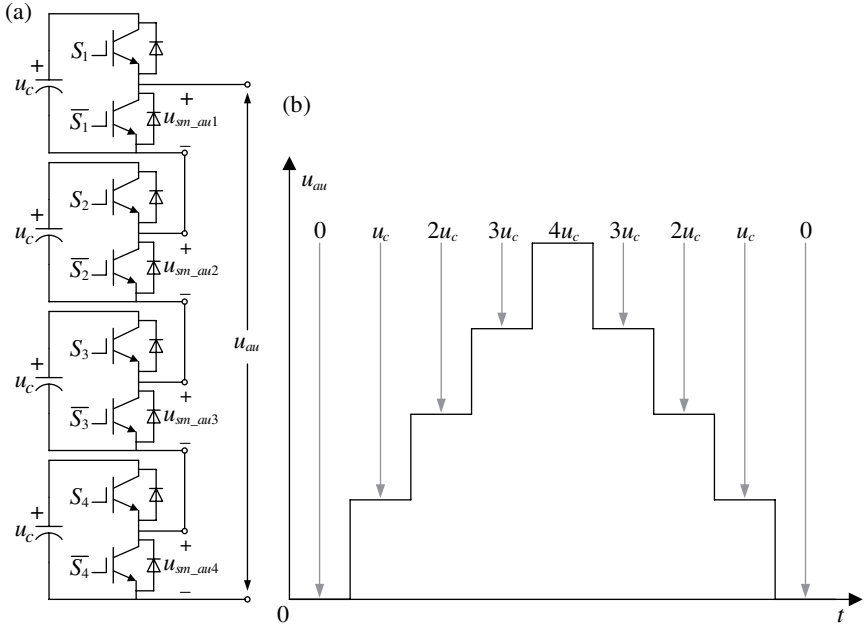


Figure 1.5 Operation principle of the MMC. (a) Upper arm of phase A. (b) Upper arm voltage of phase A.

Table 1.4 Switching functions and output voltages of SMs.

n_{on}	S_{au1}	S_{au2}	S_{au3}	S_{au4}	u_{sm_au1}	u_{sm_au2}	u_{sm_au3}	u_{sm_au4}	u_{au}
0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	u_c	0	0	0	u_c
	0	1	0	0	0	u_c	0	0	
	0	0	1	0	0	0	u_c	0	
	0	0	0	1	0	0	0	u_c	
2	1	1	0	0	u_c	u_c	0	0	$2u_c$
	1	0	1	0	u_c	0	u_c	0	
	1	0	0	1	u_c	0	0	u_c	
	0	1	1	0	0	u_c	u_c	0	
	0	1	0	1	0	u_c	0	u_c	
	0	0	1	1	0	0	u_c	u_c	
3	1	1	1	0	u_c	u_c	u_c	0	$3u_c$
	1	1	0	1	u_c	u_c	0	u_c	
	1	0	1	1	u_c	0	u_c	u_c	
	0	1	1	1	0	u_c	u_c	u_c	
4	1	1	1	1	u_c	u_c	u_c	u_c	$4u_c$

SM1–SM4 are S_{au1}, S_{au2}, S_{au3}, and S_{au4}, respectively. The arm voltage u_{au} has five different levels including 0, u_c, $2u_c$, $3u_c$, and $4u_c$, which is expressed as

$$u_{au} = \sum_{i=1}^{4} u_{sm\_aui} = \sum_{i=1}^{4} \left(S_{aui} \cdot u_c \right) = n_{on} \cdot u_c \tag{1.3}$$

with

$$n_{on} = \sum_{i=1}^{4} S_{aui} \tag{1.4}$$

where n_{on} is the number of inserted SMs in the arm of the MMC. The arm voltage u_{au} depends on different switching combinations corresponding to the SMs in the arm, as shown in Figure 1.5 and Table 1.4.

- *Fifth level ($u_{au} = 4u_c$)*: The highest arm voltage $4u_c$ is generated when all four switching functions S_{au1}, S_{au2}, S_{au3}, and S_{au4} corresponding to the SM1–SM4 are all switched to 1.

- *Forth level ($u_{au} = 3u_c$)*: The arm voltage $3u_c$ is generated when three out of four switching functions S_{au1}, S_{au2}, S_{au3}, and S_{au4} corresponding to the SM1–SM4 are switched to 1.
- *Third level ($u_{au} = 2u_c$)*: The arm voltage $2u_c$ is generated when two out of four switching functions S_{au1}, S_{au2}, S_{au3}, and S_{au4} corresponding to the SM1–SM4 are switched to 1.
- *Second level ($u_{au} = u_c$)*: The arm voltage u_c is generated when one out of four switching functions S_{au1}, S_{au2}, S_{au3}, and S_{au4} corresponding to the SM1–SM4 is switched to 1.
- *First level ($u_{au} = 0$)*: The lowest arm voltage 0 is generated when all four switching functions S_{au1}, S_{au2}, S_{au3}, and S_{au4} corresponding to the SM1–SM4 are all switched to 0.

1.4 Modulation Scheme

Modulation is a technique that produces the desired voltage in the arm or at the AC side of the MMC by controlling the drive voltage of switching devices in the MMC. It affects not only the MMC's external performance, such as AC-side voltage harmonics and AC-side current harmonics, but also the internal characteristics, such as capacitor voltage fluctuation, distribution of energy, and power losses distribution among SMs [9]. Currently, there are three modulation schemes commonly used in the MMC, which are PD-PWM, PS-PWM, and NLM, as shown in Table 1.5. Based on the modulation and the reference y for the arm of the MMC, the number n_{on} of SMs to be inserted into the arm of the MMC can be decided, as shown in Figure 1.6.

Table 1.5 Three modulation schemes [9–16].

Modulation scheme	Characteristics
PD-PWM	• High switching frequency modulation • Unevenly distributed pulses • Suitable for MMCs with not so many SMs per arm
PS-PWM	• High switching frequency modulation • Evenly distributed pulses • Suitable for MMCs with not so many SMs per arm
NLM	• Low switching frequency modulation • Easy for implementation • Suitable for MMCs with large number of SMs per arm

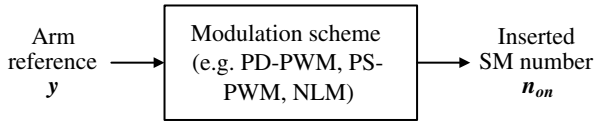


Figure 1.6 Modulation for MMCs.

1.4.1 Phase-Disposition PWM

The PD-PWM is typically suitable for the MMC with not so many SMs per arm [9–11]. For the MMC with n SM per arm, it is realized by applying n number of identical triangular carriers W_1–W_n stacked evenly in the vertical direction between −1 and 1. Through the comparison between the carriers and the reference signal y, the PD-PWM can be produced.

Figure 1.7 illustrates the implementation principle of the PD-PWM ($n = 4$) for the MMC with n SMs per arm. The n carriers W_1–W_n are at the same phase angle. The carrier frequency is f_s. The height Δh of each carrier is equal to $2/n$.

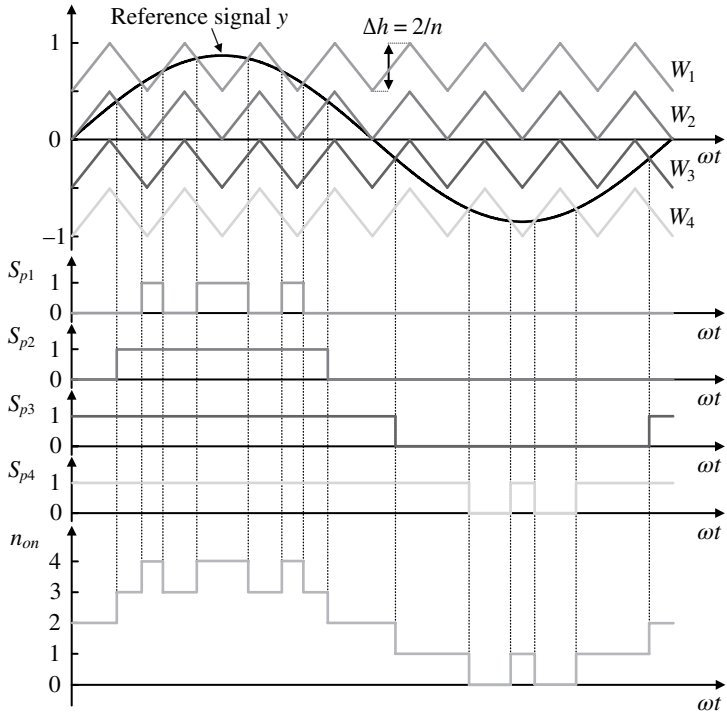


Figure 1.7 Implementation principle of PD-PWM for MMCs.

The reference signal y is compared with the carriers W_1–W_n to generate the pulses S_{p1}–S_{pn}, respectively, as follows:

- The S_{pi} is 1 if the reference y is higher than the carrier W_i ($i = 1, 2, \ldots, n$)
- The S_{pi} is 0 if the reference is lower than the carrier W_i ($i = 1, 2, \ldots, n$)

The total number n_{on} of SMs to be inserted into each arm at each instant can be expressed as the sum of S_{p1}–S_{pn}, as

$$n_{on} = \sum_{i=1}^{n} S_{pi} \tag{1.5}$$

Figure 1.7 shows that the PD-PWM results in an unevenly distributed switching frequency among S_{p1}–S_{pn}. The value of n_{on} varies in the range of 0–n in one fundamental period, which achieves the multilevel synthesized waveform. In addition, it is apparent that the switching actions of S_{p1}–S_{pn} are affected by the amplitude of the reference signal y.

The typical characteristics of the PD-PWM are summarized in Table 1.5.

1.4.2 Phase-Shifted PWM

The PS-PWM is suitable for the MMC with not so many SMs per arm [12, 13]. For the MMC with n SMs per arm, it is realized by applying n number of identical triangular carriers W_1–W_n stacked evenly in horizontal direction. The carrier is between −1 and 1. Through the comparison between the carriers W_1–W_n and the reference signal y, the PS-PWM can be achieved.

Figure 1.8 illustrates the implementation principle of PS-PWM ($n = 4$) for the MMC with n SMs per arm. The carriers W_1–W_n are all with the same carrier frequency f_s. The phase angle between two adjacent carriers of W_1–W_n is denoted as $\Delta\theta$. Generally, the $\Delta\theta$ is

$$\Delta\theta = 2\pi / n \tag{1.6}$$

The reference signal y is compared with the carriers W_1–W_n to generate the pulses S_{p1}–S_{pn}, as follows:

- The S_{pi} is 1 if the reference y is more than the carrier W_i ($i = 1, 2, \ldots, n$)
- The S_{pi} is 0 if the reference is less than the carrier W_i ($i = 1, 2, \ldots, n$)

The total number n_{on} of the SMs to be inserted into each arm at each instant can be expressed as the sum of S_{p1}–S_{pn}, as

$$n_{on} = \sum_{i=1}^{n} S_{pi} \tag{1.7}$$

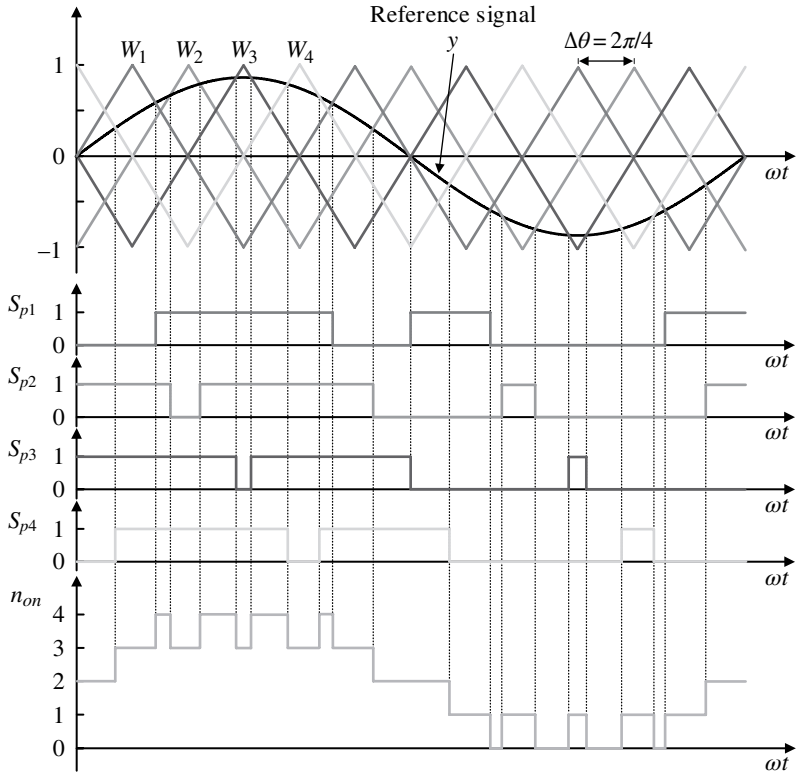


Figure 1.8 Implementation principle of PS-PWM for MMCs.

In Figure 1.8, the reference signal y is always modulated by all carriers W_1–W_n to generate the PWM pulses. The pulses and the switching frequency are distributed evenly among S_{p1}–S_{pn}. The value of n_{on} varies in the range of 0–n in one fundamental period, which achieves the multilevel synthesized waveform. In addition, the switching actions of S_{p1}–S_{pn} remain constant regardless of the modulation index of the reference signal.

The typical characteristics of the PS-PWM are summarized in Table 1.5.

1.4.3 Nearest Level Modulation

The NLM is suitable for the MMC applications with large number of SMs, e.g. high voltage direct current (HVDC) transmission [9, 14–16]. The NLM uses the staircase waveform nearest to the desired reference signal. For the MMC with n SMs per arm, the NLM can be produced with the simple rounding function for the reference y.

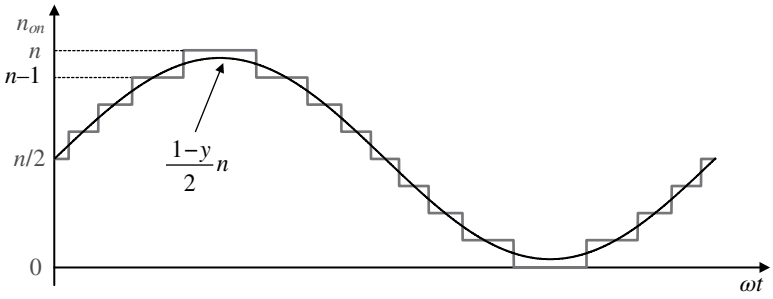


Figure 1.9 Implementation principle of NLM for MMCs.

Figure 1.9 illustrates the implementation principle of the NLM for the upper arm of the MMC ($n = 8$) with n SMs per arm. Based on the reference signal y for the phase unit, the total number n_{on} of SMs to be inserted into the upper arm at each instant can be obtained as

$$n_{on} = \text{round}\left(\frac{1-y}{2}n\right) \tag{1.8}$$

The NLM directly generates the number of inserted SMs in the arm to yield the multilevel waveforms. The waveform of n_{on} is a staircase with step height of 1. The value of n_{on} varies in the range of 0–n. Therefore, the maximum level number of n_{on} is $n + 1$. The harmonic spectrum of the NLM is dependent on n. If n is small, the staircase number is small and the harmonics will be a little high. If n is large, the staircase number is large and the multilevel waveforms will be very close to the reference signal and have very little harmonics.

The typical characteristics of the NLM are summarized in Table 1.5.

1.5 Mathematical Model

1.5.1 Submodule Mathematical Model

Figure 1.10 shows the equivalent circuit diagram of the i-th SM in the upper arm of phase A. Figure 1.10a shows the equivalent circuit diagram of the SM when its switching function S_{aui} is 1, and Figure 1.10b shows the equivalent circuit diagram of the SM when its switching function S_{aui} is 0. According to the equivalent circuit diagrams, the switching-function based model and the reference-based model of the HB SM can be derived as discussed in the following sections.

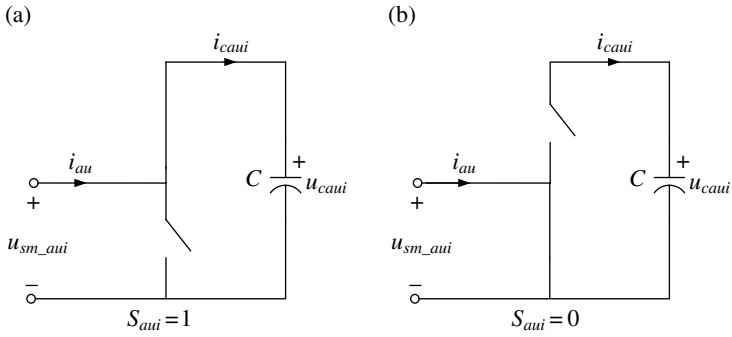


Figure 1.10 HB SM equivalent circuit. (a) S_{aui} = 1. (b) S_{aui} = 0.

1.5.1.1 Switching-Function Based Model

The relationship between the i-th SM's capacitor current i_{caui} and arm current i_{au} can be expressed as

$$i_{caui} = S_{aui} \cdot i_{au} \tag{1.9}$$

The relationship between SM's output voltage u_{sm_aui} and SM's capacitor voltage u_{caui} can be expressed as

$$u_{sm\_aui} = S_{aui} \cdot u_{caui} \tag{1.10}$$

According to the Volt–Ampere characteristic of the capacitor [17], the voltage u_{caui} imposed on the SM's capacitor C can be expressed as

$$u_{caui} = \frac{1}{C}\int i_{caui}dt = \frac{1}{C}\int\left(S_{aui} \cdot i_{au}\right)dt \tag{1.11}$$

Combining equations (1.10) and (1.11), the SM's output voltage u_{sm_uai} can be rewritten as

$$u_{sm\_aui} = \frac{S_{aui}}{C}\int\left(S_{aui} \cdot i_{au}\right)dt \tag{1.12}$$

1.5.1.2 Reference-Based Model

With the Fourier transform, the SM's switching function S_{aui} can be expressed using Fourier series as

$$S_{aui} = \frac{1}{2} + \frac{1}{2}m\sin\left(\omega t + \phi\right) + \sum_{h=2}^{\infty} A_h \sin\left(h\omega t + \phi_h\right) \tag{1.13}$$

where m is the modulation index, ω is the fundamental angular frequency, ϕ is the phase angle of the fundamental component, and A_h and θ_h are the amplitude and phase angle for the h-th harmonic, respectively.

Neglecting the harmonic components and supposing that the SMs in the arm are the same, the SM's switching function can be simplified as

$$S_{aui} \approx \frac{1}{2} + \frac{1}{2} y_{au} \tag{1.14}$$

with

$$y_{au} = m \sin\left(\omega t + \phi\right) \tag{1.15}$$

where y_{au} is the reference signal for upper arm of phase A.

Combining equations (1.9) and (1.14), the SM's capacitor current i_{caui} can be expressed as

$$i_{caui} = \frac{1 + y_{au}}{2} \cdot i_{au} \tag{1.16}$$

Based on equations (1.11) and (1.16), the SM's capacitor voltage u_{caui} can be expressed as

$$u_{caui} = \frac{1}{C} \int \left(\frac{1 + y_{au}}{2} \cdot i_{au} \right) dt \tag{1.17}$$

Combining equations (1.10), (1.14), and (1.17), the SM's output voltage u_{sm_uai} can be expressed as

$$u_{sm\_aui} = \frac{1 + y_{au}}{2} \cdot u_{caui} = \frac{1 + y_{au}}{2C} \int \left(\frac{1 + y_{au}}{2} \cdot i_{au} \right) dt \tag{1.18}$$

1.5.2 Arm Mathematical Model

Figure 1.11 shows the configurations of the upper and lower arms of phase j ($j = a$, b, c). Figure 1.11a shows the configuration of the upper arm of phase j, and Figure 1.11b shows the configuration of the lower arm of phase j. According to the arm configurations, the switching-function based model and the reference-based model of upper and lower arms can be derived as discussed in the following sections.

1.5.2.1 Switching-Function Based Model

In Figure 1.11, the upper arm voltage u_{ju} and lower arm voltage u_{jl} of phase j are equal to the sum of SM's output voltages [18]. The upper arm voltage u_{ju} and lower arm voltage u_{jl} can be expressed as

$$\begin{cases} u_{ju} = \sum_{i=1}^{n} u_{sm\_jui} \\ u_{jl} = \sum_{i=1}^{n} u_{sm\_jli} \end{cases} \tag{1.19}$$

where u_{sm_jui} is the output voltage of the i-th SM in the upper arm of phase j and u_{sm_jli} is the output voltage of the i-th SM in the lower arm of phase j.

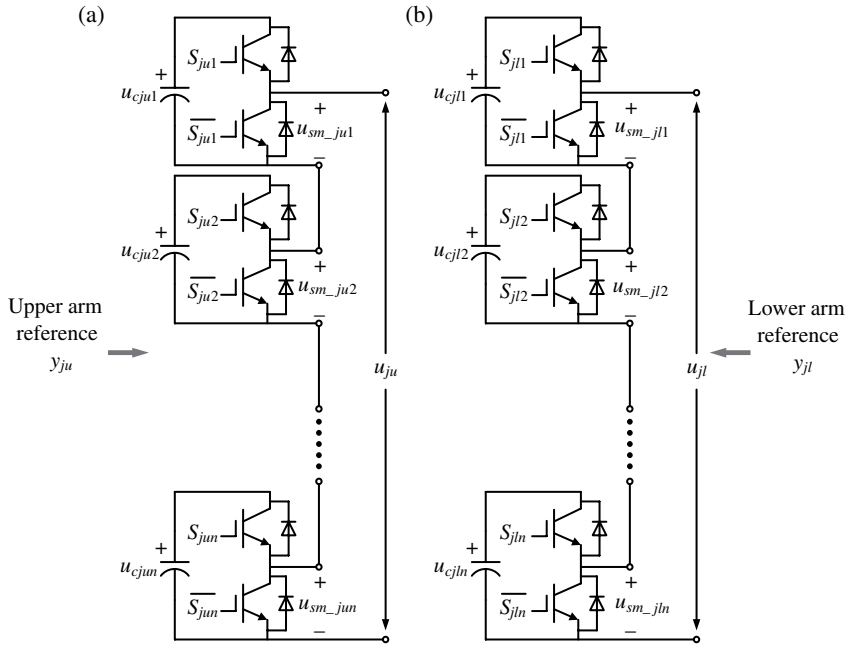


Figure 1.11 Arm configurations. (a) Upper arm of phase *j*. (b) Lower arm of phase *j*.

Combining equations (1.10) and (1.19), the upper arm voltage u_{ju} and lower arm voltage u_{jl} can be expressed as

$$\begin{cases} u_{ju} = \sum_{i=1}^{n} \left(S_{jui} \cdot u_{cjui} \right) \\ u_{jl} = \sum_{i=1}^{n} \left(S_{jli} \cdot u_{cjli} \right) \end{cases} \tag{1.20}$$

where S_{jui} is the switching function of the *i*-th SM in the upper arm of phase *j*, S_{jli} is the switching function of the *i*-th SM in the lower arm of phase *j*, u_{cjui} is the capacitor voltage of the *i*-th SM in the upper arm of phase *j*, and u_{cjli} is the capacitor voltage of the *i*-th SM in the lower arm of phase *j*.

1.5.2.2 Reference-Based Model

Combining equations (1.14) and (1.20), the upper arm voltage u_{ju} and lower arm voltage u_{jl} can be expressed as

$$\begin{cases} u_{ju} = \dfrac{1 + y_{ju}}{2} \cdot \sum_{i=1}^{n} u_{cjui} \\ u_{jl} = \dfrac{1 + y_{jl}}{2} \cdot \sum_{i=1}^{n} u_{cjli} \end{cases} \tag{1.21}$$

where y_{ju} and y_{jl} are the reference signals for the upper arm and lower arm of phase j, respectively, as shown in Figure 1.11.

1.5.3 Three-Phase MMC Mathematical Model

The configuration of the three-phase MMC is shown in Figure 1.12, and its mathematical model can be derived, as follows.

According to the Kirchhoff's voltage law, the upper arm voltage u_{ju} and the lower arm voltage u_{jl} can be expressed as

$$\begin{cases} u_{ju} = \dfrac{V_{dc}}{2} - u_j - L_s \dfrac{di_{ju}}{dt} \\ u_{jl} = \dfrac{V_{dc}}{2} + u_j - L_s \dfrac{di_{jl}}{dt} \end{cases} \tag{1.22}$$

where u_j is the AC-side voltage of phase j, i_{ju} is the upper arm current of phase j, and i_{jl} is the lower arm current of phase j.

According to the Kirchhoff's current law, the AC-side current i_j can be expressed as

$$i_j = i_{ju} - i_{jl} \tag{1.23}$$

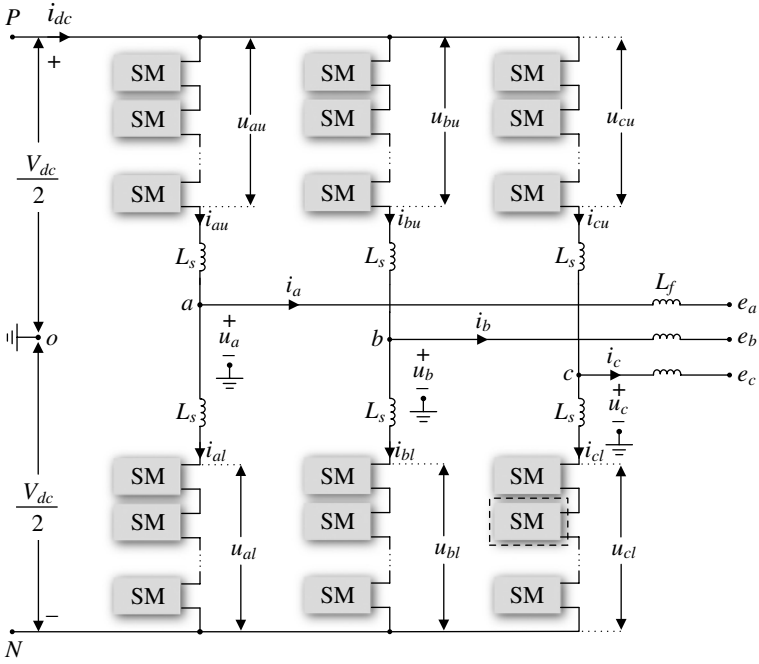


Figure 1.12 The three-phase MMC configuration.

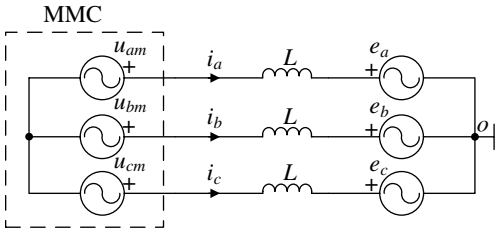


Figure 1.13 The AC-side equivalent circuit of the MMC.

1.5.3.1 AC-Side Mathematical Model

Figure 1.13 shows the AC-side equivalent circuit of the MMC. Combining equation (1.22) and Figure 1.13, the AC-side dynamics of the MMC can be expressed as

$$e_j = u_{jm} - L\frac{di_j}{dt} \tag{1.24}$$

where e_j is the AC-side voltage in phase j. u_{jm} is the internal converter voltage of the MMC and is expressed as

$$u_{jm} = \frac{u_{jl} - u_{ju}}{2} \tag{1.25}$$

L is the equivalent AC-side inductance and is expressed as

$$L = \frac{L_s}{2} + L_f \tag{1.26}$$

1.5.3.2 DC-Side Mathematical Model

Figure 1.14 shows the DC-side equivalent circuit of the MMC. According to equation (1.22) and Figure 1.14, the DC-side voltage V_{dc} of the MMC can be expressed as

$$V_{dc} = u_{ju} + u_{jl} + 2L_s\frac{di_{diff\_j}}{dt} \tag{1.27}$$

with

$$i_{diff\_j} = \frac{i_{ju} + i_{jl}}{2} \tag{1.28}$$

where i_{diff_j} ($j = a, b, c$) is the circulating current in phase j.

The i_{diff_j} mainly contains DC component and the second-order harmonic component [18], as

$$i_{diff\_j} = \frac{i_{dc}}{3} + i_{2f\_j} \tag{1.29}$$

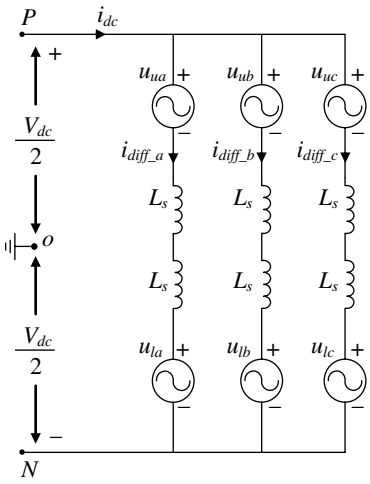


Figure 1.14 The DC-side equivalent circuit of the MMC.

where i_{dc} is the DC-side current. i_{2f_j} is the second-order circulating current in phase j. The upper arm current and the lower arm current in phase j of the MMC can be expressed as

$$\begin{cases} i_{ju} = \dfrac{i_j}{2} + i_{diff\_j} \\ i_{jl} = -\dfrac{i_j}{2} + i_{diff\_j} \end{cases} \tag{1.30}$$

1.6 Design Constraints

Parameter designs of the MMC components are important because reasonable parameters can improve the stability and dynamic performance of the system [19–23]. This section focuses on the parameter design methods of power devices, capacitor, and arm inductor in the MMC.

1.6.1 Power Device Design

The configuration of the HB SM is shown in Figure 1.15, which has four power devices, including switches T_1, T_2 and diodes D_1, D_2. According to Section 1.3, the HB SM has four operation modes under normal operation and two operation modes under blocking operation.

Figure 1.15 HB SM configuration.

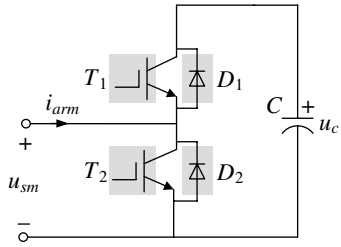


Table 1.6 Voltage stresses of power devices in the HB SM under normal operation.

						Power device voltage stress		
Mode		S	i_{arm}	T_1	T_2	u_{T1}	u_{D1}	u_{T2}	u_{D2}
Normal	1	1	>0	On	Off	0	0	u_c	u_c
	2		<0	On	Off	0	0	u_c	u_c
	3	0	>0	Off	On	u_c	u_c	0	0
	4		<0	Off	On	u_c	u_c	0	0

1.6.1.1 Rated Voltage of Power Devices

The voltages u_{T1}, u_{D1}, u_{T2}, u_{D2} of power devices T_1, D_1, T_2, D_2, respectively, in the MMC under normal operation are shown in Table 1.6. According to Table 1.6, the maximum voltage stress of power devices in four operation modes is the capacitor voltage u_c. Since the rated voltage parameters of power devices need to be selected with a margin, the rated voltage parameters of power devices can be chosen as 1.5–2 times the capacitor voltage u_c.

1.6.1.2 Rated Current of Power Devices

The current i_{T1}, i_{D1}, i_{T2}, i_{D2} flowing through power devices T_1, D_1, T_2, D_2, respectively, in the MMC under normal operation are shown in Table 1.7, as follows:

- The arm current i_{arm} flows through T_1 when $i_{arm} < 0$ and $S = 1$.
- The arm current i_{arm} flows through T_2 when $i_{arm} > 0$ and $S = 0$.
- The arm current i_{arm} flows through D_1 when $i_{arm} > 0$ and $S = 1$.
- The arm current i_{arm} flows through D_2 when $i_{arm} < 0$ and $S = 0$.

Taking the upper arm of phase A as an example, Figure 1.16 shows the arm current i_{au} in one fundamental cycle. Suppose that t_1, t_2, and t_3 are the times when $i_{au} = 0$, as shown in Figure 1.16. Then, the root mean square (RMS) values I_{rms_T1},

Table 1.7 Current through power devices in the MMC under normal operation.

						Power device current		
Mode		S	i_{arm}	T_1	T_2	i_{T1}	i_{D1}	i_{T2}	i_{D2}
Normal	1	1	>0	On	Off	0	i_{arm}	0	0
	2		<0	On	Off	i_{arm}	0	0	0
	3	0	>0	Off	On	0	0	i_{arm}	0
	4		<0	Off	On	0	0	0	i_{arm}

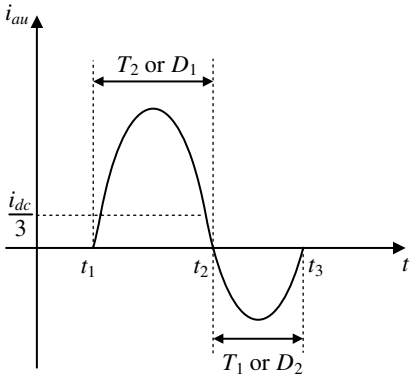


Figure 1.16 Upper arm current of phase A.

I_{rms_T2}, I_{rms_D1}, I_{rms_D2} of the current flowing through power devices T_1, T_2, D_1, D_2, respectively, in the i-th SM of the upper arm of phase A can be obtained as

$$\begin{cases} I_{rms\_T_1} = \sqrt{\dfrac{1}{T_f}\displaystyle\int_{t_2}^{t_3} S_{aui}{}^2 i_{au}{}^2 dt} \\ I_{rms\_T_2} = \sqrt{\dfrac{1}{T_f}\displaystyle\int_{t_1}^{t_2} \left(1 - S_{aui}\right)^2 i_{au}{}^2 dt} \\ I_{rms\_D_1} = \sqrt{\dfrac{1}{T_f}\displaystyle\int_{t_1}^{t_2} S_{aui}{}^2 i_{au}{}^2 dt} \\ I_{rms\_D_2} = \sqrt{\dfrac{1}{T_f}\displaystyle\int_{t_2}^{t_3} \left(1 - S_{aui}\right)^2 i_{au}{}^2 dt} \end{cases} \tag{1.31}$$

where T_f is the fundamental period of upper arm current i_{au}.

Since the rated current parameters of power devices need to be selected with a margin, the rated current parameters of power devices can be chosen as 1.5–2 times of the RMS value of the current flowing through power devices.

1.6.2 Capacitor Design

The SM's capacitor voltage u_c contains the DC component and the fluctuation component under normal operation of the MMC. The SM's capacitor voltage u_c can be expressed as

$$u_c = U_c + \Delta u_c \tag{1.32}$$

where U_c is the DC component of the SM's capacitor voltage with $U_c = V_{dc}/n$ and Δu_c is the fluctuation component of the SM's capacitor voltage.

The capacitor voltage fluctuation ratio ε is

$$\varepsilon = \frac{\max\left|\Delta u_c\right|}{U_c} \tag{1.33}$$

To simplify the analysis while neglecting the voltage of the arm inductance and the second-order circulating current, the voltage u_{au} and the current i_{au} of the upper arm in phase A of the MMC can be expressed as

$$\begin{cases} u_{au} = \dfrac{V_{dc}}{2} - u_a \\ i_{au} = \dfrac{i_a}{2} + \dfrac{i_{dc}}{3} \end{cases} \tag{1.34}$$

Suppose that the voltage u_a and current i_a of phase A are

$$\begin{cases} u_a = U_m \sin\left(\omega t\right) \\ i_a = I_m \sin\left(\omega t + \theta\right) \end{cases} \tag{1.35}$$

where U_m and I_m are the amplitudes of u_a and i_a, respectively. θ is the phase angle.

Combining equations (1.34) and (1.35), the instantaneous power p_{au} of the upper arm in phase A is

$$p_{au} = u_{au} \cdot i_{au} = \frac{U_m I_m}{4}\left[\frac{I_m}{i_{dc}}\cos\theta - 2\sin\left(\omega t\right)\right] \cdot \left[-\sin\left(\omega t + \theta\right) - \frac{I_m}{i_{dc}}\right] \tag{1.36}$$

The instantaneous power p_{au} has two zero-crossing points in one fundamental period T_f, $T_f = 2\pi/\omega$, defined as t_1 and t_2, respectively, as shown in Figure 1.17, which can be expressed as

$$\begin{cases} t_1 = \dfrac{1}{\omega} \cdot \left[-\arcsin\left(\dfrac{i_{dc}}{I_m}\right) + \theta\right] \\ t_2 = \dfrac{1}{\omega} \cdot \left[\pi + \arcsin\left(\dfrac{i_{dc}}{I_m}\right) - \theta\right] \end{cases} \tag{1.37}$$

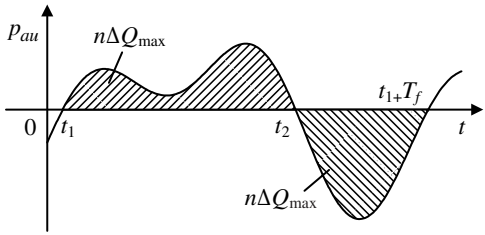


Figure 1.17 Instantaneous power of upper arm in phase A.

In Figure 1.17, the energy stored in the upper arm of phase A would be increased during the period when $p_{au} > 0$, while the arm energy would be reduced during the period when $p_{au} < 0$. In addition, the energy absorbed by the arm when $p_{au} > 0$ equals the energy discharged when $p_{au} < 0$ during one fundamental period T_f, so as to ensure the balance of the arm energy. As a result, the arm energy reaches its minimum and maximum at t_1 and t_2, respectively. Assuming that the arm energy is equally distributed among n SM's capacitors, the largest change of the capacitor energy $\Delta Q_{\max}$ during one fundamental cycle T_f can be obtained as [22]

$$\Delta Q_{\max} = Q_{\max} - Q_{\min} = \frac{1}{n} \cdot \int_{t_1}^{t_2} \left| p_{au} \right| dt = \frac{2}{3} \frac{S_N}{mn\omega} \left[1 - \left(\frac{m \cos\theta}{2} \right)^2 \right]^{3/2} \tag{1.38}$$

where $Q_{\max}$ and $Q_{\min}$ are the maximum and minimum capacitor energy, respectively. S_N is the rated apparent power of the MMC, and m is the modulation index.

In each SM of upper arm of phase A, the SM maximum capacitor energy $Q_{\max}$ and the SM minimum capacitor energy $Q_{\min}$ are

$$\begin{cases} Q_{\max} = \frac{1}{2} C \left[U_c \cdot (1 + \varepsilon) \right]^2 \\ Q_{\min} = \frac{1}{2} C \left[U_c \cdot (1 - \varepsilon) \right]^2 \end{cases} \tag{1.39}$$

Substituting equation (1.39) into (1.38), there is

$$\varepsilon = \frac{1}{3} \frac{S_N}{mn\omega C U_c^2} \left[1 - \left(\frac{m \cos\theta}{2} \right)^2 \right]^{3/2} \tag{1.40}$$

The basic consideration for selecting the SM's capacitance value is to ensure that the capacitor fluctuation ratio ε is less than the maximum allowed voltage fluctuation $\varepsilon_{\max}$ under any operation conditions of the MMC, which is usually selected within 5% to 10%. According to (1.40), when $\cos\theta = 1$, $m = 1$, the capacitor voltage fluctuation ratio ε reaches its maximum [23], as

$$\varepsilon = \frac{1}{3} \cdot \frac{S_N}{n\omega C U_c^2} \tag{1.41}$$

The SM's capacitor can be designed as

$$C \geq \frac{1}{3} \cdot \frac{S_N}{n\omega U_c^2 \varepsilon_{\max}} \tag{1.42}$$

1.6.3 Arm Inductor Design

Limiting the DC-side short-circuit fault current rise rate is the distinctive function of the arm inductor in the MMC [24]. When a short circuit fault occurs at the DC side of the MMC, the duration of the transient process is so short that the voltages of the SM capacitors are supposed to be constant. Suppose that the sum of the capacitor voltages of the SMs inserted in phase j is equal to V_{dc} after the fault

$$u_{jl} + u_{ju} = V_{dc} \tag{1.43}$$

In addition, a huge fault current would be caused under the DC-side short-circuit fault, which will flow to the fault point. According to (1.27), the DC-side mathematical model of the MMC can be expressed as

$$u_{jl} + u_{ju} + \left(L_s \frac{di_{ju}}{dt} + L_s \frac{di_{jl}}{dt} \right) = 0 \tag{1.44}$$

where $|di_{ju}/dt|$ is the fault current rise rate in the upper arm in phase j, and $|di_{jl}/dt|$ is the fault current rise rate in the lower arm in phase j. In a short period after the fault, the majority of the arm current is the transient component. Thus, the upper and lower arm currents are supposed to be equal as

$$i_{ju} = i_{jl} \tag{1.45}$$

Therefore, the fault current rise rate $|di_{ju}/dt|$ in the upper arm and the fault current rise rate $|di_{jl}/dt|$ in the lower arm of phase j are supposed to be equal as

$$\left| \frac{di_{ju}}{dt} \right| = \left| \frac{di_{jl}}{dt} \right| = \lambda \tag{1.46}$$

where λ is the fault current rise rate.

Combining equations (1.43), (1.44), and (1.46), there is

$$\lambda = \frac{V_{dc}}{2L_s} \tag{1.47}$$

To limit the DC-side short-circuit fault current rise rate, the arm inductor L_s can be designed as

$$L_s \geq \frac{V_{dc}}{2\lambda_{\max}} \tag{1.48}$$

where $\lambda_{\max}$ is the maximum allowed fault current rise rate.

1.7 Faults Overview of MMCs

This section introduces the internal and external faults of the MMC. The internal faults are caused by component failures in the MMC, while the external faults are induced by grid faults at the AC or DC side of the MMC, as shown in Figure 1.18.

1.7.1 Internal Faults of MMCs

The internal faults of the MMC can be mainly classified into two categories, namely, the IGBT faults and the capacitor faults.

The IGBT faults can be further classified into two categories based on the fault characteristics, namely the IGBT short-circuit fault and the IGBT open-circuit fault [25]. The IGBT short-circuit fault is mainly caused by incorrect driving signals or device over-stress, and it will lead to an abnormal overcurrent and cause serious damage to other components in a short time. The IGBT open-circuit fault is mainly caused by the failure of the switch gate driver and the failure of the bond wire, and it will cause an unbalanced state in the circuit, which produces distorted waveforms and voltage/current stresses and obviously deteriorates the system performance. Therefore, it is necessary to detect the IGBT faults, which are introduced in detail in Chapter 3.

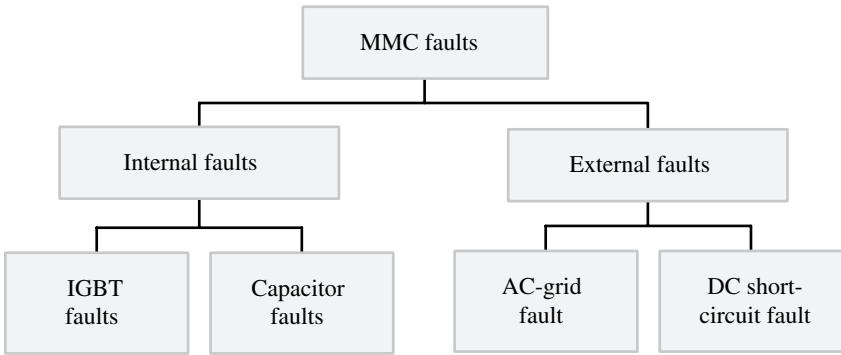


Figure 1.18 MMC faults overview.

The capacitor faults are caused by combined effects of thermal, electrical, mechanical, and environmental stress and can result in a decrease in capacitance and an increase in equivalent series resistance [26]. Once one of the capacitors fails, the normal operation of the MMC would be disrupted. Therefore, it is also necessary to provide an effective capacitor condition monitoring method for reliable, efficient, and safe operation of the MMC, which is introduced in detail in Chapter 4.

Fault tolerant operation is one of the most important challenges for the MMC, where it is desired that the MMC can continue operating without any interruption, despite some of the SMs malfunctioning. Therefore, in addition to the method of fault detection, fault tolerant control of MMCs under SM faults is introduced in detail in Chapter 5.

1.7.2 External Faults of MMCs

The external faults of the MMC can be mainly classified into two categories, namely the AC-grid fault and the DC-grid short-circuit fault.

When the AC-grid fault occurs, the AC-side current may consist of a negative-sequence component and the zero-sequence current may also exist in transformerless applications of the MMC [27]. The unbalanced AC-side current can cause overcurrent and the oscillation of active and reactive power, which is harmful to the whole MMC system. Therefore, the operation and control of the MMC system in the presence of grid imbalances is very important, which is introduced in detail in Chapter 6.

When the DC grid short-circuit fault occurs [28], the MMC will enter blocking mode and the AC grid will feed the fault on the DC side through the anti-parallel diodes of the HB SMs. In such an uncontrolled operation mode, the converter has to withstand large fault current from the AC grid until the DC fault is interrupted and the large fault current can damage the MMC due to the limited current capability of power devices. Therefore, it is also important to adopt DC-grid fault protection methods, which are introduced in detail in Chapter 7.

1.8 Summary

In this chapter, a comprehensive overview of MMCs, including MMC configuration and operation principles, are presented. The MMC can be realized by using a number of SMs. The most popular and widely used SM configuration with HB SM configuration is discussed. The mathematical relationships of the MMC, including the mathematical relationship in the SM, the mathematical relationship in the arm, and the mathematical relationship in the three-phase MMC, are presented.

PWM schemes are commonly employed to control the MMC. A comprehensive overview of the modulation schemes for the MMC is presented, including

PD-PWM, PS-PWM, and NLM. Considering the computational complexity, the PD-PWM and PS-PWM are suitable for the MMC with not so many SM per arm, while the NLM is suitable for the MMC with a large number of SMs. The power devices, capacitor, and arm inductor are the important components in the MMC. The design constraints of the power devices, capacitor, and arm inductor are presented based on their voltage and current constraints.

The internal faults of the MMC, including the power device faults such as the switch open-circuit fault, switch short-circuit fault, and capacitor faults, are harmful to the MMC, and fault detection and fault tolerant control are essential for the MMC, which are further presented in Chapters 3–5. The external faults of the MMC, including the AC-grid faults and the DC-grid faults, would harm the MMC, and the corresponding control and protection are also essential for the MMC, which are further presented in Chapters 6 and 7.

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