1

Introduction

1.1 Phase-Lock Technique

A basic concept of a phase-locked feedback system for frequency generation was proposed in the early 1930s, but the use of a phase-locked loop (PLL) circuit for mass production began with analog television systems in the 1940s. Since then, the PLL has been one of the most critical building blocks in modern communication IC systems, covering both wireless and wireline applications.

What is the main function of the PLL? From the name and a block diagram shown in Fig. 1.1, it can be deduced that it is the loop that performs a phase lock between a reference clock and an output clock. In the coherent communication systems that use the amplitude and phase information of a signal for modulation and demodulation, interestingly, the phase-lock has not been the primary goal of the PLL in most cases. Let us look at some descriptions of the PLL in other books.

- A circuit synchronizing an output signal (generated by an oscillator) with a reference or input signal in frequency as well as in phase [Best].
- A circuit that synchronizes the signal from an oscillator with a second input signal, so that they operate at the same frequency [Egan].
- When the loop is (phase) locked, the control voltage sets the average frequency of the oscillator exactly equal to the average frequency of the input signal [Gardner].
- Basically, an oscillator whose frequency is locked onto some frequency component of an input signal, which is done with a feedback control loop [Wolaver].

The first description addresses the basic function of the PLL both in phase and frequency domains. In the second or the third description, the goal of the PLL is to achieve the same frequency as the input frequency by using a phase-lock technique. In the last description, the phase lock was not even mentioned, and the PLL was simply defined as an oscillator whose frequency is locked to the input frequency. As implied by those descriptions, we can see that the primary goal of

Phase-Locked Loops: System Perspectives and Circuit Design Aspects, First Edition.
Woogeun Rhee and Zhiping Yu.

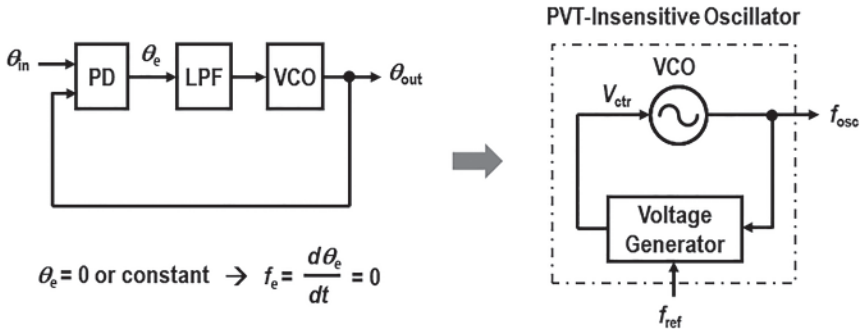

Figure 1.1 Accurate frequency control by a phase-lock technique.

the PLL is not the phase-lock but the frequency-lock. This is because the frequency offset between an input signal and a local oscillator in the coherent receiver system is much more serious than the phase offset problem.

If the main goal of the PLL is to achieve the frequency-lock, we may wonder if a frequency-locked loop (FLL) should be used instead of the PLL. The reason is that the FLL still generates a static frequency error if there exist circuit mismatches, a limited loop gain at DC, or a limited resolution in a frequency detector. To the contrary, the PLL generates a static phase error rather than the frequency error in the presence of a limited loop gain at DC or imperfect matching in a phase detector circuit. Since the frequency error f_e is the derivative of the phase error θ_e, the PLL always achieves a zero-frequency error even with the presence of a static phase error illustrated in Fig. 1.1. In other words, the PLL guarantees that the accuracy of an output frequency is the same as that of a source frequency based on the phase-lock technique. From that point of view, the PLL can be referred as a *phase-locking loop* rather than the *phase-locked loop* since the phase-lock is not the goal but an active method to achieve the frequency-lock. This explains why the PLL has been dominantly employed in the coherent communication system where the frequency offset between a carrier and a local oscillator is critical. When the PLL is used for frequency generation, we may regard the PLL as the oscillator circuit that generates an adaptive DC control voltage V_{ctr} to an internal voltage-controlled oscillator (VCO) so that a stable output frequency is maintained over process-voltage-temperature (PVT) variations as depicted in Fig. 1.1.

1.2 Key Properties and Applications

In addition to the zero-frequency error, there is another important property. The PLL is the only device that performs auto-tracking band-pass filtering with

high-quality factor Q and wide tunability. The high-Q band-pass filtering with wide tunability is possible since the bandwidth of a PLL can be independently set without limitation to an output frequency, while the tunability is determined by the tuning range of a VCO regardless of the PLL bandwidth. This feature is well utilized for clock-and-data recovery (CDR) systems to extract a clean clock from a noisy input data. In the CDR system, the phase-lock property is also used to define an optimum edge-of-clock position for data retiming. Besides those two properties, the inherent property of the PLL, phase-lock, makes the PLL play an important role in modern wireline communication systems. As data rate or clock frequency increases, clock de-skewing or phase synchronization has become critical to enhance the data throughput of serial I/O interfaces since the advent of the monolithic PLL implemented with complementary metal-oxide semiconductor (CMOS) technology in the late 1980s. Below is the summary of three fundamental properties of the PLL:

- Zero-frequency error
- High-Q auto-tracking BPF
- Phase synchronization

With those three features, the PLL has been employed for diverse communication systems. We briefly introduce several applications of the PLL, and some key applications will be discussed in detail in later chapters.

1.2.1 Frequency Synthesis

Since the PLL enables the zero-frequency offset between a reference clock and a feedback clock, this feature can be used to generate multiple output frequencies by adding counters in the reference clock path and the feedback clock path of the PLL. As depicted in Fig. 1.2(a), with a fixed reference frequency f_{ref}, the output frequency f_{out} can be set by simply changing the counting values of the digital counters, that is, M and N in the reference-path and the feedback-path counters, respectively. Then, we obtain f_{out} given by $N \times (f_{\text{ref}}/M)$ since the feedback frequency $(=f_{\text{out}}/N)$ must be equal to the phase-detector frequency f_{PD} $(=f_{\text{ref}}/M)$ after the phase-lock. Therefore, the frequency accuracy of the PLL is as good as that of the stable reference source which is typically a crystal oscillator.

1.2.2 Clock-and-Data Recovery

There are three main roles of the PLL for CDR systems. Firstly, a phase detector of the PLL directly extracts a clock information from a non-return-to-zero (NRZ) data without requiring other nonlinear circuits such as a differentiator followed by a squarer as done in traditional CDR systems. Secondly, the PLL acts as a high-Q

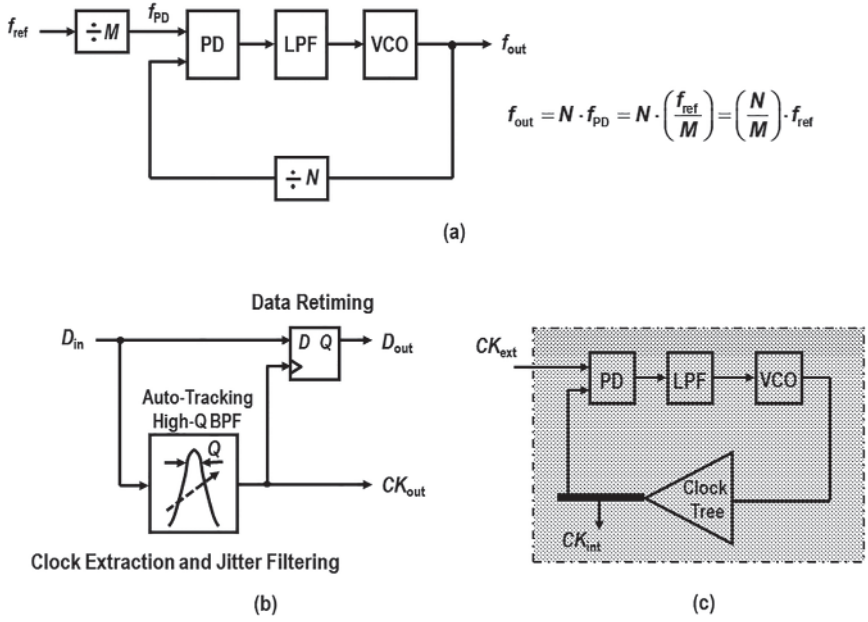

Figure 1.2 Three key applications of the PLL: (a) frequency synthesis; (b) CDR; and (c) synchronization.

auto-tracking band-pass filter to recover a clean clock from noisy incoming data by rejecting high-frequency jitter. Thirdly, the PLL recovers the data by re-timing the data with the extracted clean clock. The data retiming is normally performed with a D-type flip-flop (DFF). The phase-lock feature is also utilized for the data re-timing. For example, the falling edge of a recovered clock is used to trigger the DFF when the transition edge of the NRZ data is synchronized to the rising edge of the recovered clock, which gives an optimum clock position for bit slicing, i.e. data retiming as illustrated in Fig. 1.2(b).

1.2.3 Synchronization

Clock jitter has become more important than ever for input/output (I/O) links in recent chip-to-chip communications as clock speed increases. In addition to the clock jitter, a clock skew between an internal clock and an external clock is a concern with high clock frequency. The delay variation due to a big clock tree in a chip significantly increases a worst-case clock skew, making available phase margin much less than expected. By having the clock tree as the part of a PLL, the clock skew variation between the external clock CK_{ext} and the internal clock CK_{int} due to the clock tree can be minimized as illustrated in Fig. 1.2(c). Since the

frequency offset is negligible in the chip-to-chip communication, a delay-locked loop (DLL) having a voltage-controlled delay line can also be used to achieve better power supply rejection and more flexible clock control than the PLL.

1.2.4 Modulation and Demodulation

In modern transceiver systems, the PLL plays an important role not only as a local oscillator but also as a frequency/phase modulator. These days, digital frequency/phase modulation based on a fractional-N PLL, as shown in Fig. 1.3(a), greatly simplifies the transmitter architecture. We will discuss how a direct-digital modulation is achieved by the PLL in Chapter 9. Figure 1.3(b) also shows two cases of an FM demodulator and a PM demodulator. For the modulations and the frequency demodulation, the bandwidth of the PLL needs to be wide enough to track the frequency/phase variation. To the contrary, a very narrow bandwidth of the PLL is required to provide an averaged reference phase over a frequency drift for the phase demodulation. The narrow-bandwidth PLL is not desirable for an on-chip design as the phase noise contribution of a VCO becomes too high, which will be learned later.

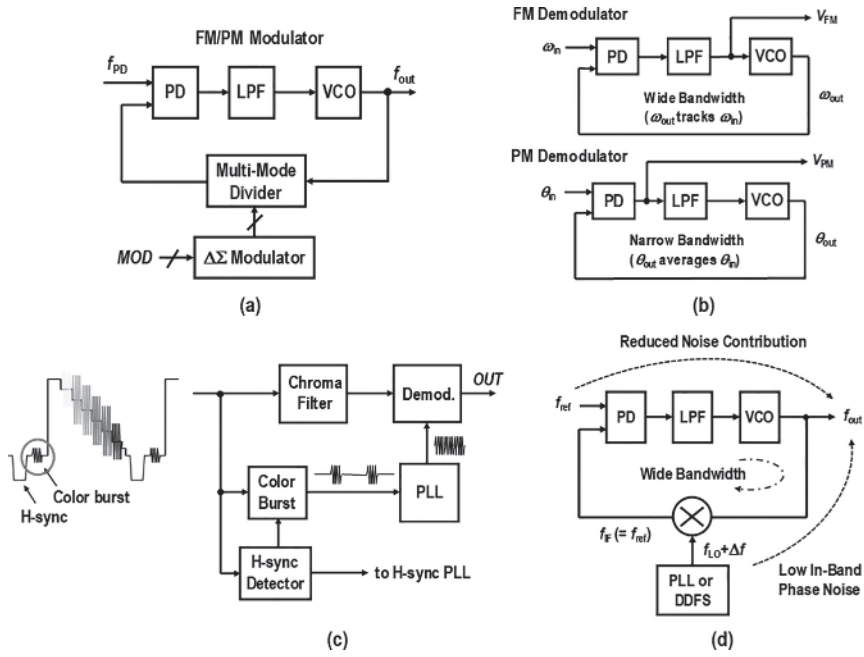

Figure 1.3 Other applications: (a) modulation; (b) demodulation; (c) carrier recovery and (d) frequency translation.

1.2.5 Carrier Recovery

A good example of a PLL-based carrier recovery system can be found in analog television systems. Figure 1.3(c) shows the simplified block diagram of a color-signal demodulator. A color-burst signal is embedded as a sub-carrier and used as a reference phase for the color-signal demodulation. The PLL generates a reference clock whose phase is synchronized to that of the color-burst signal. The phase difference between each color signal and the reference clock is used to provide different color information. Therefore, a narrow-bandwidth PLL using a highly stable VCO such as a voltage-controlled crystal oscillator (VCXO) is designed. In addition to the carrier recovery, additional PLLs are used for horizontal synchronization (*H*-sync) and vertical synchronization (*V*-sync) in the analog television system. Since the PLL was a versatile building block in the television system for mass production, many practical architectures and circuit techniques were developed, including a phase-frequency detector (PFD), a charge-pump PLL, an all-digital PLL with a numerically controlled oscillator (NCO), and so on.

1.2.6 Frequency Translation

A frequency-translation circuit offers a flexible frequency planning for frequency generation systems. As shown in Fig. 1.3(d), instead of having a large-value frequency divider, a mixer is put in a feedback path with another local oscillator (LO), making a phase-detector frequency f_{PD} become an intermediate frequency f_{IF}. Therefore, an LO frequency (f_{LO}) is effectively translated to a desired output frequency. With a high f_{PD} and the absence of a frequency divider, a wide-bandwidth PLL can be designed with low phase noise contribution from the LO and the reference source. Figure 1.3(d) shows an example of how a low-noise frequency synthesizer is implemented with the frequency-translation loop where fine frequency resolution is achieved by having another PLL or a direct-digital frequency synthesizer as the LO.

1.3 Organization and Scope of the Book

This book consists of four major parts, covering basic theories, system and application perspectives, circuit design aspects, and PLL architectures. In the first part, the essential basics of the PLL for circuit designers are described. The linear and transient behaviors of the PLL are discussed in Chapters 2 and 3, respectively. In the second part, Chapter 4 describes system design parameters by discussing the relationship between clock and frequency in the time and frequency domains. Based on the system knowledge gained from previous chapters, Chapter 5

discusses system perspectives for three key applications; frequency synthesis, clock-and-data recovery, and synchronization. The content of Chapter 5 is rather advanced and can be considered a reference for Chapters 9 and 11. Chapters 6–8 of the third part describe building blocks, putting emphasis on basic operation principles and practical design aspects for integrated circuit design. In the last part, various PLL architectures for different applications are discussed. We begin with fractional-N PLL architectures in Chapter 9, move to digital-intensive PLL architectures in Chapter 10, and discuss CDR PLL architectures in Chapter 11. This book puts more weight on the traditional PLL architectures and their analyses for frequency generation and expands the discussion of circuits and design trade-offs for other PLL architectures. This is not the thick PLL book that contains all details of system theories and circuit details but could be one of the PLL books that cover essential materials with balanced system perspectives and circuit design aspects for circuit and system designers. Other valuable resources are listed below.

Bibliography

1 R. E. Best, *Phase-Locked Loops: Design, Simulation, and Applications*, 5th ed., McGraw-Hill, New York, 2003.
2 W. Egan, *Frequency Synthesis by Phase Lock*, 2nd ed., Wiley, New York, 2000.
3 W. Egan, *Phase-Locked Basics*, 2nd ed., Wiley, Hoboken, NJ, 2008.
4 K. Feher, *Telecommunications Measurements, Analysis, and Instrumentation*, Prentice-Hall, Englewood Cliffs, NJ, 1987.
5 F. M. Gardner, *Phaselock Techniques*, 3rd ed., Wiley, Hoboken, NJ, 2005.
6 V. F. Kroupa, *Frequency Synthesis: Theory, Design et Applications*, Wiley, New York, 1973.
7 V. F. Kroupa, *Phase Lock Loops and Frequency Synthesis*, Wiley, Hoboken, NJ, 2007.
8 T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, United Kingdom, 1997.
9 W. C. Lindsey and C. M. Chie (eds), *Phase-Locked Loops*, IEEE Press, New York, 1986.
10 V. Manassewitsch, *Frequency Synthesizers, Theory and Design*, 3rd ed., Wiley, New York, NY, 1987.
11 H. Meyr and G. Ascheid, *Synchronization in Digital Communications, Phase-, Frequency-Locked Loops, and Amplitude Control*, Wiley, New York, 1990.
12 B. Razavi (ed.), *Monolithic Phase-Locked Loops and Clock Recovery Circuits*, IEEE Press, New York, 1996.

13 B. Razavi (ed.), *Phase-Locking in High-Performance Systems*, IEEE Press, New York, and Hoboken, NJ: Wiley, 2003.

14 B. Razavi, *RF Microelectornics*, 2nd ed., Prentice Hall, Upper Saddle River, NJ, 2012.

15 B. Razavi, *Design of Integrated Circuits for Optical Communications*, Wiley, New York, 2012.

16 B. Razavi, *Design of CMOS Phase-Locked Loops: From Circuit Level to Architecture Level*, Cambridge University Press, United Kingdom, 2020.

17 W. Rhee (ed.), *Phase-Locked Frequency Generation and Clocking: Architectures and Circuits for Modern Wireless and Wireline Systems*, The Institution of Engineering and Technology, United Kingdom, 2020.

18 U. L. Rohde, *Microwave and Wireless Frequency Synthesizers: Theory and Design*, Wiley, New York, 1997.

19 K. Shu and E. Sanchez-Sinencio, *CMOS PLL Synthesizers; Analysis and Design*, Springer, New York, 2005.

20 R. B. Staszewski and P. T. Balsara, *All-Digital Frequency Synthesizer in Deep-Submicron CMOS*, Wiley, Hoboken, NJ, 2006.

21 D. H. Wolaver, *Phase-Locked Loop Circuit Design*, Prentice Hall, Englewood Cliffs, NJ, 1991.