1

Fundamentals of Analog-to-Digital Data Converters (ADCs)

Sensors are devices which convert physical phenomena (sound, light, temperature, and others) into another signal, usually an electrical one. There are hundreds of applications for sensors in measurements and instrumentation, biomedical and environmental applications, Internet of Things (IoT), image sensors, and many more. In most cases, the electric output of the sensor is transmitted to a computer through an *analog interface*. This interface (often called *analog front-end or* AFE) may be used to amplify the sensor's output signal and to filter out unwanted noise from it. In most cases, it is followed by an *analog-to-digital data converter* (ADC) used to convert the AFE output into a digital form suitable for digital signal processing by a follow-up computer. The detailed structure of the AFE depends on the properties of the sensor output signal and on the application of the sensor. Figure 1.1 illustrates the block diagram of a sensor and its AFE. In this chapter, the fundamental principles of ADC are discussed, and an introduction to some high-accuracy data converters will be given.

1.1 Performance Parameters for Analog-to-Digital Converters

The ADC is often the most complex and critical part of the signal chain. Its specifications, as for those of the AFE, may vary widely, depending on the sensor signal and on the application of the device. Figure 1.2 illustrates the operation of an ADC. The input is an analog signal V_{in}, while the digital output D_{out} is a sequence of numbers which is the digital representation of V_{in}. The input–output relation is

$$V_{\text{ref}} \cdot D_{\text{out}} = V_{\text{in}} + V_{\text{q}} \tag{1.1}$$

Here, V_{ref} is the *reference voltage* of the converter, and V_{q} is the *quantization error*. The quantization error cannot be avoided, since V_{in} may take on *any value*

Incremental Data Converters for Sensor Interfaces, First Edition. Chia-Hung Chen and Gabor C. Temes.

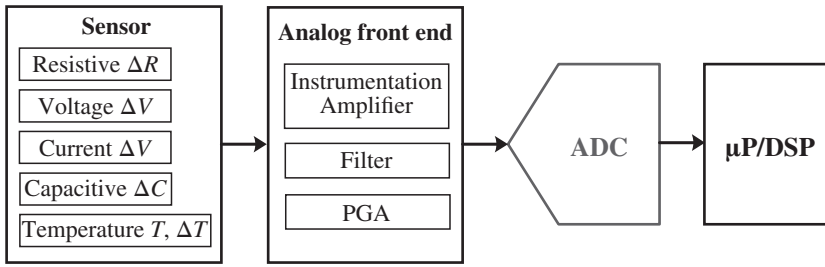

Figure 1.1 Analog front-end for sensor interface.

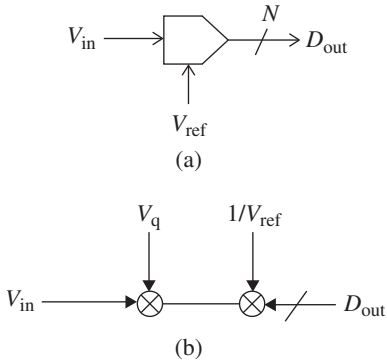

Figure 1.2 (a) The symbol of an ADC; (b) a simple ADC model.

within its range, while the digital signal is the sum of its bits (binary-weighted digits), and hence, it can only assume a *finite number of values*. The symbol of the ADC is shown in Figure 1.2, along with a simple model based on Eq. (1.1).

Figure 1.3 illustrates the normalized input–output characteristics of two M-level ADCs. $V_{ref} = 1\,V$ is assumed. Both ADCs are *bipolar*, i.e. able to convert both positive and negative inputs. Both have M steps and $M+1$ levels. The *resolution* of an M-step converter in bits is given by $N = \log_2(M+1)$. The 45° line $k \cdot y$ shows the accurate output values which an infinite resolution ADC would provide for $V_{ref} = 1\,V$. The *least significant bit* value in the figure is $V_{LSB} = \Delta = 2$. The figure shows that in a range of the input range $-(M+1) < y < (M+1)$, the magnitude of quantization error $e = v - y$ satisfies $|e| < \Delta/2 = 1$. This is the *linear input range* of the ADC.

The difference between the two ADCs shown in Figure 1.3 lies in the location of the origin on the curves. For *the mid-rise quantizer*, it lies at a transition point; for *the mid-tread converter*, it lies in the middle of a flat portion (tread) of the curve. This difference may make the choice between the two options often obvious. The mid-tread ADC is less sensitive to noise, which is often an important advantage. However, if the ADC is used as a *quantizer* in a feedback loop (as is

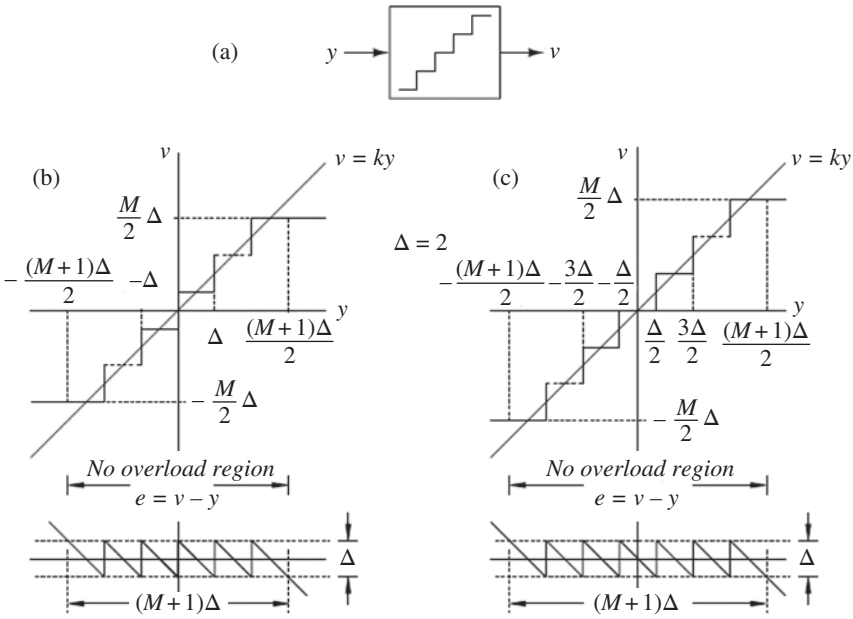

Figure 1.3 Normalized analog-to-digital converter transfer and error curves for a bipolar M-step ADC: (a) symbol; (b) curves for a mid-rise ADC; and (c) curves for a mid-tread ADC. The least significant bit value is $V_{LSB} = \Delta = 2$, and the slope is $k = 1/V_{ref} = 1$.

the case for a delta-sigma or incremental ADC), for very small input signals the mid-tread converter will not be able to change its output from zero, and an undesirable "dead zone" is created in the over-all transfer function.

Clearly, the conversion error $V_q = y - v$ is a *causal* variable, which can be found exactly from the ADC characteristic and the analog input in every clock period by analysis or simulation. However, to get a fast estimate of the expected performance, often we are treating the error as a *random white noise with a zero mean*. Its assumed mean square value can be derived by presuming that the probability of the error values outside the range $-V_{LSB}/2 < V_q < V_{LSB}/2$ is zero, and within that range it has a constant value. These approximations will be valid if the analog input of the quantizer varies sufficiently rapidly, so that the output code changes in almost every clock period. Under these conditions, the mean square value of V_q is given by

$$\sigma_q{}^2 = V_{LSB}{}^2/12 \tag{1.2}$$

The mean square value of V_{in} of a full-scale sine-wave signal is $\sigma_S = \frac{(2^N V_{LSB})^2}{8}$, and therefore, the signal-to-quantization-noise ratio (SQNR) is

$$\text{SQNR} = 10 \cdot \log\left(\sigma_s{}^2/\sigma_q{}^2\right) = 6.02\,N + 1.76\,(\text{dB}) \tag{1.3}$$

In addition to the SQNR, there are several parameters which can be used to characterize the performance of an ADC. These include its *zero error* and *gain error*. The zero error is the error of the first transition voltage in the input–output characteristic of the ADC. The gain error is the error of the difference between the first and last transition voltages.

Other ADC performance parameters are the *differential* and *integral nonlinearities* (DNL and INL). The DNL is the largest error in the analog step size which can generate a transition in the digital output. Its ideal value is V_{LSB}. The INL is the largest deviation of the characteristics from a straight line drawn from the lowest to the highest value of the characteristics. Notice that in finding the INL and DNL, we disregard the zero and gain errors.

A key performance parameter is the *signal-to-noise plus distortion ratio* (SNDR). It is the ratio of the signal power to the total noise-plus-distortion power. It can be found from

$$\text{SNDR} = 10 \cdot \log \left[\sigma_s^2 / \left(\sigma_q^2 + \sigma_n^2 + \sigma_d^2\right)\right] \tag{1.4}$$

Here, ${\sigma_s}^2$, ${\sigma_n}^2$, and ${\sigma_d}^2$ are the mean square values of the signal, the noise, and the harmonic distortion, respectively. The total mean square error is thus a combination of the errors due to the quantization, the noise, and the nonlinear effects.

The *resolution* of the converter is the number of bits in its output. As shown in Eq. (1.3), it determines the SQNR of the ADC under ideal conditions. An artificially defined quantity, the *effective number of bits* (ENOB) is often used to characterize the performance of the nonideal ADC. The ENOB is the resolution (number of bits) of a *fictitious converter*, which has the same SNDR as the actual one *but is subject only to quantization error*. It can be obtained from Eq. (1.3) as ENOB = (SNDR – 1.76)/6.02.

Yet another important characteristic of the ADC is its *spurious free dynamic range* (SFDR). For a sine-wave input signal, the output spectrum of the ADC will contain a spectral line at the input frequency, and also other spurious lines caused by harmonic distortion, intermodulation, and other nonlinear effects. The difference between the signal and the largest spurious line, expressed in dB, is its SFDR.

1.2 Algorithms and Architectures for Analog-to-Digital Converters

There are many methods for performing ADC, each suited for a different application. ADCs can be divided into *memoryless* or *Nyquist-rate converters* and *memoried* or *oversampled ADCs*. The key feature of a memoryless converter is that it performs the conversion of each analog sample individually, independent of past

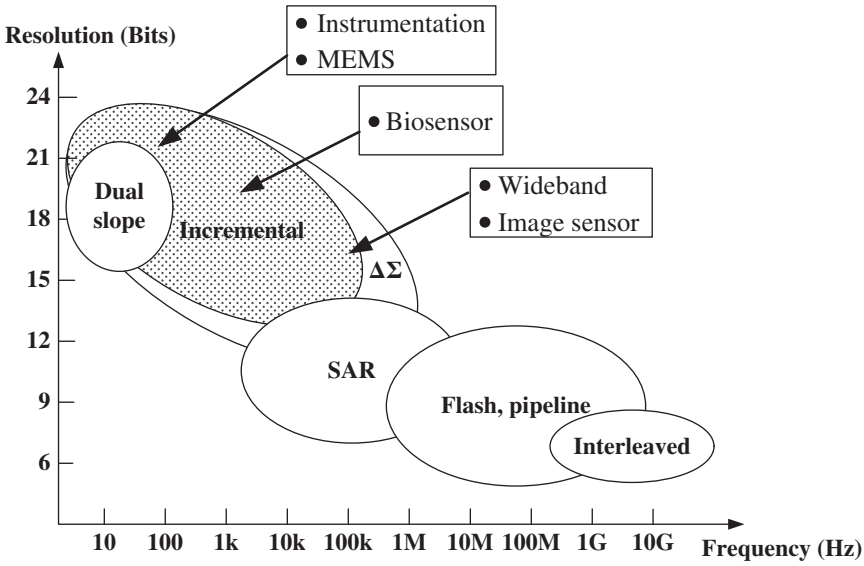

Figure 1.4 Operating regions of ADCs.

inputs. Thus, it is a *one-to-one conversion*. In a memoried ADC, the n^{th} digital output $D(n)$ depends on the history of *all analog inputs* from the first (power-up) input $V_{\text{in}}(0)$ to the current one $V_{\text{in}}(n)$. Note that the "Nyquist-rate" converter cannot in fact sample the analog input at the true Nyquist rate f_{N} (which is defined as twice the signal bandwidth [BW]) without introducing aliasing. This is due to the imperfect antialiasing filter. Hence, the input sampling is often performed at two to four times the Nyquist rate. The *oversampled converters* may sample the input at a sampling rate f_{s}, which may be many times (hundreds of times) faster than f_{N}.

The many applications of ADCs led to many different implementations. They vary in their accuracy, speed, and power requirements. With practical limits on the complexity, power dissipation, and chip area of the circuit, a trade-off exists between speed and accuracy. Figure 1.4 illustrates the typical regions of performance for a few important ADC types.

There are many excellent textbooks which discuss most of these ADC realizations [1–3]. As Figure 1.4 shows, for high-accuracy ADC conversion of sensor signals, the available options include the *dual-slope, delta-sigma, and incremental* configurations. They will be briefly discussed next.

1.2.1 Dual-Slope (Integrating) ADCs

The block diagram of the dual-slope converter is shown in Figure 1.5. The input voltage V_{in} is integrated for N_1 clock periods, so the voltage V_x reaches the value

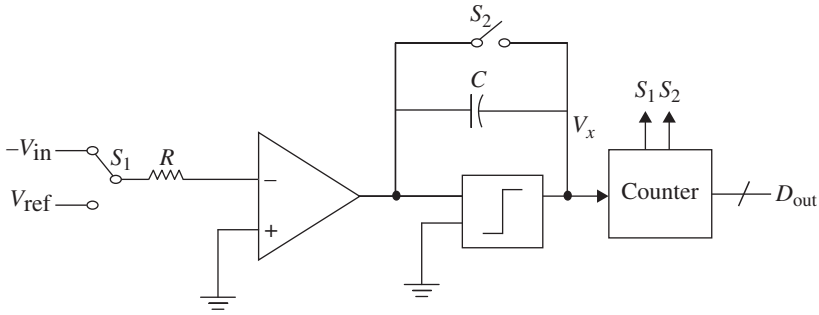

Figure 1.5 A dual-slope analog-to-digital converter.

$V_{in} \cdot N_1 \cdot T/(R \cdot C)$, where T is the clock period. Afterward, V_{ref} is integrated, causing V_x to drop by $V_{ref} \cdot T/(R \cdot C)$ in every clock period. This process is stopped after N_2 clock periods when V_x drops below 0, as detected by the comparator. The total drop is $V_{ref} \cdot N_2 \cdot T/(R \cdot C)$. Since the rise and drop are approximately equal, the relation $V_{in} \cdot N_1 \sim V_{ref} \cdot N_2$ results, giving $V_{in} \sim V_{ref} \cdot N_2/N_1$. Note that there is an error in this estimation of V_{in}, which can be as large as $V_{ref} \cdot T/(R \cdot C)$. To make this error less than the least-significant-bit (LSB) voltage for an N-bit conversion, $N_2 > 2^N$ is required. For high-accuracy ADC, this requires very long conversion time.

As the equations show, the conversion of V_{in} does not depend on the R and C values. However, it is affected by the linearity of the integration, and thus on the finite gain of the amplifier. It is also affected by its offset. Both effects can be mitigated by using circuit techniques, such as correlated double sampling.

A useful feature of the dual-slope ADC is that it can suppress some periodic noises, such as line noise ("hum") at its input. If the frequency of the noise is an integer multiple $1/(N_1 \cdot T)$, then it cancels during the input integration period.

The dual-slope ADC converts each input sample independently from the history of the ADC. It is thus a memory-less data converter.

1.2.2 Delta-Sigma A/D Converters

By allowing memory to play a role in the conversion process, the achievable accuracy within a fixed time period can be greatly enhanced. A popular architecture, which can achieve very high accuracy efficiently, is the *sampled-data delta-sigma* ADC (Figure 1.6a). The ΔΣ ADC consists of a feedback loop containing a sampled-data analog loop filter $H(z)$, a quantizer Q, and a D/A converter. The purpose of the loop is to force the spectrum of the digital output $D(z)$ to match that of the sampled analog input $V_{in}(z)$ in the signal band. To achieve this, the gain of $H(z)$ must be very large in this band. By treating the quantization error as an added

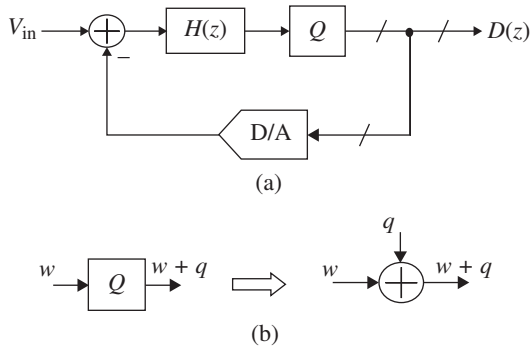

Figure 1.6 (a) The delta-sigma ADC; (b) Quantizer model.

white noise $Q(z)$ (Figure 1.6b), and assuming that the digital-to-analog converter (DAC) is ideal with a reference voltage $V_{ref} = 1$, linear analysis can be used. It gives

$$D(z) = H \cdot V_{in}/(H + 1) + Q(z)/(H + 1) \tag{1.5}$$

Equation (1.5) confirms that at frequencies where $|H(z)| \gg 1$, $D(n) \sim V_{in}$, and $Q(s) \sim 0$. The choice of $H(z)$ is limited by the stability requirements of the feedback loop. Generally, outside of the signal band $|H|$ decreases, and hence, the quantization noise increases in the output.

In the system shown in Figure 1.6a, the quantizer and the DAC are necessarily sampled-data stages, while the input branch and the loop filter may be either sampled-data or continuous-time circuits. In the first case, linear analysis needs the use of the z-transform. Then Eq. (1.5) becomes

$$D(z) = H(z) \cdot V_{in}(z)/(H(z) + 1) + Q(z)/(H(z) + 1) \tag{1.6}$$

The quantization error $Q(z)$ depends on the input w of the quantizer and thus on the input signal $V_{in}(z)$. However, as discussed earlier, an estimate of the expected performance may be obtained by assuming that $Q(z)$ can be represented by an independent random signal, with its mean square value given by Eq. (1.2). We also assume that the mean value of quantization "noise" is zero, and its spectrum is white. Then we may define the *signal transfer function* (STF)

$$\text{STF} = D(z)/V_{in}(z)\big|_{Q=0} = H(z)/(H(z) + 1) \tag{1.7}$$

and the *noise transfer function* (NTF)

$$\text{NTF} = D(z)/Q(z)|_{V\text{in}=0} = 1/(H(z) + 1) \tag{1.8}$$

In the following discussions, we shall assume that the input signal is in the baseband starting at DC, and its BW (Nyquist frequency f_B) is much lower than the clock rate. Then, by choosing $H(z)$ as a low-pass filter function with $|H(z)| \gg 1$ in the signal band, the desirable conditions $|\text{STF}| \sim 1$ and $|\text{NTF}| \ll 1$

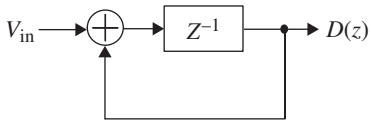

Figure 1.7 Sampled-date integrator (accumulator).

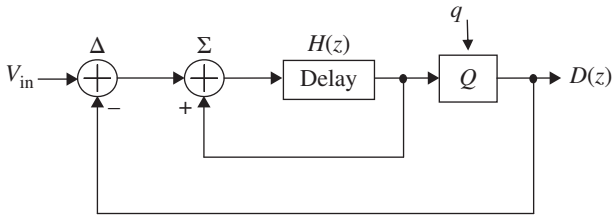

Figure 1.8 A first-order ΔΣ ADC (MOD1).

result from Eqs. (1.7) and (1.8). The simplest choice for a sampled-data filter is the accumulator shown in Figure 1.7. Its transfer function is

$$H(z) = z^{-1}/(1 - z^{-1}) \tag{1.9}$$

The resulting circuit of the ΔΣ ADC is shown in Figure 1.8. (This circuit explains the adjective ΔΣ given to this ADC, since it contains a differencing stage Δ followed by an accumulation one (Σ).)

Substituting the transfer function of Eq. (1.9) into the functions defined in Eqs. (1.7) and (1.8) gives

$$\text{STF} = z^{-1} \tag{1.10}$$

and

$$\text{NTF} = 1 - z^{-1} \tag{1.11}$$

Thus, the STF is simply a delay by a clock period T. The squared magnitude of the frequency response of the NTF is obtained by substituting $z = e^{j\omega T}$ and finding $|\text{NTF}|^2$. This results in

$$|\text{NTF}|^2 = [2 \cdot \sin(\pi f T)]^2 \tag{1.12}$$

Figure 1.9 shows the response of $|\text{NTF}|^2$ as a function of f.

To estimate the *in-band noise power* in the output signal, we need to integrate the power spectrum of the quantization noise at the output over the signal band 0 to f_B. Assuming that the noise is white, its power spectral density is ${V_q}^2 \cdot 2T = {V_{LSB}}^2 \cdot T/6$. The in-band noise power is then

$$N_q^2 = \int_0^{f_B} \frac{V_{LSB}^2 T}{6} 4 \sin^2(\pi f T) \mathrm{d}f \tag{1.13}$$

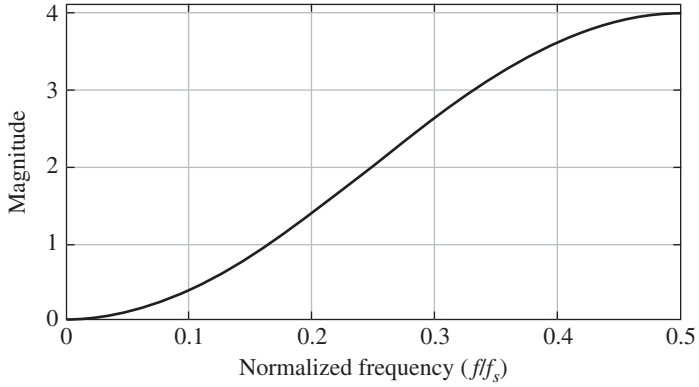

Figure 1.9 The frequency response of $|\mathrm{NTF}|^2$.

Usually, the sampling frequency $f_s = 1/T$ is much higher than the Nyquist frequency f_B. Thus, the *oversampling ratio,* $\mathrm{OSR} = f_s/2f_B$, is much larger than 1. Therefore, in the baseband the inequalities $f \cdot T < f_B/f_s \ll 1$ hold. This allows the use of the approximation $\sin^2(\pi f T) \sim (\pi f T)^2$ in Eq. (1.13), resulting in the relation given in Eq. (1.14).

$$N_q^2 \cong \frac{2}{3} V_{\mathrm{LSB}}^2 \mathrm{T} \int_0^{f_B} \pi^2 f^2 T^2 \mathrm{d}f = \frac{\pi^2}{36} \frac{V_{\mathrm{LSB}}^2}{\mathrm{OSR}^3} \tag{1.14}$$

Equation (1.14) shows that the in-band noise may be decreased by reducing V_{LSB} and increasing the OSR. Doubling the OSR reduces the in-band noise by 9 dB, and increases the SQNR by 1.5 bit. But the efficiency of this noise shaping is low. For a single-bit quantizer, it requires an OSR over 1000 to obtain an SQNR of 96 dB. To improve the effectiveness of noise shaping, higher-order loop filters may be implemented. Figure 1.10 shows a ΔΣ ADC MOD2 with a second-order loop filter. Linear analysis gives

$$\mathrm{STF} = z^{-2} \tag{1.15}$$

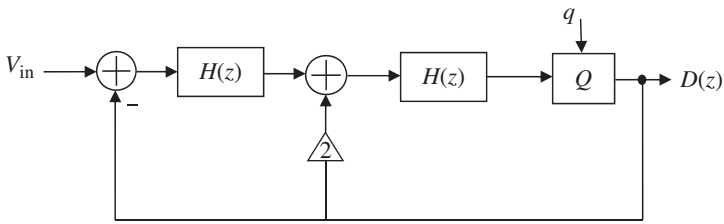

Figure 1.10 A second-order ΔΣ ADC.

and

$$\mathrm{NTF} = (1 - z^{-1})^2 \tag{1.16}$$

The STF is now a delay by *two* clock periods $2T$. The squared magnitude of the frequency response of the NTF is obtained by substituting $z = e^{j\omega T}$. The result is

$$|\mathrm{NTF}|^2 = [2 \cdot \sin(\pi f T)]^4 \tag{1.17}$$

The in-band quantization noise is now reduced by 15 dB, and the ENOB is increased by 2.5 bits if the sampling rate is doubled. An SQNR of 96 dB now requires only OSR = 128 for a single-bit quantizer. This is often acceptable.

The derivations provided for the first- and second-order delta-sigma ADCs may be generalized for the case of an L^{th}-order ADC with an N-bit quantizer, and a given OSR. The resulting formula (valid for OSR $\gg 1$) is given in Eq. (1.18):

$$\mathrm{SQNR}_{\max} \approx 6.02N + 1.76 + (2L+1)10\log_{10}\mathrm{OSR} - 10\log_{10}\frac{\pi^{2L}}{2L+1}[\mathrm{dB}] \tag{1.18}$$

The first term is the SQNR of the quantizer Q functioning alone, and the other two terms show the added contribution of the noise-shaping loop.

By increasing the order of the loop filter or the resolution of the quantizer of the ΔΣ ADC, and/or by increasing its OSR, the in-band noise may be reduced and the SQNR increased. However, there are inherent nonideal effects which will still limit the performance. The most important ones are listed below:

1. For $N > 1$, both differential and integral nonlinearities will occur in the DAC. This is due mostly to the mismatch errors of the DAC elements, and it causes harmonic distortion of the input signal. To mitigate this requires adding fairly complicated analog and digital circuitry, as shown in Chapter 2.
2. For $L > 2$, the stability of the feedback loop is not guaranteed and needs attention.
3. The power dissipation of the ADC increases approximately linearly with the OSR. The design of the active elements may also become difficult for high f_s.
4. The unavoidable correlation between the input of ADC and the quantization error neglected thus far may introduce large errors. These include the generation of *idle tones* and *dead zones*, to be described next.

There are various techniques available for mitigating the impact of these effects. Specifically, the linearity of the N-bit DAC may be improved by *dynamic element matching*. This is most easily applied to *unary DACs*, which are constructed by $2^N - 1$ equal-valued elements. For an input code of value D to the DAC then D unit elements are activated. By choosing these differently each time the same code appears, and averaging the results for many occurrences, the nonlinearity error may be converted into a white noise, or preferably into an appropriately filtered noise [4–6].

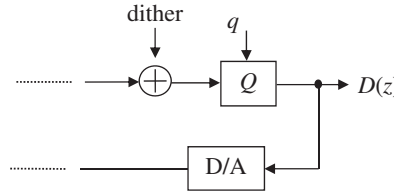

Figure 1.11 Dithering.

An alternative technique for mitigating DAC mismatches is *digital correction*. This acquires and stores the DAC errors for all possible input codes, and corrects them as they occur [7].

The stability of higher-order ΔΣ ADCs may be assured by an appropriate choice of the parameters of their NTF, such as their peak out-of-band gain. The process is discussed in Ref. [8] and will be described in Chapter 2.

Idle tones are generated for dc inputs which are rationally related to the quantizer's reference voltage, so that $V_{\text{in}} = (n/m)V_{\text{ref}}$. Here, n and m are integers and for stability $n < m$. As an illustration, assume $n = 1$ and $m = 4$, and let $V_{\text{ref}} = 1$ V. The quantizer outputs will be 0 or 1. Since the ideal NTF = 0 at dc, in steady state the output signal must have an average value of ¼. This will be the case if the sequence of the output values will be 0,0,0,1, 0,0,0,1, ... This output sequence is thus periodic, with a period of $f_s/4$. For high OSR, the tone generated will be out of the signal range, and hence, will not affect the signal-to-noise ratio (SNR) of the ADC. However, assume next that $n = 3$ and $m = 1000$. The tone generated now will have a frequency of $3f_s/1000$, which is likely to be in the signal band, greatly reducing the SNR.

Idle tone generation may be prevented by introducing a *dither* signal in front of the quantizer (Figure 1.11). This may be a random noise or an out-of-band signal. It is used to reduce or eliminate the causal relation between V_{in} and the quantization error q. To be effective, its amplitude should be larger than $V_{\text{LSB.}}$

Dead zones are input signal intervals, where the digital output does not follow variations of V_{in}. This effect is caused by leakage in the integrators of the loop due to the finite dc gain of the amplifiers used. It occurs when the charge provided by the input is less than the leaking charge.

Fortunately, tone generation and dead zones are both less likely to occur in higher-order ΔΣ ADCs and/or in the incremental ADCs which are the main subjects of this work.

1.2.3 Successive Approximation A/D Converters

The block diagram of an ADC with reduced accuracy but lower power and higher speed is shown in Figure 1.12 [1]. It is sometimes used as the quantizer of a ΔΣ or incremental ADC. The conversion scheme is based on gradually reducing the range which contains the estimated value of the analog input signal V_{in}.

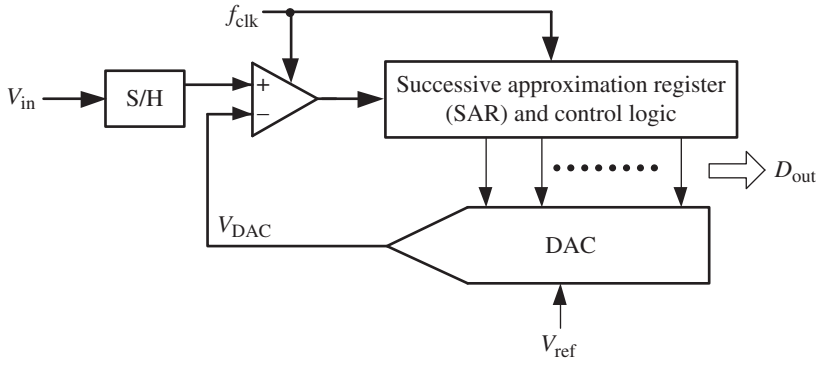

Figure 1.12 The successful approximation ADC. Source: Adapted from Carusone et al. [1].

For unipolar (positive only) conversion, assume that $0 < V_{in} < V_{ref}$. To find out whether V_{in} is in the upper or lower half of this range, it is compared with $V_{D/A} = V_{ref}/2$. The result of this comparison also provides the most significant bit b_1 of the output word. Next, it will be determined whether V_{in} is in the upper or lower half of reduced range. This can be found out by a second comparison with $(3/4)V_{ref}$ if the most significant bit (MSB) was 1, and with $(1/4)V_{ref}$ if it was 0. This reduces the range in which V_{in} must be by another factor of 2. Progressing this way for N clock periods, the N bits of the output word are obtained with an accuracy of $V_{LSB}/2$. This converter is often called *SAR ADC,* after the *successive approximation register* (SAR) used in its digital logic.

An efficient implementation of the successive approximation ADC is illustrated in Figure 1.13 for $N = 5$ bits [1]. It uses a binary-weighted capacitor array to carry out the conversion in three steps. In the *sampling step*, $V_{in} - V_{os}$ is stored in all capacitors, where V_{os} is the input offset of the opamp used here as a comparator. In the *holding* step, all capacitors hold their charge and voltage, but their common-mode voltage is shifted by $-V_{in}$. In the *conversion* phase, positive voltage steps are applied at the input of the opamp in order to compare V_{in} with fractions of V_{ref}. To find the MSB of the digital output, V_{in} is compared with $V_{ref}/2$. This is achieved by switching the bottom plate of the largest capacitor C from ground to V_{ref}. This generates a positive change by $V_{ref}/2$ in $V_{x.}$ The sign of V_x determines the MSB b_1. Next, the modified output V_x is compared with $V_{ref}/4$. This is achieved by switching the bottom plate of second largest capacitor $C/2$ from ground to V_{ref}. This gives the next bit b_2. For 5-bit conversion, the process terminates after V_{in} is compared with $V_{ref}/16$, yielding the LSB.

If the comparator is realized using dynamic biasing, then all power dissipated is due to the charging and discharging of the capacitances in the capacitive DAC and the comparator. This allows the realization of the ADC with very little bias

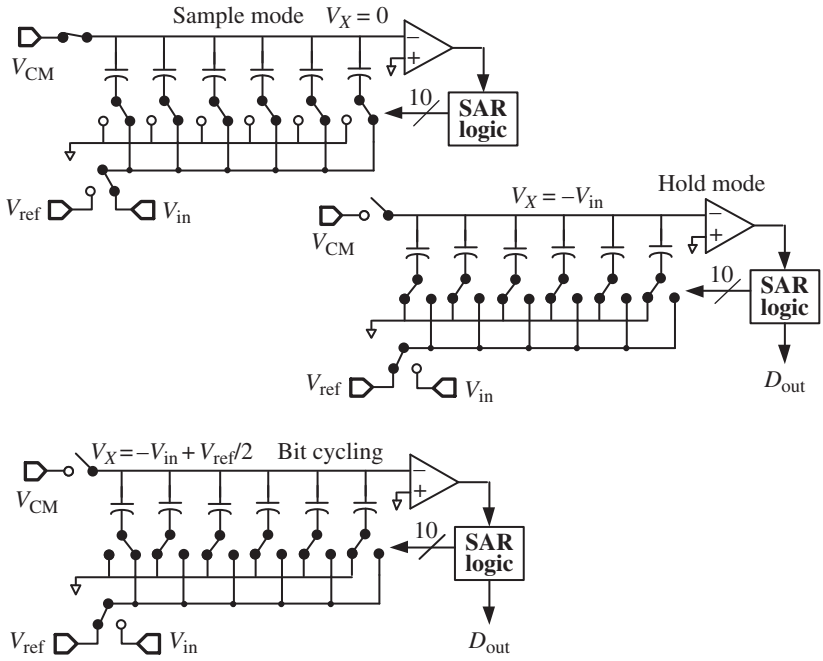

Figure 1.13 5-bit SAR ADC implementation. Source: Adapted from Carusone et al. [1].

power and makes the SAR ADC a very popular realization for micro-power A/D converters. By introducing oversampling, as well as additional capacitors and clock phases, noise-shaping SAR converters of improved accuracy can also be implemented [9, 10].

1.2.4 Flash A/D Converter

The fastest A/D converter is the appropriately named *flash ADC*. In this converter, shown in Figure 1.14 for $N = 3$ bits, the input voltage is simultaneously compared with all possible 2^N reference voltages V_{ri}. Assume that V_{in} is between V_{r3} and V_{r4}. Then the outputs of the bottom three comparators are negative, while those of the top five are positive. This information gives a digital output in the "thermometer" code. It can also readily be converted into a binary-coded digital equivalent of V_{in}.

The flash converter can be used as a stand-alone ADC. It is also often used as the quantizer of a $\Delta\Sigma$ or incremental ADC.

The complete conversion may be finished in 1 or 2 clock periods by a flash ADC, allowing low-resolution operation at very high (Gigasamples/second) conversion

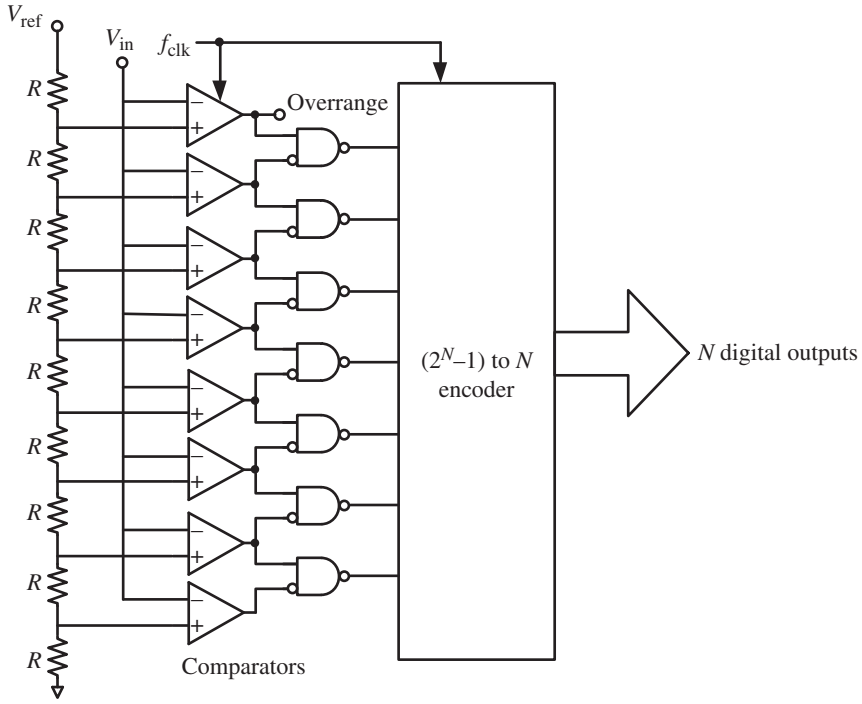

Figure 1.14 Flash A/D converter. Source: Adapted from Carusone et al. [1].

rates. The number of resistors and comparators, however, needs to be very high, around 2^N for N-bit resolution. This limits the practically achieved resolution to about 7 bits. The power dissipation is also high since the resistor string needs to recharge the input voltages of the comparators at a very fast rate. The fast charging operation of the flash ADC may also generate a large amount of noise on the chip, which may adversely affect the operation of analog circuits sharing chip area with the flash ADC.

1.2.5 Incremental A/D Converter

For very high conversion accuracy of low-frequency signals, ΔΣ ADCs are the most popular choice. However, there are applications where some of their shortcomings become critical. A few are listed below:

1. In systems which need many ADCs operating simultaneously, it may be wasteful to implement all of them separately. It then becomes economical to multiplex a single ADC between the channels. However, to multiplex a ΔΣ ADC all energy storage elements (capacitors in the analog loop, registers

in the digital filter) need to be replicated, and connected and disconnected when changing channels. A memoryless ADC by contrast may be multiplexed directly by simply moving it from channel to channel.

2. The digital filter needed in a ΔΣ ADC is usually highly complex since it is required to suppress a large amount of out-of-band quantization noise power. This requires extensive digital circuitry. Also, the high selectivity of the filter introduces a large delay (latency) between its input and output. It can be shown in Ref. [8] that for an L^{th}-order filter, this delay is at least $(L+1)T$, where T is the clock period after decimation. In ADCs used in feedback control systems, such large delay may destabilize the loop. For the modified version of the ΔΣ ADC described next, the digital filter may be designed in the time domain. This allows a simplified structure, and much reduced latency which is only one clock period T.
3. For lower-order ΔΣ ADCs the idle tone generation and dead zones may deteriorate the performance and may require additional circuitry to mitigate. For the modified ADC, the occurrence of idle tones and dead zones is reduced.

To convert the ΔΣ ADC into a memoryless ("Nyquist-rate"), the required modification is simple. The input is sampled, held for a given number of clock periods, and converted by the ΔΣ ADC and a digital filter. The digital result is a sample of the output. After this, all memory elements (capacitors in the analog circuits and registers in the digital ones) are discharged, a new input sample is acquired, and a new digital output sample is produced.

The modified $\Delta\sum$ ADC is often called an *incremental ADC* (IADC). Its properties and basic design principles are discussed in Chapters 2 and 3.

References

1 T. C. Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design,* John Wiley and Sons, New York, 2012.

2 R. van de Plassche, *Integrated Analog-to-Digital and Digital-to-Analog Converters,* Kluwer Academic Publishers, Dordrecht, the Netherlands, 1994.

3 F. Maloberti, *Data Converters*, Springer, Dordrecht, the Netherlands, 2007.

4 R. T. Baird and T. S. Fiez, "Linearity enhancement of multibit A/D and D/A converters using data weighted averaging," *IEEE Transactions on Circuits and Systems-II*, vol. 42, pp. 753–762, Dec. 1995.

5 B. H. Leung and S. Sutarja, "Multibit σ-δ A/D converter incorporating a novel class of dynamic element matching techniques," *IEEE Transactions on Circuits and Systems-II*, vol. 39, pp. 35–51, Jan. 1992.

6 O. J. A. P. Nys and R. K. Henderson, "An analysis of dynamic element matching techniques in sigma-delta modulation," *Circuits and Systems*

Connecting the World. ISCAS 96, Atlanta, GA, USA, vol. 1, pp. 231–234, May 1996.

7 M. Sarhang-Nejad and G. C. Temes, "A high-resolution multibit ΔΣ ADC with digital correction and relaxed amplifier requirements," *IEEE Journal of Solid-State Circuits*, vol. 28, pp. 648–660, Jun. 1993.

8 Pavan, S., Schreier, R. and Temes, G.C., *Understanding Delta-Sigma Data Converters*, second edition, IEEE Press/Wiley Interscience, 2017.

9 J. A. Fredenburg and M. P. Flynn, "A 90-MS/s 11-MHz-bandwidth 62-dB SNDR noise-shaping SAR ADC", *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2898–2904, Dec. 2012.

10 Y.-S. Shu, L.-T. Kuo and T.-Y. Lo, "An oversampling SAR ADC with DAC mismatch error shaping achieving 105 dB SFDR and 101 dB SNDR over 1 kHz BW in 55 nm CMOS", *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2928–2940, Dec. 2016.