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Scaling and Challenge of Si-Based CMOS: Past, Present, and Future

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Abstract

The evolution of silicon-based Complementary Metal-Oxide-Semiconductor (CMOS) technology has been essential in shaping modern semiconductor electronics. The steady scaling of transistors has contributed significantly to this evolution, and the steady development of transistors has enabled the development of high-performance semiconductor chips. In this chapter, we explore the historical scaling advancements in CMOS technology, highlighting the challenges faced in the past and present. Past challenges encompass issues such as short-channel effects and leakage currents, whereas current challenges revolve around power dissipation and quantum effects at nanoscale dimensions. This chapter also discusses potential future innovations, including novel materials, device architectures, and computing paradigms. By addressing these challenges and embracing new technologies, Si-based CMOS has been poised to continue its transformative journey in the semiconductor industry. Even though there are still a couple of issues to be overcome, it seems that CMOS technology is able to continue improving, with the help of material development and fabrication-equipment development. This chapter has been written to understand the basic principles of semiconductors and the demands for improving scaling and subthreshold swing, which are essential for designing FeFETs.

***Keywords*:** Quantum computing, digital twins, technological development, semiconductor industry, semiconductor

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1.1 Introduction to Si-Based CMOS Technology

Silicon-based Complementary Metal-Oxide-Semiconductor (CMOS) technology is a fundamental element in modern semiconductor electronics [1]. Its core principles and ability to scale have significantly advanced the semiconductor industry, leading to unprecedented performance and integration [2]. Gaining a solid understanding of the fundamentals of Si-based CMOS is crucial for recognizing its historical significance and evolutionary trajectory [3].

CMOS technology relies on silicon as its semiconductor material, leveraging its abundance, stability, and well-understood properties to create electronic components [4]. The CMOS architecture comprises complementary pairs of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), specifically NMOS (N-type MOS) and PMOS (P-type MOS). These complementary transistor pairs work together to facilitate efficient switching and logic operation.

A major strength of the Si-based CMOS technology is its scalability. Engineers and researchers have continually pushed the boundaries of miniaturization by reducing transistor dimensions to enhance performance while lowering power consumption [5]. This scaling trend, often associated with Moore's law, has resulted in an exponential growth in transistor density per unit area and improved computational capabilities in electronic devices.

The evolution of Si-based CMOS technology has seen successive generations marked by advancements in fabrication techniques, material innovation, and architectural improvements. From the early days of planar CMOS technology to the development of FinFETs and beyond, the industry has adapted to meet the demands for faster, smaller, and more energy-efficient devices.

Furthermore, Si-based CMOS technology has widespread application in various electronic devices such as microprocessors, memory chips, sensors, and integrated circuits used in communication and computing systems [6–8]. Its versatility and scalability have been instrumental in driving the digital revolution and fostering innovations in areas such as artificial intelligence, the Internet of Things (IoT), and mobile computing.

1.2 Basic Concept of Transistor Scaling

Transistor scaling is a fundamental concept in semiconductor technology, which involves reducing the size of transistors while improving their performance and energy efficiency [9, 10]. This concept is essential for meeting the demands of modern electronic devices that require smaller, faster, and more power-efficient components.

At its core, transistor scaling refers to shrinking the dimensions of transistors, such as the gate length and channel width, to enhance their switching speed and reduce power consumption [11, 12]. The basic idea behind scaling is to pack more transistors onto a semiconductor chip, thereby increasing its computational power and functionality.

One of the key metrics used to quantify transistor scaling is feature size, typically measured in nanometers (nm). As technology advances, feature sizes decrease, allowing more transistors to be integrated into smaller areas [13–18]. This trend, often described by Moore's law, has driven rapid advancements in semiconductor technology over the past few decades. Specifically, as the transistor size decreases, the time constant (T_d) of the transistor can also be decreased (Equations 1.1–1.5). Equations 1.1–1.5 and Figure 1.1 can explain the earlier sentence (I_D, C, V, W, L, and μ represent the drain current, capacitance, voltage applied to MOSFET (V_{DS}), width of MOSFET, length of MOSFE, and electron mobility, respectively).

$$I_D = \frac{C\Delta V}{\Delta t} \tag{1.1}$$

$$T_d = \Delta t = \frac{C\Delta V}{I_D} \tag{1.2}$$

when $V_G - V_T = V_{DD}$,

$$C = C_o * W * L \tag{1.3}$$

$$I_D = \frac{\mu W C_o V_{DD}^2}{2L} \tag{1.4}$$

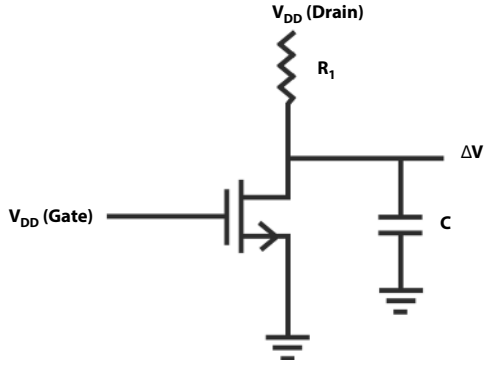

Figure 1.1 Illustration shows the example-circuit for explaining the importance of scaling.

$$T_d = \frac{2L^2}{\mu V_{DD}} \tag{1.5}$$

As shown in Equation 1.5, the length (L) of the transistor decreases and the time constant (T_d) decreases [19–27]. It is important to note that the time constant decreases 'quadratically' as the transistor length decreases. This implies that when the length of the transistor becomes half (1/2), the time constant can be 0.25 times smaller, and therefore the frequency can become four times larger. This implies that the transistor can operate four times faster than before (for example, from 1 GHz to 4 GHz) [28–35].

Transistor scaling provides several advantages for electronic devices. First, smaller transistors have shorter gate lengths, which reduce the time required for signals to propagate through the transistor, leading to faster switching speeds [36–42]. This speed improvement is crucial for high-performance applications, such as microprocessors and memory chips.

Second, scaled transistors typically consume less power during their operation [13–16]. This is due to the reduced leakage currents and improved control over the flow of electrons through the transistor channels [13–15]. Lower power consumption is desirable for extending the battery life in portable devices and reducing the overall energy consumption in large-scale computing systems. However, transistor scaling also poses challenges as the dimensions reach nanoscale. Issues such as leakage currents, short-channel effects, and variability have become more prominent, requiring innovative solutions in transistor design, materials, and fabrication processes [43–49].

In the above paragraph, I explained the importance of scaling by showing the improvement in the speed of the transistor (frequency) and low power consumption [50–56]. However, the recent research shows that it is difficult to improve 'the speed of transistor.' The reason for this can include several self-heating effects in transistors, the generation time of electrons and holes, and power consumption issues [16–18]. Therefore, it seems that many semiconductor companies have recently fabricated multi-core CPU [57–64].

1.3 Past Challenges in Scaling Si-Based CMOS

The scaling of silicon-based Complementary Metal-Oxide-Semiconductor (CMOS) technology has been a remarkable journey, filled with achievements and challenges that must be overcome [65–72]. As engineers and researchers have pushed the limits of miniaturization to improve the performance and integration density, several significant challenges have emerged in the past [73–79].

One of the primary challenges in scaling the Si-based CMOS technology is the onset of short-channel effects. As the transistor dimensions were scaled down, the channel length of MOSFETs became shorter, leading to increased leakage currents and reduced control over the transistor's behavior [80–87]. Short-channel effects limit the performance gains achieved through scaling and require innovative solutions for transistor design and material engineering [19–21].

Another notable challenge is the escalation of power consumption and heat dissipation as transistors become smaller and more densely packed on semiconductor chips [22–26]. This increase in power density poses thermal management challenges, affecting device reliability and overall system performance [27, 28]. Engineers have to develop new thermal management techniques and materials to effectively address these issues [29–34].

Furthermore, as feature sizes approach the nanoscale, variability in transistor characteristics has become a significant concern [35–42]. Process variations during fabrication, inherent material fluctuations, and random dopant fluctuations lead to variations in the transistor performance across a chip and between manufacturing batches [43–47]. Managing and mitigating these variability challenges require advanced modeling, process control, and statistical techniques [48–57].

For further understanding, Figure 1.2 and Equations 1.6–1.9 can be used to explain the effect of scaling on the threshold voltage. As the channel length (L) decreases because of scaling, the threshold voltage usually

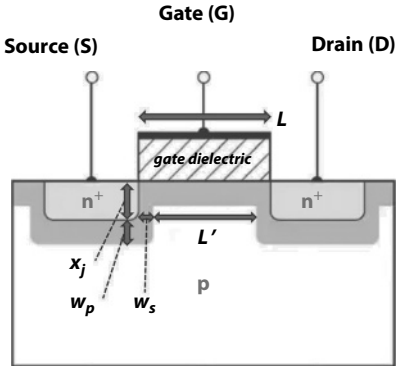

Figure 1.2 Schematic illustration describes the effect of scaling on decrease of threshold voltage.

increases. This phenomenon is often called 'threshold voltage roll-off' [88–93]. In Equations 1.6–1.9, V_T, V_{FB}, Q_d, and C_{ox} represent threshold voltage, flat-band voltage, depletion charge, and oxide-capacitance.

$$V_T = V_{FB} + 2\varphi_F - \frac{Q'_d}{C_{ox}} \tag{1.6}$$

$$Q'_d L = Q_d \frac{L + L'}{2} \tag{1.7}$$

$$(x_j + x_D)^2 = (x_j + w_s)^2 + x_D^2 \tag{1.8}$$

$$V_T = V_{FB} + 2\varphi_F - \frac{Q_d}{C_{ox}}\left[1 - \left(\frac{x_j}{L}\right)\left(\sqrt{1 + 2x_D / x_j} - 1\right)\right] \tag{1.9}$$

Equations 1.6–1.9 explains the decrease of threshold voltage, according to 'charge-sharing model.' According to the charge sharing model, as the channel length decreases, the depletion charges on the source and drain sides are shared [94–99]. Namely, under a long-channel device, it is possible to neglect the depletion region because of the source and drain; however, under a short-channel device, 'the depletion region because of the source and drain' cannot be neglected. Therefore, in short-channel devices, the threshold voltage decreases (Equation 1.9) and the off current (I_{off})

increases. Therefore, short-channel devices consume a significant amount of power [100–106].

Moreover, achieving manufacturability and yield at smaller technology nodes is a challenge. The fabrication of complex integrated circuits with billions of transistors requires highly precise and reliable manufacturing processes. Defects, lithography limitations, and yield issues have become more pronounced as feature sizes decrease, necessitating continuous advancements in manufacturing technology and process optimization [107–112].

Despite these challenges, the semiconductor industry has successfully navigated past hurdles in scaling the Si-based CMOS technology. Innovative solutions such as new transistor architectures (e.g., FinFETs), advanced materials (e.g., high-k dielectrics), process enhancements, and design optimizations play pivotal roles in overcoming past scaling challenges and enabling continued progress in semiconductor technology [113–120].

1.4 Present Challenges and Limitations of Si-Based CMOS

Despite significant advancements in silicon-based Complementary Metal-Oxide-Semiconductor (CMOS) technology over time, there are various challenges and limitations in the current landscape, especially as transistor sizes continue to decrease recently (under 20 nm) and new performance requirements have emerged [121–126].

A primary present challenge for Si-based CMOS technology relates to managing power dissipation and heat. Shrinking transistors and their denser integration on semiconductor chips lead to increased power density and elevated heat generation. This rise in power dissipation not only affects device reliability but also calls for effective thermal management solutions to prevent overheating and maintain optimal operational performance [127–132].

Furthermore, as transistor dimensions approach the atomic scale (under 20 nm), quantum effects become more prominent, presenting significant hurdles for Si-based CMOS devices. Quantum phenomena, such as tunneling, limitations in carrier mobility, and confinement effects, can negatively impact transistor behavior, resulting in performance decline and heightened variability. Tackling these quantum-related challenges requires innovative device designs, novel materials, and advanced fabrication techniques [133–138].

In addition, further scaling in Si-based CMOS technology encounters limitations due to physical constraints. The conventional planar transistor structure reaches its scaling thresholds, leading to issues such as short-channel effects, gate leakage, and subthreshold currents. These limitations impede the continuous reduction of transistor dimensions without compromising the functionality or reliability [139–141].

Another critical limitation is the growing complexity of manufacturing processes at advanced technology nodes. Smaller feature sizes and intricate device structures pose challenges, such as process variability, higher defect density, and the need for enhanced yield optimization. Overcoming these manufacturing hurdles requires substantial investments in research, development, and production technologies [142–145].

1.5 Representative Methods for Scaling MOSFET

Three scaling methods are widely accepted for scaling technologies (Figure 1.3). Constant voltage (CV) scaling, quasi-constant voltage (QCV) scaling, and constant electric field (CE) scaling are representative scaling methods [146, 147]. Each has its own strengths and weaknesses, and their characteristics are shown in Tables 1.1 and 1.2. It is worth noting that CE, CV, and QCV scaling methods have their own strengths and weaknesses (Table 1.2).

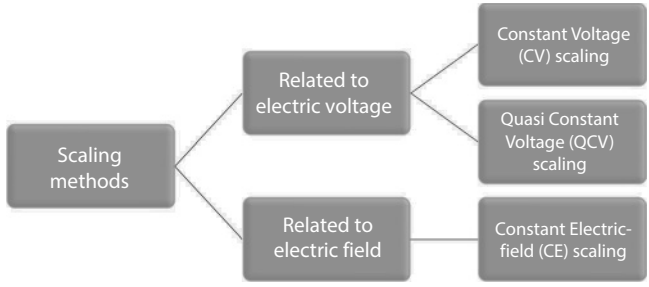

Figure 1.3 Representative methods for MOSFET scaling.

Table 1.1 Explanation of three scaling methods.

Type	Description
CV scaling	Constant voltage scaling is a strategy in which the supply voltage (V_{dd}) is decreased in proportion to the reduction in the transistor feature size. This method aids in lowering the power consumption because the power dissipation in CMOS circuits is directly proportional to the square of the supply voltage. Decreasing the voltage reduces the dynamic power consumption. However, lowering the supply voltage also presents challenges such as heightened sensitivity to process variations and diminished noise margins. Techniques such as adaptive voltage scaling (AVS) and dynamic voltage and frequency scaling (DVFS) are utilized to dynamically adjust the supply voltage based on workload demands, while ensuring performance and energy efficiency.
QCV scaling	Quasi-constant-voltage scaling is a variant of constant-voltage scaling, where the supply voltage is decreased at a slower rate compared to the reduction in feature sizes. This method helps balance the trade-off between power consumption and performance degradation. This allows for some level of voltage scaling, while maintaining acceptable performance levels. Quasi-constant voltage scaling techniques aim to alleviate the impact of reduced voltage on circuit performance by optimizing the circuit design, enhancing transistor characteristics, and employing adaptive control mechanisms.
CE scaling	Constant electric-field scaling is an approach that aims to maintain a constant electric field across the gate oxides of transistors as their dimensions are scaled down. The electric field across the gate oxide influences transistor behavior, including the threshold voltage and subthreshold slope. By preserving a constant electric-field, transistor performance can be maintained or even enhanced despite scaling. This technique requires adjustments to the gate oxide thickness, doping profiles, and device geometries to achieve the desired electric field characteristics while scaling down the transistor dimensions.

Table 1.2 Comparison between three scaling methods.

	CE	**CV**	**QCV**
Linear dimension	1/λ	1/λ	1/λ
Potential	1/λ	1	$1/\lambda^{0.5}$
Electric field	1	λ	$\lambda^{0.5}$
Current	1/λ	λ	1
Power density	1	λ^3	$\lambda^{0.5}$
Capacitance	1/λ	1/λ	1/λ
Impurity concentration	λ	λ	Λ
Gate delay	**1/λ**	**$1/\lambda^2$**	**$1/\lambda^{1.5}$**

1.6 Future Prospects and Innovations in Si-Based CMOS Technology

Several technologies have contributed to potential future advancements and innovations in the Si-based CMOS technology. As these technologies progress simultaneously, the Si-based CMOS technology can continue to evolve and innovate. The key technologies used are summarized in Table 1.3.

1.7 Navigating the Evolution of Si-Based CMOS Technology

The progression of silicon-based Complementary Metal-Oxide-Semiconductor (CMOS) technology has been a dynamic journey characterized by notable advancements and transformative innovations. As we explore the historical, current, and future aspects of Si-based CMOS technology, several fundamental insights have emerged that influence its ongoing development.

Si-based CMOS technology has served as a fundamental pillar in modern semiconductor electronics, driving exceptional levels of performance, integration density, and energy efficiency. The persistent focus on scalability and innovation has propelled the semiconductor industry, facilitating the creation of robust computing systems, communication devices, and sensor technologies.

Table 1.3 Possible methods to realize further scaling in the future.

Categories	Explanation
Novel Materials	The incorporation of new semiconductor materials holds significant promise for overcoming the limitations of Si-based CMOS technology. Materials such as high-k dielectrics can enhance charge transport properties, power consumption, and overall performance.
Negative Capacitance (NC)	Achieving negative capacitance through continuous deposition of extremely thin films is a groundbreaking approach. When applied to gate dielectric materials, this technology enables devices to operate at significantly lower gate voltages, leading to a substantial reduction in the power consumption. Further elaboration on this topic can be found in subsequent chapters of this book.
3D Integration	Advancements in 3D chip design and integration techniques have enabled the integration of more transistors into smaller spaces. Implementing structures such as FinFETs within 3D transistor designs can lower the power consumption and boost the performance.
Quantum Computing	Quantum computing technologies offer a complementary approach to the traditional CMOS technology. Quantum computing demonstrates a superior performance for specific computational tasks, making it an attractive alternative for future high-speed computing requirements.
2D Materials	Innovations in nanodevices and the use of 2D materials, such as graphene and transition metal dichalcogenides, can revolutionize CMOS technology. These materials exhibit exceptional electronic properties in confined spaces, paving the way for future advancements in CMOS technology.
Energy-Efficient Design	Emphasizing energy efficiency in circuit and algorithm designs is crucial for the future of the CMOS technology. Energy-efficient designs play a pivotal role across various sectors, from mobile devices to datacenters.

Nevertheless, this journey encountered a number of challenges. Previous obstacles in scaling Si-based CMOS, such as short-channel effects and power dissipation, have demanded inventive solutions and advancements in materials. Current challenges, including quantum effects and physical constraints, require interdisciplinary approaches and innovative technologies to be surmounted.

In the future, the Si-based CMOS technology holds substantial promise and potential. Emerging technologies, such as negative capacitance materials, 3D integration, quantum computing, and nanodevices, present new avenues for further innovation and enhanced performance. When combined with energy-efficient designs and materials, these technologies can reshape the landscape of CMOS technology and facilitate groundbreaking applications in diverse industries.

Successfully navigating the evolution of Si-based CMOS technology requires a strategic mindset that fosters collaboration, extensive research, and continuous development. It is crucial to address technical hurdles while also considering broader implications such as environmental sustainability and societal impacts.

In summary, Si-based CMOS technology is poised to continuously advance, driving technological progress, economic prosperity, and societal advantages. By remaining at the forefront of innovation and embracing emerging technologies, we can navigate the evolving realm of CMOS technology and unlock new opportunities in the future.

1.8 The Future of Transistors: 2D FET

The future of transistors lies in the 2D Field-Effect Transistor (FET) technology, which represents a significant and remarkable paradigm shift in semiconductor design. This paradigm shift from silicon technology to 2D materials would enable more scaling because 2D materials are known to have few dangling bonds [Figure 1.4]. Unlike traditional transistors made from bulk materials, such as silicon, 2D FETs are constructed using atomically thin materials, such as graphene, transition metal dichalcogenides (TMDs), and black phosphorus. Graphene is known for its excellent electrical and thermal conductivity, and it could act as semi-metal [Figure 1.4]. In contrast, hexagonal boron nitride (h-BN) and MoS_2 act as insulators and semiconductors, respectively. 2D materials include semi-metallic 2D materials, semiconductor 2D materials, and insulator 2D materials.

First, semi-metallic 2D materials possess characteristics similar to those of metals and semiconductors. For example, graphene, a widely recognized

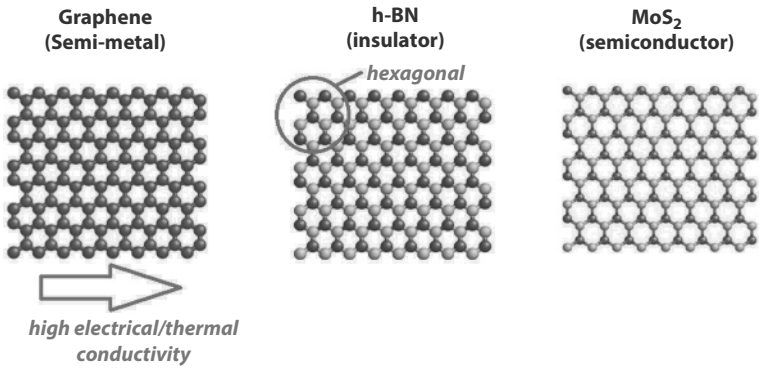

Figure 1.4 Example of 2D materials: Graphene (semi-metal, hexagonal boron nitride (h-BN)), and MoS_2 (semiconductor). The characteristics of 2D materials could depend on fabrication method, fabrication-temperature, and their width (W).

semi-metallic material, demonstrates this duality. In graphene, the conduction and valence bands intersect at a singular point called the Dirac point, which results in distinctive electronic properties. Because of its semi-metallic attributes, graphene displays notable electrical conductivity and remarkable mechanical strength, rendering it applicable across a spectrum of fields, including electronics, photonics, and materials science.

Second, semiconductor 2D materials, on the other hand, feature a bandgap between their valence and conduction bands, facilitating semiconducting behavior. Transition metal dichalcogenides (TMDs) are notable examples of semiconductor 2D materials. Unlike graphene, TMDs possess a finite bandgap, which allows for precise control over the electron flow, thus enabling the development of electronic and optoelectronic devices. Semiconductor 2D materials are instrumental in the fabrication of transistors, light-emitting diodes (LEDs), and photovoltaic devices.

Finally, insulating 2D materials are distinguished by their wide bandgap, which impedes the flow of electrons under normal circumstances. Hexagonal boron nitride (h-BN) is one of the most recognized insulator 2D materials. H-BN exhibits excellent insulating properties, high thermal stability, and chemical inertness, rendering it a promising candidate for encapsulating other 2D materials and safeguarding against their degradation. Insulator 2D materials play a vital role in device manufacturing by furnishing dielectric layers to isolate the electronic components and mitigate leakage currents.

One of the key advantages of 2D FETs is their atomic-scale thickness, which allows precise control over the flow of electrons. This enables better

electrostatic control and reduces leakage current, leading to improved transistor performance. Additionally, the unique electronic properties of 2D materials, such as their high carrier mobility and tunable bandgaps, make them highly attractive for transistor applications. However, there are some challenges. For example, black phosphorous is unstable. It would be much better if future engineering could enable more stable black phosphorous.

Furthermore, 2D FETs offer potential for device miniaturization beyond the limits of traditional silicon-based transistors. Their ultrathin nature allows the fabrication of densely packed transistor arrays, paving the way for higher transistor densities and more powerful integrated circuits.

Another area of interest is the potential for novel functionalities in 2D FETs. Researchers are exploring phenomena such as quantum tunneling and spintronics in these devices that could enable new types of logic operations and information processing.

Overall, 2D FETs hold great promise for advancing transistor technology and driving innovation in various fields, including computing and telecommunications. As research in this area continues, we expect to see further improvements in transistor performance, energy efficiency, and device functionality, ushering in a new era of electronics.

1.9 Conclusion

Overall, although there have been some challenges in achieving continuous scaling of CMOS transistors, it seems that several emerging techniques that adopt new materials could further enable more scaling. Engineers should select the proper scaling method or a new scaling method to effectively design next-generation transistors. By suppressing several short-channel effects using emerging technologies, it seems like it is possible to design and fabricate more scaled CMOS transistors for integrated semiconductor chips.

Acknowledgment

In this chapter, the knowledge in previous research has been widely utilized, and the source of information is listed in a reference format (e.g., [1], [2], …). The author would like to sincerely thank the authors who have made their sincere efforts to publish many articles and research related to this chapter.

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