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Active Devices and Modeling

For accurate power amplifier simulation and its circuit design at different operating frequencies and output power levels, it is important to represent an active device in the form of a nonlinear equivalent circuit, which can adequately describe the small- and large-signal electrical behaviors of the power amplifier up to the device transition frequency f_T and higher to its maximum frequency f_{max} that allows a sufficient number of harmonic components to be taken into account. Better approximation of the final design to the expected performance can only be achieved if the nonlinear device behavior is described accurately. Generally, the power amplifier design based on the nonlinear device models rather than on the blind black-box models enables better understanding and predicting both the active device behavior in particular and power amplifier performance in general, considering that the elements of the device nonlinear equivalent circuit will be the parts of the matching or harmonic-control circuits and directly affect stability and linearity of the power amplifier operation.

1.1 MOSFET Device Modeling

Accurate MOSFET device modeling is an extremely important procedure to develop low-cost silicon integrated circuits using CMOS technology for higher-speed and higher-frequency integrated circuits and subsystems within a shorter design time. The accuracy of MOSFET models to describe their nonlinear behavior is crucial to predict the entire circuit performance. The lumped-parameter equation-based equivalent circuit model provides a clearer physical description and more design flexibility.

The complete small-signal MOSFET equivalent circuit with intrinsic nonlinear model and extrinsic parasitic elements, including the gate–drain substrate coupling network and substrate parameters, is shown in Figure 1.1 [1]. Here, C_{gs} and R_{gs} are the gate–source capacitance and gate channel resistance, C_{gd} and R_{gd} are the gate–drain capacitance and drain ohmic resistance, g_m is the device transconductance, R_{ch} is the differential channel resistance as a result of the channel-length modulation by the drain voltage, C_{ds} is the drain–source capacitance, L_g is the gate lead inductance, R_s and L_s are the source bulk and ohmic resistance and lead inductance, and R_d and L_d are the drain bulk and ohmic resistance and lead inductance, respectively. A coupling path between the gate and the drain through the substrate may significantly affect the transfer performance of the transistor. Under an active bias condition, the conductive channel isolates the gate–bulk coupling and the capacitances C_{gb} and C_{gs} can be merged when the substrate coupling path between the gate and drain terminals can be ignored. However, under pinch-off bias conditions, the conductive channel does not exist, and the signal at the gate terminal is directly coupled to the substrate. This equivalent small-signal device model can accurately characterize the performance of the transistors in nanometer CMOS technology up to 60 GHz and above.

Several degradation mechanisms can significantly affect the performance of CMOS power amplifiers, such as gate-oxide breakdown, hot-carrier degradation, punchthrough, drain–bulk breakdown, or negative bias temperature instability. The gate-oxide breakdown and hot-carrier effect are the two most critical issues

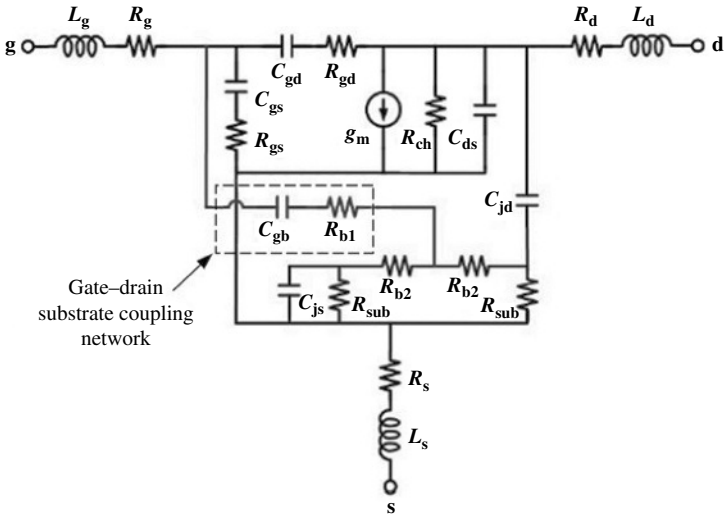

Figure 1.1 Equivalent small-signal circuit of MOSFET device.

of deep submicron CMOS device reliability. The gate-oxide breakdown is the sudden formation of a conductive path in the gate oxide of a MOSFET device as a result of high-voltage application. The allowable gate-oxide voltage becomes smaller as the gate-oxide thickness is reduced. Since the channel voltage varies from the source to the drain, the oxide stress (the voltage difference between the top of the oxide and the bottom of the oxide) is a function of position. The highest stress areas occur at the source and drain oxide edges, and therefore, from a design standpoint, the gate–source and the gate–drain voltages (V_{gs} and V_{gd}) should never exceed prespecified values [2]. There are two basic types of oxide breakdown: hard breakdown and soft breakdown. In hard breakdown, a large gate current increase can be observed, and it has the most disastrous effect on the device performance. This type of breakdown is typically found in thick-oxide devices because of high-voltage stress. In soft breakdown, a small sudden gate current increase and a sudden gate current noise increase are observed [3].

The electrical field near the corner of a silicon–silicon dioxide (Si–SiO_2) interface, where the drain junction is directly under the gate, is the largest in the device and results in the following hot-carrier effects: electron injection into the SiO_2 layer producing a gate current; an avalanche hole–electron pair production process, increasing the substrate potential and resulting in the built-in bipolar transistor and current source between the drain and substrate; or punchthrough for shortened channel lengths of less than 1 μm contributing to a drain–source leakage current [4, 5]. Consequently, for high-efficiency operation modes with a large drain voltage peak factor, the device is liable to a hot-carrier effect when it is turned off.

In short-channel devices, the lateral field can be extremely high, and consequently, carriers can achieve very high energy before losing momentum to a collision with the crystal lattice. Some of the hot energy carriers collide with the lattice before arriving at the drain with sufficient energy to result in impact ionization [2]. This, in addition to potential avalanche multiplication, can result in surface defects, thus resulting in a reduced carrier mobility in the channel. This can also result in a trapped charge in the gate oxide or oxide/silicon interface, shifting the local threshold voltage. Usually, this damage occurs in the drain region where the electric field is very high, resulting in an increase in the device on-resistance and knee voltage.

In a normal operating condition, the drain–source current of a MOSFET device flows close to the surface when a large enough gate bias is applied to create an inversion channel. In the absence of a gate bias, a very little current flows because the drain–bulk and the source–bulk diodes are effectively connected back-to-back with opposite polarities. As larger voltages are applied to the drain, the drain–bulk depletion region extends farther to accommodate the electric potential drop. This depletion region will eventually extend all the way to meet the depletion region of

the source–bulk junction, thereby diminishing the potential barrier that stops the direct flow of current between the drain and the source [2]. This punch-through process results in a large current flow that can occur even in the absence of any significant gate bias.

If the gate breakdown is a catastrophic phenomenon, the hot-carrier effect contributes to a long-term power amplifier performance. Because of this hot-carrier effect, the output power of the CMOS power amplifier decreases exponentially, and the slope of this decrease becomes sufficiently small after about 70–80 hours of its operation, suggesting that most of the created trap sites at the Si–SiO_2 interface have been filled by electrons. The recovery of the overall degradation in the output power from its nominal value can be achieved by slightly increasing the gate bias voltage, which indicates that the performance degradation is mainly because of the increase in threshold voltage [6].

1.2 LDMOSFETs

Silicon MOSFET devices have found widespread worldwide applications due to their reliable, low-cost, and high-performance technology. For example, the laterally diffused MOSFET (LDMOSFET) device structures have proven to be highly efficient, high-gain, and linear for high-power RF and microwave base station applications. Initially, several well-known physically based MOSFET models were developed to describe the device's electrical behavior [7, 8]. However, some of them, such as Level 1, Level 2, or Level 3 large-signal models, were very simple and could not describe the current–voltage and voltage–capacitance characteristics with acceptable accuracy. At the same time, the BSIM3 and later BSIM4 models are too complicated and quite formal in general, so, for better learning of the device's basic properties, it is useful to consider its intrinsic nonlinear core circuit only. Moreover, microwave parasitic effects in silicon MOSFETs are not easily physically predictable. The table-based models, such as the Root model, are only accurate for the characterized structures and measurement conditions. An empirical analytical modeling approach is an explicit and valid compromise between physical models and data-based models and provides a clear relationship between the device equivalent circuit parameters and power amplifier performance.

1.2.1 Small-signal Equivalent Circuit

To describe accurately the nonlinear properties of the large-size MOSFET devices, it is necessary to consider the distributed nature of the gate capacitance, because the channel resistance is not equal to zero. In this case, the device

channel can be modeled as a bias-dependent distributed transmission line along the channel length, as shown in Figure 1.2, demonstrating the physical structure of an LDMOSFET device. Here, a heavily doped p^+ layer (enhancement and sinker) is inserted between the top source and p^+-substrate (source grounding) for low resistivity to provide high current flow between the drain and source terminals [9]. The lightly doped p-epilayer and n^- layer are required to provide sufficient distance between regions to prevent latchup (forward-biased p–n diodes) and for the drain–source breakdown protection. The parasitic gate–drain capacitance is directly related to the overlap of the gate oxide onto the heavily doped n^+-source region.

This one-dimensional approach assumes a gradual channel approximation when the quantity of charge in the channel is controlled completely by the gate electrode, only fields in the vertical dimension influence the depletion region, and channel current is provided entirely by drift with constant mobility. Despite some drawbacks related to short-channel devices, this approach allows a compromise between accuracy and simplicity of a model derivation.

The *ABCD*-matrix of the given *RC* transmission line can be written as

$$[ABCD] = \begin{bmatrix} \cosh\gamma L & Z_0 \sinh\gamma L \\ \dfrac{\sinh\gamma L}{Z_0} & \cosh\gamma L \end{bmatrix} \tag{1.1}$$

where $\gamma = \sqrt{j\omega R'_{\text{ch}} C'_{\text{g}}}$ is the propagation constant, $Z_0 = R'_{\text{ch}}/\gamma$ is the characteristic transmission-line impedance, L is the channel length, $R'_{\text{ch}} = R_{\text{ch}}/L$, $C'_{\text{g}} = C_{\text{g}}/L$, R_{ch} is the channel charging resistance, which is a result of noninstantaneous response to the changes of the gate–source voltage, and C_{g} is the total gate capacitance.

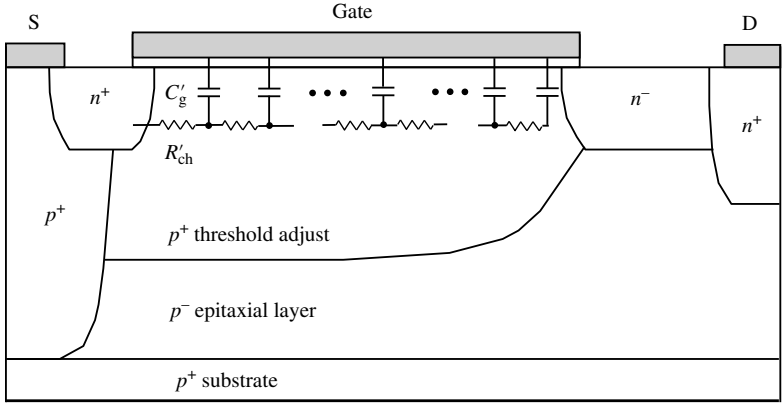

Figure 1.2 Schematic representation of MOSFET distributed channel structure.

In this case, the equivalent gate–source impedance Z_{gs} can be estimated from Eq. (1.1) (matrix) as

$$Z_{gs} = \frac{A}{C} = R_{ch}\frac{\coth\gamma L}{\gamma L} \tag{1.2}$$

The first-order approximation of Z_{gs}, obtained from a power series expansion of Eq. (1.2), yields

$$Z_{gs} = R_{ch}\frac{\coth\gamma L}{\gamma L} \cong \frac{R_{ch}}{\gamma L}\left(\frac{1}{\gamma L} + \frac{\gamma L}{3}\right) = \frac{R_{ch}}{3} + \frac{1}{j\omega C_g} \tag{1.3}$$

From Eq. (1.3), it follows that the MOSFET intrinsic gate–source circuit can be modeled using a simple series circuit with the resistance $R_{gs} = R_{ch}/3$ and the capacitance $C_{gs} = C_g$. Figure 1.3a shows the intrinsic transistor equivalent circuit corresponding to the first-order channel approximation, where τ is the effective channel carrier transit time.

Better accuracy for channel approximation can be obtained from the second-order approximation of Z_{gs}, derived from a power series expansion of Eq. (1.2) as

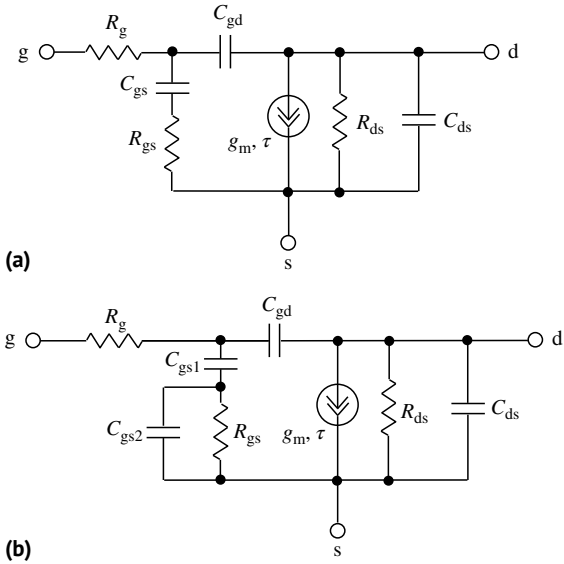

Figure 1.3 Intrinsic MOSFET equivalent circuit corresponding to (a) first- and (b) second-order channel approximation.

$$Z_{gs} = R_{ch}\frac{\coth\gamma L}{\gamma L} \cong \frac{R_{ch}}{\gamma L}\left[\frac{1}{\gamma L} + \frac{\gamma L}{3} - \frac{(\gamma L)^2}{45}\right] = \frac{R_{ch}}{3}\left(1 - \frac{j\omega C_g R_{ch}}{15}\right) + \frac{1}{j\omega C_g} \cong \frac{R_{ch}}{3}/\left(1 + j\omega\frac{R_{ch}}{3}\frac{C_g}{5}\right) + \frac{1}{j\omega C_g} \tag{1.4}$$

As a result, the second-order approximation of the device channel structure can be realized by the series connection of the capacitance $C_{gs1} = C_g$ and the parallel RC circuit, which consists of the resistance $R_{gs} = R_{ch}/3$ and capacitance $C_{gs2} = C_g/5$. The intrinsic transistor equivalent circuit corresponding to the second-order approximation is shown in Figure 1.3b.

For a high-power MOSFET device whose channel width is significantly larger than its channel length, the distributed nature of the total gate resistance $R_{tot} = R_{sh}W/L$ across the width W, where R_{sh} is the sheet resistance of the gate material, must be taken into consideration. In this case, silicon MOSFET can be decomposed into n devices, each with a width of W/n and a gate resistance of R_{tot}/n. For $n \to \infty$, it will be viewed as an array of small transistors distributed along the gate of the device. Commonly, it is necessary to consider a two-dimensional power MOSFET distributed model because it shows a distributed-gate nature along both the channel length and channel width. However, for a short-channel MOSFET, the distributed-gate effect along the channel length can be considered only in the frequency range close to the transition frequency f_T and higher. When $\omega R_{gs}C_{gs} \ll 1$ an analysis of the distributed-gate model along the channel width based on transmission line theory shows that all transistor Y-parameters should be modified $\tanh(\gamma W)/(\gamma W)$ by the term $\tanh(\gamma W)/(\gamma W)$ [10]. However, the linear power series expansion of this term as

$$\frac{\tanh(\gamma W)}{\gamma W} = 1 - j\omega C_g\frac{R_{tot}}{3} \cong \frac{1}{1 + j\omega C_g\frac{R_{tot}}{3}} \tag{1.5}$$

leads to only the additional use of a series lumped gate resistance $R_{tot}/3$ that does not alter the structure of the transistor equivalent circuit. Consequently, the overall gate resistance R_g can generally be divided into two consecutive series resistances as $R_g = R_{ge} + R_{gi}$, where R_{ge} is the extrinsic contact and ohmic gate electrode resistance and $R_{gi} = R_{tot}/3$ is the intrinsic gate resistance due to the distributed-gate structure of the power MOSFET.

Figure 1.4 shows the nonlinear MOSFET equivalent circuit with extrinsic parasitic elements, which can properly describe the nonlinear behavior of both VDMOSFET (vertical double-diffused MOSFET) and LDMOSFET devices [11, 12]. The nonlinear current source $i(v_{gs}, v_{ds}, \tau)$ as a function of the input gate–source

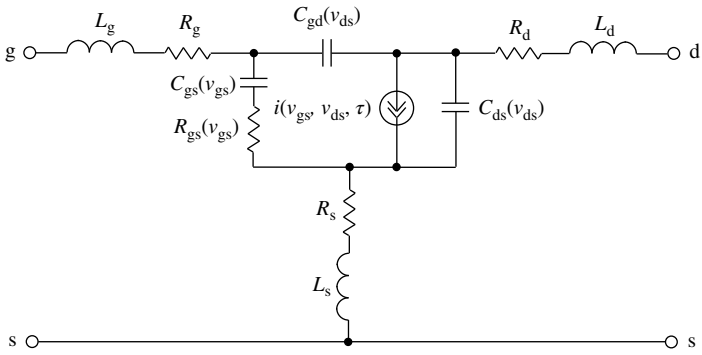

Figure 1.4 Small-signal MOSFET equivalent circuit with extrinsic linear elements.

and output drain–source voltages incorporating self-heating effect can be described sufficiently simply and accurately using hyperbolic functions [12, 13]. Careful analytical description of the transition from quadratic to linear regions of the device transfer characteristic enables more accurate prediction of the intermodulation distortion (IMD) [14]. The overall channel carrier transit time τ also includes an effect of the transcapacitance required for charge conservation. The drain–source capacitance C_{ds} and gate–drain capacitance C_{gd} are considered as junction capacitances that strongly depend on the drain–source voltage. The extrinsic parasitic elements are represented by the gate and drain bondwire inductances L_g and L_d, source inductance L_s, source and drain bulk and ohmic resistances R_s and R_d, and gate contact and ohmic resistance R_g. The effect of the gate–source channel resistance R_{gs} becomes significant at higher frequencies close to transition frequency $f_T = g_m/2\pi C_{gs}$, where g_m is the device transconductance. To account for the self-heating effect and substrate loss, a special four-port thermal circuit and a series combination of the resistance and capacitance between the external drain and source terminals can be included [15].

1.2.2 Nonlinear *I–V* Models

An empirical analytical approach to approximate the nonlinear behavior of the drain current source $I_{ds}(V_{gs}, V_{ds})$ using hyperbolic functions was first applied to a JFET device [16]. In this case, instead of using separate equations for the triode and pinch-off regions, irrespective of the device geometry and material parameters, a general expression based on a hyperbolic tangent function was proposed, written as

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2 \tanh\alpha\left|\frac{V_{ds}}{V_p - V_{gs}}\right| \tag{1.6}$$

where I_{dss} is the saturation drain current for $V_{gs} = 0$, α is the saturation voltage parameter, and V_p is the pinch-off voltage. As a result, a good agreement was obtained between the predicted and experimental results, showing a promising future of such a simple empirical model.

A similar and sufficiently simple nonlinear model using a hyperbolic tangent function and incorporating the self-heating effect was later proposed to describe the *I–V* characteristics of a MOSFET device, written as

$$I_{ds} = \beta_{eff} V_{gst}^{VGexp} (1 + \lambda V_{ds}) \tanh\left(\frac{\alpha V_{ds}}{V_{gst}^{SATexp}}\right) \tag{1.7}$$

where

$$\beta_{eff} = \beta / \left(1 + \mu_{crit} V_{gst}^{GMexp}\right)$$
$$V_{gst} = V_{st} \ln\left[1 + \exp\left(\frac{V_{gst1}}{V_{st}}\right)\right]$$
$$V_{gst1} = V_{gs} - V_{th0} - \gamma V_{ds}$$

where VGexp, GMexp, SATexp, and μ_{crit} are the channel current parameters, β and γ are the first-order functions of the channel temperature increase, and α, λ, and V_{st} are the fitting parameters [17, 18]. Similarly, an empirical nonlinear model using both hyperbolic tangent and exponential functions, which is single-piece and continuously differentiable, was developed for silicon LDMOSFET devices [13].

In many applications, it is necessary to take into consideration the MOSFET operation in the weak-inversion region when the gate–source voltage V_{gs} is smaller than the threshold voltage V_{th}. For example, to reduce the IMD of a Class-AB power amplifier when the device is biased around the onset of the strong-inversion region from the weak-inversion region for low drain quiescent current. The drain current in the weak-inversion region is mainly dominated by the diffusion component that increases exponentially with the gate voltage [5]. On the other hand, in the strong-inversion saturation region, when the gate-source voltage is greater than the threshold voltage, the drain current is proportional to the square of $\left(V_{gs} - V_{th}\right)$.

To obtain continuous behavior from the weak-inversion region to the strong-inversion region for the drain current and a compromise between accurate device modeling and ease of circuit analysis, the following analytical function can be used:

$$I_{ds}\left(V_{gs}\right) = A\left\{\ln\left[1 + \exp\left(B\left(V_{gs} - V_{th}\right)\right)\right]\right\}^2 \tag{1.8}$$

where A and B are the approximation parameters. In this case, the drain current is effectively proportional to the square of $\left(V_{gs} - V_{th}\right)$ when V_{gs} is larger than V_{th} and

exponentially decreases with the gate–source voltage when V_{gs} is smaller than V_{th}. The approximation parameters A and B are defined by the following conditions:

$$I_{ds}\big|_{V_{gs}=V_{th}} = I_{th} \qquad \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{gs}=V_{th}} = S_{th} \tag{1.9}$$

where I_{th} is the threshold drain current, as shown in Figure 1.5a, and S_{th} is the slope of the current–voltage transfer characteristic at the threshold point. Then,

$$A = \frac{I_{th}}{(\ln 2)^2} \qquad B = \frac{S_{th}}{I_{th}} \ln 2 \tag{1.10}$$

Consequently, the device transfer characteristic can be defined in terms of only two physical parameters I_{th} and S_{th}, which are easily calculated from the device measurements.

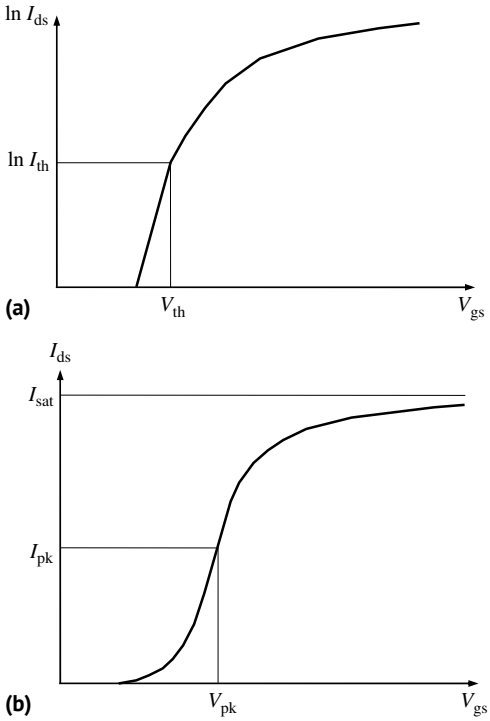

Figure 1.5 Drain current versus gate–source voltage.

To link the linear and saturation regions by a suitable continuous analytical dependence, the following function to describe the *I–V* curves can be used:

$$I_{ds}(V_{gs}, V_{ds}) = \left(I_{max}^{-1} + I_{dso}^{-1}\right)^{-1} \tag{1.11}$$

where I_{dso} is the exponential function of V_{gs} and V_{ds}, and I_{max} is the maximum channel current obtained by

$$I_{max}(V_{ds}) = I_{pk}(1 + \lambda V_{ds})\tanh(\alpha V_{ds}) \tag{1.12}$$

where I_{pk} is the drain current, which corresponds to the maximum slope of the $I_{ds}(V_{gs})$ curves, as shown in Figure 1.5b [19]. The saturation voltage parameter α affects the slope of the $I_{ds}(V_{ds})$ curves in the linear region, whereas the parameter λ determines the slope of the same drain characteristics in the saturation region.

In view of the monotonous behavior of $I_{ds}(V_{ds})$ curves, the entire drain current–voltage characteristics of a MOSFET device can be described as

$$I_{ds}(V_{gs}, V_{ds}) = I_0 / \left[1 + \left(\frac{I_0}{I_{max}}\right)^n\right]^{\frac{1}{n}} \tag{1.13}$$

where

$$I_0 = \frac{I_{th}}{(\ln 2)^2(1 - \beta V_{gs})}\left\{\ln\left[1 + \exp\left(\frac{S_{th}\ln 2}{I_{th}}(V_{gs} - V_{th})\right)\right]\right\}^2$$

$$I_{max} = I_{sat}(1 + \lambda V_{ds})\tanh(\alpha V_{ds})$$

where I_{sat} is the saturated drain current, α is the saturation voltage parameter affecting the slope of the $I_{ds}(V_{ds})$ characteristics in the linear region, λ is the parameter that determines a slope of the same drain characteristics in the saturation region, $V_{th} = V_{th0} - \sigma V_{ds}$, n and β are the fitting parameters that determine the slope of the transfer characteristics under large values of V_{gs}, and σ is the parameter that expresses empirically the dependence of the threshold voltage on V_{ds} [12]. Better accuracy can be achieved by using I_{sat} instead of I_{pk} in Eq. (1.12).

To verify this empirical *I–V* model, a high-power LDMOSFET with a gate width of 4 cm and a gate length of 1.1 μm (LP801 from Polyfet) was used. The theoretical and experimental output $I_{ds}(V_{ds})$ curves are shown in Figure 1.6, with the resulting current mean-square error of a family of the output I_{ds}–V_{ds} characteristics of 0.5%. The values of the simulated model parameters are indicated in Table 1.1.

The theoretical approximation of $I_{ds}(V_{ds})$ curves is sufficient and accurate for a high-power LDMOSFET and requires only six fitting parameters, four of which

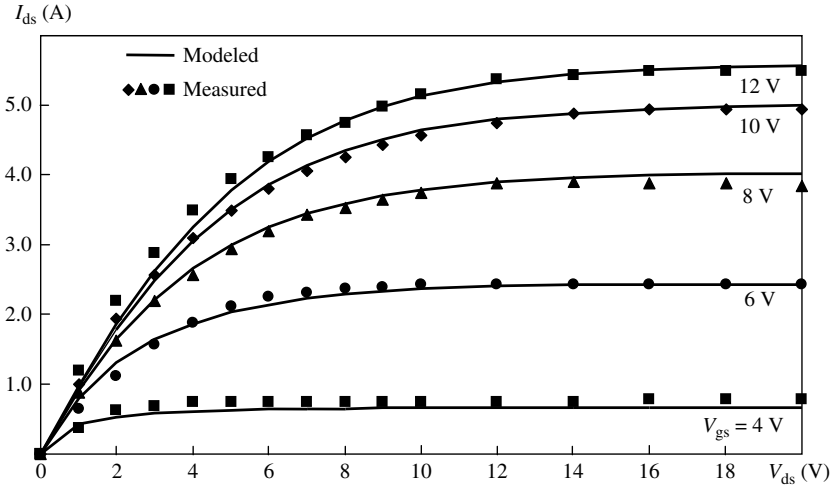

Figure 1.6 Measured and modeled $I_{ds}(V_{ds})$ curves of high-voltage LDMOSFET.

Table 1.1 Simulated *I*–*V* model parameters of high-voltage LDMOSFET.

Parameters	α (1/V)	β (1/V)	λ (1/V)	V_{th} (V)	I_{th} (A)	S_{th} (A/V)	I_{sat} (A)	n	σ
Values	0.15	0	0.0005	2.7	0.115	0.2	6.8	1.0	0

are easily determined by the experimental curves. An empirical analytical model allows the description of I_{ds} and g_m as the functions of V_{gs} in the weak-inversion region, as well as in the strong-inversion region of the LDMOSFET operation. Substantially better fitting with $I_{ds}(V_{gs})$ and $g_m(V_{gs})$ experimental curves is achieved compared with the results obtained from two-dimensional simulations, as shown in Figure 1.7 [20].

To verify that this model can be applicable to low-voltage MOSFET devices, the proper low-voltage RF power MOSFET with a gate width of 2 mm was selected [21]. Figure 1.8 shows the theoretical and experimental drain current $I_{ds}(V_{ds})$ curves. In this case, to improve the sensitivity of the drain current I_{ds} under large values of V_{gs}, the term $(1 - \beta V_{gs})$ was added into the denominator for I_0 in Eq. (1.13). The resulting current mean-square error of a family of the output $I_{ds}(V_{ds})$ curves was 0.42% only. The parameters of the simulated $I_{ds}(V_{ds})$ curves are presented in Table 1.2. The comparison of the transfer $I_{ds}(V_{gs})$ curves with the same characteristics calculated by means of the BSIM3v3 model developed for

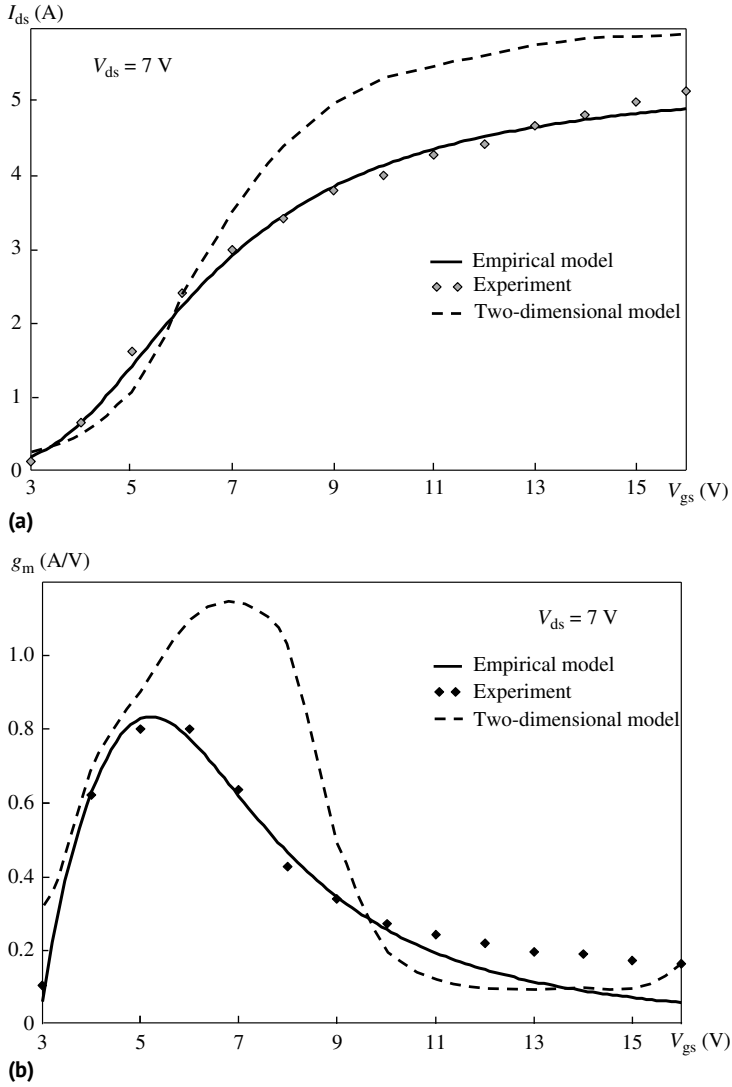

Figure 1.7 Measured and modeled $I_{ds}(V_{gs})$ and $g_m(V_{gs})$ curves of high-voltage LDMOSFET.

modeling of deep submicron devices is shown in Figure 1.9, demonstrating a good agreement with the experimental curves, and they are practically the same as in the case of the BSIM3v3 approximation.

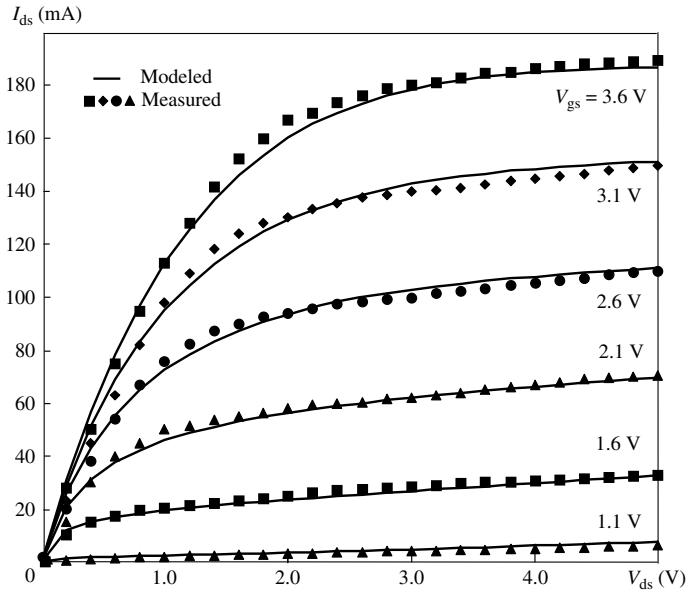

Figure 1.8 Measured and modeled $I_{ds}(V_{ds})$ curves of low-voltage MOSFET.

Table 1.2 Simulated *I–V* model parameters of low voltage MOSFET.

Parameters	α (1/V)	β (1/V)	λ (1/V)	V_{th} (V)	I_{th} (mA)	S_{th} (mA/V)	I_{sat} (A)	n	σ
Values	0.58	0.17	0	0.9	0.029	1.05	0.31	0.78	0.05

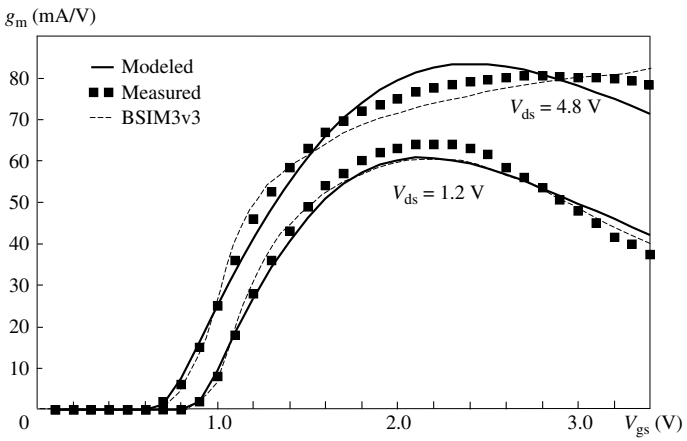

Figure 1.9 Measured and modeled $g_m(V_{gs})$ curves of low-voltage MOSFET.

1.2.3 Nonlinear *C–V* Models

Generally, all capacitances corresponding to the intrinsic equivalent circuit of the LDMOSFET device are nonlinear. However, their nonlinear behavior is different, and the input gate–source capacitance C_{gs} has a dominant effect on the IMD level, especially when the frequency increases in the microwave region [22]. However, the calculation of the gate–source capacitance C_{gs} or the gate–drain capacitance C_{gd} from the charges corresponding to the strong-inversion model only results in a mathematically complicated expression [5]. Therefore, in most cases, when it is necessary to predict efficiency, power gain, or output power of the power amplifier, the capacitances C_{gs} and C_{gd} can be modeled as the fixed capacitances measured at the quiescent bias voltage, and the p–n junction diode capacitance model can be applied to the capacitance C_{ds} [20]. The gate–drain capacitance C_{gd} can also be considered as the bias-dependent junction capacitance [23]. With the increase in the drain bias voltage, a depletion region is formed under the oxide in the lightly doped drain region. Therefore, the capacitance C_{gd} can be considered as the junction capacitance, which strongly depends on the drain–source voltage V_{ds}. According to the accurate charge model calculations, the gate–drain capacitance C_{gd} has a strong dependence on V_{gs} only in the moderate-inversion region when $V_{gs} - V_{th} < 1$ V [5]. In this region, the behavior of C_{gd} is similar to C_{gs}, and can be evaluated using the same hyperbolic tangent functions. However, for high-voltage LDMOSFET devices, since the dependence of C_{gd} on V_{gs} is quite small, it seems sufficient to limit its dependence on V_{ds} only. The drain–source capacitance C_{ds} varies due to the change in the depletion region, which is mainly determined by the value of V_{ds}.

To describe the nonlinear gate–source capacitance C_{gs} in a small-signal operation mode as a function of the gate–source voltage V_{gs}, it needs first to consider an appropriate behavior of each of its main composite parts: the intrinsic gate–source capacitance C_{gsi}, including both the gate–source and the source–substrate charge fluctuations, and the gate–substrate capacitance C_{gbi}. The gate–source voltage dependence of these components is substantially different [5]. The intrinsic gate–substrate capacitance C_{gbi} is constant in the accumulation region, where it is equal to the total intrinsic oxide capacitance C_{ox}, slightly decreases in the weak-inversion region, significantly reduces in the moderate-inversion region, and becomes practically constant in the strong-inversion or saturation region. The intrinsic gate–source capacitance C_{gsi} grows rapidly in the moderate-inversion region and equals $2C_{ox}/3$ in the saturation region. The voltage dependence of the total gate–source capacitance C_{gs} as a sum of its components C_{gsi} and C_{gbi} on V_{gs} is shown in Figure 1.10.

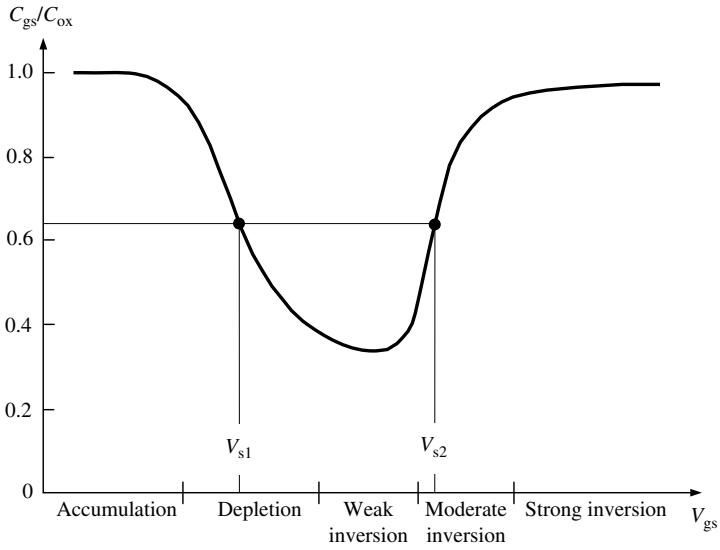

Figure 1.10 Gate–source capacitance versus gate–source voltage.

A hyperbolic tangent function can be used for each of two parts of the dependence $C_{gs}(V_{gs})$, where the gate–source capacitance can be approximated by

$$C_{gs} = C_{gsmin} + C_s\left\{1 + \tanh\left[\frac{S}{C_s}(V_{gs} - V_s)\right]\right\} \tag{1.14}$$

where $C_s = (C_{gsmax} - C_{gsmin})/2$, C_{gsmax} is the maximum gate–source capacitance, C_{gsmin} is the minimum gate–source capacitance, $S = (S_1, S_2)$ is the slope of $C_{gs}(V_{gs})$ at each bend point $V_{gs} = (V_{s1}, V_{s2})$, as shown in Figure 1.10.

$$S_1 = \left.\frac{\partial C_{gs}}{\partial V_{gs}}\right|_{V_{gs}=V_{s1}} \qquad S_2 = \left.\frac{\partial C_{gs}}{\partial V_{gs}}\right|_{V_{gs}=V_{s2}} \tag{1.15}$$

The total gate–source capacitance C_{gs} as a function of V_{gs} can be modeled as

$$\begin{aligned} C_{gs} = {} & C_{gsmax} - C_{gso}\left\{1 + \tanh\left[\frac{S_1}{C_s}(V_{gs} - V_{s1})\right]\right\} \\ & \times \left\{1 + \tanh\left[\frac{S_2}{C_s}(V_{gs} - V_{s2})\right]\right\} \end{aligned} \tag{1.16}$$

where $C_{gsmax} = C_{ox}$ and C_{gso} is the model fitting parameter [12].

The approximation function for the gate–source capacitance C_{gs} modeling the dependence on V_{gs} can also be expressed by using the two components, both containing the hyperbolic tangent functions:

$$\begin{aligned} C_{gs} = {} & C_{gs1} + C_{gs2}\left\{1 + \tanh\left[C_{gs6}\left(V_{gs} + C_{gs3}\right)\right]\right\} \\ & + C_{gs4}\left[1 - \tanh\left(C_{gs5}V_{gs}\right)\right] \end{aligned} \tag{1.17}$$

where C_{gs1}, C_{gs2}, C_{gs3}, C_{gs4}, C_{gs5}, and C_{gs6} are the approximation parameters [13].

For submicron MOSFET devices, when C_{gs} slightly increases with the increase of V_{ds}, the approximation expression for C_{gs} as a function of both V_{gs} and V_{ds} can be written as

$$\begin{aligned} C_{gs} = {} & C_{gs0} + C_{gs1}\left\{A_s + B_s \tanh\left[C_s\left(V_{gs} - V_{th}\right)\right]\right\} \\ & \times \left\{D_s + E_s\left[1 + \tanh\left(V_{gs} - V_{ds}\right)\right]\tanh\left[F_s V_{ds} - G_s V_{gs}\right]\right\} \end{aligned} \tag{1.18}$$

where C_{gs0} is the bias-dependent capacitance, V_{th} is the threshold voltage, C_{gs1} is the scaling factor, and A_s, B_s, C_s, D_s, E_s, F_s, and G_s are the model fitting parameters [24].

On the other hand, for high-voltage MOSFET devices, the dependencies of the gate–drain capacitance C_{gd} and the drain–source capacitance C_{ds} on V_{ds} can be evaluated with sufficient accuracy by the junction capacitance model as

$$C_{gd(ds)} = C_{gdo(dso)}\left(\frac{\phi + V_{dso}}{\phi + V_{ds}}\right)^{m} \tag{1.19}$$

where m (m_g for C_{gd} or m_d for C_{ds}) is the junction sensitivity depending on a doping profile ($m = 1/3$ for the linearly graded junction, $m = 1/2$ for the abrupt junction, and $m > 1/2$ for the hyperabrupt junction), ϕ is the contact potential, and C_{gdo} and C_{dso} are the junction capacitances when $V_{ds} = V_{dso}$. For practical profiles of the junction, which are neither exactly abrupt nor exactly linearly graded, one often chooses the parameters m and ϕ to obtain the best matching between the theoretical model and the measurements.

The results of the approximation of C_{ds} and C_{gd} as the junction capacitances for high-power LDMOSFET (LP801 from Polyfet) are shown in Figures 1.11 and 1.12, respectively. The fitting parameters of the approximation curves $C_{gd}(V_{ds})$ and $C_{ds}(V_{ds})$ are given in Table 1.3.

For submicron MOSFET devices, to consider the dependence of C_{gd} on both V_{gs} and V_{ds}, the approximation expression for the C_{gd} is written as

$$C_{gd} = C_{gd0} + C_{gd1}\left\{A_d + B_d \tanh\left[C_d\left(D_d V_{gs} - V_{ds}\right) - V_{th}\right]\right\} \tag{1.20}$$

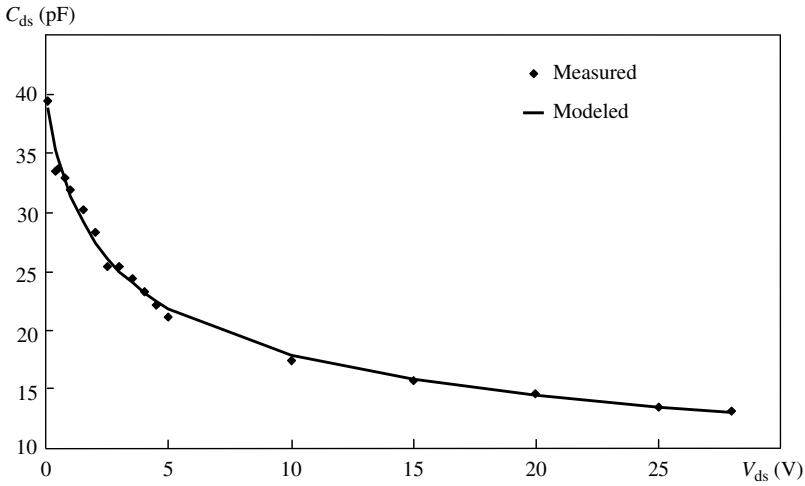

Figure 1.11 Measured and modeled $C_{ds}(V_{ds})$ dependencies of high-voltage LDMOSFET.

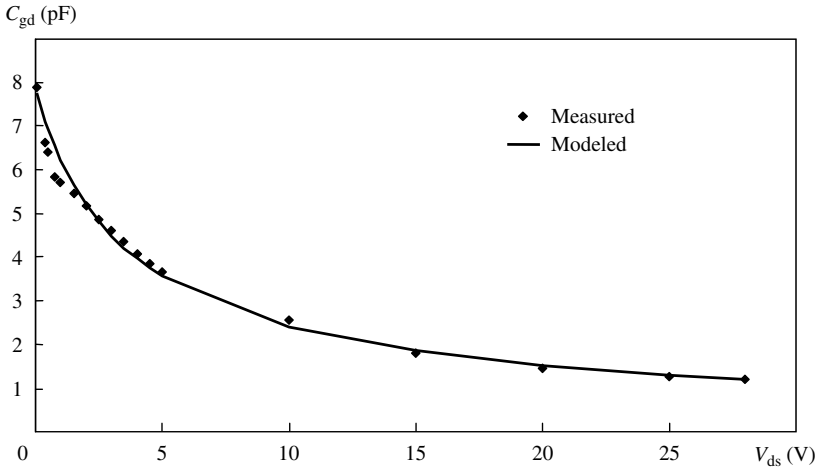

Figure 1.12 Measured and modeled $C_{gd}(V_{ds})$ dependencies of high-voltage LDMOSFET.

Table 1.3 Simulated *C–V* junction model parameters.

Capacitance	$C_{gd(ds)o}$ (pF)	m	ϕ (V)
C_{gd}	7.88	0.8	2.94
C_{ds}	39.42	0.33	1.0

where C_{gd0} is the bias-dependent capacitance, V_{th} is the threshold voltage, C_{gd1} is the scaling factor, whereas A_d, B_d, C_d, and D_d are the model fitting parameters [24].

1.2.4 Charge Conservation

To properly describe the nonlinear device models under the small- and large-signal operation modes, it is necessary to satisfy the charge conservation condition. For a three-terminal MOSFET device, the matrix equation for the small-signal charging circuit in the frequency domain is given by

$$\begin{bmatrix} I_g \\ I_d \\ I_s \end{bmatrix} = j\omega \begin{bmatrix} C_{gg} & -C_{gd} & -C_{gs} \\ -C_{dg} & C_{dd} & -C_{ds} \\ -C_{sg} & -C_{sd} & C_{ss} \end{bmatrix} \begin{bmatrix} V_g \\ V_d \\ V_s \end{bmatrix} \tag{1.21}$$

where I_g, I_d, and I_s are the terminal current amplitudes, V_g, V_d, and V_s are the terminal voltage amplitudes, and the capacitance between any two device terminals (k, l) is described as $C_{kl} = \partial Q_k / \partial V_l$ [5]. To transform a three-terminal device into a two-port network with a common source terminal, the current and voltage terminal conditions should be respectively set as $I_g = I_{gs}$, $I_d = I_{ds}$, $I_s = -(I_{gs} + I_{ds})$, $V_g - V_s = V_{gs}$, $V_d - V_s = V_{ds}$, and the relationships between the terminal capacitances as

$$\begin{aligned} C_{gg} &= C_{gd} + C_{gs} = C_{dg} + C_{sg} \\ C_{dd} &= C_{dg} + C_{ds} = C_{gd} + C_{sd} \\ C_{ss} &= C_{sg} + C_{sd} = C_{gs} + C_{ds} \end{aligned} \tag{1.22}$$

As a result, the admittance Y_c-matrix for such a capacitive two-port network is written as

$$Y_c = \begin{bmatrix} j\omega(C_{gs} + C_{gd}) & -j\omega C_{gd} \\ -j\omega(C_{gd} + C_m) & j\omega(C_{ds} + C_m + C_{gd}) \end{bmatrix} \tag{1.23}$$

where $C_m = C_{dg} - C_{gd}$ is the transcapacitance, C_{gd} represents the effect of the drain on the gate, and C_{dg} represents the effect of the gate on the drain, and these effects are different [8, 25]. Similarly to the *I–V* characteristics, there is no reason to expect that the effect of the drain voltage on the gate current, which is zero without leakage current, is the same as the effect of the gate voltage on the drain current, which is significantly large.

Therefore, for power MOSFET devices, because the transcapacitance C_m is substantially less than C_{gs}, it can be translated to an additional delay time τ_c

in a frequency range up to f_T by combining it with the transconductance g_m according to

$$g_m - j\omega C_m = g_m\sqrt{1+\left(\frac{\omega}{\omega_T}\frac{C_m}{C_{gs}}\right)^2}\exp\left[-j\tan^{-1}\left(\frac{\omega}{\omega_T}\frac{C_m}{C_{gs}}\right)\right] \cong g_m\exp(-j\omega\tau_c) \tag{1.24}$$

where $\tau_c = C_m/(\omega_T C_{gs})$. To satisfy the charge conservation condition, the total delay time τ shown in the MOSFET equivalent circuit in Figure 1.4 represents both the ideal transit time and delay time due to the transcapacitance. The transcapacitance C_m can be easily added to the drain–source capacitance C_{ds} under parameter extraction procedure.

1.2.5 Gate–Source Resistance

The gate–source resistance R_{gs} is determined by the effect of the channel inertia in responding to rapid changes of the time-varying gate–source voltage, and it varies in such a manner that the charging time $\tau_g = R_{gs}C_{gs}$ remains approximately constant. Thus, the increase of R_{gs} in the velocity saturation region (when the channel conductivity decreases) is partially compensated by the decrease of C_{gs} due to nonuniform channel charge distribution [26]. The effect of R_{gs} becomes significant at higher frequencies close to the transition frequency f_T of the MOSFET and may not be considered when designing RF circuits operating below 2 GHz [21, 27].

1.2.6 Temperature Dependence

Silicon MOSFET devices are very sensitive to the operation temperature T, and their characteristics are strongly temperature-dependent [5]. The main parameters responsible for this are the effective carrier mobility μ and the threshold voltage V_{th}, resulting in the increase in the drain current through $V_{th}(T)$ and the decrease in the drain current through $\mu(T)$ with temperature. Increasing temperature decreases the slope of the $I_{ds}(V_{gs})$ curves. A certain value of V_{gs} can be found, at which the drain current becomes practically temperature-independent over a large temperature range. The variation of V_{th} with temperature in a wide range from −50 to +200 °C represents a nonlinear function, which slowly decreases with temperature and can be approximated by

$$V_{th}(T) = V_{th}(T_{nom}) + V_{T1}\Delta T + V_{T2}\Delta T^2 \tag{1.25}$$

where $\Delta T = T - T_{nom}$, $T_{nom} = 300\,\mathrm{K}(27\,^{\circ}\mathrm{C})$, and V_{T1} and V_{T2} are the linear and quadratic temperature coefficients for threshold voltage [20].

The variation of μ with temperature is related to the appropriate temperature variation of I_{sat} in Eq. (1.13), representing an almost straight line, which decreases with temperature [20]. The temperature dependence $I_{sat}(T)$ can be approximated by the linear function as

$$I_{sat}(T) = I_{sat}(T_{nom}) + I_T \Delta T \tag{1.26}$$

where I_T is the linear temperature coefficient for the saturation current.

The temperature dependencies of the MOSFET capacitances and series resistances can be described by the following linear equations:

$$C(T) = C(T_{nom}) + C_T \Delta T \tag{1.27}$$

$$R(T) = R(T_{nom}) + R_T \Delta T \tag{1.28}$$

where $C = (C_{gs}, C_{ds}, C_{gd})$, $R = (R_g, R_s, R_d)$, and R_T and C_T are the linear temperature coefficients for the capacitances and resistances, respectively [7, 28].

Figure 1.13 shows the modeled temperature dependencies of $V_{th}(T)$ and $g_m(T)$ for high-power LDMOSFET LP801. The results obtained by using the simple approximations in Eqs. (1.25) and (1.26) with the values $V_{T1} = -2\,\mathrm{mV/^{\circ}C}$, $V_{T2} = -8.55\,\mu\mathrm{V/(^{\circ}C)^2}$, and $I_T = -4.5\,\mathrm{mA/^{\circ}C}$ show a good prediction of the I–V characteristics in a wide temperature range.

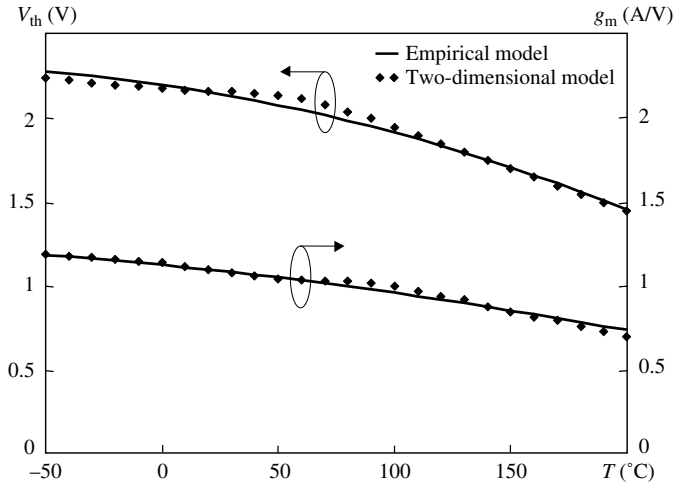

Figure 1.13 Modeled temperature dependencies of V_{th} and g_m.

At high values of V_{gs} and V_{ds} under DC measurement, the slope of $I_{ds}(V_{ds})$ curves can be negative, which occurs due to the self-heating effect in a highly dissipated power region. For the drain current model given by Eq. (1.7), this effect can be considered by adding a linear component describing the temperature dependence as

$$\beta(T) = \beta(T_{nom}) + \beta_T \Delta T_j \tag{1.29}$$

$$\gamma(T) = \gamma(T_{nom}) + \gamma_T \Delta T_j \tag{1.30}$$

where $\Delta T_j = R_{th} P_{dis} + \Delta T$, $R_{th}(°C/W)$ is the thermal resistance, P_{dis} is the DC power consumption in watts caused by DC biasing, and β_T and γ_T are the linear temperature coefficients with negative values, respectively [18].

Another way of considering the effect of the negative conductance at high biasing is to present the nonlinear $I_{ds}(V_{ds})$ model as

$$I_{ds}(T, p_T) = \frac{I_{ds}(T)}{1 + p_T V_d I_{ds}(T)} \tag{1.31}$$

where the drain current source $I_{ds}(T)$ is given by Eq. (1.13), $V_d = V_{ds}/\sqrt{1 + (\omega\tau_{th})^2}$, p_T is the self-heating temperature coefficient, V_{ds} is the drain–source supply voltage, $\tau_{th} = R_{th}C_{th}$ is the thermal time constant, R_{th} is the thermal resistance, C_{th} is the thermal capacitance, and T_j is the function of ambient temperature T and p_T. A thermal equivalent circuit can be added to the nonlinear MOSFET model as a parallel $R_{th}C_{th}$ circuit [13]. The thermal resistance R_{th} can be extracted from the temperature measurement of the DC characteristics. Because the slope of the DC measured $I_{ds}(V_{ds})$ curves changes its sign from positive to negative, the temperature coefficient p_T can be evaluated under the condition of

$$\frac{dI_{ds}(T, p_T)}{dV_{ds}} = 0 \tag{1.32}$$

As a result,

$$p_T = \frac{1}{I_{ds}^2(T)} \frac{dI_{ds}(T)}{dV_{ds}} \tag{1.33}$$

where $I_{ds}(V_{ds})$ curves are determined by measurement of the pulsed $I_{ds}(V_{ds})$ curves at ambient temperature T, and the value of $I_{ds}(T)$ is fixed the same as for zero slope of $I_{ds}(T, p_T)$.

The thermal time constant τ_{th} can be extracted by comparing pulsed $I_{ds}(V_{ds})$ curves calculated under different pulse widths and duty factors. A plot of I_{ds} as a function of pulse width under the fixed gate–source and drain–source bias voltages gives an appropriate value of τ_{th}.

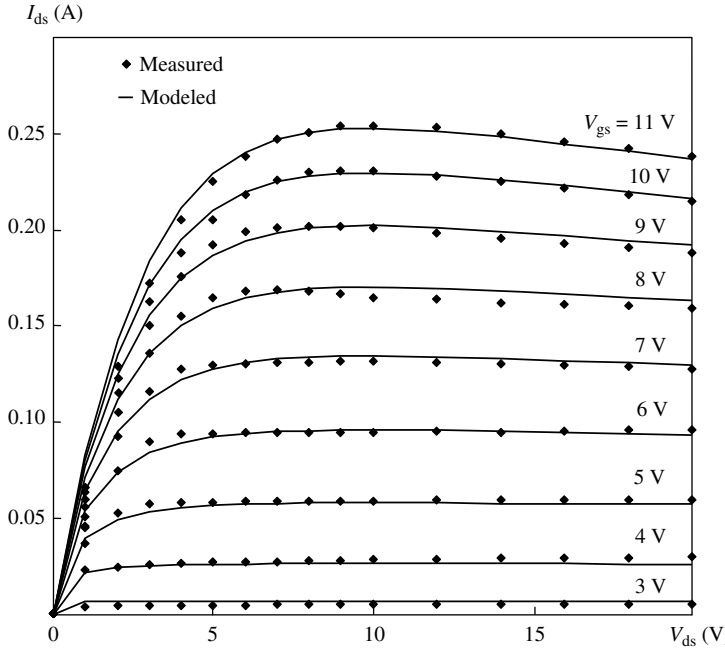

Figure 1.14 Measured and modeled $I_{ds}(V_{ds})$ curves of low-voltage LDMOSFET.

Figure 1.14 shows the comparison between the measured (DC measurement) and modeled $I_{ds}(V_{ds})$ curves for a 12.5-V LDMOSFET cell with the gate geometry of $1.25\,\mu m \times 1.44\,mm$. The effect of self-heating for the model parameters $p_T = 0.035\,1/AV$, $\alpha = 0.2\,1/V$, $\beta = \sigma = 0$, $S_{th} = 37\,mA/V$, $I_{th} = 1.5\,mA$, $V_{th} = 2.25\,V$, $I_{sat} = 0.48\,A$, $n = 1$, and $\lambda = 0.0005\ 1/V$ is described by Eq. (1.31).

1.3 Equivalent Circuits Characterizing Device Input and Output Impedances

To apply the proper matching and harmonic-control techniques to the high-efficiency power amplifier, which is necessary to design, and to make this design clear and comprehensible, it is very important to represent the input and output device impedances separately through the equivalent circuits, the elements of which will be the parts of the corresponding matching and harmonic-control circuits. For example, the series parasitic inductance at the device input may be considered a part of the low-pass matching section, or the shunt capacitance at the device output may represent an important element of the Class-E load

network with shunt capacitance. Besides, it helps to improve the power amplifier stability by choosing the proper impedances, thus preventing the formation of parasitic oscillators and potential excitation of self-oscillations.

Figure 1.15 shows the simplified small-signal silicon MOSFET equivalent circuit where the series source inductance L_s and device transit time τ are not considered because of their sufficiently small values for high-power MOSFETs in a frequency range of $f \leq 0.3f_T$, where $f_T = g_m/2\pi C_{gs}$. When the load resistor R_L is connected between the drain and source terminals, an analytical expression for the input device impedance Z_{in} can be obtained as

$$Z_{in} = R_g + \left(R_{gs} + \frac{1}{j\omega C_{gs}}\right) / \left[1 + \frac{C_{gd}}{C_{gs}} \frac{(1 + j\omega\tau_g)(1 + j\omega C_{ds}R_{L0}) + g_m R_{L0}}{1 + j\omega R_{L0}(C_{ds} + C_{gd})}\right] \tag{1.34}$$

where $R_{L0} = (R_L + R_d)\big/\left[1 + (R_L + R_d)/R_{ds}\right]$, R_L is the load resistance, and $\tau_g = R_{gs}$ C_{gs}, assuming that the series drain inductance L_d is compensated by the load-network capacitive reactance.

Next step is to derive the equivalent circuit corresponding to the input device impedance Z_{in} from Eq. (1.34), which is reduced to the equivalent circuit shown in Figure 1.16a. For preliminary estimation, when $\omega\tau_g \leq 0.3$ and the device output capacitive reactance is inductively compensated, the input equivalent circuit simplifies significantly and can represent an inductance, a capacitor, and a resistor connected in series, as shown in Figure 1.16b, where

$$L_{in} = L_g \tag{1.35}$$

$$R_{in} \cong R_g + R_{gs} \tag{1.36}$$

$$C_{in} \cong C_{gs} + C_{gd}\left[1 + g_m \frac{R_L + R_d}{1 + R_L/(R_{ds} + R_d)}\right] \tag{1.37}$$

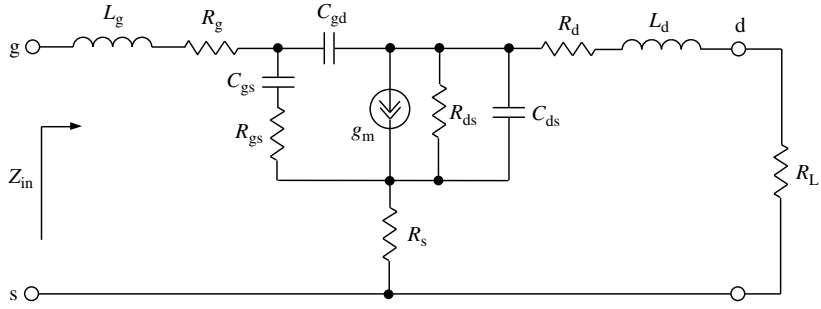

Figure 1.15 Simplified small-signal silicon MOSFET equivalent circuit.

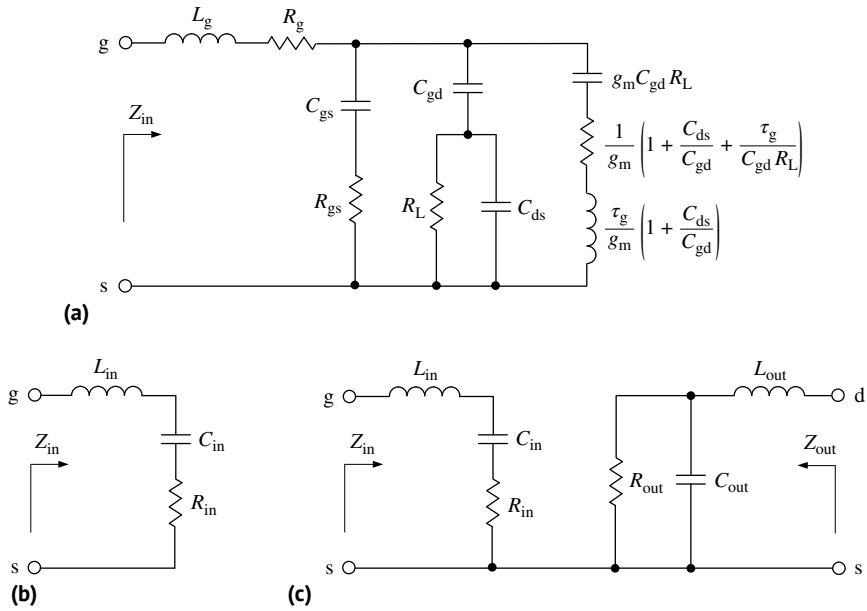

Figure 1.16 Equivalent circuits, characterizing device input and output.

Considering that usually $C_{gd} \ll C_{gs}$, the device equivalent output circuit can be represented by the series inductance $L_{out} = L_d$ and a parallel connection of the equivalent output resistance R_{out} estimated as the ratio of the fundamental voltage and fundamental current Fourier components (presented in Section 3.7 for different operation modes) and the output capacitance $C_{out} = C_{ds} + C_{gd}$, as shown in Figure 1.16c.

1.4 GaAs MESFETs and GaN HEMTs

Adequate representation for MESFETs and HEMTs in a frequency range up to millimeter-wave frequencies can be provided using the nonlinear device model shown in Figure 1.17a, which is very similar to a nonlinear MOSFET model [29, 30]. The intrinsic model is described by the channel charging resistance R_{gs} representing the resistive path for the charging of the gate–source capacitance C_{gs}, the feedback gate–drain capacitance C_{gd}, the drain–source capacitance C_{ds}, the gate–source diode to model the forward conduction current $i_{gs}(v_{gs})$, and the gate–drain diode to account for the gate–drain avalanche current $i_{gd}(v_{gs},v_{ds})$, which can occur at large-signal operation conditions. The gate–source capacitance

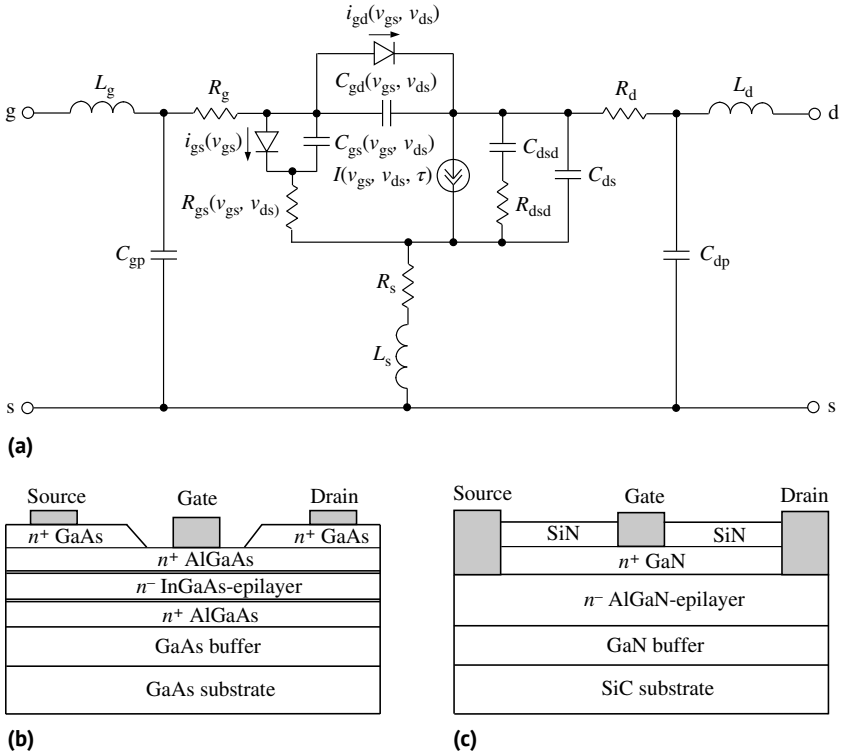

Figure 1.17 Nonlinear MESFET and HEMT model with HEMT physical structures.

C_{gs} and gate–drain capacitance C_{gd} represent the charge depletion region and can be treated as the voltage-dependent Schottky-barrier diode capacitances, being the nonlinear functions of the gate–source voltage v_{gs} and drain–source voltage v_{ds}. For negative gate–source voltage and small drain–source voltage, these capacitances are practically equal. However, when the drain–source voltage is increased beyond the current saturation point, the gate–drain capacitance C_{gd} is much more heavily back-biased than the gate–source capacitance C_{gs}. Therefore, the gate–source capacitance C_{gs} is significantly more important and usually dominates the input impedance of the MESFET or HEMT device. The influence of the drain–source capacitance C_{ds} on the device behavior is insignificant and its value is bias-independent. The capacitance C_{dsd} and resistance R_{dsd} model the dispersion of the MESFET or HEMT current–voltage characteristics due to trapping effect in the device channel, which leads to discrepancy between DC measurement and *S*-parameter measurements at higher frequencies [31, 32]. A large-signal model for monolithic power amplifier design should be

accurate for all operating conditions. In addition, the model parameters should be easily extractable, and the model must be as simple as possible. Various nonlinear MESFET and HEMT models with different complexities are available, and each one can be considered sufficiently accurate for a certain application. However, it is preferable to use the Angelov model for MESFETs and HEMTs, in particular to predict the large-signal behavior of the pHEMT devices using in high-power, high-efficiency millimeter-wave MMICs [33, 34]. By using three additional terms of the gate power-series function in Angelov model, better accuracy can be achieved in a large-signal modeling of AlGaN/GaN HEMT devices on SiC substrate [35]. This model can also be improved by incorporating two additional analytical expressions to model the device behavior in saturation region, which is important to design high-efficiency switchmode power amplifiers, for example, in inverse Class-F mode [36].

Figure 1.17b shows the cross-section of a physical structure of an InGaAs/AlGaAs HEMT device, where an undoped InGaAs *n*-epilayer is used as a channel and two heavily *n*-doped AlGaAs layers with a high energetic barrier for holes are necessary to maximize high electron mobility in the channel. In this case, spacing between AlGaAs layer and InGaAs channel is optimized to achieve a high breakdown voltage. An example of the physical structure of an AlGaN/GaN HEMT device is shown in Figure 1.17c, where an undoped AlGaN *n*-epilayer is used as a channel, *n* -type-doped GaN layer can suppress dispersion in the device current–voltage characteristics, and a SiN passivation layer with optimized parameters contributes to a lower-trap device structure [37]. Thermal conductivity of a GaN HEMT device is improved by using a SiC substrate. Note that the GaN-based technology can provide wider bandwidth and higher efficiency of the power amplifier due to high charge density and the ability to operate at higher voltages for GaN HEMT devices that are characterized by lower output capacitance and on-resistance [38, 39].

The basic electrical properties of the MESFET or HEMT device can be characterized by the admittance *Y*-parameters expressed through the device intrinsic small-signal equivalent circuit as

$$Y_{11} = \frac{j\omega C_{gs}}{1 + j\omega C_{gs} R_{gs}} + j\omega C_{gd} \tag{1.38}$$

$$Y_{12} = -j\omega C_{gd} \tag{1.39}$$

$$Y_{21} = \frac{g_m \exp(-j\omega\tau)}{1 + j\omega C_{gs} R_{gs}} - j\omega C_{gd} \tag{1.40}$$

$$Y_{22} = \frac{1}{R_{ds}} + j\omega\left(C_{ds} + C_{gd}\right) \tag{1.41}$$

where g_m is the device transconductance and R_{ds} is the differential drain resistance [40]. In this case, the dispersion effect, which is important at higher frequencies and modeled by C_{dsd} and R_{dsd}, cannot be considered.

By separating Eqs. (1.38)–(1.41) into their real and imaginary parts, the elements of the small-signal equivalent circuit can be analytically determined as

$$C_{gd} = -\frac{\mathrm{Im}Y_{12}}{\omega} \tag{1.42}$$

$$C_{gs} = -\frac{\mathrm{Im}Y_{11} - \omega C_{gd}}{\omega}\left[1 + \left(\frac{\mathrm{Re}Y_{11}}{\mathrm{Im}Y_{11} - \omega C_{gd}}\right)^2\right] \tag{1.43}$$

$$R_{gs} = \frac{\mathrm{Re}Y_{11}}{\left(\mathrm{Im}Y_{11} - \omega C_{gd}\right)^2 + \left(\mathrm{Re}Y_{11}\right)^2} \tag{1.44}$$

$$g_m = \sqrt{\left(\mathrm{Re}Y_{21}\right)^2 + \left(\mathrm{Im}Y_{21} + \omega C_{gd}\right)^2}\sqrt{1 + \left(\omega C_{gs} R_{gs}\right)^2} \tag{1.45}$$

$$\tau = \frac{1}{\omega}\sin^{-1}\left(\frac{-\omega C_{gd} - \mathrm{Im}Y_{21} - \omega C_{gs} R_{gs}\mathrm{Re}Y_{21}}{g_m}\right) \tag{1.46}$$

$$C_{ds} = \frac{\mathrm{Im}Y_{22} - \omega C_{gd}}{\omega} \tag{1.47}$$

$$R_{ds} = \frac{1}{\mathrm{Re}Y_{22}} \tag{1.48}$$

which are valid for a wide frequency range up to the transition frequency f_T [41].

If all extrinsic parasitic elements are known from the data sheet or directly determined from measurements performed at zero drain bias with the gate voltages lower than pinch-off voltage, the only problem is to obtain the admittance Y-parameters of the intrinsic two-port network from on-bias experimental data [42]. Consecutive steps shown in Figure 1.18 can represent such a determination procedure [43]:

- Measurement of the S-parameters of the extrinsic device.
- Transformation of the S-parameters to the impedance Z-parameters with subtraction of the series inductances L_g and L_d.
- Transformation of the impedance Z-parameters to the admittance Y-parameters with subtraction of the parallel capacitances C_{gp} and C_{dp}.
- Transformation of the admittance Y-parameters to the impedance Z-parameters with subtraction of series resistances R_g, R_s, R_d, and inductance L_s.
- Transformation of the impedance Z-parameters to the admittance Y-parameters of the intrinsic device two-port network.

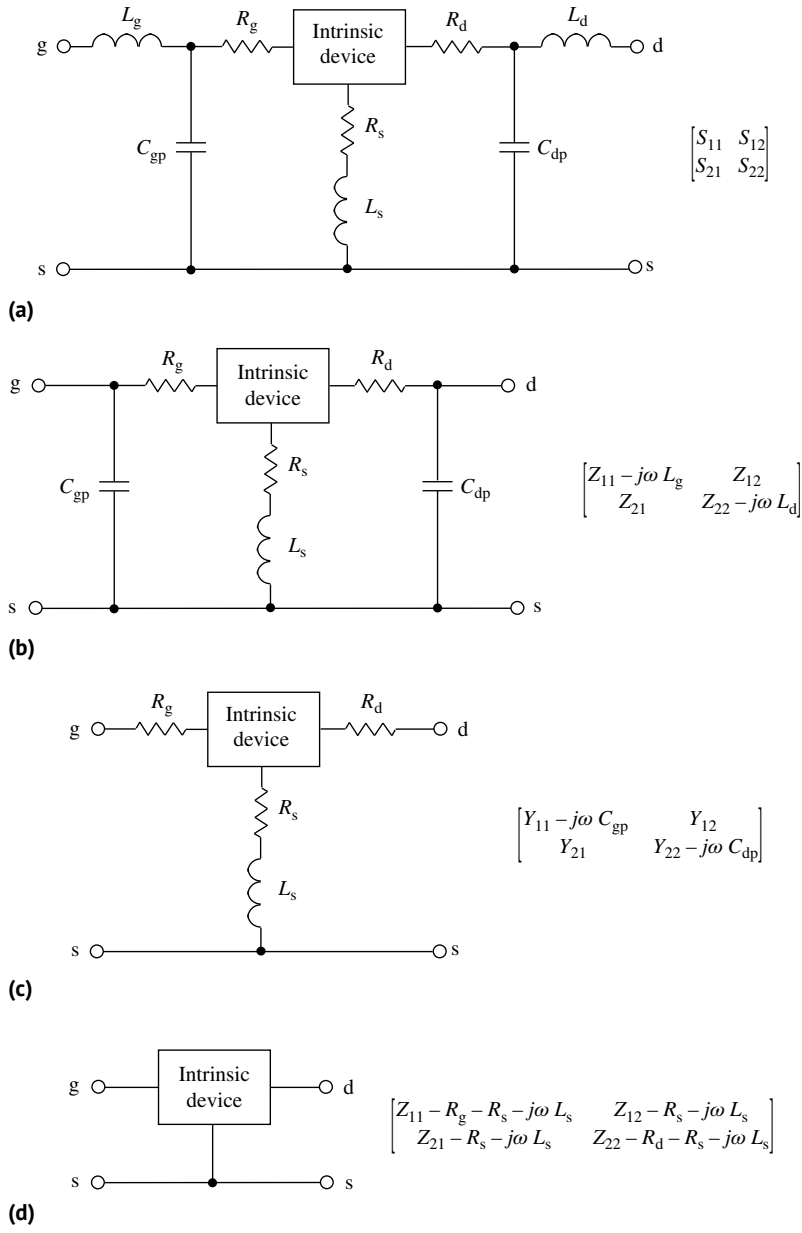

Figure 1.18 Method for extracting device intrinsic *Z*-parameters.

A simple and accurate nonlinear Angelov model can model the drain current–voltage characteristics and its derivatives, as well as the gate–source and gate–drain capacitances, for different submicron gate-length HEMT devices and commercially available MESFETs. The drain current source is described by using hyperbolic tangent functions as

$$I_{ds} = I_{pk}(1 + \tanh\psi)(1 + \lambda V_{ds})\tanh\alpha V_{ds} \tag{1.49}$$

where I_{pk} is the drain current at maximum transconductance with the contribution from the output conductance subtracted, λ is the channel-length modulation parameter, and $\alpha = \alpha_0 + \alpha_1\tanh\psi$ is the saturation voltage parameter, where α_0 is the saturation voltage parameter at pinch-off and α_1 is the saturation voltage parameter at $V_{gs} > 0$. The parameter ψ is a power-series function centered at V_{pk} with bias voltage V_{gs} as a variable:

$$\psi = P_1\left(V_{gs} - V_{pk}\right) + P_2\left(V_{gs} - V_{pk}\right)^2 + P_3\left(V_{gs} - V_{pk}\right)^3 + \cdots \tag{1.50}$$

where V_{pk} is the gate voltage for maximum transconductance g_{mpk}. The model parameters, as a first approximation, can be easily obtained from the experimental $I_{ds}\left(V_{gs}, V_{ds}\right)$ dependences at a saturated channel condition when all higher terms in ψ are assumed to be zero, and λ is the slope of the $I_{ds}(V_{ds})$ curves.

To evaluate the gate voltage V_{pk} and parameter P_1, it is necessary to define the derivatives of the drain current. If higher-order terms of ψ are neglected, the transconductance g_m becomes equal to

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = I_{pk}P_1\,\mathrm{sech}\left[P_1\left(V_{gs} - V_{pk}\right)\right]^2(1 + \lambda V_{ds})\tanh(\alpha V_{ds}) \tag{1.51}$$

The gate voltage V_{pk} that depends on the drain voltage can be extracted by finding the gate voltages for maximum transconductance, at which the second derivative of the drain current is equal to zero, resulting in the simplified expression

$$V_{pk}(V_{ds}) = V_{pk0} + \left(V_{pks} - V_{pk0}\right)(1 + \lambda V_{ds})\tanh(\alpha V_{ds}) \tag{1.52}$$

where V_{pk0} is measured at V_{ds} closely to zero and V_{pks} is measured at V_{ds} in the saturation region.

A good fitting of P_1 can be obtained using

$$P_1 = P_{1sat}\left[1 + \left(\frac{P_{10}}{P_{1sat}} - 1\right)\frac{1}{\cosh^2(B V_{ds})}\right] \tag{1.53}$$

where $P_{10} = g_{m0}/I_{pk0}$ at V_{ds} close to zero and B is the fitting parameter ($B \approx 1.5\alpha$). The parameter P_2 makes the derivative of the drain current asymmetric, whereas the parameter P_3 changes the drain current values at voltages V_{gs} close to pinch-off

voltage V_p. Three terms in Eq. (1.50) are usually enough to describe the behavior of the different MESFET or HEMT devices with acceptable accuracy.

The same hyperbolic functions can be used to model the intrinsic device capacitances C_{gs} and C_{gd}. When an accuracy of 5–10% is enough, the gate–source capacitance C_{gs} and gate–drain capacitance C_{gd} can be described by

$$C_{gs} = C_{gs0}\left[1 + \tanh\left(P_{1gsg}V_{gs}\right)\right]\left[1 + \tanh\left(P_{1gsd}V_{ds}\right)\right] \tag{1.54}$$

$$C_{gd} = C_{gd0}\left[1 + \tanh\left(P_{1gdg}V_{gs}\right)\right]\left[1 - \tanh\left(P_{1gdd}V_{ds} + P_{1cc}V_{gs}V_{ds}\right)\right] \tag{1.55}$$

where the product $P_{1cc}V_{gs}V_{ds}$ reflects the cross-coupling of V_{gs} and V_{ds} on C_{gd} and the coefficients P_{1gsg}, P_{1gsd}, P_{1gdg}, and P_{1gdd} are the fitting parameters. The approximate behavior of normalized gate–source capacitance C_{gs}/C_{gs0} (curve 1) and gate–drain capacitance C_{gd}/C_{gd0} (curve 2) as functions of V_{ds} for zero gate–source voltage is shown in Figure 1.19, where C_{gs0} and C_{gd0} are the gate–source and gate–drain capacitances at $V_{ds} = 0$, respectively. The character of the curves is the same for both positive and negative V_{gs}, except that the capacitance range decreases for the same range of V_{ds} with the decrease of V_{gs}.

The drain–source dispersive resistance R_{dsd} as a nonlinear function of the gate–source voltage V_{gs} can be defined by

$$R_{dsd} = R_{dsd0} + \frac{R_{dsdp}}{1 + \tanh\psi} \tag{1.56}$$

where R_{dsd0} is the minimum value of R_{dsd} and R_{dsdp} determines the value of R_{dsd} at the pinch-off [44].

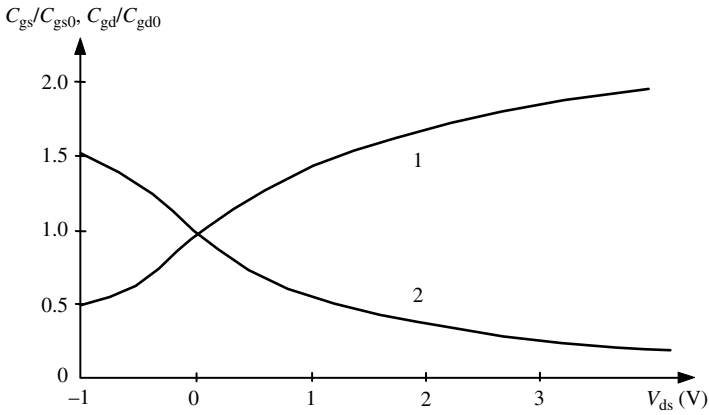

Figure 1.19 Gate–source and gate–drain capacitances versus drain–source voltage.

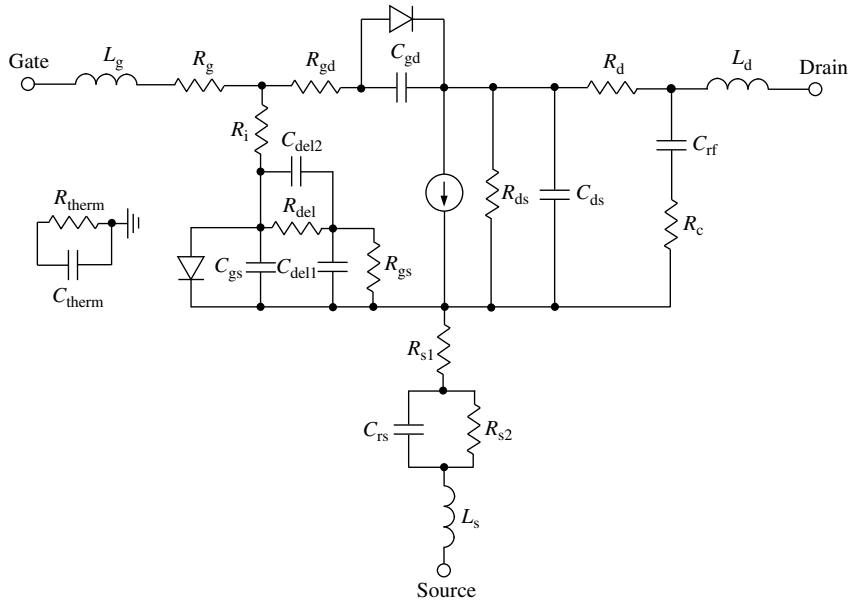

Figure 1.20 Generalized nonlinear equivalent circuit of GaN HEMT and SiC MESFET.

Figure 1.20 shows the generalized nonlinear equivalent circuit, which can describe the nonlinear behavior of GaN HEMT and SiC MESFET devices [35, 45]. Here, the delay network consisting of the resistance R_c and capacitance C_{rf} is introduced to address the dispersion phenomena, whereas the resistance R_{del} and capacitances C_{del1} and C_{del2} are included to more accurately describe the transistor response at high frequencies. The values of C_{del1} and C_{del2} are so small that they do not significantly affect the input impedance, but they directly shunt the input capacitance C_{gs} and effectively change the device response at higher frequencies. The thermal sub-circuit composed of the resistor R_{therm} and capacitor C_{therm} describes the dynamic self-heating effect. The presence of the source *RC* network (R_{s1}, R_{s2}, C_{rs}) is very important for the SiC MESFET devices to describe an increase in magnitude of S_{21} versus frequency.

1.5 BJTs and HBTs

Unlike LDMOSFETs, MESFETs, or HEMTs, which are voltage-controlled devices, the bipolar junction transistors (BJTs) and heterojunction bipolar transistors (HBTs) are current-controlled devices that control the amount of current

flowing through them from the emitter to the collector terminal in proportion to the amount of biasing voltage applied to their base terminal, resulting in a small current flowing into the base terminal to control a much larger collector current forming the basis of transistor action. The principal difference between the BJTs and HBTs is in the use of different semiconductor materials for the emitter–base junction and the base–collector junction, creating a heterojunction that limits the injection of holes from the base into the emitter region. Unlike BJT technology, this allows a high doping density to be used in the base, reducing the base resistance and providing higher gain and maximum operating frequency. As a result, HBTs have become very promising devices for different applications at microwave and millimeter-wave frequencies.

1.5.1 Nonlinear BJT and HBT Models

Figure 1.21a shows the nonlinear model of the bipolar transistor with extrinsic parasitic elements [46, 47]. Such a hybrid-Π equivalent circuit can model the nonlinear electrical behavior of bipolar transistors, particularly HBT devices, with sufficient accuracy up to about 20 GHz or even higher. The intrinsic model is described by the dynamic diode resistance r_π, the total base–emitter junction capacitance and base charging diffusion capacitance C_π, the base–collector diode required to account for the nonlinear effects at the saturation, the internal collector–base junction capacitance C_{ci}, the external distributed collector–base capacitance C_{co}, the collector–emitter capacitance C_{ce}, and the nonlinear current source $i(v_{be},v_{ce})$. The lateral and base semiconductor resistances underneath the base contact and the base semiconductor resistance underneath the emitter are combined into a base-spreading resistance r_b. The extrinsic parasitic elements are represented by the base bondwire inductance L_b, the base ohmic resistance R_b, the emitter ohmic resistance R_e, the emitter inductance L_e, the collector ohmic resistance R_c, and the collector bondwire inductance L_c. To increase the usable operating frequency range of the device up to 50 GHz and higher, it is necessary to include the collector-current delay time τ in the collector current source as $g_m \exp(-j\omega\tau)$.

Figure 1.21b shows the modified version of a bipolar transistor equivalent circuit, where $C_c = C_{co} + C_{ci}$, $r_{b1} = r_b C_{ci}/C_c$, and $r_{b2} = r_b C_{co}/C_c$ [48]. Such an equivalent circuit becomes possible due to an equivalent Π- to T-transformation of the elements r_b, C_{co}, and C_{ci} and a condition $r_b \ll (C_{ci} + C_{co})/\omega C_{ci} C_{co}$, which is usually fulfilled over the frequency range close to the device maximum frequency f_{max}. Then, from a comparison of the transistor nonlinear models, for a bipolar transistor in Figure 1.21b, for a MOSFET device in Figure 1.4, and for a MESFET (or HEMT) device in Figure 1.17a, it is easy to detect the circuit similarity of all these equivalent circuits, which means that the basic circuit design procedure is

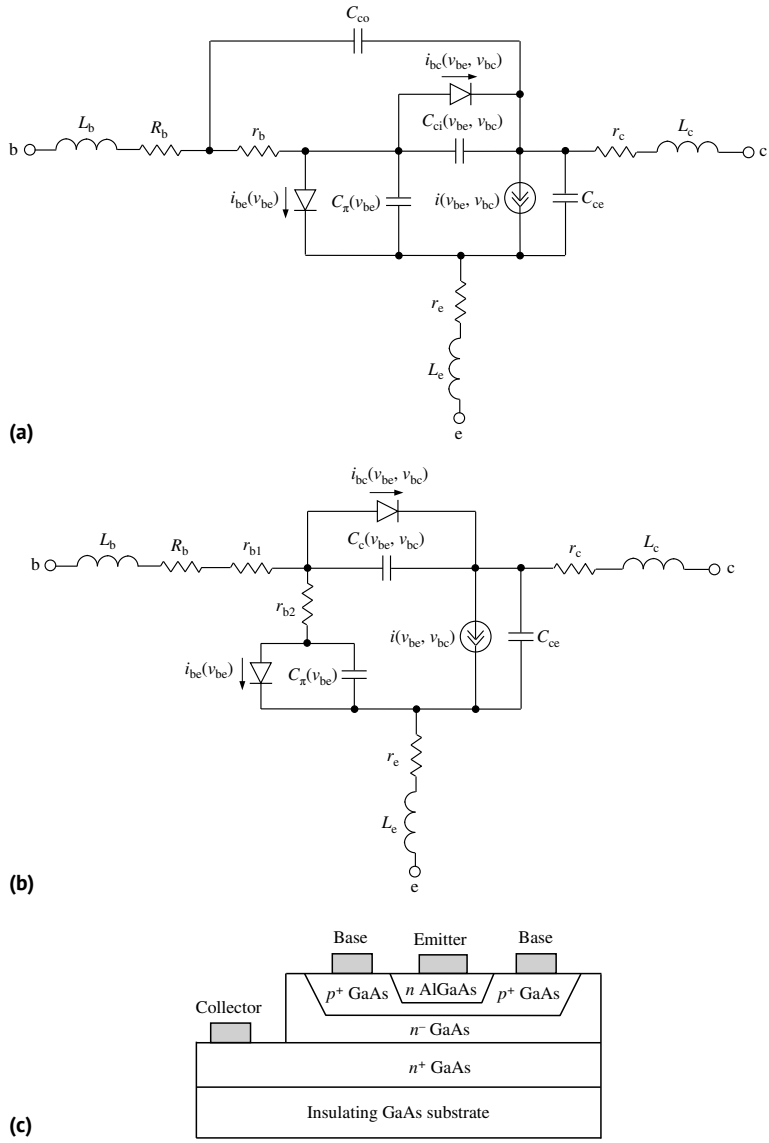

Figure 1.21 Nonlinear BJT and HBT models and HBT physical structure.

very similar for any type of bipolar or field-effect transistors. The difference is in the device physics and values of the model parameters. However, techniques for the representation of the input and output impedances, stability analysis based on feedback effect, and derivation of power gain and efficiency are very similar.

The cross-section of a physical structure of an AlGaAs/GaAs HBT device is shown in Figure 1.21c, with heavily *p*-doped base to reduce base resistance and lightly *n*-doped emitter to minimize emitter capacitance [49]. The lightly *n*-doped collector region allows the collector–base junction to sustain relatively high voltages without breaking down. The forward-bias emitter-injection efficiency is very high because the wider-bandgap AlGaAs emitter injects electrons into the GaAs *p*-base at a lower energy level, but the holes are prevented from flowing into the emitter by a high energy barrier, thus resulting in the ability to decrease the base-length and base-width modulation and to increase the frequency response. By using a wide-bandgap InGaP layer instead of an AlGaAs layer, the device performance over temperature can be improved [50]. The high linearity power performance in a Class-AB condition at the backoff power level, the ruggedness under mismatch and overdrive conditions, and the long lifetime of the InGaP/GaAs HBT technology make it very attractive for the 28-V power amplifier applications [51]. The growth process used for a high-voltage HBT device is identical to the process used for the conventional low-voltage HBT device, which is widely used in handset power amplifiers, except for changes to the collector because of the higher voltage operating requirements. The epitaxial growth process starts with a highly doped *n*-type collector layer and lightly *n*-doped collector drift region, then followed by a heavily doped *p*-type base layer and an InGaP emitter layer and finishes with an InGaAs cap layer [52]. As a result, the high-voltage HBT devices exhibit collector-base breakdown voltages higher than 70 V.

1.5.2 Determination of Equivalent Circuit Elements

The complete bipolar transistor small-signal equivalent circuit with extrinsic parasitic elements is shown in Figure 1.22. Based on this hybrid Π-type representation, the electrical properties of the bipolar transistors, particularly HBT devices, can be described with sufficient accuracy up to 30 GHz [53, 54]. Here, the extrinsic elements R_b, L_b, R_c, L_c, R_e, and L_e are the series resistances and lead inductances associated with the base, collector, and emitter, and C_{pbe}, C_{pbc}, and C_{pce} are the parasitic capacitances associated with the contact pads, respectively. The lateral resistance with the base semiconductor resistance underneath the base contact and the base semiconductor resistance underneath the emitter are combined into a base-spreading resistance r_b. The intrinsic model is described by the dynamic diode resistance r_π, the total base–emitter junction capacitance and base charging capacitance C_π, the transconductance g_m, and the output Early resistance r_{ce}, which model the effect of base-width modulation on the transistor characteristics due to variations in the collector–base depletion region [55]. To increase the usable operating frequency range of the device up to 50 GHz and higher, it is necessary to properly include the collector-current delay time in the current source as $g_m \exp(-j\omega\tau_\pi)$, where $\tau_\pi = r_\pi C_\pi$ is the transit time [56].

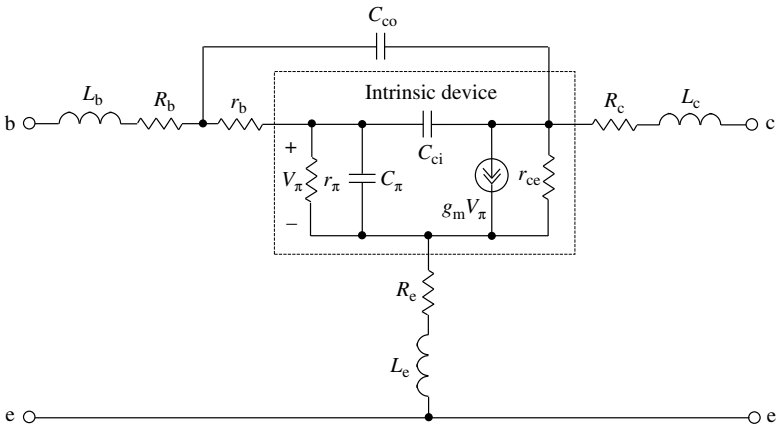

Figure 1.22 Bipolar transistor small-signal equivalent circuit.

If all extrinsic parasitic elements of the device equivalent circuit shown in Figure 1.22 are known, the intrinsic two-port network parameters can be embedded with the following determination procedure [53]:

- Measurement of the *S*-parameters of the transistor with extrinsic elements.
- Transformation of the *S*-parameters to the impedance *Z*-parameters with subtraction of the parasitic series elements L_b, R_b, L_e, R_e, L_c, and R_c.
- Transformation of the new *Z*-parameters to the *Y*-parameters with subtraction of the parasitic shunt capacitance C_{co}.
- Transformation of the new *Y*-parameters to the *Z*-parameters with subtraction of the parasitic series resistance r_b.
- Transformation of the new *Z*-parameters to the *Y*-parameters of the intrinsic device two-port network.

The bipolar transistor intrinsic *Y*-parameters can be written as

$$Y_{11} = \frac{1}{r_\pi} + j\omega(C_\pi + C_{ci}) \tag{1.57}$$

$$Y_{12} = -j\omega C_{ci} \tag{1.58}$$

$$Y_{21} = g_m \exp(-j\omega\tau_\pi) - j\omega C_{ci} \tag{1.59}$$

$$Y_{22} = \frac{1}{r_{ce}} + j\omega C_{ci} \tag{1.60}$$

After separating Eqs. (1.57)–(1.60) into their real and imaginary parts, the elements of the intrinsic small-signal equivalent circuit can be determined analytically as

$$C_{\pi} = \frac{\mathrm{Im}(Y_{11} + Y_{12})}{\omega} \tag{1.61}$$

$$r_{\pi} = \frac{1}{\mathrm{Re}Y_{11}} \tag{1.62}$$

$$C_{\mathrm{ci}} = -\frac{\mathrm{Im}Y_{12}}{\omega} \tag{1.63}$$

$$g_{\mathrm{m}} = \sqrt{(\mathrm{Re}Y_{21})^2 + (\mathrm{Im}Y_{21} + \mathrm{Im}Y_{12})^2} \tag{1.64}$$

$$\tau_{\pi} = \frac{1}{\omega}\cos^{-1}\frac{\mathrm{Re}Y_{21} + \mathrm{Re}Y_{12}}{\sqrt{(\mathrm{Re}Y_{21})^2 + (\mathrm{Im}Y_{21} + \mathrm{Im}Y_{12})^2}} \tag{1.65}$$

$$r_{\mathrm{ce}} = \frac{1}{\mathrm{Re}Y_{22}} \tag{1.66}$$

The series parasitic resistances r_{b}, R_{b}, R_{e}, and R_{c} can be calculated on the basis of physical parameters of the device or by adding them to the intrinsic device parameters [54]. The external parasitic parallel capacitance C_{co}, as well as the other device capacitances, can be estimated from the device behavior at low frequencies and cutoff operating conditions [57, 58].

1.5.3 Nonlinear Bipolar Device Modeling

The bipolar transistor can be considered as an interacting pair of *p*–*n* junctions, therefore the approach to describe its nonlinear properties is the same as that used for the diode modeling. The simple large-signal Ebers–Moll model with a single current source between the collector and the emitter is shown in Figure 1.23 [7, 59]. The collector–emitter source current I_{ce} is defined by

$$I_{\mathrm{ce}} = I_{\mathrm{sat}}\left[\exp\left(\frac{V_{\pi}}{V_{\mathrm{T}}}\right) - \exp\left(\frac{V_{\mathrm{bc}}}{V_{\mathrm{T}}}\right)\right] \tag{1.67}$$

where I_{sat} is the bipolar transistor reverse saturation current, and V_{T} is the thermal voltage obtained by

$$V_{\mathrm{T}} = \frac{kT}{q} \tag{1.68}$$

where q is the electron charge, k is Boltzmann's constant, and T is the temperature in kelvin.

The device terminal currents are defined as $I_{\mathrm{c}} = I_{\mathrm{ce}} - I_{\mathrm{bc}}$, $I_{\mathrm{e}} = -I_{\mathrm{ce}} - I_{\mathrm{be}}$, and $I_{\mathrm{b}} = I_{\mathrm{be}} + I_{\mathrm{bc}}$, where the diode currents are given by

$$I_{\mathrm{be}} = \frac{I_{\mathrm{sat}}}{\beta_{\mathrm{F}}}\left[\exp\left(\frac{V_{\pi}}{V_{\mathrm{T}}}\right) - 1\right] \tag{1.69}$$

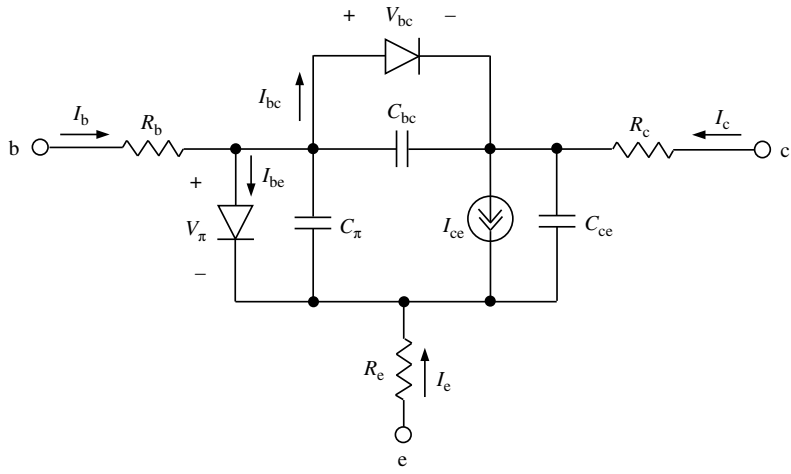

Figure 1.23 Large-signal Ebers–Moll model.

$$I_{bc} = \frac{I_{sat}}{\beta_R}\left[\exp\left(\frac{V_{bc}}{V_T}\right) - 1\right] \tag{1.70}$$

where β_F and β_R are the large-signal forward current gain and reverse current gain of a common emitter bipolar transistor, respectively.

The device capacitances C_π and C_{bc} consist of two components each and are modeled by the diffusion capacitance and junction capacitance, respectively, as

$$C_\pi = \tau_F \frac{dI_{be}}{dV_\pi} + C_{jeo}\left(1 - \frac{V_\pi}{\phi_e}\right)^{-m_e} \tag{1.71}$$

$$C_{bc} = \tau_R \frac{dI_{bc}}{dV_{bc}} + C_{jco}\left(1 - \frac{V_{bc}}{\phi_c}\right)^{-m_c} \tag{1.72}$$

where τ_F and τ_R are the ideal total forward time and reverse transit time, C_{jeo} and C_{jco} are the base–emitter and base–collector zero-bias junction capacitances, and m_e and m_c are the base–emitter and base–collector junction grading factors, respectively.

The collector–emitter substrate capacitance C_{ce} should be considered when designing the integrated circuits. Its representation is adequate for many cases, because the epitaxial-layer–substrate junction is reversed-biased for isolation purposes, and usually it is modeled as a capacitance with constant value.

The Ebers–Moll model cannot describe the second-order effects that can influence the accuracy of Eq. (1.67). One deals with the width of the neutral base

region when the widths of the depletion regions change with V_π and V_{bc}, thus providing a base-width modulation (Early effect [55]). Others involve the device behavior at low and high currents, resulting in a variation of the large-signal forward current gain β_F with collector current I_{ce}. For example, as the number of electrons injected into the base approaches the background doping concentration, the number of holes will increase to maintain space-charge neutrality, and the gain will drop (Webster effect [60]). At the same time, if the electron concentration overwhelms the doping in the collector, the base will push out, increasing the neutral base region and again reducing the gain (Kirk effect [61]). In addition, to find a better approximation of the distributed structure of the base–collector junction at microwave frequencies, the junction capacitance C_{bc} should be divided into two separate capacitances: internal C_{ci} and external C_{co}. The lateral resistance and the base semiconductor resistance underneath the base contact and the base semiconductor resistance underneath the emitter are combined into a base-spreading resistance r_b.

Figure 1.24 shows the modified Π-type Gummel–Poon nonlinear model of the bipolar transistor, which can describe the nonlinear electrical behavior of bipolar transistors, particularly HBT devices, with sufficient accuracy up to microwave frequencies [7, 62]. For the Gummel–Poon large-signal model, the collector source current I_{ce} is determined by

$$I_{ce} = \frac{I_{ss}}{q_b}\left[\exp\left(\frac{V_\pi}{n_F V_T}\right) - \exp\left(\frac{V_{bc}}{n_R V_T}\right)\right] \tag{1.73}$$

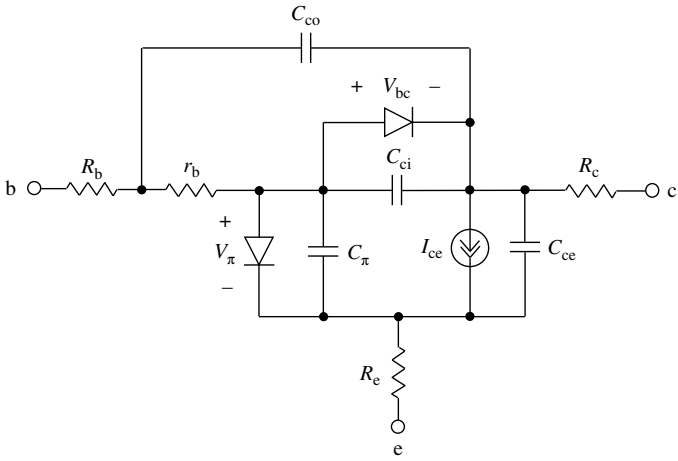

Figure 1.24 Large-signal Gummel–Poon model.

where I_{ss} is the BJT fundamental constant defined at zero-bias condition, n_F is the forward current emission coefficient, n_R is the reverse current emission coefficient, and q_b is the variable parameter defined by

$$q_b = \frac{q_1}{2} + \sqrt{\left(\frac{q_1}{2}\right)^2 + q_2} \tag{1.74}$$

where

$$q_1 = 1 + \frac{V_\pi}{V_B} + \frac{V_{bc}}{V_A} \tag{1.75}$$

$$q_2 = \frac{I_{ss}}{I_{KF}}\left[\exp\left(\frac{V_\pi}{n_F V_T}\right) - 1\right] + \frac{I_{ss}}{I_{KR}}\left[\exp\left(\frac{V_{bc}}{n_R V_T}\right) - 1\right] \tag{1.76}$$

where V_A is the forward Early voltage, V_B is the reverse Early voltage, I_{KF} is the forward knee current for high-level injection in the normal active region, and I_{KR} is the reverse knee current for low-level injection in inverse region. Although the physical mechanism of the collector current behavior given by Eqs. (1.74)–(1.76) is related to silicon BJTs, the highly doped base found in HBTs makes it unlikely that their base–collector potential will significantly change the base width, or that the injected electron concentration will approach the background doping at typical current levels [63]. However, mainly for historical reasons, and so that the model can still be used for silicon BJTs, they are usually retained for HBTs, although their physical behaviors are not exactly relevant.

The currents through model diodes are defined by

$$I_{be} = \frac{I_{sat}(0)}{\beta_{FM}(0)}\left[\exp\left(\frac{V_\pi}{n_F V_T}\right) - 1\right] + C_2 I_{sat}(0)\left[\exp\left(\frac{V_\pi}{n_{EL} V_T}\right) - 1\right] \tag{1.77}$$

$$I_{bc} = \frac{I_{sat}(0)}{\beta_{RM}(0)}\left[\exp\left(\frac{V_{bc}}{n_R V_T}\right) - 1\right] + C_4 I_{sat}(0)\left[\exp\left(\frac{V_{bc}}{n_{CL} V_T}\right) - 1\right] \tag{1.78}$$

where $I_{sat}(0)$ is the saturation current for $V_{bc} = 0$, $\beta_{FM}(0)$ and $\beta_{RM}(0)$ are the large-signal forward and reverse current gains of a common-emitter BJT in the mid-current region for $V_{bc} = 0$, C_2 and C_4 are the forward and reverse low-current nonideal base current coefficients, respectively, and n_{EL} and n_{CL} are the nonideal low-current base–emitter and base–collector emission coefficients, which are usually close to 2, respectively.

The nonlinear behavior of the intrinsic base resistance r_b can be described by

$$r_b = r_{bm} + 3(r_{b0} - r_{bm})\frac{\tan z - z}{z\tan^2 z} \tag{1.79}$$

where

$$z = \frac{\sqrt{1 + \frac{144}{\pi^2}\frac{I_b}{I_{rb}}} - 1}{\frac{24}{\pi^2}\sqrt{\frac{I_b}{I_{rb}}}} \tag{1.80}$$

where r_{bm} is the minimum base resistance that occurs at a high current level, r_{b0} is the base resistance at zero bias with a small base current level, and I_{rb} is the current where the base resistance falls halfway to its minimum value [7, 62].

The intrinsic device capacitances C_π, C_{ci}, and C_{co} are modeled by the diffusion capacitance and junction capacitance, each being

$$C_\pi = \frac{d}{dV_\pi}\left(\tau_{FF}\frac{I_{cc}}{q_b}\right) + C_{jeo}\left(1 - \frac{V_\pi}{\phi_e}\right)^{-m_e} \tag{1.81}$$

$$C_{ci} = \tau_R\frac{dI_{bc}}{dV_{bc}} + k_c C_{jco}\left(1 - \frac{V_{bc}}{\phi_c}\right)^{-m_c} \tag{1.82}$$

$$C_{co} = C_{jco}(1 - k_c)\left(1 - \frac{V_{bco}}{\phi_c}\right)^{-m_c} \tag{1.83}$$

where k_c is the fraction of the base–collector junction capacitance connected to the base resistance r_b, V_{bco} is the voltage through the capacitance C_{co}, and τ_{FF} is the modulated transit time defined by

$$\tau_{FF} = \tau_F\left[1 + X_{\tau F}\left(\frac{I_{cc}}{I_{cc} + I_{\tau F}}\right)^2 \exp\left(\frac{V_{bc}}{1.44V_{\tau F}}\right)\right] \tag{1.84}$$

where $X_{\tau F}$ is the transit time bias dependence coefficient, $I_{\tau F}$ is the high-current parameter for effect on τ_F, $V_{\tau F}$ is the value of V_{bc} where the exponential equals 0.5, and

$$I_{cc} = \frac{I_{ss}}{q_b}\left[\exp\left(\frac{V_\pi}{n_F V_T}\right) - 1\right] \tag{1.85}$$

From Eq. (1.81), the nonlinear behavior of the capacitance C_π strongly depends on the effect of the transit time modulation characterized by τ_{FF}. This transit charge variation results in significant changes of the transition frequency f_T at various operation conditions. For example, at medium currents, f_T reaches its peak value and is practically constant. Here, the ideal transit time is defined by $\tau_F = 1/(2\pi f_T)$ and the dominated base–emitter diffusion capacitance increases linearly with collector current. At low currents, f_T is dominated by junction

capacitance and increases with the increase in collector current. At high currents, the widening of the charge-neutral base region and pushing of the entire space-charge region toward the heavily doped collector region (Kirk effect) degrades the frequency response of the transistor by increasing the transit time and decreasing f_T. In this case, the transit time is modeled by τ_{FF}.

The extended nonlinear HBT equivalent circuit developed for computer-aided simulations, which is shown in Figure 1.25, is based on the representation of the collector current source through the power series and diffusion capacitances through the hyperbolic functions [64]. Here, to fully describe the losses related to the base–emitter and base–collector junctions, additional model resistances R_{be1}, R_{be2}, R_{bc1}, and R_{bc2} are included, as well as the delay time $\tau_{del} = R_{del}C_{del}$ is taken into account for better accuracy of the collector current frequency response.

The more complicated large-signal models, such as VBIC, HICUM, or MEXTRAM, include the effects of self-heating of a bipolar transistor, take into account the parasitic *p*–*n*–*p* transistor formed by the base, collector, and substrate regions, provide an improved description of depletion capacitances at large forward bias, and consider the avalanche and tunneling currents and other nonlinear effects corresponding to distributed high-frequency effects [63, 65]. The most common implementation of a lumped equivalent thermal network, describing the HBT self-heating behavior, represents a single- or two-section low-pass *RC* network with thermal resistances and capacitances.

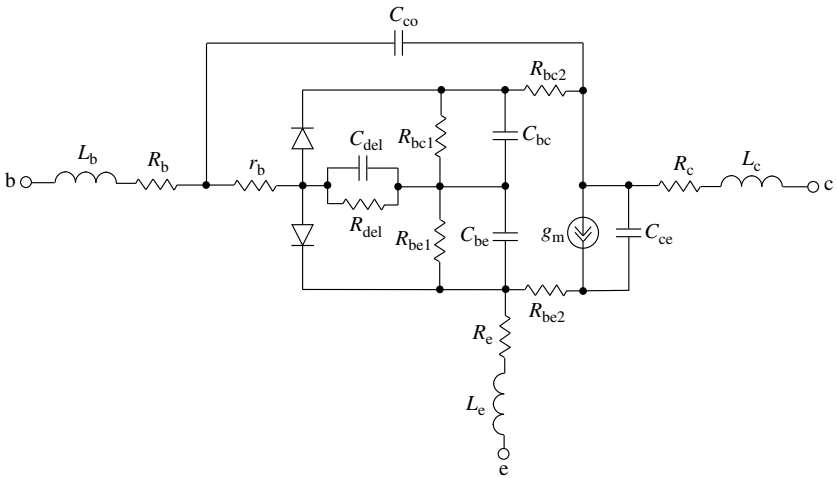

Figure 1.25 Extended nonlinear HBT equivalent circuit.

1.5.4 Large-signal Collector Capacitance

To equivalently estimate the input and output impedances of a bipolar transistor under large-signal operation, it makes sense to simplify the bipolar transistor nonlinear equivalent circuit, by limiting to the main nonlinear elements only. In this case, the external elements can be omitted as their effect is not so significant, especially at lower frequencies, and they can be included within the input matching circuit and load network, respectively, when, for example, the series parasitic base inductance can be considered as a part of a low-pass L-type matching circuit. For instance, for a bipolar transistor, the simplified equivalent circuit of which is shown in Figure 1.26, all elements of its equivalent circuit are nonlinear, depending significantly on operation mode, especially the transconductance g_m and base–emitter capacitance C_π. The base–emitter capacitance C_π consists of the diffusion and junction capacitances, and, at high frequencies, its reactance is sufficiently low, enabling the shunting of the base–emitter forward-biased diode. Because the transition frequency is defined by $\omega_T = g_m/C_\pi$, it is sufficient to consider only the nonlinear elements g_m, ω_T, and collector capacitance C_c, considering that the base resistance r_b poorly depends on the bias mode. As a result, the equivalent output capacitance can be defined as $C_{out} \cong C_c$ because $C_\pi \gg C_c$. The real part of the input impedance R_{in} can approximately be represented by the base resistance r_b, whereas the input equivalent capacitance can be defined as $C_{in} \cong C_\pi + C_c$. The feedback effect of the collector capacitance C_c through C_{c0} and C_{ci} is sufficiently high when load variations are directly transferred to the device input to a significant extent. At higher frequencies, since the input impedance of the high-power bipolar transistor is sufficiently low, it becomes inductive in view of the significant effect of the series parasitic base inductance.

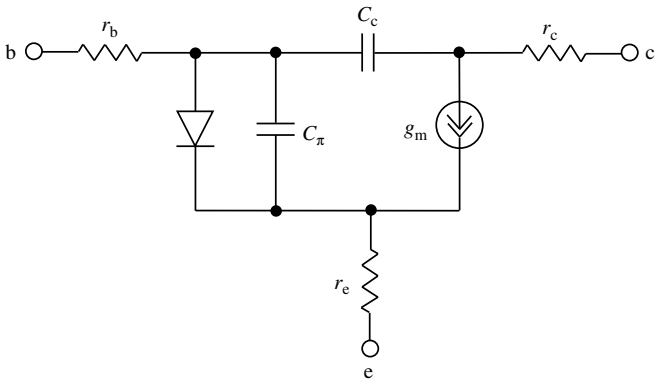

Figure 1.26 Bipolar transistor simplified equivalent circuit.

The collector capacitance C_c represents a junction capacitance and can be approximated by

$$C_c = \frac{C_{c0}}{\left(1 + \frac{v_c}{\phi}\right)^{\gamma}} \tag{1.86}$$

where ϕ is the built-in junction potential, γ is the junction sensitivity corresponding to the base–emitter and base–collector junction grading factors (m_e and m_c), and C_{c0} is the initial capacitance when $v_c = 0$. Note that similar equation is used to describe the behavior of the gate–drain and drain–source capacitances of high-power LDMOSFETs where the junction sensitivity γ corresponds to the gate–drain and drain–source junction grading factors (m_g and m_d) given by Eq. (1.19).

In a quasilinear case when considering the fundamental frequency only, the voltage across the capacitance is written as $v_c = V_{cc} + V_c \sin\omega t$, where V_{cc} is the collector DC-supply voltage and V_c is the fundamental voltage amplitude. Then, the current flowing through the collector capacitance can be defined as

$$\begin{aligned} i_c = C_c(v_c)\frac{dv_c}{dt} &= \frac{\omega C_{c0} V_c \cos\omega t}{\left(1 + \frac{V_{cc}}{\phi} + \frac{V_c}{\phi}\sin\omega t\right)^{\gamma}} \\ &= \frac{\omega C_c(V_{cc}) V_c \cos\omega t}{(1 + \xi \sin\omega t)^{\gamma}} \end{aligned} \tag{1.87}$$

where $C_c(V_{cc})$ is the small-signal capacitance in the operating point and $\xi = V_c/(V_{cc} + \varphi)$.

As a result, the average large-signal collector capacitance C_{c1} can be calculated through the fundamental Fourier series component as

$$C_{c1}(V_c) = \frac{I_{c1}}{\omega V_c} = \frac{C_c(V_{cc})}{\pi} \int_0^{2\pi} \frac{\cos^2\omega t}{(1 + \xi \sin\omega t)^{\gamma}} d(\omega t) \tag{1.88}$$

Figure 1.27 shows the voltage dependencies of the average collector capacitance for different junction sensitivity. Within a range of $\xi < 1$, the maximum large-signal value of $C_{c1}(V_c)$ deviates from the small-signal value of $C_c(V_{cc})$ by not more than 20% for an abrupt junction with $\gamma = 0.5$. This means that, for the load-network design procedure, initially it is enough to use the small-signal capacitance value from the transistor data sheet given for the specified DC-supply voltage, and then just need to increase this value by 20%.

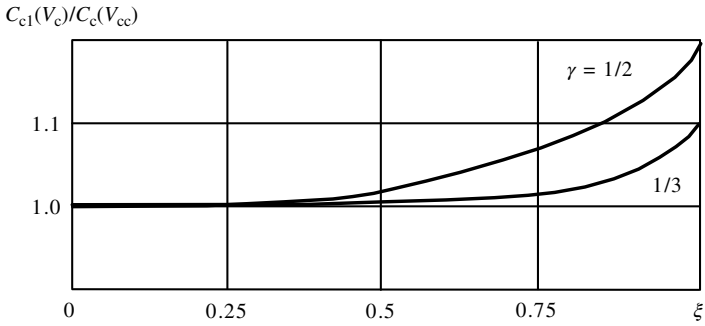

Figure 1.27 Large-signal behavior of collector capacitance.

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