1

Control Strategies and CAD Approach

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This chapter recalls the fundamentals of the switched-mode power supply control strategy on the one hand, and some general issues on the computer-aided design (CAD) approach on the other. Section 1.2 introduces the fundamentals on the buck, boost and buck-boost non-isolated converters. Relevant issues on MOSFET switching behavior are summarized in section 1.3.1 with emphasis on parameter identification for the system-level analysis of converters with respect to the control strategy. Optimization of the power stage with respect to specifications is presented in section 1.3.3 for the reader's convenience. So far, it is considered that the reader has sufficient background knowledge to understand the operation of non-isolated converters.

The focus is then turned to the transient performances of a given converter. Fast response to the line transient or load transient is a key issue for power density at the highest possible efficiency [COR 15a]. The control strategy is critical with regard to transient performances. A fast converter can limit the output capacitor, for example. Various control strategies may be envisaged, as shown in Figure 1.1. The control strategies are listed in section 1.4 [COR 15d]. Figure 1.1 shows that an extension of the so-called $V^2 I_C$ control generalizes ripple contributions to build a control quantity. The so-called ripple-based control is finding adoption as analogue implementations [CHE 16].

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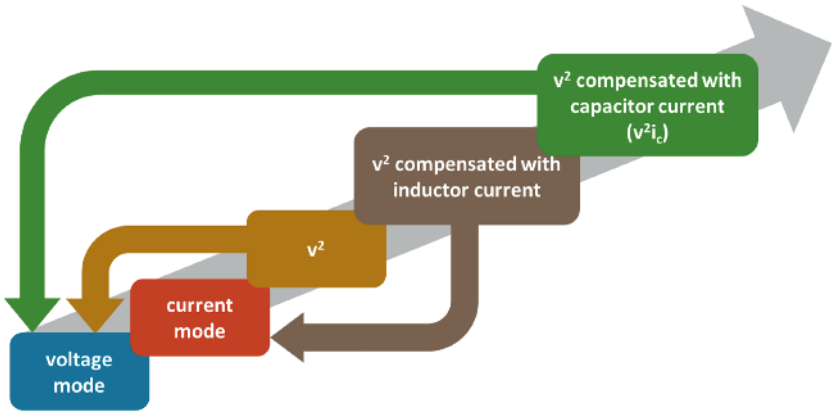

Figure 1.1. *Chart of a classical control strategy for non-isolated DC/DC converters. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

Analogue versus digital implementation provides insights into the control strategy. A rich literature exists on this topic [GUO 09, LI 12a]. A non-classical control strategy in digital form is presented in section 1.5 as a specific example from this perspective; however, the example covers the important issue of the minimum voltage deviation strategy.

Finally, section 1.6 introduces the fundamentals for a system-level optimization of a given converter architecture. Necessary models as well as optimization concerns are recalled. Examples are provided for the exploration of converter capabilities offered by a CAD design approach.

1.1. Objectives

Power converters that supply microprocessors, digital signal processors (DSP), field programmable gate arrays (FPGA) and similar digital loads must meet very demanding specifications:

– Steady-state specifications: accurate regulation of the supply voltage, very low-voltage ripple ($<1\%$ of V_{OUT} amplitude), high efficiency;

– Fast dynamic response under load steps (Figures 1.2 and 1.3): the converter must meet a tight voltage regulation under aggressive load current

steps from a full load to an idle state; it is an effective way of saving energy in the microprocessor, but it is very demanding for the power converter;

– Adaptive voltage positioning (Figure 1.4): the supply voltage depends on the current demanded by the load;

– Fast voltage tracking (Figure 1.5): the supply voltage must follow a dynamic reference. This technique is also used to save energy from the load side, but it becomes very demanding for the power converter. For example, dynamic voltage scaling to supply microprocessors or similar loads [LU 15], [SOT 07], [SU 08a] and [BUR 00] or envelope tracking use in RF amplifiers to minimize losses in the amplifier [CHE 14b].

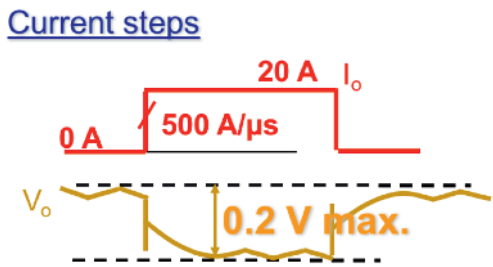

Figure 1.2. *Load-step transient. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

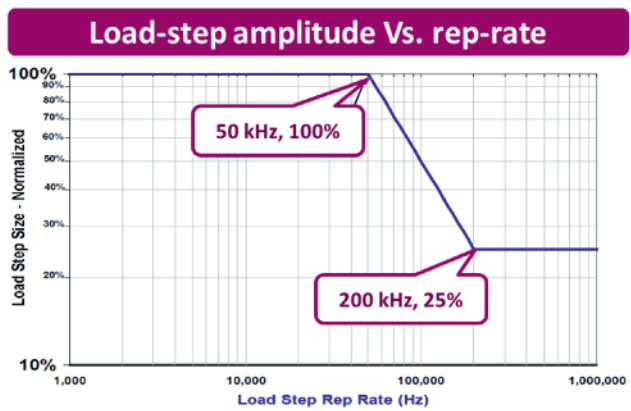

Figure 1.3. *Frequency of the load step for an INTEL microprocessor*

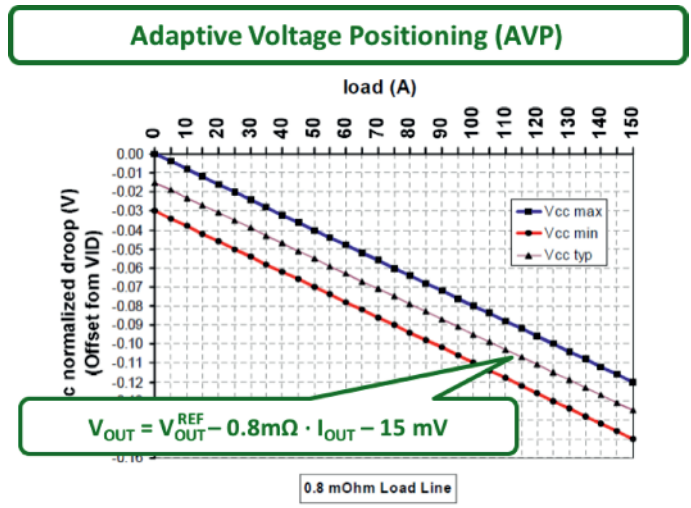

Figure 1.4. *Adaptative voltage positioning. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

The traditional design of the voltage regulation module (VRM) has been developed with a huge effort to reduce the size and cost of the output capacitor by including a very fast converter with a very low inductance and a very fast control. A slow converter would require huge output capacitors. To achieve this goal, it is required to operate at very high switching frequency and to use very fast control techniques (even nonlinear techniques) to optimize the capabilities of the power stage. Designing integrated power converters, very small capacitors and inductors becomes even more critical to be able to integrate them.

Regarding dynamic voltage scaling, the reduction of output capacitors is not only a cost or size issue, but also it is required to meet tracking time and tracking energy [STR 99]. Designing for a given tracking time, less charge (or discharge) current and less inductor slew rate are necessary if the output capacitance is small, thus reducing the tracking energy and increasing the efficiency. Clearly, a low output capacitance and a relatively high inductance design would be very suitable to changing the voltage fast with low tracking energy and high efficiency. However, there would be two problems encountered with this solution: (1) poor regulation under load current steps and (2) large size of the inductor.

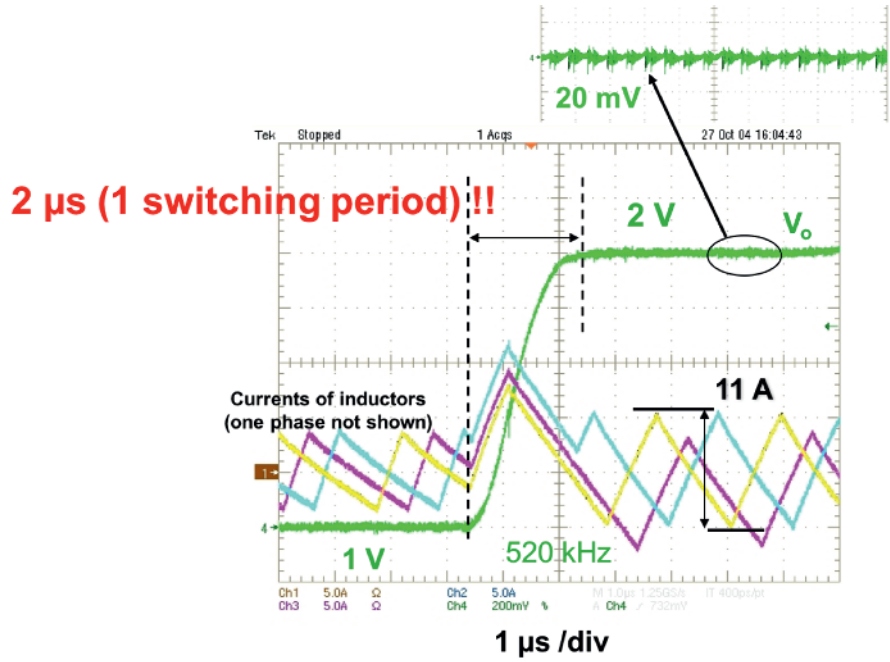

Figure 1.5. *Example of a dynamic voltage scaling. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

High switching frequency is very convenient from the perspective of the dynamic response and size, but from the point of view of the efficiency, it becomes a burden. The multiphase concept, several converters in parallel and time-shifted, can help to meet the dynamic response specs without an excessive increment of the switching frequency. A new degree of freedom appears to find the appropriate trade-off between switching frequency, efficiency and number of phases.

Many questions arise with respect to the design: which output filter (inductance and capacitance) must be used, which switching frequency, how many phases, which is the most appropriate control strategy?

The specifications are very demanding, which results in a very complex task to optimize the design that meets all the required specifications. To optimize

this power converter, CAD tools become mandatory. These CAD tools must account for both the power stage and the control stage.

It is important to highlight that even with an ideal control, the LC filter represents a limit to the fastest response that can provide the power converter. The minimum time for a state transition in the buck converter is obtained by applying the maximum principle or Pontryagin's principle [MAS 16]. This principle gives the necessary conditions for the input to a system if a defined state has to be reached within a minimum time. In [SOT 07], this principle is applied to a buck converter, for obtaining the minimum time control law: there must be at most one transition of the voltage applied to the filter, from 0 to V_{in} or vice versa to achieve minimum time (Figure 1.6).

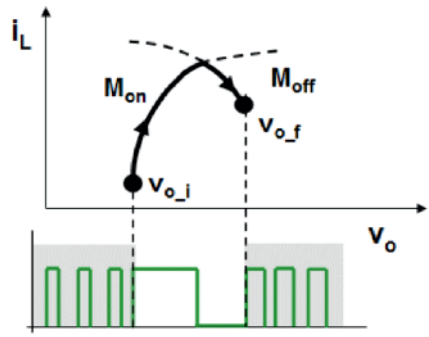

Figure 1.6. *Up-step transition in the buck converter: phase-plane trajectories (top) and minimum time control law (bottom)*

Figure 1.7 shows the minimum time transition when the control law is applied to a buck converter to move from one state to another. Figure 1.8 shows the comparison of the minimum time transition with the duty cycle step transition in the same converter. Clearly, the minimum time transition is much better. There is no overshoot and the stable state is reached within the minimum time achievable by the converter.

The minimum time concept provides the maximum dynamic response that a given LC filter can achieve. This is really valuable information for designing a converter. This concept can be applied to either voltage steps or current steps, which are used in the following section to determine the LC filter design space that can meet the defined specifications.

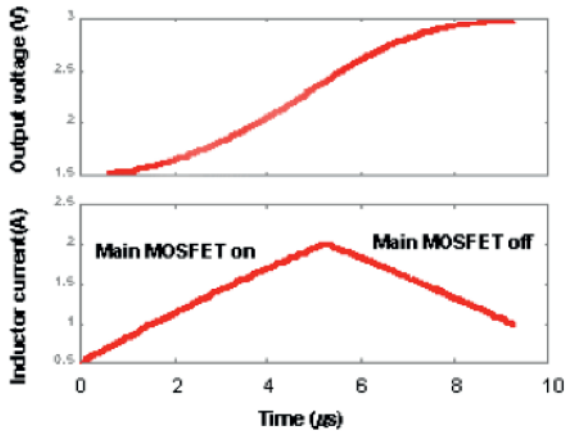

Figure 1.7. *Minimum time transition of the voltage step*

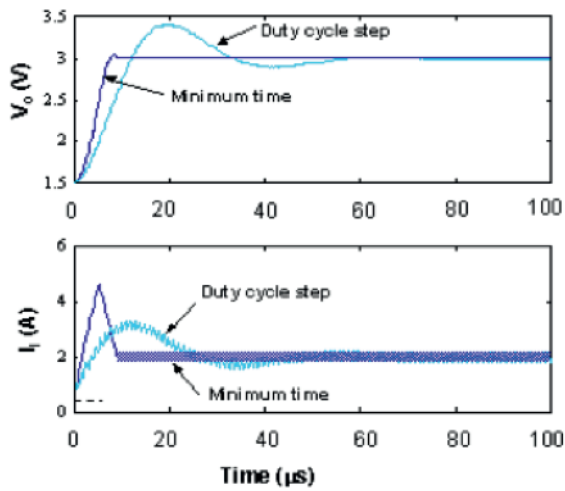

Figure 1.8. *Comparison of the minimum time transition with the response to a duty cycle step. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

1.2. Operation principle of three non-isolated converters

Converters for Internet of things (IoT) and mobile devices are mostly non-isolated converters. Galvanic isolation is required for line-connected equipment, mainly for safety purposes. However, a typical mobile device operates on a battery with reduced voltage levels; thus, isolation or large voltage transformation ratio is not required. This section briefly describes three non-isolated power converters that can step-down, step-up or follow the input voltage.

1.2.1. *Buck converter operation*

A buck or step-down regulator is shown in Figure 1.9 (top). An inductor and a capacitor form the output filter that is switched to the input voltage or to the ground by the high-side switch (sw1) or the low-side switch (sw2), respectively. Most low-voltage buck converters use the low-side switch as a freewheeling diode. However, this switch can be replaced by a diode at the expense of higher conduction losses. The output voltage is generated by alternatively switching the inductor to the battery voltage during an on-time, as shown in Figure 1.9 (middle), or the ground during an off-time, as shown in Figure 1.9 (bottom). The inductor current rises during the on-time and decreases during the off-time, while the capacitor maintains almost a constant output voltage. A conduction cycle is defined as one on-time, T_{on}, followed by one off-time, T_{off}. The length of the conduction cycle is the switching period, T_{sw}, and the rate of the conduction cycle is the switching frequency, F_{sw}. During the on-time, the inductor follows the relationship:

$$\frac{dI_L}{dt} = \frac{V_{in} - V_{out}}{L} \qquad [1.1]$$

Similarly, during the off-time, the inductor follows the relationship:

$$\frac{dI_L}{dt} = -\frac{V_{out}}{L} \qquad [1.2]$$

During a steady-state operation, the inductor current at the end of the cycle reaches the same value as at the beginning of the cycle. Therefore, the overall current variation through the inductor is zero:

$$\Delta I_L = I_L\left(T_{sw}\right) - I_L\left(0\right) = 0 \qquad [1.3]$$

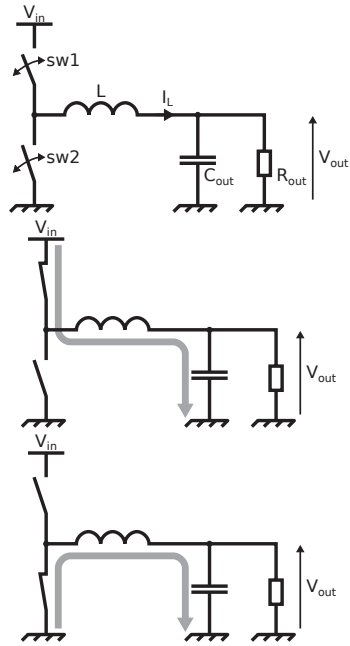

Figure 1.9. *Synchronous buck converter and its conduction states*

Using equations 1.1 and 1.2 in 1.3, we obtain:

$$\Delta I_L = 0 = \frac{V_{in} - V_{out}}{L} T_{on} - \frac{V_{out}}{L} T_{off} \qquad [1.4]$$

Rearranging the terms, we obtain:

$$V_{out} = \frac{T_{on}}{T_{on} + T_{off}} V_{in} = \frac{T_{on}}{T_{sw}} V_{in} = D V_{in} \qquad [1.5]$$

Thus, the output voltage of the buck converter depends on the input voltage and the ratio of the on-time over the switching period, which is also called the duty cycle, D. This simple equation assumes perfect elements that are not available to the designer; however, non-idealities will only introduce small variations. The output voltage is theoretically limited between the battery and the ground. Practical limitations such as a limited duty cycle and the resistance of various elements will reduce that range.

Input and output voltages are part of the specifications of the system. The designer focuses on the time-domain variables by selecting a switching frequency and a control mode that will adjust the on-time or off-time, or both. This also outlines the fact that time-domain simulations are extensively used to design a switched-mode converter since the mode of operation of the converter is based on time sequences.

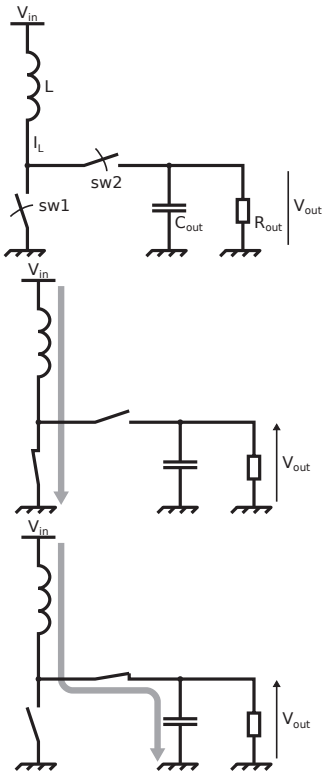

Figure 1.10. *Synchronous boost converter and its conduction states*

1.2.2. *Boost converter operation*

A boost or step-up converter is presented in Figure 1.10 (top). During the on-time, the switch sw1 connects the switching end of the inductor to the

ground, as shown in Figure 1.10 (middle). The inductor current rises according to the relationship:

$$\frac{dI_L}{dt} = \frac{V_{in}}{L} \qquad [1.6]$$

During the off-time, the switch sw2 connects the switching end of the inductor to the output, as shown in Figure 1.10 (bottom). A diode can be used instead of a switch at the expense of higher conduction losses. The inductor current decreases according to the relationship:

$$\frac{dI_L}{dt} = \frac{V_{in} - V_{out}}{L} \qquad [1.7]$$

For the buck converter, charge-balance principle during a steady-state operation can be used to determine the DC transfer ratio:

$$V_{out} = \frac{T_{on} + T_{off}}{T_{off}} V_{in} = \frac{1}{1 - D} V_{in} \qquad [1.8]$$

The output voltage of the boost converter depends on time-related ratios as well as the input voltage. Second-order elements come into play, but they do not change the fundamental results of the time-domain analysis.

The output voltage of the boost converter can only be controlled to be above its input voltage. The output voltage can theoretically reach an infinitely high value. However, practical limitations are induced by parasitic resistances and maximum duty cycles that can be generated by the control circuit.

1.2.3. *Buck-boost converter operation*

A four-switch buck-boost converter is shown in Figure 1.11 (top). It can be used as a buck converter by turning on switch sw4, turning off switch sw3 and using switches sw1 and sw2 with the states shown in Figures 1.11 (middle-down) and 1.11 (bottom). Similarly, it can be used as a boost converter by turning on switch sw1, turning off switch sw2 and using switches sw3 and sw4 with the states shown in Figures 1.11 (middle-up) and 1.11 (middle-down). A third operation mode can be achieved by switching on switches sw1 and sw3 during the on-time and turning on switches sw2 and sw4 during the off-time

using the states shown in Figures 1.11 (middle-up) and 1.11 (bottom). During the on-time, the inductor current rises according to the relationship:

$$\frac{dI_L}{dt} = \frac{V_{in}}{L} \qquad [1.9]$$

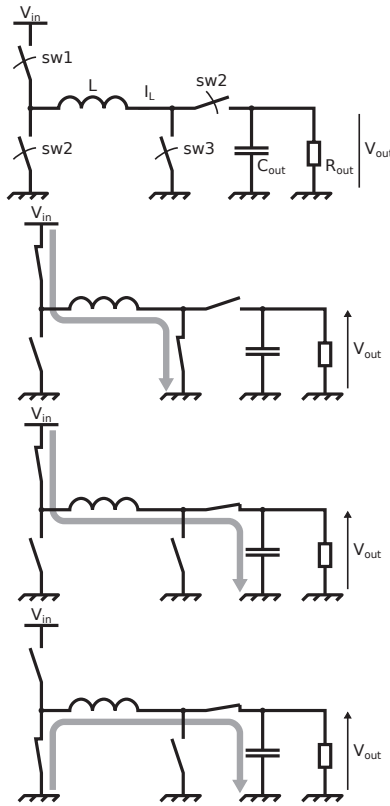

Figure 1.11. *Synchronous buck-boost converter and its conduction states*

During the off-time, the inductor current decreases according to the relationship:

$$\frac{dI_L}{dt} = \frac{-V_{out}}{L} \qquad [1.10]$$

Using the charge-balance equation, we can determine the DC transfer ratio of the buck-boost converter as follows:

$$V_{out} = \frac{Ton}{T_{off}} V_{in} = \frac{D}{1-D} V_{in} \qquad [1.11]$$

Depending on the duty cycle, the output voltage can be either lower or higher than the input voltage of the converter. This flexibility has a cost as the four switches are constantly switching and the RMS current through the inductor is higher than in the boost-only or buck-only operation, hence a degraded efficiency. Therefore, we can use the buck-boost converter as a boost or buck when the input voltage is lower or higher than the output voltage, respectively. When the output voltage is close to the input voltage, the input voltage can also follow a four-switch buck-boost. We still benefit from the line rejection and the accuracy of the converter when the converter works in the buck-boost mode.

1.3. Power stage

The power stage of the converter includes the switches and their associated drivers as well as power passive components. For the three converters considered (buck, boost and buck-boost), it can be two or four switches and drivers, two capacitors and an inductor. We may include other subcircuits such as various current detectors and current sensors. The design of these elements as such is not detailed in this chapter.

1.3.1. *MOSFET switching an inductive load*

Converters that are taken into consideration are hard-switching converters, i.e. the on-time switch switches a non-zero voltage V_{drain} with an inductive load carrying a non-zero current I_{ind}. A simplified model of a MOSFET transistor is shown in Figure 1.12 (top). During the off-state, the transistor is modeled as three capacitors between each terminal and a diode, as shown in Figure 1.12 (middle-up). During the switching transition, the transistor behaves as a voltage-controlled current source, as shown in Figure 1.12 (middle-down). When in the on-state, the transistor can be modeled as a resistor, as shown in Figure 1.12 (bottom). The parasitic capacitors are not constant capacitors, i.e. their actual value changes when the voltage between their two terminals changes. The on-state resistance is not constant either, which mainly depends on the driving voltage.

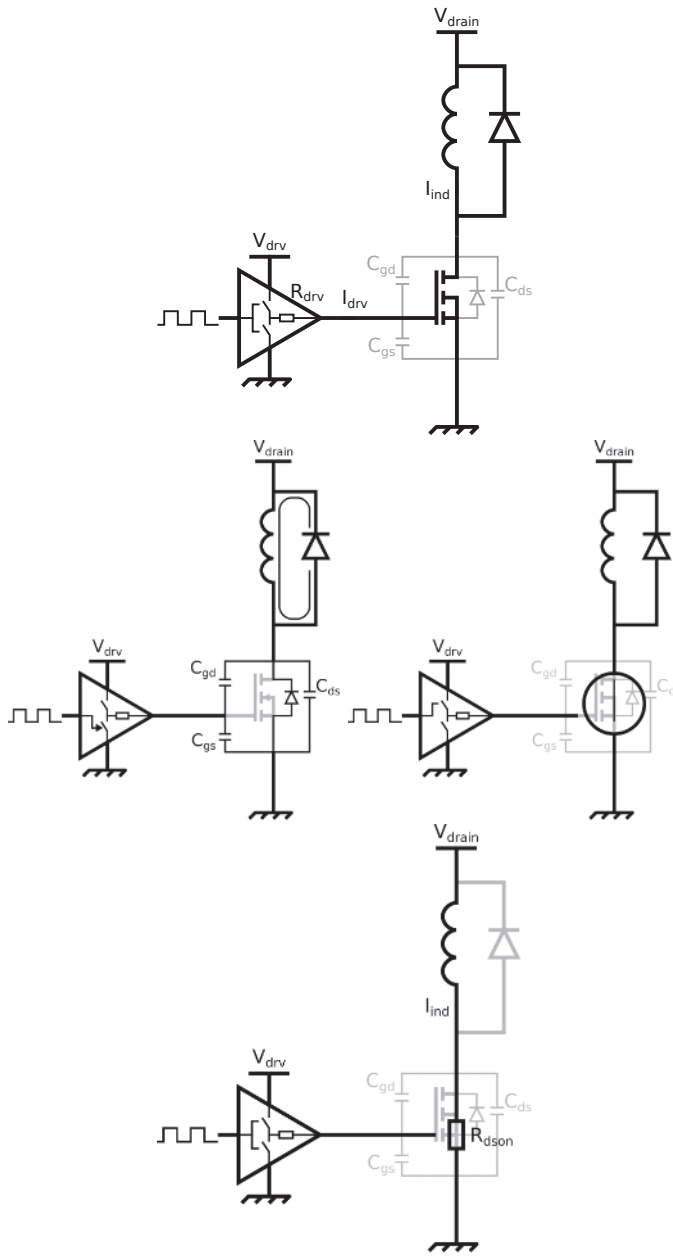

Figure 1.12. *Model of a transistor switching an inductive load*

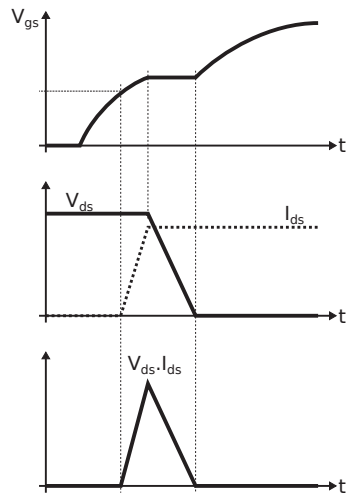

Figure 1.13. *Turn-on sequence of a MOS transistor switching an inductive load*

The turn-on sequence of an N-type MOSFET transistor switching an inductive load is shown in Figure 1.13. The inductor current is assumed to be constant over the transition time; therefore, the inductive load is modeled as a constant current source and an ideal diode. The gate driver is modeled as an ideal logic buffer with a constant output resistance R_{drv} and a supply voltage V_{drain}. When the transistor is initially in the off-state, the parasitic capacitor charges are:

$$Q_{gs} = 0$$
$$Q_{gd} = -C_{gd}V_{drain}$$
$$Q_{ds} = C_{ds}V_{drain}$$

When the transistor is in the on-state, the parasitic capacitor charges are:

$$Q_{gs} = C_{gs}V_{drv}$$
$$Q_{gd} = C_{gd}V_{drain}$$
$$Q_{ds} = 0$$

At this point, we can note that the charge and discharge of the parasitic capacitors dissipate a finite amount of energy. This energy is transferred from the power source to the transistor and discharged through the driver at each conduction cycle. Then, the average power dissipated by the driver and the transistor to charge and discharge the parasitic capacitors of the transistor can be approximated as:

$$P_{sw} = 0.5 \left(C_{gs} V_{drv}^2 + C_{gd} \left(V_{drv} + V_{drain} \right) V_{drv} + C_{ds} V_{drain}^2 \right) f_{sw} \qquad [1.12]$$

where f_{sw} is the switching frequency of the converter. Equation 1.12 describes the losses related to the charge and discharge of the parasitic capacitors of the transistor. Switching the transistor also generates crossover losses. These losses are related to the turn-on speed of the transistor.

Figure 1.13 shows the turn-on signals of a MOSFET. When the control signal rises, the driver charges the gate-source and gate-drain capacitors of the transistor. When the gate-source voltage reaches the threshold voltage of the transistor, the transistor becomes a voltage-controlled voltage source. The gate-source voltage increases until the drain-source current of the transistor reaches the inductor current value and the diode turns off. When the freewheeling diode turns off, the drain voltage decreases as well as the voltage of the gate-drain capacitor of the transistor. The decrease rate mainly depends on the gate-drain capacitor of the transistor and the driver strength. The transistor remains in the voltage-controlled current source until the drain-source voltage becomes equal to the gate-source voltage minus the threshold voltage of the transistor. Then, the nonlinear resistor shown in Figure 1.12 (bottom) applies and the driver fully charges the gate of the transistor.

During the turn-on of the transistor, the drain-source voltage and the drain-source current reaches a peak value of $V_{drain} \cdot I_{ind}$. The instantaneous power dissipated through the transistor is shown in Figure 1.13. These crossover losses depend on the drain voltage, the inductor current, the gate-to-drain capacitor of the transistor, the transistor transconductance and the driver strength. An estimate of these losses is proposed in [MAN 12]; however, the nonlinear behaviors of the transconductance and the driver strength make this estimate difficult. Furthermore, for low-voltage systems switching battery-level voltages, the crossover time is short and the switching speed is for the most part not limited by the device itself but by the

packaging. Any impedance between the source of the transistor and the ground plane acts as degeneration impedance and reduces the switching speed. After a first initial sizing, it is often quicker to extensively simulate the system when accurate electrical models are available.

The turn-off of the transistor is similar to the turn-on sequence. The driver discharges the gate-source and gate-drain capacitor of the transistor until the transistor leaves the resistive model region defined as:

$$V_{ds} < V_{gs} - V_t \qquad [1.13]$$

where V_t is the threshold voltage of the transistor. Then, the transistor becomes a voltage-controlled current source whose current is almost equal to the inductor current. Therefore, the inductor charges the drain-source and gate-drain parasitic capacitors of the transistor. For the turn-on of the switch, the rate of change of the drain voltage is highly dependent on the driver strength and the gate-to-drain capacitor of the transistor. When the drain voltage of the transistor reaches V_{drain}, the drain-source current through the transistor decreases significantly until the gate-source voltage crosses the threshold voltage of the transistor.

It is worth mentioning that the switching speed depends not only on the switch transistor but also on the driver. Nonetheless, the loop impedance comes into play very quickly as the switching speed increases. Packaging, decoupling and PCB impedance are of some importance. As a general guideline, we will try to minimize the parasitic inductances between the switch and its driver and optimize the decoupling of the driver supply voltage. Power modules including a pair of transistors and their associated drivers are commercially available. These modules minimize the parasitic elements by a tight integration of a different element in a single package as well as the integration of active elements on a single silicon die, or the use of an integrated power converter.

Equation 1.12 outlines the role of the driver supply voltage in the switching losses and assumes a 100% efficient driver supply. This is the case when the driver is supplied directly by the input power source, for instance. However, this is not the case when the maximum gate-source voltage is lower than the input voltage, or in a boost case or when a linear regulator supplies the driver. We need to emphasize the switching losses of the device related to the driver

voltage with a proper driver efficiency for such a case. For instance, using an ideal linear regulator to supply the driver with a voltage V_{drv} from the power input of the driver whose voltage is V_{drain}, we obtain:

$$P_{sw} = 0.5\big(C_{gs}V_{drv}^2\frac{V_{drain}}{V_{drv}} + C_{gd}(V_{drv} + V_{drain})V_{drain} + C_{ds}V_{drain}^2\big)f_{sw} \quad [1.14]$$

1.3.2. *Extracting the parasitic capacitance values using simulations*

Parasitic capacitances of the transistor play a key role in the overall efficiency of the converter. However, these elements are often partially documented or not documented at all. As the capacitance values are voltage-dependent, equivalent values are extracted following the charge equation of an ideal capacitor:

$$C_i = \frac{Q_i}{V_i} \quad [1.15]$$

where Q_i is the amount of charge needed to charge the capacitor at the voltage V_i. Schematic representations of the extraction of the parasitic elements for an N-MOSFET are shown in Figure 1.14. This method requires accurate models for the parasitic capacitances of the transistor. The scheme shown in Figure 1.12 (top) is used to extract the output capacitance C_{oss} that combines the drain-to-source and part of the gate-to-drain capacitances. A voltage source increases the drain-source voltage of the transistor from 0 V up to the drain voltage of operation. Integrating the current delivered by the voltage source gives the amount of charge stored in the equivalent capacitors. Figure 1.12 (bottom) shows the extraction of the input capacitance of the transistor C_{iss}. This capacitance is a compound of the gate-to-source, gate-to-bulk and gate-to-drain capacitance. Again, integrating the current delivered by the voltage source gives the amount of charge stored in the equivalent capacitors. It is worth mentioning that the amount of charge needed to invert the voltage across the gate-drain parasitic capacitor, C_{gs}, depends on the drain voltage. Therefore, the equivalent capacitance seen by the driver increases when the off-state drain voltage of the transistor increases.

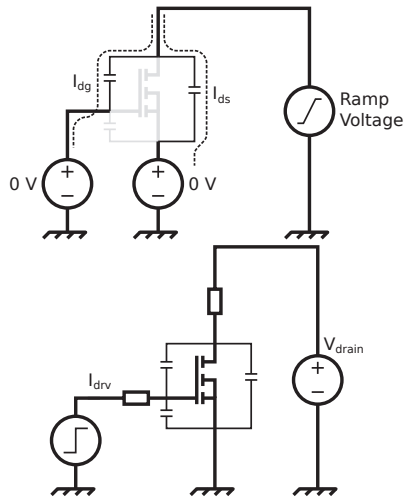

Figure 1.14. *Simulation setup for the extraction of the parasitic capacitances*

1.3.3. *Power-stage design issues*

The usual process to optimize a power stage is to select a switching frequency and an inductor, use a transistor or design a transistor so that its losses are shared equally between the switching losses and the conduction losses, and repeat this process for each transistor in the circuit and design the best possible drivers. This simplistic way of describing the process hides the reality of a much more iterative and nonlinear process. This section discusses how these few design choices interact together and with the requirements.

The inductor of the converter is a critical component that often defines a significant portion of the solution cost, volume and performances. Its choice results from a multivariable trade-off. We can define the, "Current ripple ratio", r, as:

$$r = \frac{I_{pkpk}}{I_{av}} \qquad [1.16]$$

where I_{av} and I_{pkpk} are the average current and the peak-to-peak current through the inductor, respectively. As a rule of thumb, a current ripple ratio

close to $0.3 \approx 0.4$ ends up being a good trade-off for most applications. This statement can be used to discuss three features:

– What is the best average current to take into account? Is it at peak output current or at typical output current? The answer to this question leads to the specification of the load current profile. On the one hand, extreme current peaks that occur rarely probably need not be optimized. On the other hand, if the average load current is 10 times less than the maximum output current, a good trade-off is certainly in between the average and the peak value.

– The peak-to-peak current depends not only on the inductor value but also on the switching frequency, which is still not firmly defined. The higher the switching frequency, the smaller the size and value of the inductor. High switching frequencies tend to increase the power density of the converter. However, switching losses can become a significant dissipation factor as the switched voltages are defined by the application, and the parasitic capacitors of the devices cannot be decreased without an increase in the R_{dson} of the devices.

– The ripple factor remains a rule of thumb and there are good reasons to avoid its use. For instance, some low-noise applications tend to require less current ripple even if self-resonance frequencies and skin effects through the inductor can create switching frequency-dependent problems in the noise spectrum. The higher the inductance, the lower the current slew rate delivered by the converter. The best-in-class transient response converters tend to keep the inductance value low in order to maintain di/dt as high as possible. For instance in [LAB 13], the falling load current slew rate at the on-board converter output reaches values up to 6.55×10^6 A.s^{-1}, while the current slew rate through the inductor can be up to 2.5 times lower (2.55×10^6 A.s^{-1}). Even an ideal transient controller would require a minimum amount of decoupling capacitor to absorb the residual energy that is left in the inductor. Otherwise the excess of residual energy could lead to exceeding the maximum load voltage.

Generally, finding an optimum solution requires several iterations. A good starting point is to use as much space as possible given the project constraints. This allows low switching frequencies and low switching losses. Conduction losses for the inductor can be maintained under control, thanks to a large inductor package and a high value inductor. Transient performances will be discussed later, but adding decoupling output capacitors can mitigate the large inductance value and the poor current slew rate. However, non-mechanical

requirements can come into play. Among others, start time of a variation of the DC output voltage of the load for different operation points restricts the amount of decoupling capacitor that can be used. This is the case for the average power tracking for a radio-frequency power amplifier. Between each plateau, the converter must charge and discharge the output decoupling capacitors as fast as required by the application.

The input power source of an Internet of things (IoT) device is likely to vary as well as the output voltage of the converter. The former varies because of the discharge of the battery and the latter varies because of the various power states of the load. A good knowledge of the load distribution helps us to find the best optimization point where switching losses of the devices equal conduction losses. We may choose two slightly different points for the switch and the rectifier of the converter in order to flatten the efficiency curve. A trial and error method and a good understanding of the loss mechanism often give satisfying results.

1.3.4. *Segmented power stage and multiphase operation*

For highly variable operation conditions, a single set of transistors may not be sufficient to keep the efficiency high. A technique is to connect several transistors in parallel and to switch only some of them when the current is low, as shown in Figure 1.15. For instance, two transistors can be connected in parallel with each independent driver. At high output current, both transistors are switched. The switching losses are the sum of the two transistor switching losses and the overall on-resistance is equivalent to the two R_{dson} in parallel. At low output current, only one transistor is switched while the other is turned off. The R_{dson} of the active transistor generates the conduction losses. The switching transistor generates switching losses as well as the output capacitance, C_{oss}, of the passive switch that is charged and discharged at the switching rate. Hence, the efficiency is degraded with respect to a single device at low current, but at high current, the efficiency is higher than that of a single transistor. Fine-grain automatic tuning of the sizing of the switches is presented in [MIC 14]. Despite a notable improvement at medium current, only a reduced number of segments are sufficient to extend the efficiency of the converter. Therefore, most commercial integrated products offer only a few segments.

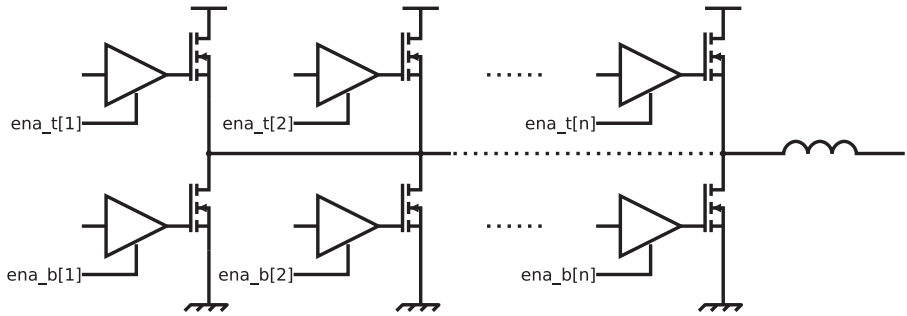

Figure 1.15. *Operation principle of a segmented power-stage*

We can take the segmentation principle further and use several inductors, as shown in Figure 1.16. Each pair of switches and inductors is called the phase, hence the name of the multiphase converter. At low output current, a single phase is used and the other ones are turned to high impedance mode. When the load current increases, the number of active phases also increases, maintaining each phase close to its optimum efficiency point. This concept can be used with two phases or with a large number of phases. It is worth mentioning that the current through each phase must be balanced. This requires an active current-balancing control circuit and some sort of current sensing through each phase.

1.3.5. *LC filter design space*

As explained above, the design and optimization of power converters is very complex since there are tight connections between dynamic and static specifications, LC filter design, switching frequency, number of phases, MOSFET design, inductor design and capacitor design. The LC filter design space provides physical insight, decoupling the design process in two steps:

1) LC filter design to meet dynamic and static specifications: determination of the constraints for the filter to meet tracking time and tight regulation under load current changes. Other requirements such as tracking energy and size of output capacitors and inductors can be considered at this point. Identification of the control speed constraints is done. The control speed of the converter limits the minimum output capacitance and hence the minimum tracking energy. If linear control is considered, the design process must account for the minimum switching frequency that the system bandwidth requires. However, if nonlinear

control is considered, it is possible to decouple the switching frequency and the dynamic response, thus making minimum output capacitance designs feasible at low switching frequency.

2) Power stage optimization: when the degrees of freedom are obtained in terms of dynamic response and control, in this step, the design of the power stage, the selection of the switching frequency, the number of phases, MOSFETs, inductances and output capacitors is done to achieve the efficiency and size requirements.

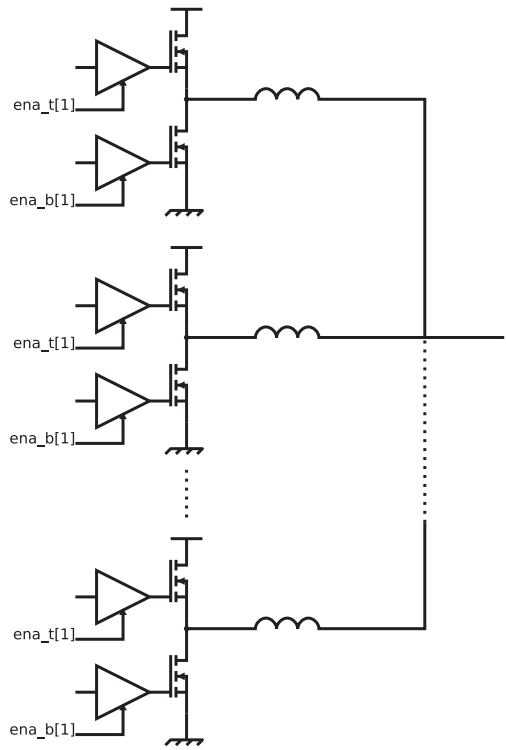

Figure 1.16. *Operation principle of a multi-phase power stage*

The key of this methodology is based on the one-phase equivalent concept (Figure 1.17). The one-phase equivalent has the same total silicon area for the MOSFETs than a generic N-phase solution. In the first case, the channel area per switch is N times higher than in the N phase solution to keep the same

losses and the same size. The equivalent inductance L_{eq} of the one-phase equivalent is designed to have the same maximum current slew rate as a generic N-phase solution, $L_{eq} = L_{phase}/N$; therefore, both power stage solutions present the same maximum dynamic response.

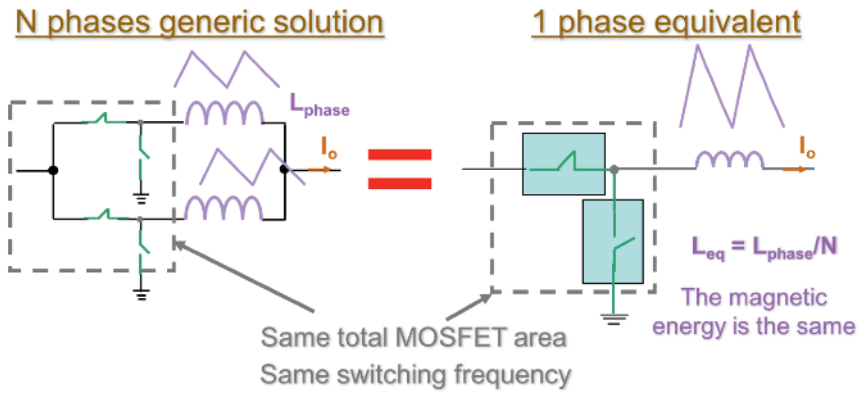

Figure 1.17. *One-phase equivalent: same behavior as N phases, same dynamic response, same efficiency and same size. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

The LC design space guarantees that the one-phase equivalent solution meets the dynamic and static specifications. Once the LC filter of the one-phase equivalent is selected, the design effort is focused on the power stage optimization: switching frequency, number of phases, MOSFET design, inductor design and capacitor design.

The LC design space is explained by means of a design example. The design specifications are:

– 5 V input voltage, 20 A load current;

– output voltage range from 1 V to 2 V and 2 λs tracking time;

– the tolerance band for dynamic regulation under current steps (20 A, 1000 A/λs) is 200 mV. The minimum output voltage at which the load step can occur is 1.5 V. The output voltage ripple should be less than 20 mV. The data refer to the values at the processor pins.

Figure 1.18 shows the LC design space to meet the dynamic specifications. The shaded area represents the design space that meets the dynamic specifications. The red border line is given by the voltage tracking time when the minimum time control law is applied. The blue border line corresponds to the load steps when the minimum time control law is again applied. The green border line corresponds to the maximum output capacitance that can be given by the maximum allowed tracking energy or by the bandwidth; if a linear control is used, the higher the bandwidth, the lower the output capacitance. All the LC values inside these borders (shaded area) meet the dynamic specifications. All the equations and details to determine these border lines are given in [SOT 05]

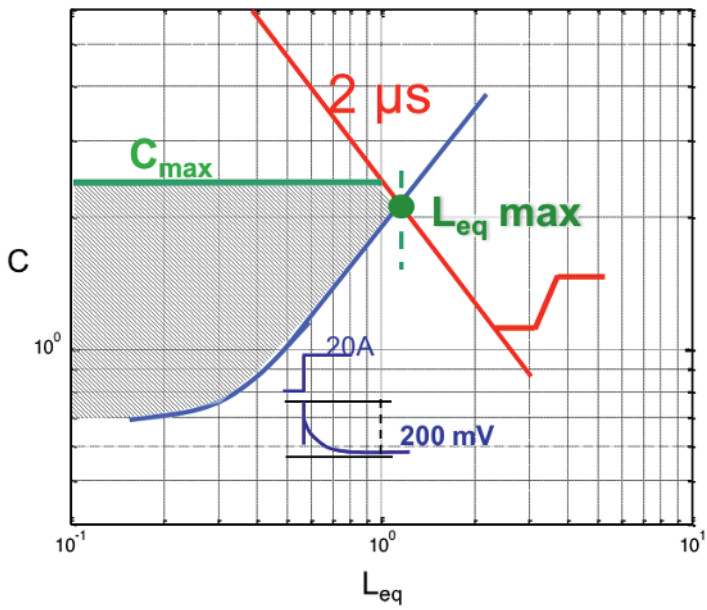

Figure 1.18. *LC design space to meet dynamic specifications: load steps, dynamic voltage scaling, energy tracking and bandwidth. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

The next step is to consider the output voltage ripple at high frequency. It defines an additional LC design space. Figure 1.19 shows the LC design space to meet the ripple specification, and the shaded area on the upper part

corresponds to high values of L and C. The higher the switching frequency, the lower the required values for the inductance and the capacitance. Figure 1.20 shows both LC design spaces, corresponding to the dynamic and the static specifications. To achieve a LC design space that meets dynamic and static specifications, both shaded areas must overlap to have some common solutions. With a one-phase converter, the only way to find a solution is to increase the switching frequency. For the considered specifications, a one-phase converter would switch at 8 MHz to meet all the specifications.

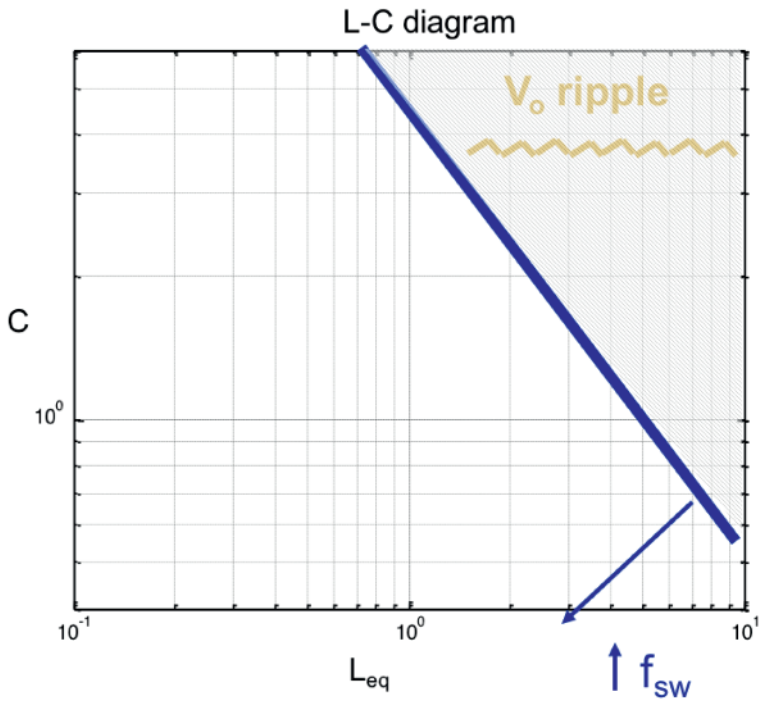

Figure 1.19. *LC design space to meet static specifications (output voltage ripple)*

However, the LC design space is valid not only for the one-phase equivalent but also for a generic N-phase solution. Therefore, a degree of freedom comes into play to optimize the design of the power topology, and the overlapping of the design spaces can be achieved either by increasing the switching frequency or by increasing the number of phases (Figure 1.21). For

the considered specifications, a four-interleaved phase converter switching at 500kHz meets all the specifications (Figure 1.22). Only a one-phase converter running at 500 kHz presents a 300 mV ripple, a value much larger than the specified one (20 mV); however, by interleaving four phases, the ripple cancellation among phases allows us to meet the ripple specifications [SOT 05].

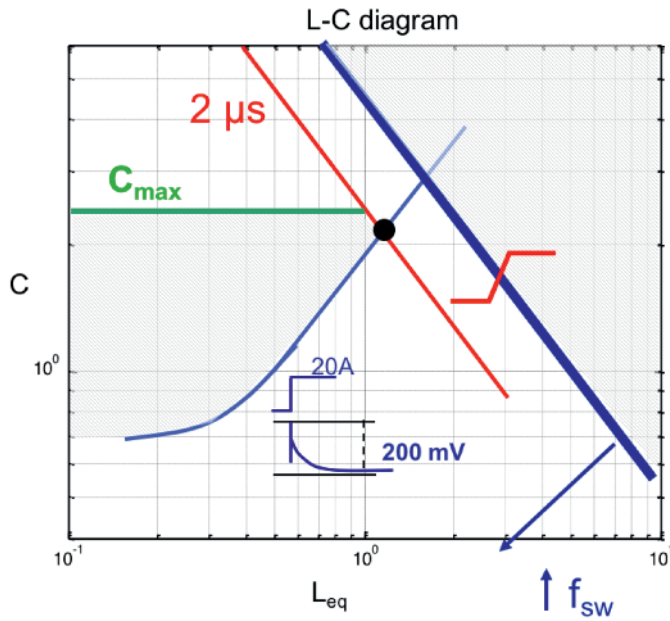

Figure 1.20. *LC design space to meet dynamic specifications (load steps, dynamic voltage scaling, energy tracking and bandwidth) and static specifications (output voltage ripple): increasing switching frequency to match both design spaces. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

In summary, the LC design space allows us to decouple the selection of the LC filter to meet the dynamic and static specifications from the power stage optimization. In the second stage of the design process, power stage design, switching frequency, number of phases, MOSFET design, capacitor design and inductor design are completed. A CAD tool could really help to optimize this complex design.

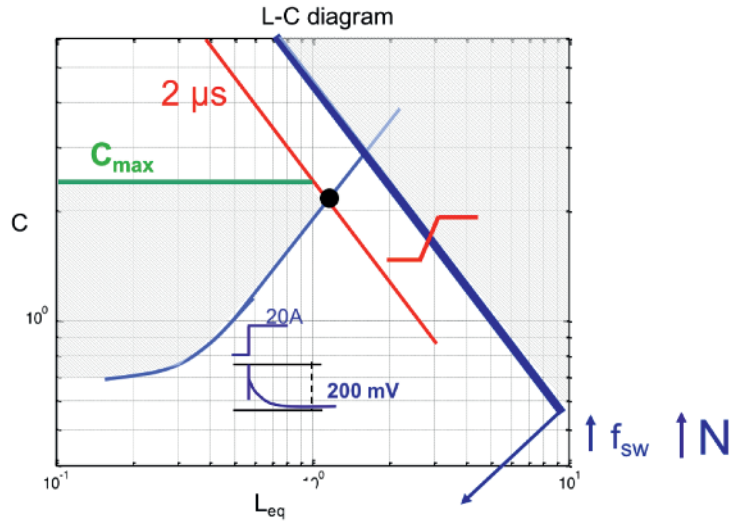

Figure 1.21. *LC design space to meet dynamic specifications (load steps, dynamic voltage scaling, energy tracking and bandwidth) and static specifications (output voltage ripple): increasing switching frequency or number of phases to match both design spaces. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

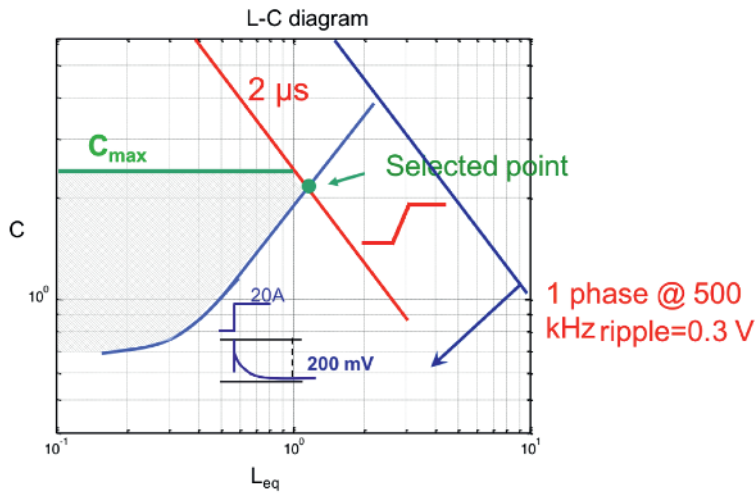

Figure 1.22. *LC design space: an example. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

1.4. Control stage

Numerous control strategies coexist to control the power stage. However, they are mainly derivatives of a few ones. First of all, the voltage-mode pulse width modulation (PWM), voltage mode control (VMC), is one of the most commonly used strategy. The current-mode control strategy is derived from the voltage-mode PWM strategy by the addition of an inner current loop. The control of two variables (the inductor current and the output voltage) provides additional advantages like load balance among converters operating in parallel, operation under overload or short-circuited conditions. From the perspective of dynamic response, current-mode control presents better line transient performance (audio susceptibility); however, under load steps, it presents worst performance since the output impedance is higher than the corresponding VMC. Since voltage-mode and current-mode PWM control use a clock-synchronized modulation, they are referred to as "hard-synchronized" methods, i.e. each cycle is synchronized with the reference clock. On the contrary, strategies where a conduction cycle can start out of phase with respect to a reference clock are considered as "soft-synchronized".

1.4.1. *Voltage-mode control of the buck converter*

A general PWM scheme of the voltage-mode control is shown in Figure 1.23. The control part is built around a PWM modulator whose input is a linear compensation function. The output of the modulation (duty cycle) is directly fed to the power stage.

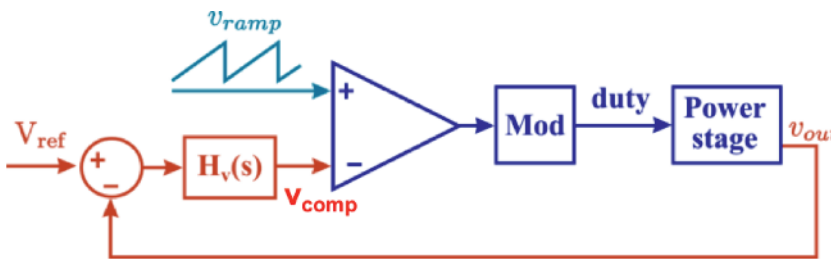

Figure 1.23. *General scheme of a voltage-mode PWM control. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

1.4.1.1. *Closing the loop of the voltage-mode-controlled buck converter*

A model of the converter has to be defined in order to determine the linear compensation function. The simplest methodology is the small-signal AC characterization associated with phase-margin and gain-margin criteria [ERI 01]. Although it is widely used in conventional design, some limitations have been outlined in [TRO 05]. However, this methodology offers a good first step and provides sufficiently accurate results to properly model the converter behaviors.

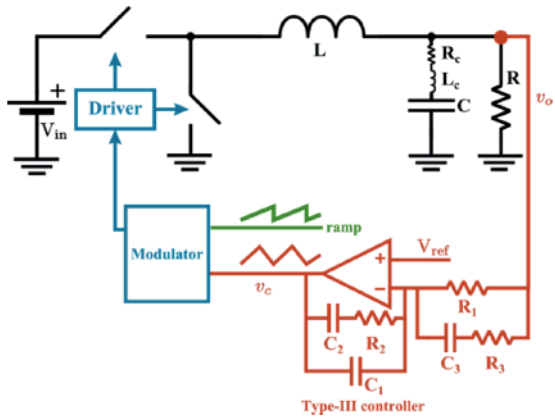

Figure 1.24. *Voltage-mode PWM control of a buck converter with type III regulator*

The scheme of buck converter with voltage mode PWM control is shown in Figure 1.24. PWM modulator signals are shown in Figure 1.25. The input signal is compared with a sawtooth and the output signal has a duty cycle proportional to the input signal. The higher the input signal, the wider the output pulse. A small change in the compensation voltage, v_{comp}, induces a small change in the duty cycle, d, as shown in Figure 1.26. The PWM modulator and the power switches can be modeled as a single gain.

$$G_{pwm} = \frac{V_{in}}{V_H} \qquad [1.17]$$

where V_H is the height of the modulation ramp. Using feedforward action on the power input voltage, the sawtooth height V_H can be adjusted to V_{in}. In doing so, the PWM modulator and power switches become a unitary gain.

This technique is commonly used to reduce the line-to-output sensitivity and simplifies the compensation function design. Assuming the feedforward action on the PWM modulator rising slope so that $V_H = V_{in}$, the control to output transfer function of the buck converter becomes:

$$\frac{\hat{v}_{out}(s)}{\hat{v}_{comp}(s)} = \frac{1}{\frac{s^2}{\omega_0^2} + 2m\frac{s}{\omega_0} + 1} \qquad [1.18]$$

where m is the damping factor of the output filter, which is load-dependent, and ω_0 is the time constant of the LC filter. The linear compensation function provides key characteristics:

– A high DC gain to diminish the static output error. This gain is provided by an integration function;

– Two zeros to compensate the filter double pole;

– A wide small-signal bandwidth to provide satisfying transient performances.

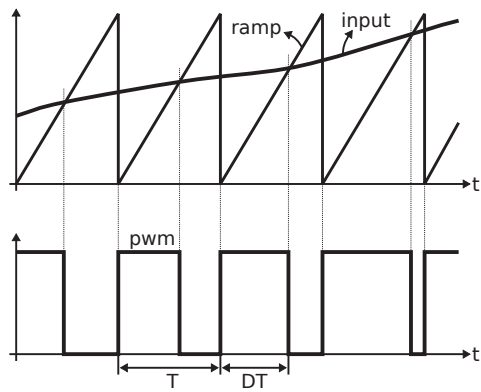

Figure 1.25. *Operation of a PWM modulator*

A type III provides these characteristics. A possible implementation is presented in 1.23. The two higher frequency poles are designed in order to set the cut-off frequency 5 to 10 times below the switching frequency. This widely

used trade-off is set in order to average the switching effects while maximizing the regulation speed. A common design method is to set:

– The two zeroes at the LC double pole;

– A high-frequency pole at the capacitor ESR zero;

– The other high-frequency pole at the switching frequency or higher;

– The integration constant in order to provide an open-loop bandwidth 5 to 10 times lower than the switching frequency.

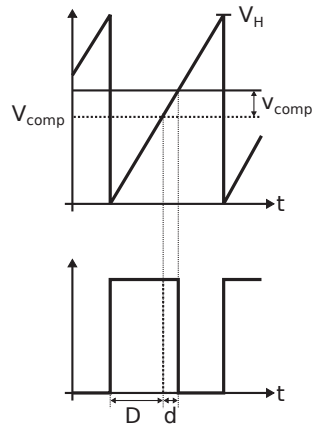

Figure 1.26. *Small signal modeling of a PWM modulator*

This methodology for stability suffers from approximations. First, the switching events of the power stage are nonlinear. The converter bandwidth has to be an order of magnitude below the switching frequency to ensure the validity of the stability criterion. Second, the stability analysis is valid for steady-state analysis only. It does not prevent large-scale instabilities that can result from a large output transient. Last but not least, it does not prevent period doubling or chaotic behaviors.

1.4.1.2. *Transient performances of the voltage-mode-controlled buck converter*

Load-transient performances of a converter can be studied in both the time domain and the frequency domain. Time-domain characterization consists of several measurements of overshoot and undershoots of the output voltage

when applying various load current steps. Using load transient profiles that represent the load behaviors, it can be determined whether the transient response of the converter is good enough to meet the specifications. However, the transient response of a highly optimized, fixed-frequency PWM converter varies depending on the phase of the converter when a transient occurs. This phenomenon is shown in Figure 1.27, where 554 load current steps are measured and plotted with persistence. If a load transient occurs at the beginning of the conduction cycle, the converter reacts as fast as allowed by the feedback loop. On the other hand, if a load transient occurs at the beginning of the second subcycle, i.e. when the switching node is tied to the ground, the converter waits for the beginning of the next conduction cycle to react. This behavior leads to a non-negligible variability in the load transient response and should be carefully checked during the design phase of the converter.

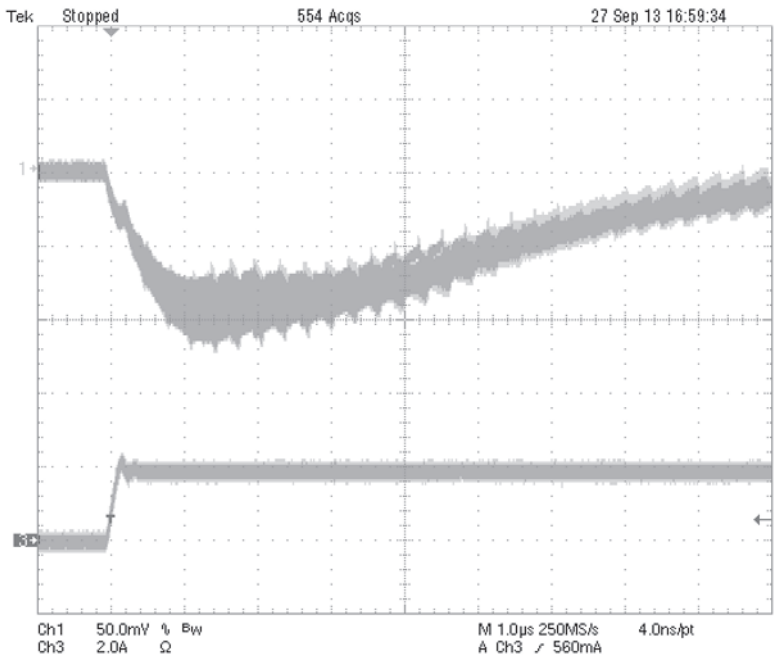

Figure 1.27. *Load step response of a general-purpose voltage-mode-controlled PWM converter, up: output voltage (AC coupled), down: load current*

Frequency-domain characterization is useful for simulating the converter behaviors while taking into account the power delivery network model (Power Delivery Network (PDN)). The latter can be extracted using 3D electromagnetic solvers, and unwanted resonances between the converter and the PDN can be avoided. The output impedance aims to characterize the converter behavior when a small and repetitive output transient occurs. A small change in the output current yields a small change in the output voltage. The resulting output impedance is defined as:

$$Z_o(s) = \left.\frac{\hat{v}_{out}(s)}{\hat{i}_o(s)}\right|_{\hat{v}_{ref}(s)=0, \hat{v}_{in}(s)=0} \quad [1.19]$$

Without control, the buck open-loop output impedance is simply the parallel combination of the passive output network [MAN 12]:

$$Z_{o_{OL}}(s) = R_o \parallel \frac{1}{C_o s} \parallel (R_l + Ls) \quad [1.20]$$

where R_o is the equivalent load impedance. The open-loop impedance exhibits a peak at the filter self-oscillation frequency that can degrade the load. A proper feedback control aims to divide the output impedance by its gain as:

$$Z_o(s) = \frac{Z_{o_{OL}}(s)}{1 + T_{comp}(s)} \quad [1.21]$$

where $T_{comp}(s)$ is the feedback transfer function. Thus, a high DC gain feedback is best suited to compensate the uncompensated DC drop caused by the power-stage parasitic elements. The amount of high-frequency gain, i.e. the compensation bandwidth, to apply to the feedback controller is more difficult to evaluate. The output impedance in the open loop ($Z_{out}(s)$) and in the closed loop ($Z_{CLout}(s)$) is shown in Figure 1.28. It clearly shows the effect of closing the loop; the closed-loop output impedance is much lower than the open-loop output impedance up to the bandwidth. In this case, the bandwidth is 700 kHz for a 5 MHz switching buck converter.

We can consider that increasing the controller bandwidth even within the switching frequency limit is sufficient to diminish the output impedance of the converter. This technique hits the linearization limits, i.e. the current though the inductor is slew rate limited, and quantification effects due to the

switching frequency create nonlinear behaviors. Simulation and experimental measurement of the output impedance can be performed using a controlled load that generates a sinusoidal load current at the measurement frequency. The output voltage and load currents spectrum are extracted using an FFT and the relative amplitudes are used to determine the output impedance at the frequency of interest. During the experiment, we must make sure that the system operates in the small-signal linear domain. This can be verified by checking the harmonic distortion of the current through the inductor. The latter increases rapidly when nonlinear effects come into play.

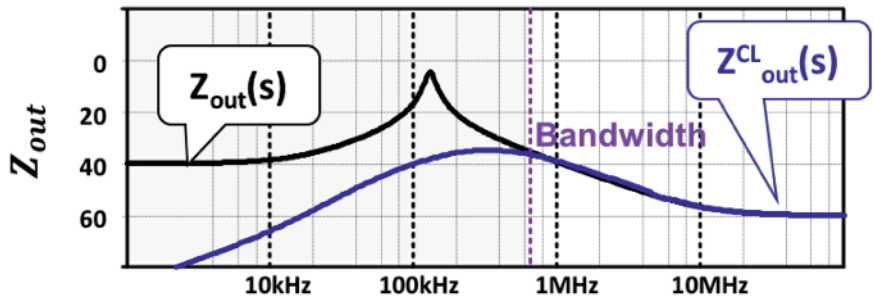

Figure 1.28. *Output impedance in the open loop and closed loop of a voltage-mode PWM buck converter with type III regulator. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

For a given power stage design, the voltage loop is responsible for the dynamic response of the converter. Figure 1.29 shows the response of a voltage-mode PWM buck converter under a fast load down step. The loop demands a very low duty cycle, v_{comp}, but it is lower than the minimum one, saturating the duty cycle and falling out of the small signal linear domain. It is called the large signal response of a converter, which must be taken into account for fast dynamic specifications.

1.4.2. *The RHP zero of the boost converter*

Several methods for determining a linear transfer function for a switched-mode converter have been proposed and discussed in the literature. Among them, the state-space averaging technique gives a consistent framework for the derivation of any transfer function of most common converters [RAS 10].

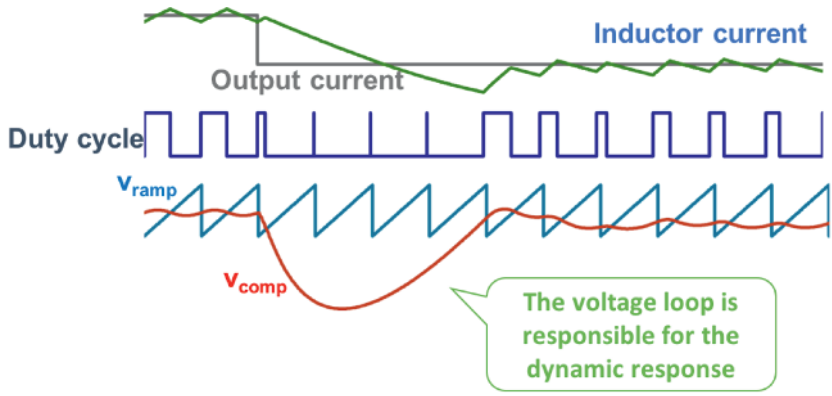

Figure 1.29. *Large signal response of a voltage-mode PWM control buck converter under a load down step. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

This modeling technique models the duty cycle to output the voltage transfer function, $\frac{\hat{v}_{out}}{\hat{d}}$, of a boost converter or a buck-boost converter in four-switch mode with a transfer function containing a positive zero, which is also called a right-half plane zero. For instance, the transfer function of a boost converter proposed in [ERI 01] is given by:

$$\frac{\hat{v}_{out}(s)}{\hat{d}(s)} = G_{d0}\frac{1-\frac{s}{\omega_z}}{1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2} \quad [1.22]$$

where

$$G_{d0} = V_{out}\frac{T_{on}+T_{off}}{T_{off}} \quad [1.23]$$

$$\omega_z = \left(\frac{T_{off}}{T_{on}+T_{off}}\right)^2 \frac{R_{load}}{L} \quad [1.24]$$

Both G_{d0} and ω_z are positive; therefore, the numerator of the transfer function contains the positive zero term. From a harmonic-domain perspective, the positive zero increases the gain of the transfer function but decreases the phase. The system becomes a non-minimum phase system and its closed-loop control is difficult.

From a time-domain perspective, this can be described as follows: when a load step occurs, the output voltage decreases. The inductor current must increase in order to compensate for this output voltage drop. However, increasing the inductor current means that the boost (or four-switch buck-boost) locally increases its on-time. During the on-time, the output voltage decreases as energy is not transferred to the output capacitor by the inductor. Therefore, to compensate for an output drop, the converter must allow the output voltage to decrease further in order to increase the average inductor current and to compensate for the drop later on. This non-intuitive control justifies the need for a current-mode control, i.e. detecting a change in the output voltage, the compensation function must control the inductor current to increase. The output capacitor converts this current change into a voltage change.

1.4.3. *Current-mode control*

The general scheme of the current-mode control (current-mode control (CMC)) of a converter is shown in Figure 1.30. An inner loop is used to regulate the inductor current, while an outer loop regulates the output voltage. The ripple of the inductor current modulates the duty cycle in the steady state (Figure 1.31).

A current-mode-controlled PWM buck regulator is shown in Figure 1.32. The current loop is a peak current-type loop, where the positive peak current of the inductor is regulated. On the contrary, valley current control regulates the negative peak current of the inductor. A peak current loop works as follows: when the clock cycle starts, the clock rising edge sets an RS-type or a D-type flop, with the switching node being tied to Vin, and the inductor current rises. An artificial slope is sometimes added to the measured current and compared with the loop input voltage, V_{comp}, to stabilize the converter when the duty cycle is greater than 50%. A larger control voltage implies a larger inductor peak current that results in a larger average inductor current.

The inductor current is regulated and the resulting current loop can be considered as a voltage-controlled current source. A simple approach is to model the inner loop as a voltage-to-current gain. This gain is only

determined by the current-sensing circuit gain. Then, the output filter is now a first-order system with a single pole formed by the output capacitor, which is much easier to stabilize. The current loop gain does not depend on the input voltage. Therefore, the line to output characteristic is improved with respect to that of the voltage mode control. The control of the inductor current removes the LC filter resonance, making the design of the voltage loop simpler. However, this simple model is only valid for very slow dynamic specifications. As explained below, within this chapter, more advanced models are required to maximize the dynamic response of the CMC, and are mandatory to include the current ripple information inside the model.

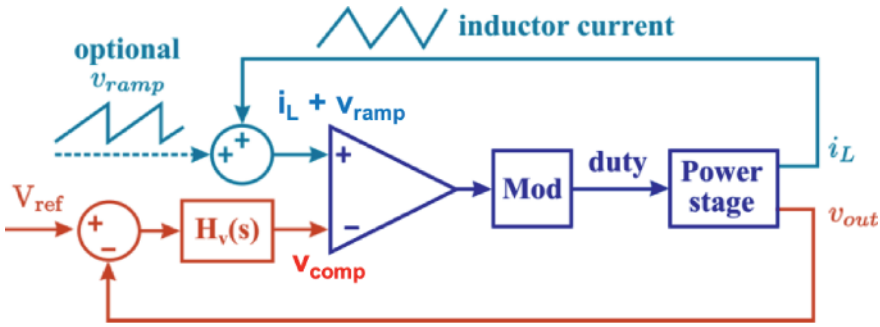

Figure 1.30. *General scheme of a current-mode control (CMC) of power converter. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

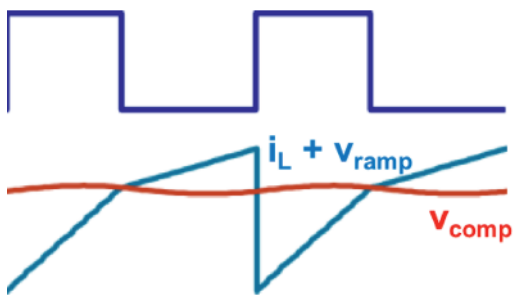

Figure 1.31. *Current-mode control (CMC): duty cycle modulation. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

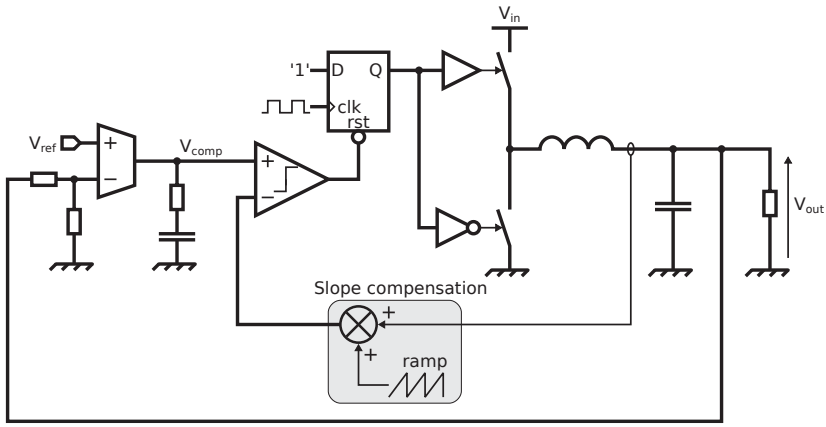

Figure 1.32. *Current-mode PWM converter: simplified diagram*

However, the peak current of the inductor does not reflect the average current through the inductor over a single cycle. A more accurate model of the current loop can be derived using a state-space averaging method or the similar approach proposed in [ERI 01]. It reintroduces a small line to output characteristic and a second pole to the control to output transfer function. Nevertheless, this second pole appears at high frequency and can usually be neglected, making the previous simplified assumption of a first-order current control to output transfer function valid.

Advanced models for peak current-mode control that take into account the subharmonic oscillations are reviewed in section 1.4.5.

Current-mode control alters the positive zero of the boost and the buck-boost converters so that it becomes negligible for most designs. The two-step approach for compensating a boost converter presented in the previous section is performed by design with an inner-current loop and an outer voltage loop. The voltage loop compensates for the output voltage changes while the current loop is in charge of controlling the required inductor current.

The main design issue when designing current-mode control is to sense the inductor current with a sufficient bandwidth and accuracy. This issue becomes even more difficult with the increase in the switching frequency and the output current dynamic. A common solution that preserves the converter efficiency is to sense the voltage drop across a switch. However, a high

current-low voltage power stage presents a low voltage drop that requires a high current sense gain and accuracy. Furthermore, a few MHz of switching frequency require a sensor of much wider bandwidth than the switching frequency that is difficult to obtain. On the other hand, current-mode control eases the design of the compensation function, that can become a type-II compensation function with a high-DC gain, a low-frequency pole and a single zero. The gain-bandwidth product requirements of the amplifier are simplified and even a transconductance amplifier can be used.

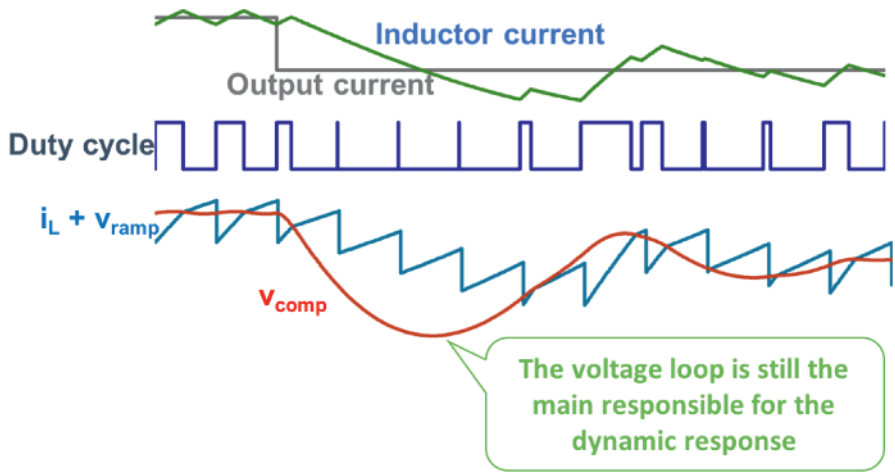

Figure 1.33. *Current-mode control (CMC): dynamic response under a load down step. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

The dynamic response of a buck converter with peak current mode (peak current-mode control (PCM)) control is shown in Figure 1.33. This figure clearly shows that the dynamic response of the converter still depends on the voltage loop rather than the current loop. The derivative of the current loop ($i_L + v_{ramp}$) is limited by the inductor current slope while the voltage loop (v_{comp}) is the variable that reacts faster to the load step.

1.4.4. *Hysteretic and sliding-mode control*

Limitations of linear-based control of a DC/DC converter make these solutions unsuitable for some high-performance mobile devices. The first

limitation is the difficulty in reducing the output filter of a voltage mode-controlled PWM converter. The second limitation is the lack of fast and power-friendly solutions for current sensing in a current-mode-controlled PWM converter. To circumvent the limitations of linear-based analysis and design of DC/DC controllers, the simplest approach is to start from the other side of control theories, i.e. from the nonlinear approach.

1.4.4.1. *Hysteretic current loop and current-mode hysteretic converter*

A hysteretic current-mode loop is shown in Figure 1.34. As presented in section 1.2, the current through the inductor of the converter rises when the switch is turned on and decreases when the switch is turned off and the rectifier is active. Hence, the current can be maintained within a known interval using a comparator with a hysteresis cycle. When the inductor current is lower than the low boundary of the hysteresis cycle, the comparator is high and the converter is in on-time. Figure 1.35 shows this operation mode. The inductor current rises until it reaches the high bound of the hysteresis cycle. Then, the comparator switches low, and the converter starts the off-time. The inductor current decreases during the off-time until it reaches the low bound of the hysteresis cycle. Then, the comparator switches and starts a new switching sequence. This operation principle guarantees that the inductor current tracks the control input (i.e. the hysteresis cycle) as long as the current can reach the upper and lower bounds of the hysteresis cycle.

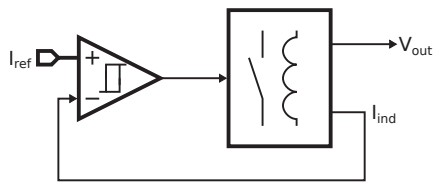

Figure 1.34. *Schematic of a hysteretic current loop. The power stage can be any of the three non-isolated converter presented in this chapter*

The hysteretic current-mode loop does not switch according to an externally provided reference clock. Its switching frequency depends on the ripple current and can be determined using the fundamental equations of the

converters presented in section 1.2. For instance, the on-time of a buck converter with hysteretic current-mode control is:

$$T_{on} = \frac{L}{V_{in} - V_{out}} \Delta I_L \qquad [1.25]$$

And the off-time is:

$$T_{off} = \frac{L}{V_{out}} \Delta I_L \qquad [1.26]$$

where ΔI_L is the width of the hysteresis cycle. Hence, the switching frequency of the hysteretic current-mode loop for the buck converter is:

$$f_{sw} = \frac{V_{out}\left(V_{in} - V_{out}\right)}{V_{in} L \Delta I_L} \qquad [1.27]$$

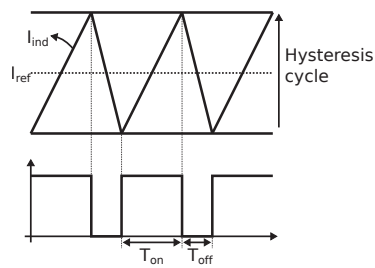

Figure 1.35. *Operation principle of a hysteretic current loop*

The switching frequency of the converter varies with respect to the input voltage, the output voltage and the width of the hysteresis cycle. We assume a fixed inductor value and neglect its variations so far. Variable switching frequency offers some benefits such as a simple control that does not require a slope compensation circuit, a nonlinear and fast transient response and its ability to reject high frequency phenomenon that are aliased by the sampling of a fixed-frequency modulation. This latter characteristic is useful in envelope tracking application, for instance. On the other hand, an uncontrolled switching frequency can be problematic. It makes the power-stage efficiency difficult to predict and optimize. Furthermore, the interferences generated by the converter are less predictable and more difficult to control. The application dictates its requirements, and when a wide

input voltage range, a wide output voltage range and a precise switching frequency are required, the hysteretic current-mode loop itself is certainly not the best candidate.

At high switching frequency, the hysteresis cycle becomes small and the propagation delays through the comparator and the power stage come into play. Turning the hysteresis cycle down to zero, the switching frequency becomes:

$$f_{sw} = \left[\frac{V_{in}}{V_{in} - V_{out}} T_{don} + \frac{V_{in}}{V_{out}} T_{doff} \right]^{-1} \quad [1.28]$$

where T_{don} and T_{doff} are the propagation delays. This is the so-called sliding-mode operation, as the current slides along the control surface as fast as possible.

So far, a nonlinear current loop that maintains the inductor current of the converter in the boundaries of a controlled value has been described. This current loop can then be used as an inner current loop for a current-mode-controlled converter. The design of the compensation function is similar to that of a peak current-mode control without the need for a slope compensation circuit.

1.4.4.2. *Current-mode sliding-mode converter*

This converter converges with the theoretical sliding-mode approach by the use of a sliding function that mixes the output voltage and the inductor current, as shown in Figure 1.36. This control structure is simply called the "hysteretic regulator" or the "hysteretic PWM regulator" [CAS 07, HAZ 05b, LI 11, RED 09] and is described as a way to increase the useful ripple. The added RC network integrates the voltage across the inductor and produces a scaled representation of the inductor current. Thus, "current-mode sliding-mode converter" or "hysteretic current-mode converter" are more explicit descriptions of this control scheme.

The AC part of the inductor current is equivalent to the output capacitor current since the output voltage is kept quasi-constant. Thus, another way to achieve the current-mode sliding-mode control is to measure or emulate the current through the output capacitor, C_o, as proposed in [HUE 13].

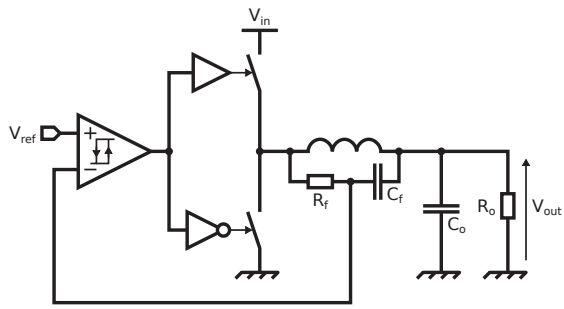

Figure 1.36. *Current-mode sliding-mode converter*

Considering the converter in Figure 1.36, the current-to-voltage transfer function of the current emulation circuit made up with R_f and C_f is [HUA 07]:

$$\frac{V_{C_f}(s)}{I_L(s)} = R_l \frac{1 + \frac{L}{R_L}s}{1 + R_f C_f s} = R_L \frac{1 + \tau_l s}{1 + \tau_c s} \qquad [1.29]$$

where R_L is the inductor equivalent series resistance, τ_l is the inductive branch time constant and τ_c is the capacitive branch time constant. This current measurement technique can be used in any current-mode control technique where the accuracy of the current measurement is not critical.

Once the sliding-mode existence condition is verified, the converter slides along a sliding surface S that can be expressed by making the comparator input error and input error dynamics equal to zero:

$$S(s) = V_{out}(s) + R_l \frac{1 + \tau_l s}{1 + \tau_c s} I_L(s) - V_{ref} = 0 \qquad [1.30]$$

When considering a single conduction cycle, the observer becomes a single gain K_{obs} (i.e. the slope gain) since the two time constants are larger than the switching period. Writing $i_L = I_L - I_o$, with i_l being the AC current component in the inductor, this assumption yields:

$$S(t) = V_{out}(t) + R_l I_o(t) + K_{obs} i_L(t) - V_{ref} = 0 \qquad [1.31]$$

Ideal sliding-mode operation implies that the converter switches with an infinite frequency; however, for the hysteretic current loop, the effective switching frequency is limited by delays in the control loop.

Neglecting the ripple in the inductor and averaging the converter behavior gives a simple model:

$$\overline{V}_{ref}(t) = \overline{V}_{out}(t) + R_l \overline{I}_o(t) \quad [1.32]$$

where $\overline{X}$ is the average value of X.

It is obvious that the DC output impedance of the converter is non-negligible since the output voltage is load-dependent. A load-dependent drop is used to perform adaptive voltage positioning (AVP) as proposed in [CAS 07, LEE 09, MIY 14]. This method involves the reduction of the output voltage when the load current of a digital load increases. Voltage margin is not required to compensate for an output voltage undershoot when the load is operating at maximum current. Therefore, the output voltage of the converter can be reduced slightly without degradation of the performances of the digital circuit, and the power dissipation is slightly reduced.

1.4.5. *Ripple-based controls for fast dynamics*

Applications with highly demanding load steps and dynamic voltage scaling such as point-of-load converters and voltage regulator modules need very fast controls in order to comply with the dynamic requirement and still maintain an output capacitor as small as possible.

Ripple-based controls (Figure 1.37) are very appropriate to achieve a fast dynamic response. They are composed of a fast feedback path (FFB) and a slow feedback path (SFB). The FFB path is a rippled signal that provides information about the power stage, and it is responsible for the modulation of the duty cycle and the dynamic behavior of the control. The SFB path is an integrator designed to have a very low bandwidth, which is responsible for regulating the output voltage in the steady state. The peak current-mode control (Figure 1.30) is a ripple-based control, but the inductor current feedback cannot be considered a fast feedback since it is very limited by the maximum inductor current slope. However, if a feedforward of the output current is applied to the inductor current feedback, as shown in Figure 1.37, the corresponding loop becomes a fast feedback path. The duty cycle modulation in the steady state is defined by the inductor current ripple (Figure 1.38) as in the peak current-mode control. However, in

the case of the ripple-based controls, the dynamic response is also defined by the ripple signal (Figure 1.39) while the voltage loop signal (v_{comp}) is almost constant during the load step.

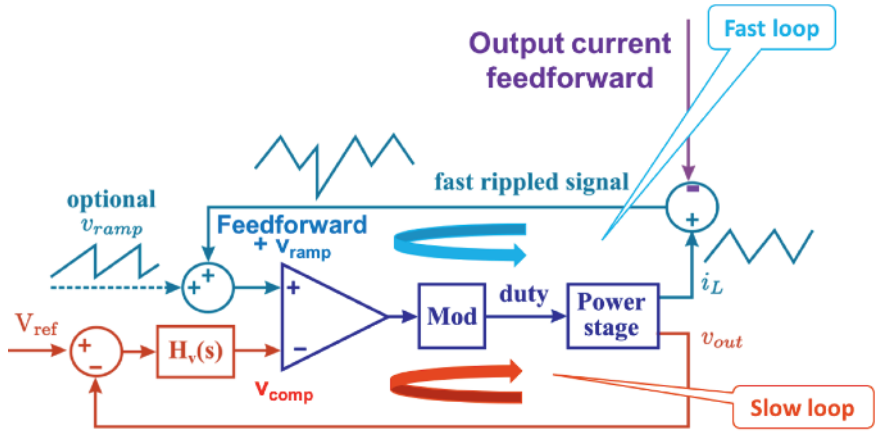

Figure 1.37. *Ripple-based control: general scheme dynamic. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

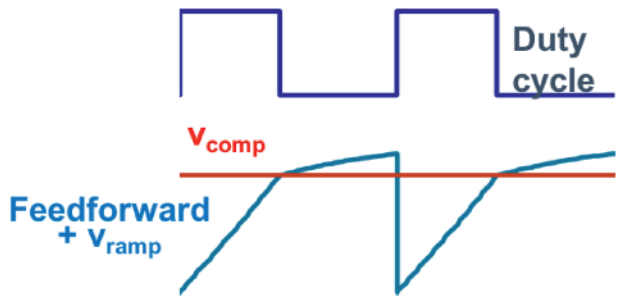

Figure 1.38. *Ripple-based control: duty cycle modulation. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

Analyzing the general scheme of the ripple-based control (Figure 1.37), it can be derived that the fast ripple signal, that is really fedback through the fast path, is the output capacitor current (Figure 1.40). This variable has all the needed information: 1) inductor current ripple for steady-state modulation and 2) feedforward of the output current for the load steps.

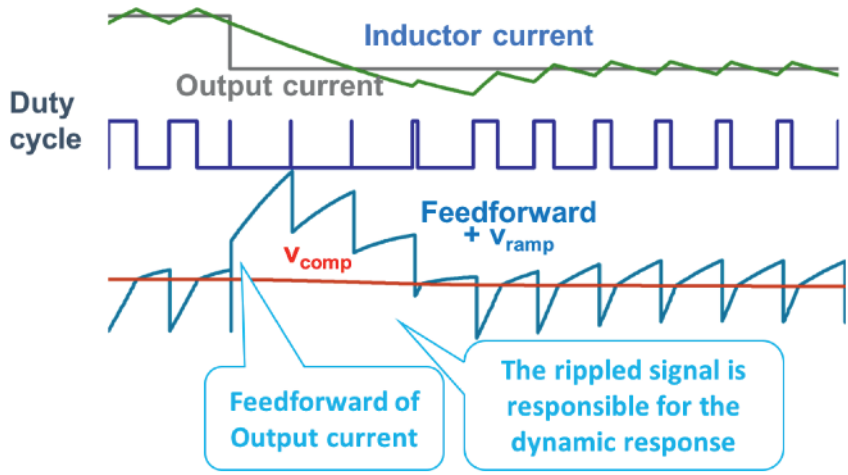

Figure 1.39. *Ripple-based control: response under a load down step*

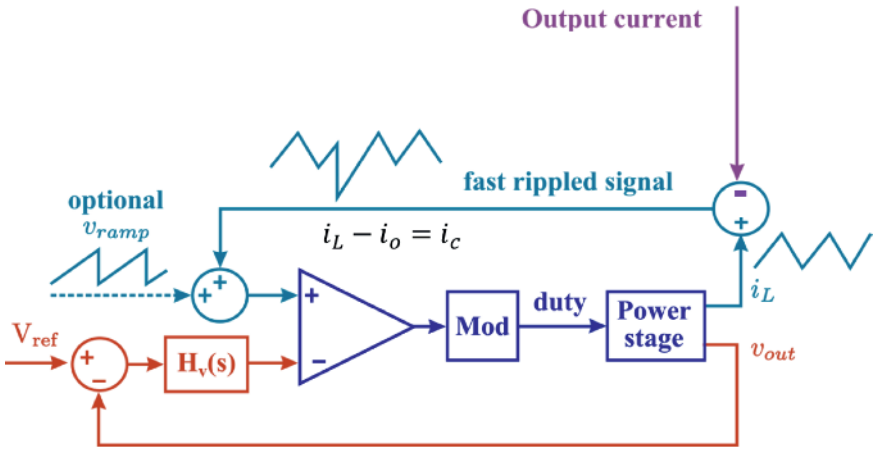

Figure 1.40. *Ripple-based control: output capacitor current feedback*

1.4.5.1. *V², quasi V² and V²I_C converters*

The V^2 control is the most popular ripple-based control (Figure 1.41) [GOD 96], [ON 09]. It uses the output voltage in an accurate and slow loop in parallel with a fast loop that uses the output voltage ripple. In the V^2 control, the rippled signal of the FFB path is the output voltage (Figure 1.41a). In the

case where the output capacitor has dominant equivalent series resistance (ESR), the output voltage ripple provides information about the capacitor current, which has the combined information of the inductor current and the output current. Consequently, the output voltage is shaped as the inductor current and can be used to modulate the duty cycle as in current-mode control, while exhibiting a fast dynamic response due to an inherent feedforward of the output current (Figure 1.41b).

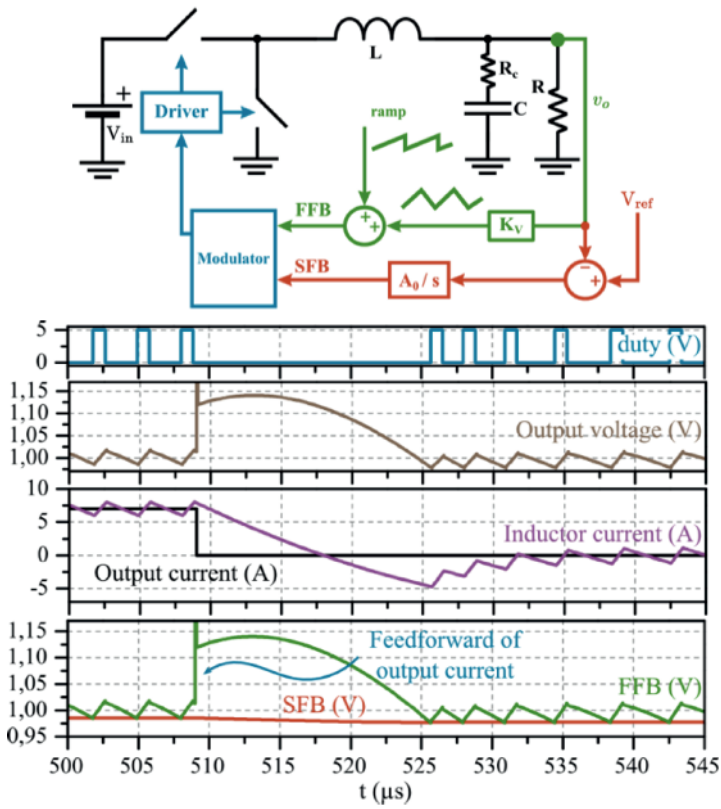

Figure 1.41. *V^2 control of a buck converter: (a) general scheme of a V^2 control on a buck converter; (b) load transient response for V^2 with constant on-time modulation. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

Note that the V^2 control only uses the output voltage but behaves like a current-mode control when the ESR of the output capacitor is large. For low ESR capacitors such as ceramic capacitors, the current information in the ripple of the output voltage is not dominant and, therefore, an additional current ripple has to be added to stabilize the converter. A popular way in the

industry is to add the inductor current directly to the rippled signal (Figure 1.42), usually sensed with an R-C network. Then, the FFB path is composed of the sum of the output voltage and the inductor current (Figure 1.42a). This control is called enhanced-V^2 control [HUA 01], which is also named V^2 control with current injection [TEX 11], called V^2I_L for simplicity. As the information of the load current is limited, when low ESR capacitors are used, this control does not provide an optimum response under load transients since ceramic capacitors (low ESR) do not provide a good feedforward of the load current (Figure 1.42b).

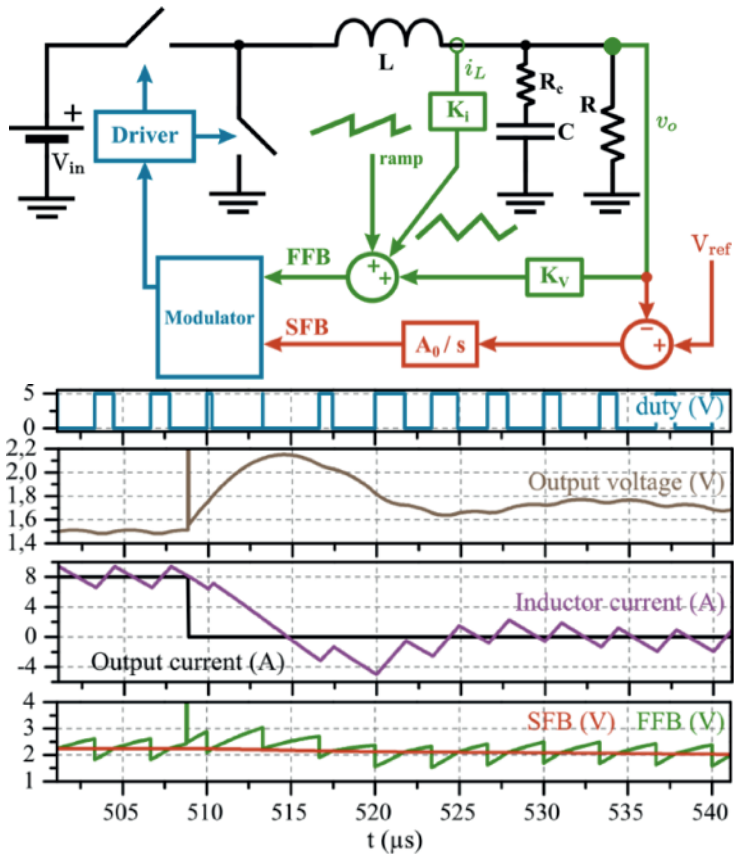

Figure 1.42. *IL control of a buck converter: (a) general scheme of a V^2I_L control of a buck converter; (b) load transient response for V^2I_L with constant frequency modulation. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

Instead of adding the inductor current, a better approach is to add the capacitor current (Figure 1.43). Then, the FFB path is composed of the sum of the output voltage and the capacitor current (Figure 1.43a). This control is named V^2I_C [VIE 11] and it was later proposed in [YAN 13] and [VOI 14] with different implementations but the same concept. As the capacitor current provides the control with information about the load current, V^2I_C reacts under load transient almost optimally even for low ESR capacitors [COR 14a] (Figure 1.43b). The dynamic response can be further improved by synchronizing the modulator with the load step [COR 15b].

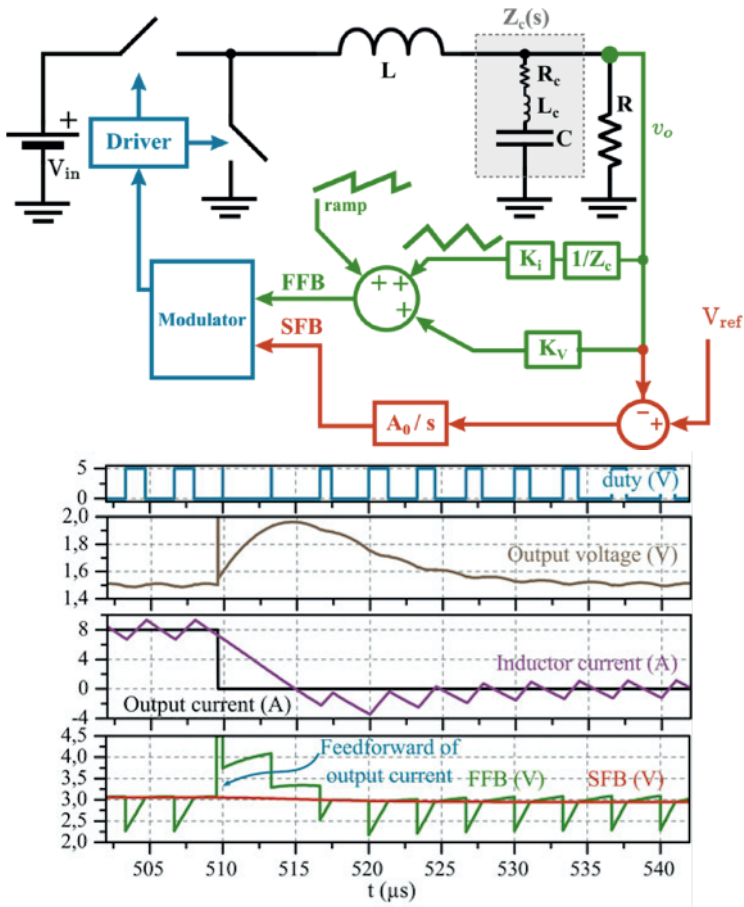

Figure 1.43. *V^2I_C control of a buck converter: (a) general scheme of a V^2I_C control of a buck converter; (b) load transient response for V^2I_C with constant frequency modulation. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

For the implementation of V^2I_C, the capacitor current can be estimated by sensing only the output voltage and designing a transimpedance amplifier with an impedance proportional to the impedance of the real output capacitor, including the ESR and the equivalent series inductance (ESL) [HUE 09a]. An alternative scheme of the implementation of V^2I_C is shown in Figure 1.44, where $K_i/Z_c(s)$ represents the sensor of the capacitor current. Note that, as with V^2 control with high-ESR capacitors, V^2I_C behaves like a current-mode control, but only senses the output voltage.

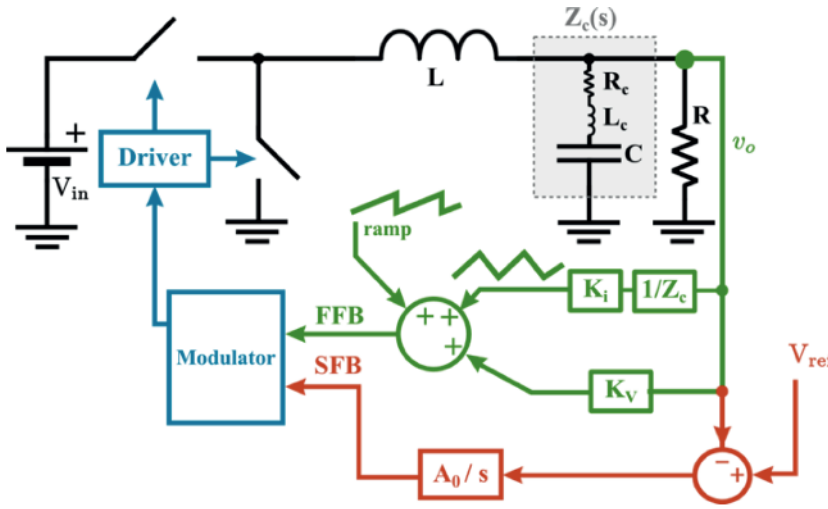

Figure 1.44. *V^2I_C scheme where capacitor current is estimated only by sensing the output voltage. This sensor of the capacitor current is explained in [HUE 09a]. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

V^2I_C control can be designed to provide an almost optimal response under load steps and under voltage reference steps for dynamic voltage scaling (DVS) applications or voltage tracking applications. Figure 1.45 shows the simulation results of design optimized for both dynamic specifications, load steps and voltage reference steps.

VMC, CMC, V^2, V^2I_L and V^2I_C are designed to be optimized for each control technique for the same specification and the same power stage. It is a 10 MHz buck converter, whose input voltage is 5V, output voltage is 1.2V and load steps range from 0 A up to 4 A and from 4 A down to 0 A. The

worst transient is the down step since the steady-state duty cycle is very small. Figure 1.46 shows the results obtained with each control technique under the down step. V^2I_C presents the best results, with the output voltage deviation of 25% over the nominal output voltage. VMC, V^2 and V^2I_L present a very similar response with 33% output voltage deviation while CMC presents the worst response with 41% voltage deviation.

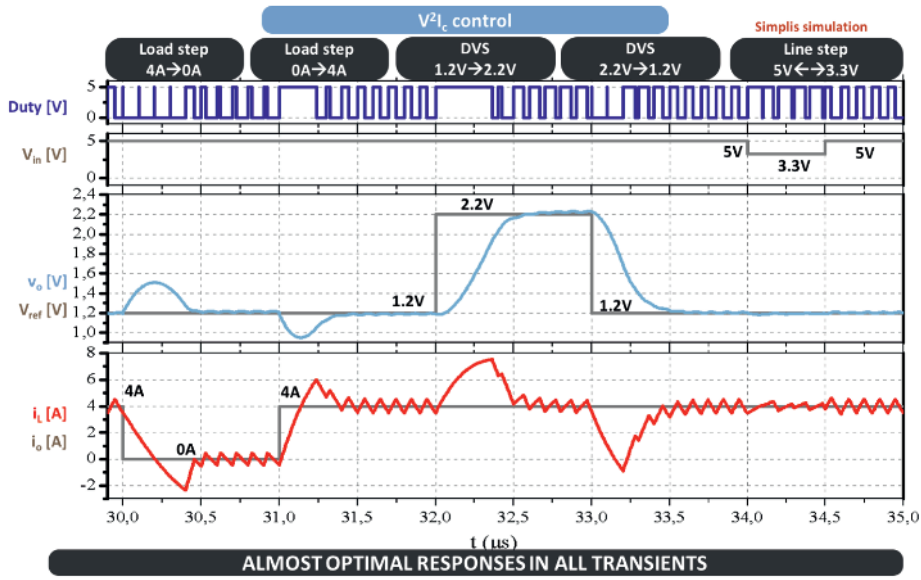

Figure 1.45. *V^2I_C simulations, designed optimized for both load steps and DVS. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

1.4.6. *V^1 concept: description and applicability*

Even if ripple-based controls only sense the output voltage (V^2 and V^2I_C), they are by nature current-mode controls. This is because the output voltage has inherent information of the capacitor current (from the ESR of the capacitor or by using a transimpedance amplifier). Also, the capacitor current itself has information from both the inductor current and the output current. This information about the output current is very important because it is what allows the V^2 and V^2I_C controls to behave almost time optimally under a load

transient. Additionally, the inductor current has information from the input voltage during the on-time. This concept of only sensing once the output voltage and using its inherent information about the power stage is called $\mathbf{V^1}$. Following the $\mathbf{V^1}$ concept, the question then arises whether a traditional voltage-mode control can be designed in a way so that this intrinsic information is exploited and, consequently, it behaves like a current-mode control with a very fast dynamic response. This voltage-mode control could be modulated, as ripple-based and current-mode controls, with constant-frequency (peak or valley), constant on-time, constant off-time or hysteretic modulations. Figure 1.43 shows the structure of the $\mathbf{V^2}I_C$ control where the capacitor current is sensed with a transimpedance amplifier with an impedance proportional to the impedance of the output capacitor and implemented in two paths, the SFB and the FFB path. Now, as an alternative equivalent representation, both the sensing of the capacitor current and the output voltage of the FFB path can be deducted from the output of the integrator (Figure 1.47).

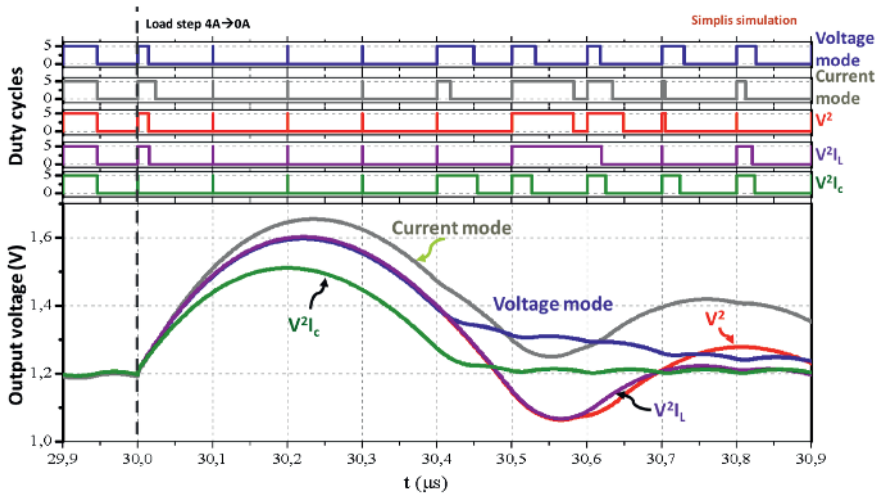

Figure 1.46. *Comparison of VMC, CMC, V^2, V^2I_L and V^2 IC. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

The equivalent regulator $H_t(s)$ is:

$$H_t(s) = \frac{A_0}{s} + K_v \qquad [1.33]$$

where $Z_C(s)$ is the output capacitor impedance [1.34], with C being the capacitance value, RC the series resistance of the capacitor (ESR) and LC the series inductance of the capacitor (ESL):

$$Z_C(s) = (1 + sCR_C) \cdot (1 + s\frac{L_s}{R_C}) \qquad [1.34]$$

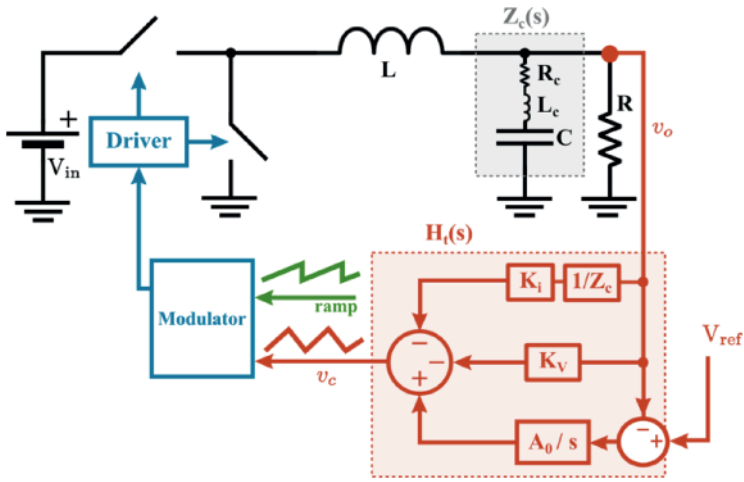

Figure 1.47. *Alternative representation of V^2I_C control. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

Figure 1.48 shows the Bode diagram of the controller $H_t(s)$. This regulator has an integral action, A0/s, which closely regulates the output voltage, a proportional action Kv, that provides a zero to the regulator, boosting the phase, and a weighted estimator of the capacitor current, $K_i/Z_C(s)$, that converts voltage information into current information. This current sensor is very important because it provides to the control a feedforward of the output current, needed to obtain a near time-optimal response under load transients.

In [COR 15d], it has been presented how this regulator can be designed with a classical type-III regulator of a VMC. It can be done for either low-Q capacitors or high-Q capacitors.

To obtain a voltage-mode control that behaves like a current mode with near time-optimal response under load transients, the regulator needs to mirror the impedance of the output capacitor at high frequencies. It is

important to state that a perfect matching of the impedance of the output capacitor is not possible in an actual product. Tolerances of the output capacitor due to aging, temperature and DC bias will have to be considered when designing the controller. Its effect on the stability can be studied and the control can be optimized by means of the procedure proposed in [COR 15c] and [COR 14b], respectively.

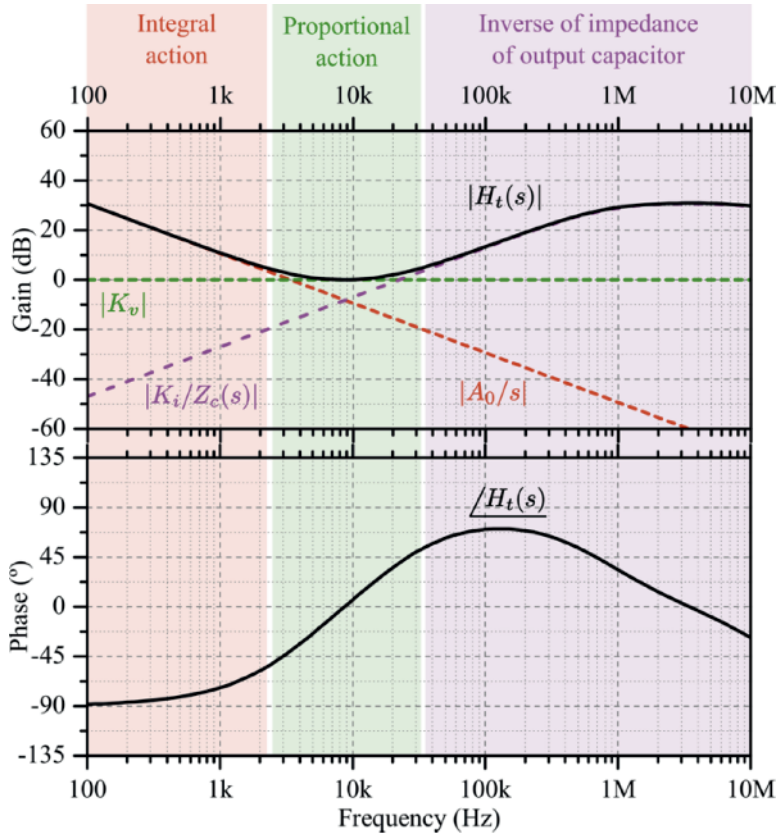

Figure 1.48. *Decomposition of the frequency response of the equivalent regulator of V^2I_C ($H_t(s)$). For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

The key of the V^1 concept states the fact that a V^2I_C control can be implemented using a VMC with type III regulator (Figure 1.49). The block diagram shown in Figure 1.49 is the same as a traditional VMC with a type III

regulator. The difference lies in the design of the regulator that must match equation [1.33]. Figure 1.50 shows two type III regulators; one designed as a traditional VMC and the other following the V^1 concept. The V^1 regulator follows the reverse of the output capacitor impedance at high frequencies, keeping the ripple information in the loop. On the contrary, a traditional VMC regulator filters the ripple information. Figure 1.51 shows the output of the regulator for both designs; the ripple information is kept in the loop in the case of the V1 regulator. Figure 1.52 shows the dynamic response of a VMC buck converter whose type III regulator is designed based on the V^1 concept to behave like the V^2I_C control; the response is almost identical to that shown in Figure 1.43, validating the V^1 concept.

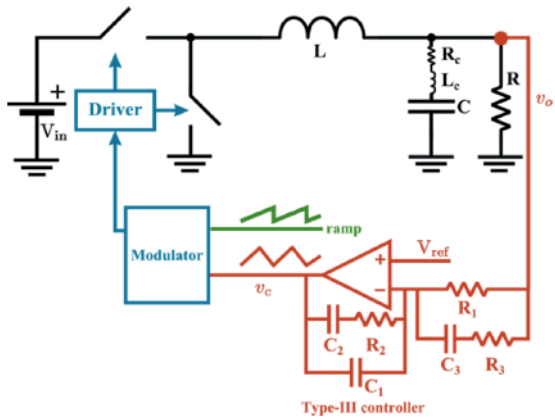

Figure 1.49. *V^1 concept: V^2I_C control implemented using a VMC with type III regulator. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

In summary, the V^1 regulator needs to behave as the inverse of the impedance of the output capacitor at high frequencies. In this way, the voltage information is converted to current information, and then the voltage loop has information about the capacitor current and therefore about the output current. This provides the control a kind of feedforward of the output current by only sensing the output voltage. As a result, the controller does not attenuate the side-band frequencies produced by the modulator. Thus, the control is prone to subharmonic oscillations as in ripple-based controllers.

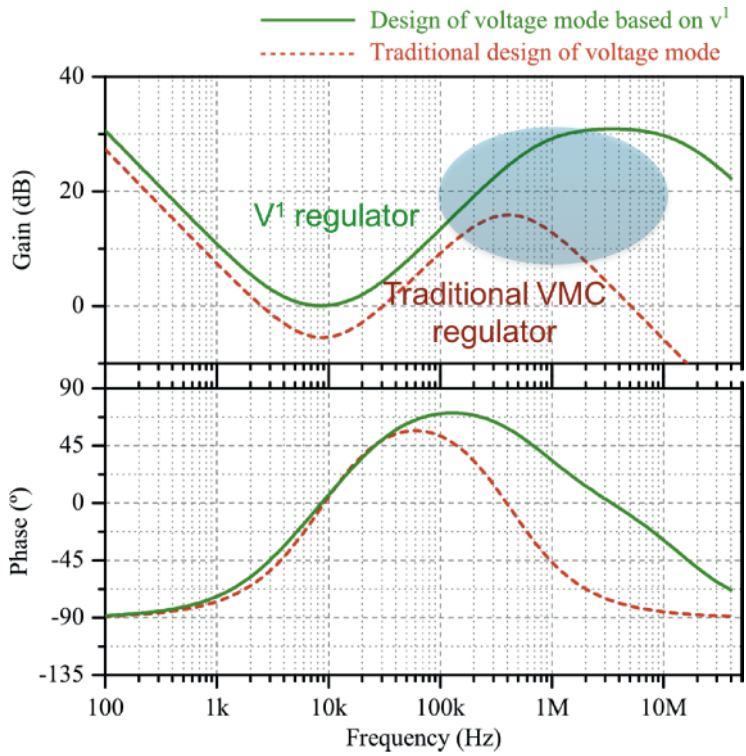

Figure 1.50. *V^1 concept regulator versus traditional VMC regulator design*

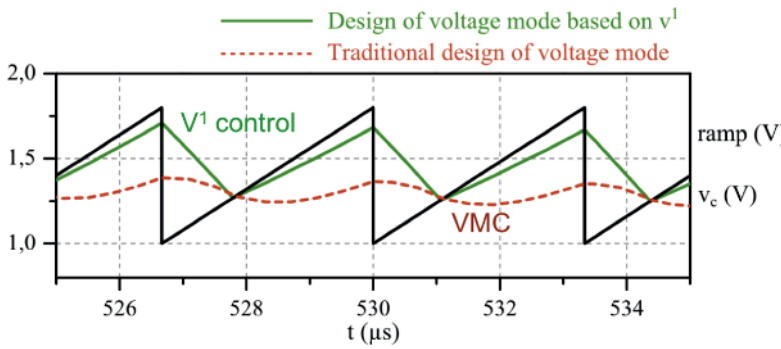

Figure 1.51. *V^1 concept: ripple information in the loop. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

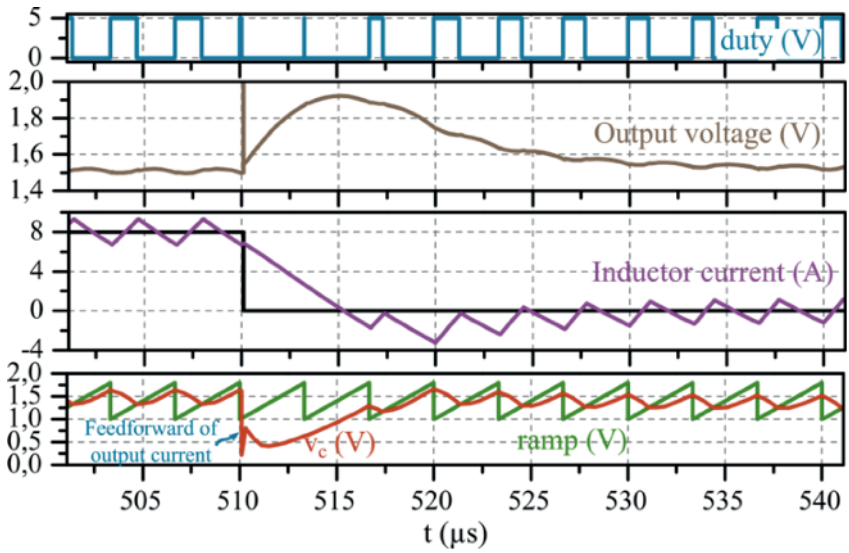

Figure 1.52. *V^1 concept: V^2I_C control implemented using a VMC with a type III regulator. Response under a load step. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

Therefore, a more accurate analysis is needed to account for tolerances of the parameters and mismatches of the current sensor. In [COR 15c], a methodology that takes into account all the above is proposed to evaluate the stability of converters based on discrete modeling and Floquet theory. Using these tools, an optimization algorithm that can design a very fast control can be developed, while assuring robustness under the whole operation region and accounting for tolerances of parameters and sensing networks [COR 14b]. Additionally, a commercial simulation program that can work with switched-mode power supplies and frequency responses is a good supplementary tool to design the $\mathbf{V^2}I_C$ control.

Given this information and methodology, low-cost, robust and very fast controls that only sense the output voltage can be designed and manufactured. As explained in [COR 15d], the $\mathbf{V^1}$ concept can also be applied to $\mathbf{V^2}$ and $\mathbf{V^2}I_C$; $\mathbf{V^2}$ can be designed as VMC, and $\mathbf{V^2}I_L$ can be designed as a current-mode control (Figure 1.1).

1.4.7. *Overview of the synchronization of asynchronous modulations*

1.4.7.1. *Hard synchronization paradigm*

The converter works in hard synchronization (HS) mode when each cycle is started by a reference clock. This synchronization paradigm does not allow asynchronous transient response but provides a better control of the generated EMI.

The first solution for phase synchronization in sliding-mode control is to use a RS or D-flop synchronization scheme to force each cycle as proposed in [RED 09]. The reference clock starts the cycle by setting the flop in a positive state and the pulse is generated until the sliding function is reached. When the comparator input reaches zero, the flop changes its state until the start of the next clock change. This operation mode is called the "fixed-frequency sliding-mode control" in [NI 09b] and "constant-frequency peak (or valley) voltage ripple regulator" in [RED 09]. Nevertheless, this synchronization scheme converts the sliding-mode controller into a current-mode-like control, with the drawback that a significant slope compensation or a complex system to switch between the peak and valley modes is required depending on the conversion ratio as proposed in [NI 09b]. Furthermore, the intrinsic sliding-mode asynchronous transient response is transformed into a current-mode synchronous transient response.

A hard synchronized converter is mandatory when the output noise and EMI have to be precisely controlled. When dealing with digital core power supply, things are very different. The output voltage has to be accurate and quickly modulated, but a particular spectrum of the supply voltage is not required.

In [RED 09], the sliding function is also modulated by a clock-synchronized ramp at the targeted switching frequency. The higher the sliding function modulation, the lower the sensitvity of the converter. If the sliding function is highly modulated, the transient has to have a high impact on the voltage error to produce a modulation variation; otherwise, the duty cycle will not be significantly changed and the perturbation will not be quickly rejected.

1.4.7.2. *Soft synchronization: compensated frequency control*

A constant on-time or a constant off-time (COT) configuration controls the converter in order to keep the advantage of asynchronous response. When the converter hits the sliding surface, the switch that is connected to the battery voltage is activated for a defined amount of time (on-time of the switch connected to the battery). The switch that is connected to the ground is also activated for a defined amount of time (off-time), respectively. The switching frequency is kept quasi-constant by adjusting the on or off-time using feedforward operation at both the input voltage and output voltage and eventually load current as in [HUA 11]. A feedforward action on the potentially controllable delays, T_{don} and T_{doff}, or hysteresis cycle, V_{hyst}, based on the measured voltage, can compensate the switching frequency variation since the input voltage and the output voltage are the most prominent external terms in the switching frequency expression:

$$f_s = \left[\frac{V_{in} V_{hyst}}{(V_{in} - V_{oout})\, V_{out}} R_f C_f + \frac{V_{in}}{V_{in} - V_{out}} T_{don} + \frac{V_{in}}{V_{out}} T_{doff} \right]^{-1} \quad [1.35]$$

AOT control is well suited when the converter operates as a stand-alone solution where clock synchronization is not required, thanks to a dedicated battery decoupling network. The switching frequency is kept quasi-constant in a controlled band and preserved from any unwanted drop in efficiency. The on-time control degrades the falling transient performances, but this can be improved by the use of a ramp pulse modulation (RPM) strategy as proposed in [RED 09]. Last but not least, the sliding-mode-based asynchronous response is preserved.

The drawback that makes a feedforward synchronization-based strategy unsuitable for integration in a complex environment is the lack of phase synchronization. Instantaneous or average switching phase synchronization of the converters combined in a large power management integrated circuit is mandatory to reduce the ripple current in the battery and avoid possible interactions between the different DC/DC converters that share the same power line.

1.4.7.3. *Soft synchronization: regulated frequency control*

A more precise frequency control of the switching frequency of a converter can be achieved by the regulation of the free-running switching frequency.

Frequency locked loop (FLL) synchronization schemes for a buck converter are proposed in [FEN 09, HUE 09b] and a principle schematic is shown in Figure 1.53. The natural switching frequency (f_{out}) of the converter is sensed and converted into a voltage by a frequency-to-voltage converter. The reference clock (f_{in}) is converted into a voltage, which is compared with the observed switching frequency. The resulting error is then amplified and filtered by a compensation function prior to being used as a frequency-control input of the free-running DC/DC converter. As a result, the whole DC/DC converter is used as a VCO in the frequency loop.

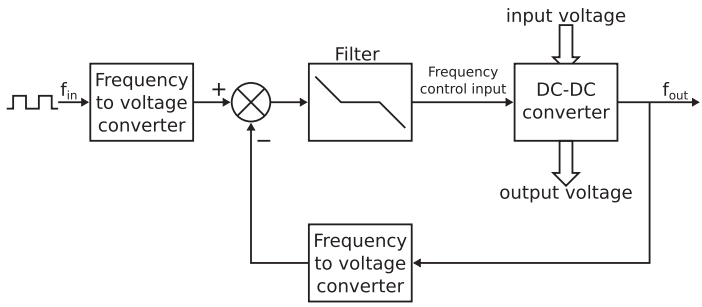

Figure 1.53. *Frequency locked-loop synchronization*

The frequency-to-voltage converters have to be properly matched to avoid unwanted offset in the frequency loop that generates a switching frequency error. The high DC gain provided by an arbitrary compensation function that stabilizes the frequency loop helps achieve no voltage error and therefore no frequency error. However, FLL synchronization still does not provide the phase synchronization effect. The converter behaves as an AOT control with a more accurate switching frequency, thanks to the feedback regulation.

The phase locked loop (PLL) synchronization operation principle is shown in Figure 1.54. The DC/DC converter operates as an oscillator in the frequency loop. The output phase is compared with the reference clock phase by a phase frequency detector (PFD). The PFD output is filtered and used to control the oscillator frequency. In [LU 14], the PLL synchronization is used in a multioutput converter.

A negligible phase error indicates a negligible frequency error between the desired switching frequency, f_{ref}, and the effective switching frequency, f_{sw}. Obviously, no phase error indicates that the switching cycles start

synchronously in the steady-state operation. This ensures a good overall phase control while transient operation can start asynchronously.

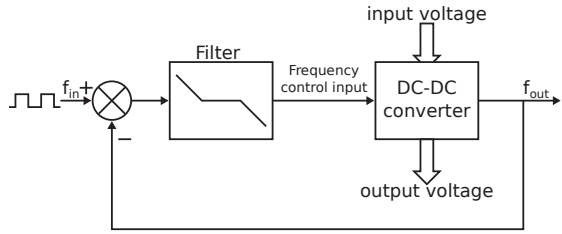

Figure 1.54. *Phase locked-loop synchronization*

1.4.8. *PFM - pulse skipping: burst modes*

The inductor current of any of the three converters can become momentarily negative at low load current. This significantly degrades the efficiency, as the RMS currents are high while the average currents are small and switching losses remain almost constant despite the low output power. Therefore, for low load, current-mode converters use some kind of discontinuous conduction mode in order to improve the low load efficiency of the converter.

These discontinuous conduction mode (DCM) modulation principles introduce a high impedance state where both switch and rectifier are turned off. The most straightforward solution is to drive the rectifier as an ideal diode so that the inductor current is always positive. Hence, a conduction cycle becomes an on-time, followed by an off-time and then by a high impedance state until the start of the next conduction cycle. This modulation scheme keeps the switching frequency of a PWM-controlled converter constant. However, switching losses do not scale down with a reduced load current and the efficiency rapidly falls. Furthermore, this scheme requires a fast zero-current-crossing detection that is difficult to design for high-frequency, multi-MHz converters.

In pulse frequency modulation, an on-time and off-time are generated followed by a high impedance state. The controller generates a conduction sequence (on- and off-time) when the output voltage hits the reference

voltage. By appropriately setting the conduction times, the converter turns into high impedance mode when the inductor current is zero. The output voltage is maintained by the output capacitor and slowly discharges until the start of the next cycle. The PFM modulates the frequency of the current pluses in order to control the output voltage, and therefore the switching frequency is not controlled. However this does not significantly affect the efficiency as switching losses and conduction losses are proportional to the pulse density. Last but not the least, the bias current of the converter is the only current drawn from the battery during the high impedance state and can significantly affect the efficiency of the converter. For instance, 10 uA drawn from a 3.8 V battery represents 3.8% of a 1 mW load, such as a small digital circuit in retention mode.

In pulse-skipping mode, the converter skips one clock cycle in high impedance in order to avoid reversing current to the battery. This scheme keeps the effective switching frequency of the converter at an integer multiple of the clock frequency.

Burst mode operation increases the low load efficiency by delivering a burst of a few conduction cycles when the output voltage falls below the reference threshold. This operation must take place between the pulse-skipping mode and the PFM mode, in which the frequency of the burst is modulated but the length of the cycles is controlled.

1.5. Minimum voltage deviation controller

This section describes a hardware-efficient mixed-signal controller integrated circuit (IC) for DC/DC converter that recovers from load transients with practically minimum possible output voltage deviation. In the steady state, the IC behaves as a conventional voltage mode pulse-width modulation controller. During load changes, it enters the transient suppression mode that uses a simple algorithm, requiring no knowledge of the converter parameters and almost no processing power, to seamlessly recover back to the steady state without exposing components to a high current stress. To compensate the effects of converter losses and system delays on the controller operation, the IC also incorporates the duty ratio correction logic and dual extreme point-based detection. The simplicity of the control method enables the

development and utilization of an application-specific asynchronous track-and-hold analogue-to-digital converter (ADC), with 10 times smaller silicon area and power consumption compared with state-of-the-art flash ADC. The entire IC is implemented in a CMOS 0.18μm process on a 0.26 mm^2 silicon area, which is comparable to the state-of-the-art analogue solutions. The IC enables about three times smaller output voltage deviation, when used in typical PoL 12V-to-1.8V 60W/120W applications, compared with PID compensators having a 1/10th of the switching frequency bandwidth.

1.5.1. *Introduction*

High-frequency low-power switch-mode power supplies (SMPS), used in consumer electronics, portable applications and computers, are required to meet stringent voltage regulation requirements [INT 08, PAN 01, SAG 04] using a cost-effective, small-volume implementation. The regulation is usually achieved by an application-specific on-chip integrated controller (controller IC) occupying a small silicon area [ON 11, INT 15, MAX 14]. The controller is often required to effectively minimize voltage deviations caused by load transients and, in that way, minimize requirements for the bulky output filter capacitor [ERI 01].

Conventional controller ICs [ON 11, INT 15, MAX 14] most frequently use constant-frequency voltage or current-programmed mode control [LIN 08], [TEX 07], where a linear PID compensator provides accurate output voltage regulation and system robustness over a wide range of operating conditions. To obtain a fast response and thus small output voltage deviations, a high bandwidth control loop is usually designed. However, since the validity of the averaged converter models used in compensator designs is constrained to frequencies that are significantly lower than the switching frequency [ERI 01], the bandwidth of the feedback loop is quite limited. Hysteretic-control-based analogue IC solutions, which belong to the ripple-based class of controllers [RED 09], have a very simple structure and, generally, provide a faster transient response. However, those systems usually operate at a variable switching frequency, which is not desirable in the targeted noise-sensitive applications. Also, in these systems, as well as in other ripple-based solutions, great care is required to mitigate stability problems [RED 09], such as jitter, high noise sensitivity and fast-scale

instability. Constant-frequency ripple-based systems [RED 09], [MIC 08] eliminate the variable frequency and stability problems. The improvements are usually achieved by the introduction of an additional feedback loop that often slows down the transient response. Also, during transients, in hysteretic systems, the switching components and the inductor are often exposed to currents that are significantly larger than nominal [LEU 05]. As a result, the power stage is usually overdesigned. While the ripple-based solutions provide a very fast transient response, they are still not able to recover the output voltage with the minimum possible deviation. The recently developed digital controller ICs for high-frequency DC/DC converters [COR 09b], [COS 08] can further improve transient response through advanced control laws. Among the most notable examples are time-optimal [COS 08, GUA 06, GUA 07, MEY 12, ZHA 08, YOU 08, COR 09a, JIA 10, EFF 08, COR 10] and digital hysteretic [COR 09b, LEU 05, SU 08, HUE 11, COR 11, COR 08, CHE 10] controllers. For a given power stage, these solutions achieve almost the fastest possible recovery time and thus the smallest deviation. These advantages are most often demonstrated with large-scale prototypes consisting of discrete components and general-purpose digital logic. However, on-chip implementation of these controllers has not been widely adopted. This is mainly due to the challenges related to the complexity of the hardware needed for their implementation. The controllers require fairly demanding computational algorithms, to calculate the optimum switching sequence, and use complex analogue-to-digital converters (ADC) consuming relatively large power and silicon area. Furthermore, their operation is significantly affected by the imperfections of the converter circuit, i.e. converter losses and parasitic resistances, as well as by the system delays. All these characteristics make the implementation of the on-chip minimum-deviation controllers challenging and overly expensive for the targeted cost-sensitive applications. As demonstrated in [COR 09b, COS 08], an application-specific ADC for digital hysteretic and time-optimal controller occupies a larger silicon area than an entire conventional controller IC [CHE 08, TRE 11, LIO 08, CHA 10, AHN 11, WU 10].

The main goal of this section is to describe a simple minimum-deviation mixed-signal controller IC for DC/DC converters that does not suffer from the previously mentioned drawbacks and can be implemented with simple hardware. Similar to solutions presented in [GUA 06, GUA 07, MEY 12, ZHA 08], [GUA 06, GUA 07, MEY 12, ZHA 08], [COR 09a], [COR 10], the controller IC shown in Figure 1.55 has two distinctive modes of operation.

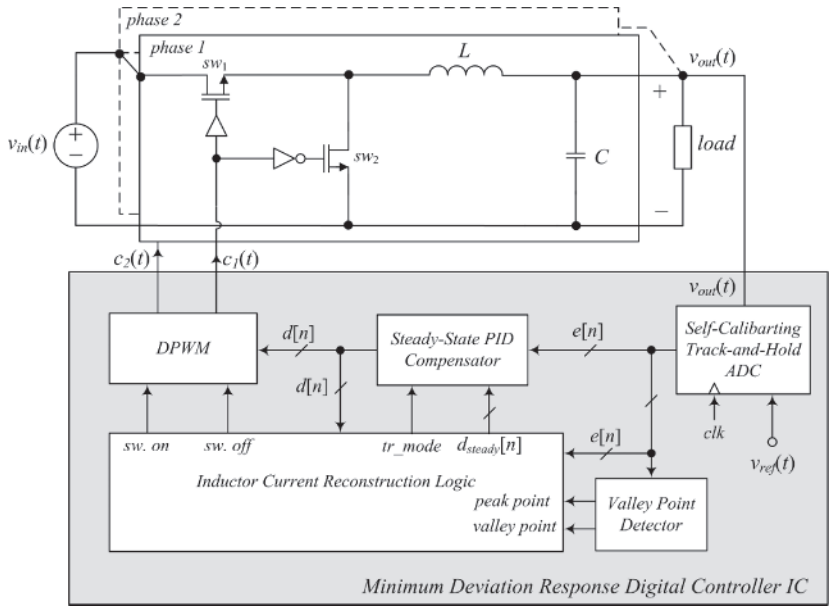

Figure 1.55. *Minimum deviation controller IC regulating operation of a two-phase buck converter*

In the steady state, the controller IC operates as a conventional constant-frequency pulse-width modulated voltage-mode controller. It uses a PID compensator to provide robust operation over a wide range of operating conditions. During transients, the controller provides recovery from load step changes with practically minimum possible output deviation by charging/discharging the inductor current to the new steady-state current value using a single on-off control action.

In this case, an accurate reconstruction of the entire current waveform, i.e. both the DC and ripple components, is very important. This is because, in modern converters, the ripple component can be as large as 40% of the maximum load current value [NXP 07a, FAI 07] and thus any ripple mismatch can have the same effect as a large load transient. The operation of the controller during a sudden light-to-heavy load change can be explained by the waveforms shown in Figure 1.56. As soon as the output voltage drop exceeds the threshold value, i.e. the detection of a transient, the controller turns on the converter main switch (SW1, Figure 1.55) causing the ramp up of the inductor current. This process continues until the detection of the output voltage valley point, by the track-and-hold ADC [RAD 13] shown in

Figure 1.55. At this point, the initial on-time of the transistor control signal, c(t), is extended by the time interval t_{on} in [1.36], followed by a turn-off period in [1.37], where D is the steady-state duty ratio value and T_{sw} is the switching period:

$$t_{on} = \frac{D \cdot T_{sw}}{2} \quad [1.36]$$

$$t_{off} = (1 - D) \cdot T_{sw} \quad [1.37]$$

As shown in Figure 1.56, this switching sequence results in a current waveform that is practically identical to that of the new steady state. As soon as this current reconstruction period is completed, the PID compensator is reactivated to perform charge recovery, bringing the output voltage to the reference value. It should be noted that the new operating conditions are well suited for the PID compensators, as the converter operates close to the steady state, where the small-signal assumption [ERI 01] is valid. As a result, smooth mode transition can be achieved despite system delays, power converter parasitics and non-idealities [RAD 13]. In addition, the simplicity of the minimum-deviation concept lends itself well to utilization in multi-phase systems [RAD13], [STR 14].

1.5.2. *Integrated circuit implementation and experimental results*

A single/dual-phase minimum-deviation digital controller IC [RAD 13], designed and fabricated in a 0.18μm CMOS process, is shown in Figure 1.57. The complete digital logic takes about 4500 gates, including 500 digital blocks used for testing and debugging, and is fully implemented through the Verilog hardware description language (HDL) and automated design tools. The main characteristics of the IC are listed in Table 1.1.

The closed-loop verification of the minimum-deviation controller IC was performed with a state-of-the-art industrial two-phase, 12 V to 1.8 V, 500 kHz, buck converter module, providing 35 A per phase [NXP 07a, NXP 07b]. The ESR of the 400 μF output capacitor is just 0.5 mΩ and each phase uses a 0.47 μH inductor. The experimental waveforms shown in Figure 1.58 indicate the transient response results of the conventional PID compensator, designed to have the bandwidth of a 1/10th of the switching frequency, during a 0A-to-30A light-to-heavy transient. In Figure 1.59, the suppression logic is active. In this case, the duty ratio correction logic is not used.

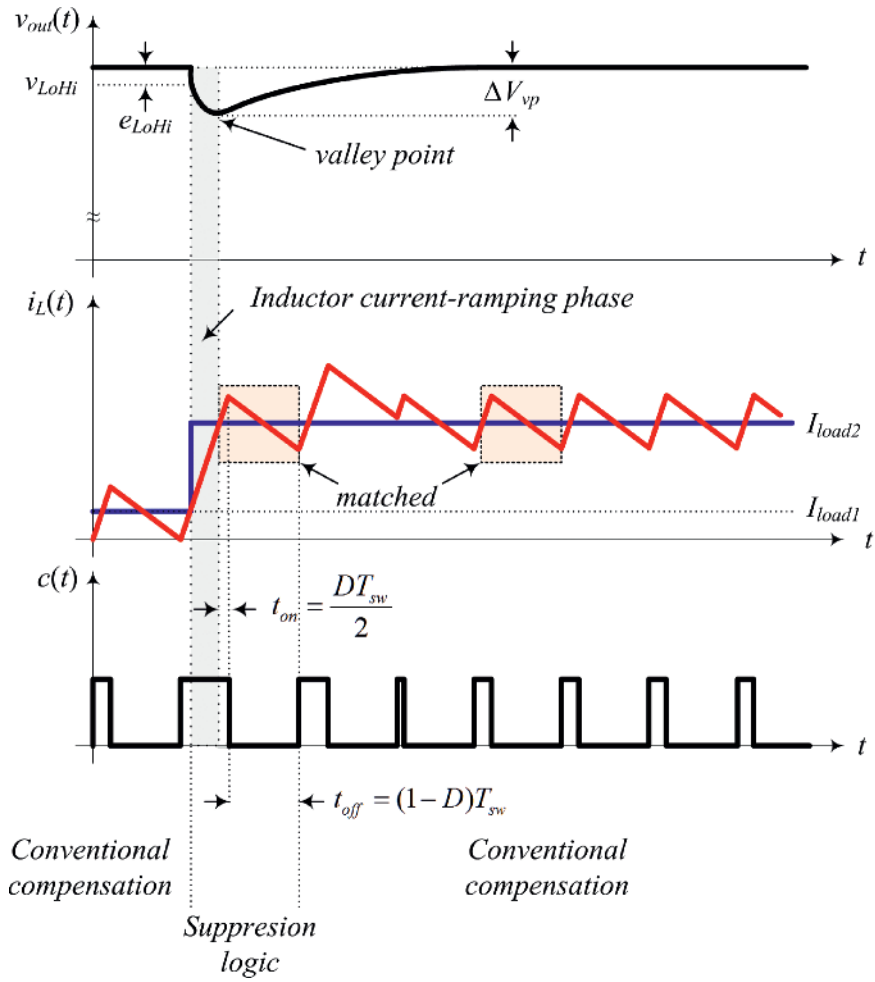

Figure 1.56. *Operation of the large–small signal digital controller during the light-to-heavy load transient with a single-phase buck. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

The results indicate that the activation of the suppression logic results in about three times smaller deviation, allowing for a proportional reduction of the output capacitor. Similar improvements can be achieved for both conventional multiphase interleaved buck topologies [RAD 13] and hybrid inductive-capacitive SMPS [NXP 07b, RAD 14].

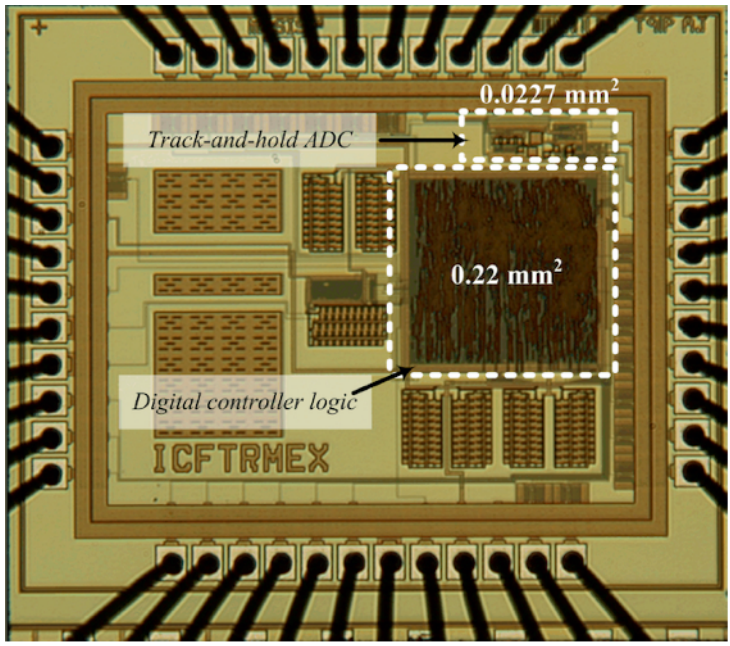

Figure 1.57. *Photograph of the minimum-deviation digital controller IC. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

Technology	TSMC 0.18μm CMOS
Supply voltage (digital/analogue)	1.8 V / 3.3 V
DPWM resolution	13 bits
DPWM nominal frequency	500 kHz
ADC area	0.02 mm^2
ADC current consumption	0.24 mA
ADC quantization voltage	4 mV
Digital logic area	0.22 mm^2
Digital logic current consumption	0.2 mA
Total area	0.24 mm^2

Table 1.1. *Minimum-deviation digital controller IC summary*

1.6. CAD tools for PwrSoC design and optimization

The design of integrated power converters on-chip can be formulated as an optimization problem that satisfies some electrical and thermal requirements

subject to geometrical constraints with given technologies (semiconductors, magnetic materials, integrated capacitors and packaging). In this chapter, as an application example, we will focus on the optimization of a single-stage buck converter that will be optimized in terms of efficiency at typical load, satisfying the static and dynamic electrical requirements with constraints in the total area occupied by the passives (integrated inductor and capacitors). Finally, the optimization can be seen as a process in which many designs that comply with all the requirements are carried out, and the results are ordered according to some performance metrics that allow the selection of the best design according to the selected metrics. For example, one performance metric can be the cost, and the design can be optimized according to that metric satisfying all the electrical requirements and physical constraints.

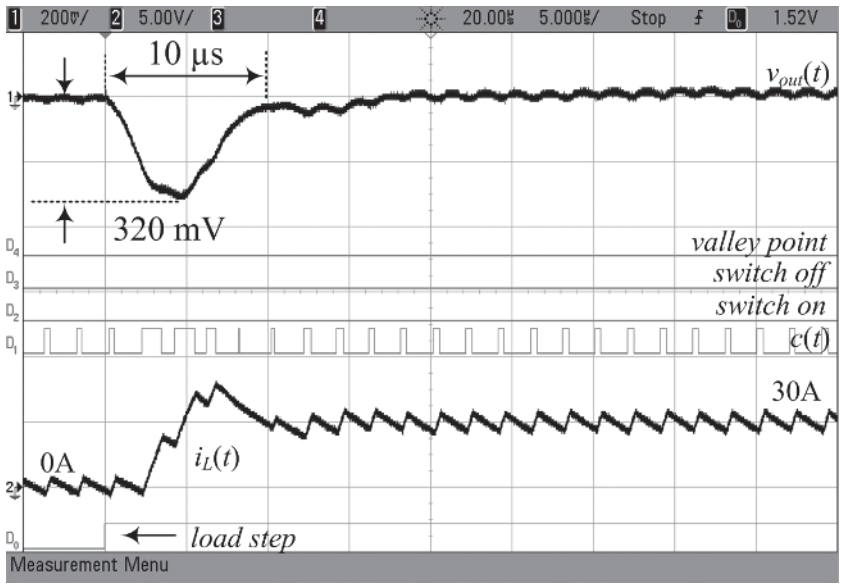

Figure 1.58. *Transient response waveforms for a 0 A-to-30 A load step (wide-bandwidth conventional compensator): Ch1, output converter voltage (200 mV/div); Ch2, actual inductor current iL(t) 30 A/div; D_0, load transient triggering signal; D_1, pulse-width modulated control signal; D_2, main switch control signal created by suppression logic; D_3, synchronous rectifier control signal created by the suppression logic; D_4, peak/valley point detection; time scale is 5 μs/div*

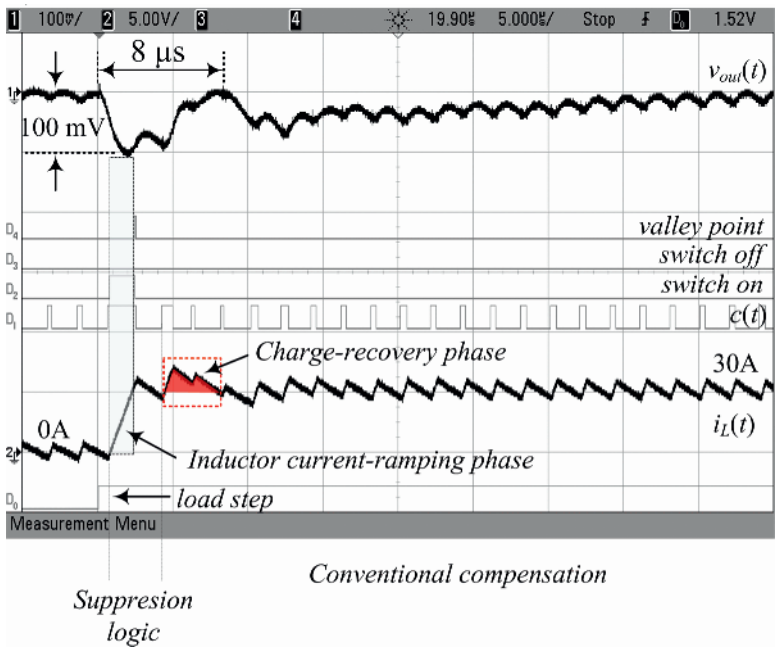

Figure 1.59. *Transient response waveforms for a 0 A-to-30 A load step (minimum-deviation controller IC): Ch1, output voltage (200mV/div); Ch2, inductor current iL(t) 30A/div; D_0, load transient triggering signal; D_1, pulse-width modulated control signal; D_2, main switch control signal created by suppression logic; D_3, synchronous rectifier control signal created by the suppression logic; D_4, peak/valley point detection; time scale is 5 μs/div*

1.6.1. *Overview of the CAD requirements*

The key element in the optimization is the design process. The design flow is shown in Figure 1.60. From the specifications, at the top of the process to the final design at the bottom, three layers can be identified.

Design options – These are the building blocks of the integrated power converter:

– technology for the semiconductor devices, the integrated inductors and the integrated capacitors. The designer can select from among different technologies for all these components that will affect the final result;

– topology. Different topologies can be used to process the energy (single-phase buck, multiphase buck, coupled inductors, switched capacitors, hybrid,

etc.). The selection of the topology is coupled with the available technology and the control;

– control. As has been shown in this chapter, the control has a strong influence on the size of the LC filter; as a result, its selection and optimization will affect the final results;

– modes of operation. To improve the efficiency at light load, different strategies to modulate the converter can be applied. The trade-off between the higher complexity and the efficiency benefit can be assessed based on the optimization results.

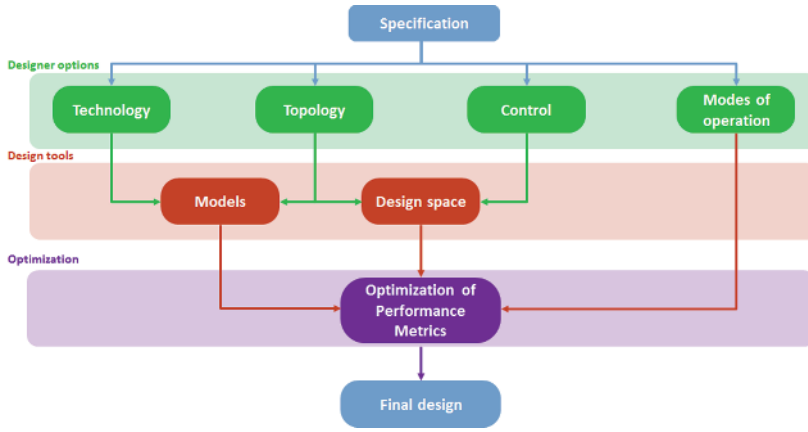

Figure 1.60. *Design layers for the optimization of integrated converters on-chip. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

Design tools – The design of the converter to meet the specifications with the designer options of the previous level has to be done based on:

– models. Different types of models (losses, static, dynamic) will be needed in the design process depending on the type of metric to be evaluated. The models will help to quantify losses, to evaluate the static behavior of the converter (waveforms in the steady state) and to design the controller to meet, if possible, the dynamic requirements of the converter;

– design space. Based on the design options selected at the design option level, and based on the specifications to be met by the converter, a design space will be identified for each switching frequency. The design space is represented by the values of the output inductor and the output capacitor, for a given switching frequency, topology and type of control, which will provide a valid solution (meeting all the requirements).

Optimization – Based on the above definition of the models and the design space, the optimization algorithm will search for the optimum solution according to some performance metrics. The optimization can be either single-objective optimization, such as optimizing the efficiency at a given operating point (meeting all the requirements), or multiobjective, such as optimizing a weighted function of several performance metrics. For this purpose, different optimization algorithms can be used. Nevertheless, even though the optimization algorithm has a strong effect on the speed of the search and to avoid local minima, the biggest effort has to be placed on the models used for the design.

1.6.2. *Loss models for integrated inductors and semiconductors*

One of the key design metrics is the losses. To carry out the design, it is necessary to have accurate loss models for the semiconductors, integrated magnetics and capacitors, as a function of the operating conditions. The models can shift from simplified analytical models that allow a first-order approximation and to gain physical insight, to highly complex 3D models based on finite element analysis calculations for the losses on the magnetic components. Although the complex models are more accurate, and allow taking into account high-order effects, the computation time required restricts its use on the optimization algorithms. They can be used, at the end of the optimization process, to validate the end results.

1.6.2.1. *Analytical models for magnetic components*

Magnetic components have to be designed in an ad hoc manner during the optimization process. As long as the value of the inductance, the switching frequency or the available area for the inductor change during the optimization, a new inductor needs to be designed for these operating conditions. The models for the inductors will help optimize their design and quantify their influence in terms of losses in the overall design. Since the optimized design of the inductor is within the power converter optimization loop, analytical models that quantify the losses will be preferable to speed up the process.

To obtain an analytical model of the inductor, 1D approximations can be used [DOW 66]. In this case, the analytical model of a basic inductor, validated by 2D FEA simulations, can be implemented based on the equations presented in [AND 13a]. The losses of the inductor are divided into DC

conduction losses, $PL_{(Cu\_DC)}$, AC conduction losses, $PL_{(Cu\_AC)}$, core hysteresis losses, $PL_{(Fe\_Hyst)}$, and core eddy current losses, $PL_{(Fe\_Eddy)}$. The inductor conduction losses are estimated using the inductor DC resistance, R_{DC}, and AC resistance factor for k^{th} switching frequency harmonic, F_k; therefore, the conduction losses are calculated by using [1.38] and [1.39], where $I_{(L\_DC)}$ is the DC inductor current and I_{LK} is the amplitude of the inductor current k^{th} switching frequency harmonic:

$$P_{L\_Cu\_DC} = R_{DC} \cdot I_{L\_DC}^2 \quad [1.38]$$

$$P_{L\_Cu\_AC} = R_{DC} \cdot \sum_{k=1}^{k_{max}} F_k \cdot \frac{I_{LK}^2}{2} \quad [1.39]$$

Core losses are calculated by adding hysteresis and eddy current losses. Hysteresis losses, created due to the hysteretic dependence of the flux density (B) versus magnetic field (H), are calculated using [1.40], where K_H and b are material-dependent parameters, V_C is the core volume, f_{SW} is the switching frequency and ΔB_{PP} is the peak-to-peak flux density, calculated using [1.41]:

$$P_{L\_Fe\_Hyst} = K_H \cdot f_{sw} \cdot (\frac{\Delta B_{PP}}{2})^b \cdot V_C \quad [1.40]$$

$$\Delta B_{PP} = B_{DC} \cdot \frac{\Delta IL_{PP}}{IL_{DC}} \quad [1.41]$$

The eddy current losses of the magnetic core are calculated by using proximity loss estimation. It is assumed that the eddy currents are generated due to the proximity effect of the generated magnetic field in the core. For detailed information about the calculation, the reader can refer to [SVI 14] and [AND 13a].

1.6.2.2. *Semiconductor loss models based on combined simulation and analytical models*

To calculate the losses in the semiconductors, three typical approaches can be adopted:

– Analytical models. Analytical models are based on simplified analytical equations that describe the behavior of the devices and allow the calculation

of the losses by solving a simplified equivalent circuit. One example is the calculation of MOSFET switching losses provided in this chapter. Other approaches that take into account the parasitic inductances can be found in [REN 06]. The main advantage of this approach is that it fits very well into the optimization process and its main drawback is the accuracy;

– simulation models. The use of accurate SPICE models provided by the IC manufacturer allows the use of detailed simulations to calculate losses in the semiconductor devices. It requires running a detailed simulation whenever a design parameter is changed, with the corresponding increment of computation time;

– combined simulation and analytical models. The idea is to combine both approaches, i.e. the accuracy of the SPICE simulations with the speed of the analytical models. In this approach, the device losses are computed by running an extensive set of simulations once, and the results are stored in multidimensional matrices than can be accessed very quickly during the optimization process [AND 13a].

Due to its usefulness, this approach will be explained in more detail in this chapter. The process will be illustrated using a buck converter as an example, as shown in Figure 1.61, where the high-side and low-side switches are PMOS and NMOS transistors. The process is divided into two steps:

1) characterization of the devices by means of SPICE simulations;

2) calculation of losses under any operating condition of the converter based on analytical equations.

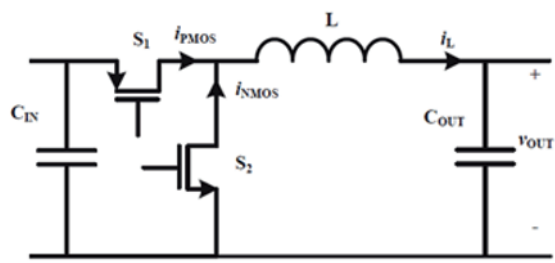

Figure 1.61. *Schematic of a buck converter*

1.6.2.2.1. Evaluation of energy losses

A discrete number of accurate calculations can be performed using SPICE simulations. From these calculations, interpolated piece-wise linear functions are constructed, allowing the estimation of the losses for all the points that belong to the input domain of the model. The computations are performed by sweeping the independent variables of the measured function (w and I and v_{GS}, if needed).

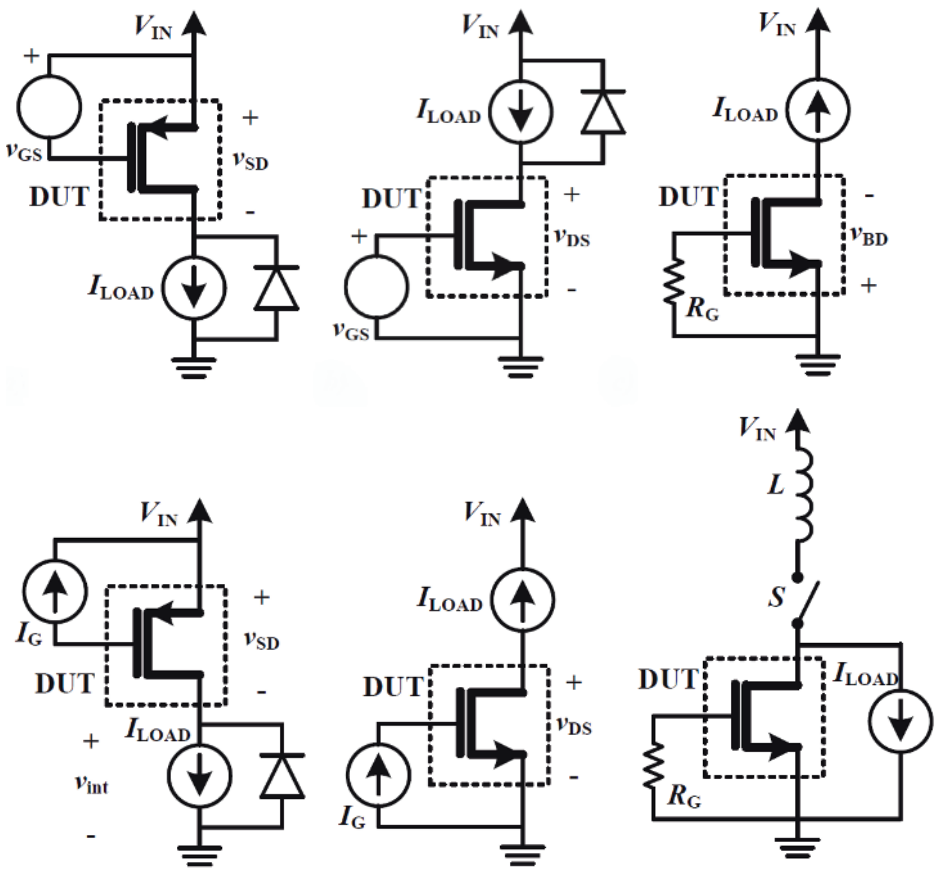

Figure 1.62. *Circuits for characterizing MOSFETs: a) PMOS on resistance, b) NMOS on resistance, c) NMOS body-diode voltage drop, d) PMOS turn-on and turn-off energies and driving gate charge, e) NMOS driving gate charge and f) NMOS body-diode reverse recovery energy loss*

To calculate the ON resistance of the PMOS, the circuit shown in Figure 1.62(a) is used varying the MOSFET width w_P, the load current I_{LOAD} and the gate-to-source voltage v_{GS}. Finally, by measuring the source-to-drain voltage drop v_{SD}, the on-resistance is calculated and the dependence $R_{PMOS}(w_P, v_{GS}, I_{LOAD})$ is obtained. Similarly, the circuit shown in Figure 1.62(b) is used to obtain the on-resistance of the NMOS, obtaining $R_{NMOS}(w_P, v_{GS}, I_{LOAD})$.

The circuit shown in Figure 1.62(c) is used to measure the NMOS body-diode voltage drop sweeping the MOSFET width w_N and the load current I_{LOAD}, while the gate is connected to the source via a small resistance R_G, which emulates the driver output resistance. Finally, the dependence $v_{(D_MOS)}(W_N, I_{LOAD})$ is obtained.

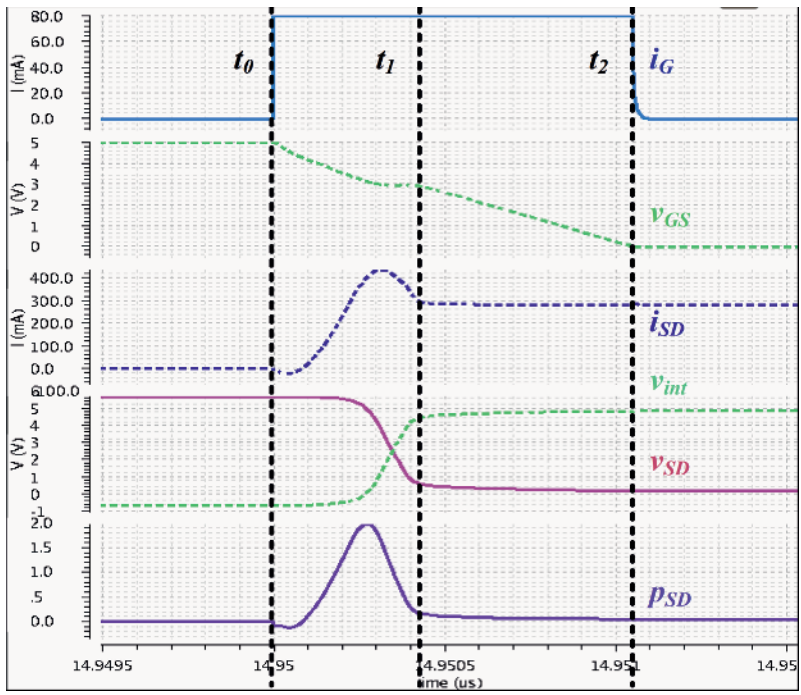

Figure 1.63. *SPICE simulation – PMOS turn-on energy loss and gate-charge calculation: gate current i_G (blue, solid), PMOS gate-to-source voltage v_{GS} (green, dotted), PMOS source-to-drain current i_{SD} (blue, dotted), intermediate voltage v_{int} (green, dotted), PMOS source-to-drain voltage v_{SD} (purple, solid) and PMOS source-to-drain power loss P_{SD} (light green, solid). For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

The dynamic characteristics of the switches are obtained using circuits shown in Figure 1.62(d-f), and using the simulation results shown in Figure 1.63. To perform the SPICE calculations, the driver is modeled as the current source injecting a constant current during the transient. The circuit shown in Figure 1.62(d) is used to calculate both turn-on and turn-off energy loss and gate charge. The turn-on energy loss calculation and gate-charge calculation are shown in Figure 1.64 for a load current of 280 mA, a PMOS width of 8 mm and an input voltage of 5V.

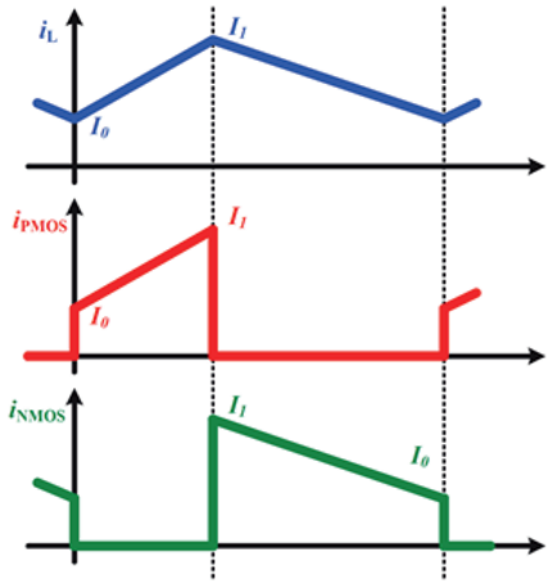

Figure 1.64. *Buck converter currents: inductor current i_L (blue), PMOS current i_{PMOS} (red) and NMOS current i_{NMOS} (green). For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

The simulations are relatively fast as a single switch action is performed. Initially, the PMOS is turned-off and the ideal diode carries the load current while the PMOS blocks the input voltage. At the time instant t_0, the driver current saturates to a maximum value I_{DR} (80 mA for the present case) and the gate-to-source voltage v_{GS} starts to decrease. When the PMOS current i_{SD} reaches the load current, the source-to-drain voltage v_{SD} starts to decrease up to the voltage drop defined with the product of on-resistance and the load

current at moment t_1. On the contrary, the gate-to-source voltage continues to decrease up to the targeted value v_{GSP}.

The product of the PMOS current i_{SD} and the source-to-drain voltage v_{SD} provides the instantaneous power loss p_{SD}. Integrating the power loss from t_0 to t_1, turn-on energy loss, $E_{(PMOS\_turn\_on)}(w_P,I_0)$, is calculated for a given PMOS width and instantaneous current. Similarly, integrating the gate current i_G from 0 to t_2, the gate-charge $Q_{PMOS}(v_{GSP},w_P,I_0)$ dependence is obtained for the same PMOS width and the load current I_{LOAD} and the driving voltage V_{GSP}.

Similarly, using the same circuit, the turn-off energy characteristic $E_{(PMOS\_turn\_off)}(w_P,I_1)$ can be calculated. Furthermore, using the circuit shown in Figure 1.62e, the NMOS gate-charge dependence is obtained. Initially, the NMOS is turned off and the body diode carries the entire load current. Again, the gate current is saturated at its maximal value I_G at moment t_0 and the gate-to-source voltage starts to increase. Because the NMOS is turned-on with small drain-to-source voltage (determined by the body-diode voltage drop), it can be assumed that the switching is nearly lossless (ZVS is achieved). When the gate-to-source voltage reaches the targeted value V_{GSN} at t_2, the transient is finished and the gate charge is calculated by integrating the gate current from t_0 to t_2.

Finally, the gate-charge dependence $Q_{NMOS}(v_{GSP},w_P,I_1)$ is obtained. The circuit shown in Figure 1.62f is used to calculate reverse-recovery energy loss of the NMOS body diode. Again, the NMOS is turned-off since the gate is connected to the source via a small resistance R_G. Initially, all the current is carried by the body diode. At time t_0, the ideal switch is turned on, imposing a positive voltage at the drain and thus turning off the body diode. The inductance L is used to limit the slew rate of the body-diode current, which should be selected based on the slew rate of the PMOS source-to-drain current from simulations performed with the circuit shown in Figure 1.62d. When the inductor current reaches the load current at t_1, the body diode enters in reverse recovery mode, creating energy loss. The transient is finished at t_2 when the diode current returns to zero. Integrating the product of the body-diode current and the voltage from t_0 to t_2, the reverse-recovery energy dependence $E_{(N\_rev\_rec)}(w_P,I_0)$ is obtained.

After the construction of the piece-wise linear functions, it is possible to apply analytical equations to calculate both conduction and switching losses. Conduction losses can be calculated by using the analytical equation given in Table 1.2, were $R_{PMOS}(W_P,V_{GSP},I_L)$ are the on-resistance of the devices as a function of the device width, the gate-source voltage and the current through the device obtained by means of simulations.

Type of losses	Time instant	Equations
P_{PMOS_cond}	0 - T_{SW}	$R_{PMOS}(W_P,V_{GSP},I_L)\cdot I^2_{PMOSRMS}$
$P_{PMOS\_turn\_on}$	0 - T_{SW}	$E_{PMOS\_turn\_on}(w_P, I_0)\cdot f_{SW}$
$P_{PMOS\_turn\_off}$	D·T_{SW}	$E_{PMOS\_turn\_off}(w_P, I_1)\cdot f_{SW}$
P_{PMOS_gate}	0 - T_{SW}	$Q_{PMOS}(v_{GSP}w_P, I_0)\cdot v_{GSP}\cdot f_{SW}$
P_{NMOS_cond}	0 - T_{SW}	$R_{NMOS}(W_N,V_{GSN},I_L)\cdot I^2_{NMOSRMS}$
P_{NMOS_gate}	D·T_{SW}	$Q_{NMOS}(v_{GSN}w_N, I_1)\cdot v_{GSN}\cdot f_{SW}$
$P_{NMOS\_rev\_rec}$	0 - T_{SW}	$E_{N\_rev\_rec}(w_N, I_0)\cdot f_{SW}$
P_{Ndiode_N2P}	0 - T_{SW}	$I_0\cdot v_{D\_NMOS}(w_N, I_0)\cdot f_{SW}\cdot t_{dead\_N2P}$
P_{Ndiode_P2N}	D·T_{SW}	$I_1\cdot v_{D\_NMOS}(w_N, I_1)\cdot f_{SW}\cdot t_{dead\_P2N}$

Table 1.2. *Calculation of semiconductor losses*

For the calculation of switching losses, the following considerations are important. As the PMOS switch operates with hard switching, the switching losses can be divided into driving, turn-on and turn-off losses. Using the steady-state waveforms shown in Figure 1.64, the turn-on energy loss can be found to occur at the beginning of the cycle, which depends on the instantaneous inductor current I_0, the width of the PMOS, W_P, and the input voltage. As stated previously, since the input voltage is fixed, it can be omitted from the model, thus degrading the dependence to only two variables (W_P and I_0).

Similarly, the turn-off energy loss, which occurs at the end of the on-time, also depends on the instantaneous inductor current I_1 and the width of the PMOS, W_P, assuming that the input voltage has been incorporated into the model. The piece-wise linear function obtained by means of simulations for the turn-off energy is shown in Figure 1.65. The final component of PMOS switching losses is the driving loss, which occurs at the beginning of the cycle. The driving energy loss can be estimated as the product of the charge needed to turn on the device and the driving voltage. Again, the charge required depends on the width W_P, the instantaneous current I_0 and the driving voltage V_{GSP}.

Driving losses, occurring at time instant $D{\cdot}T_{SW}$, can be calculated as a product of the gate charge and the driving voltage v_{GSN}. The charge is dependent on the width, w_N, the instantaneous current I_1 and the driving voltage v_{GSN}. The energy losses of the body-diode conduction occur at the beginning of the cycle as well at the time instant $D{\cdot}T_{SW}$, which can be calculated as a product of the voltage drop of the diode, the instantaneous currents (I_0 and I_1) and the duration of the dead times ($t_{(dead\_N2P)}$ and $t_{(dead\_P2N)}$).

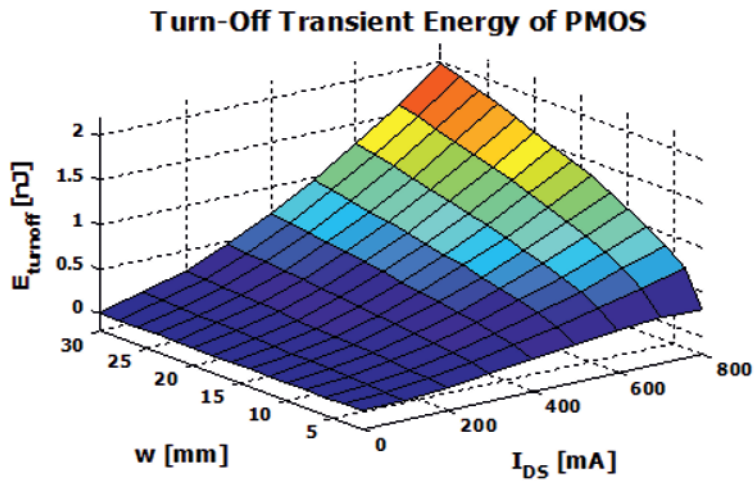

Figure 1.65. *Turn-off transient energy of the PMOS as a function of width and drain current. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

On the contrary, as the low-side NMOS operates with ZVS, the switching losses can be divided into the driving loss, the body-diode conduction losses and the reverse recovery of the body diode. Similarly, for the PMOS, the driving energy loss, occurring at time instant $D{\cdot}T_{SW}$, can be calculated as a product of the charge and the driving voltage v_{GSN}. The charge is dependent on the width W_N, the instantaneous current I_1 and the driving voltage v_{GSN}. The voltage drop is proportional to the corresponding currents and the width of NMOS. Characterizing all the functions of the model, the total losses can be calculated using equations presented in Table 1.65.

1.6.3. *Optimization algorithms*

The optimization algorithm searches for a set of design variables (switching frequency f_{SW}, inductor area A_L, inductance L, output and input capacitance C_{OUT} and C_{IN} and widths of MOSFETs w_P and w_N) to obtain maximal efficiency at a nominal operating point defined by the typical output current I_{TYP}, the output voltage V_{OUT} and the input voltage V_{IN}. During the optimization process, the static and dynamic behavior of the system is simulated to verify that both static and dynamic constraints are satisfied under the worst-case steady-state operation and under the load steps and input voltage step transients.

To search the optimum design, different algorithms can be applied. In this case, where the metric to be optimized is the efficiency at typical load, a possible implementation of the search algorithm is shown in Figure 1.66, from which it can be seen that the optimization is performed in two steps:

1) Coarse exhaustive search of the design space obtaining the intermediate optimal point (OPT_{INT}). During this approach, the design space is searched with relatively large step in order to avoid local maxima. The algorithm starts by defining the current switching frequency $f_{SW}(k_F)$, the inductor area $A_L(k_{AL})$ and the inductance $L(k_L)$. If the implementation of the inductor is possible, the optimal design is passed downwards and the algorithm selects the current output capacitor $C_{OUT}(k_C)$ and indirectly the input capacitor $C_{IN}(k_C)$, which is defined by difference between the total implementable capacitance C_{Total} and the current output capacitance $C_{OUT}(k_C)$. The total implementable capacitance C_{Total} is defined by the capacitance density and an available capacitor area, obtained as the difference between the total area of the device and the current inductor area $A_L(k_{AL})$. After obtaining all the electrical parameters, $L(k_L)$, $C_{OUT}(k_C)$, $C_{IN}(k_C)$ and $f_{SW}(k_F)$, the converter is simulated both in the steady state and under transients. If the performance obtained satisfies the constraints of the system, the algorithm selects current NMOS and PMOS widths, $w_N(i_{(W\_N)})$ and $w_P(i_{(W\_P)})$, and estimates the efficiency at a typical operating point. After calculating all the possible combinations, the intermediate optimal design OPT_{INT} is obtained.

2) Fine gradient search from that point to the optimal design (OPT). For each variable x, the efficiency is estimated in points $x-\Delta x$, x, $x+\Delta x$. The initial step, Δx, is equal to half of the step in the exhaustive search. If the efficiency is increased for one of the new designs in any direction, the new design is taken as the optimal and the process is repeated. If there is no increase in the efficiency, all the steps are reduced by half and the process is repeated.

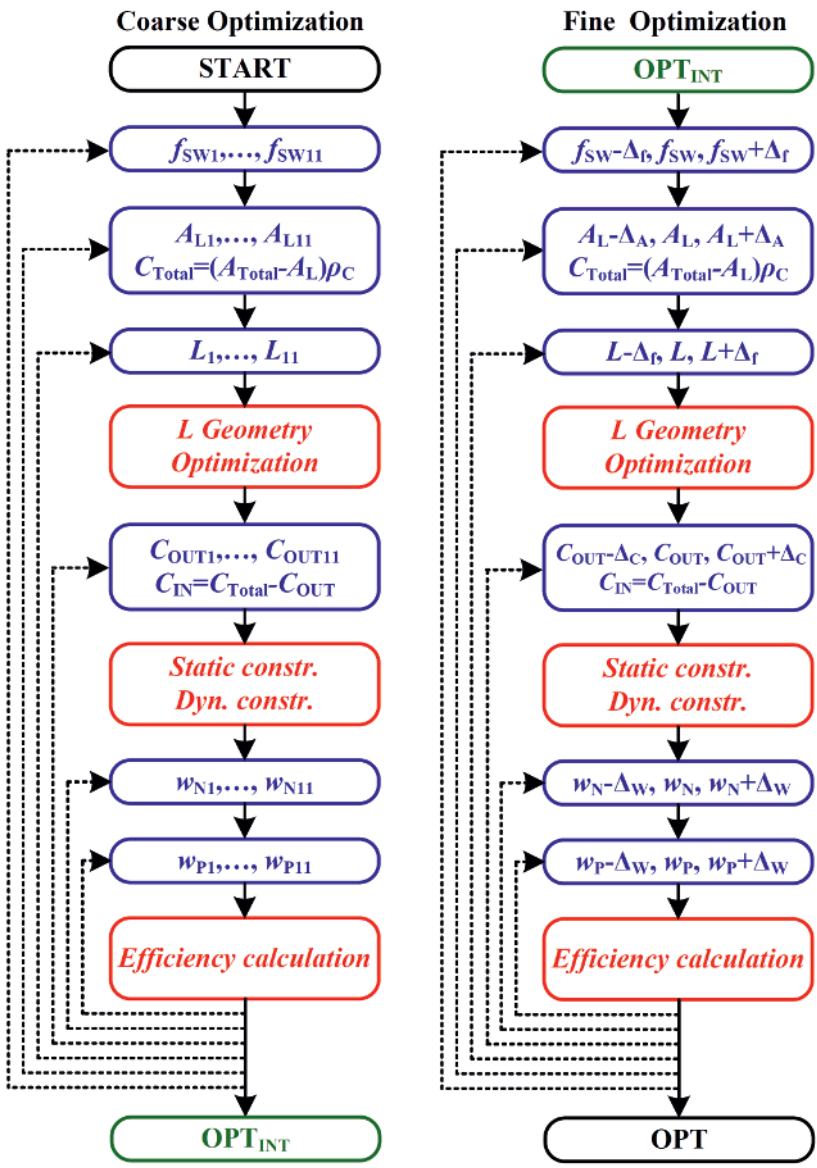

Figure 1.66. *Optimization algorithm flowchart. For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

1.6.4. *Outcome of the optimization (topology, area, loss, f_{sw}, detailed design)*

As a result of the optimization process, a complete design of the power stage is obtained with detailed information about the individual optimization of all the components.

– semiconductors: optimum size of the high-side and low-side MOSFETs and their driving gate-to-source voltage;

– inductor: optimum area dedicated to the inductor, geometrical parameters (core length, width and thickness), number of turns, trace width and height. Eventually, if different core materials can be used for integration, the optimization algorithm will provide the most suitable;

– integrated capacitors: optimum area dedicated to input and output capacitors and the optimum combination of cells (with different capacitance per unit area vs. ESR per capacitance) for a given specification;

– control: the optimization algorithm will provide a design of the controller that satisfies the dynamic requirements under parameter variations of the components. The controller type (voltage mode, current mode, ripple-based) can be either an input to the optimization algorithm or selected by it;

– light load modulation: the optimization results can show the efficiency as a function of the load for different light load modulation strategies and the designer can select the most suitable one for its applications, taking into account the trade-off between the benefit (loss reduction) and the complexity of the implementation. Figure 1.67 shows the efficiency versus load results for a buck converter (5V to 1.2V) optimized for a typical load of 270 mA. It shows how burst mode operation (red) improves the efficiency at light load compared with the operation in CCM (blue) or DCM (green). It will be the designer's decision to assess whether the improvement obtained is worth.

The optimization algorithm has to provide not only the final design, optimum according to the selected performance metrics, but also how the design variables affect the results. For example, Figure 1.68 shows the breakdown of losses for an optimized design of a buck converter with an output voltage of 1.2V and an output current of 270 mA: semiconductor

losses in red, inductor losses in blue, capacitor losses in black and total losses in blue. According to the metric of efficiency, or lower losses, the best design is achieved with a switching frequency of 12 MHz. Nevertheless, the difference in losses of all designs with switching frequency between 8 MHz and 20 MHz is less than 4 mW, i.e. the efficiency varies only by 1% in all this range.

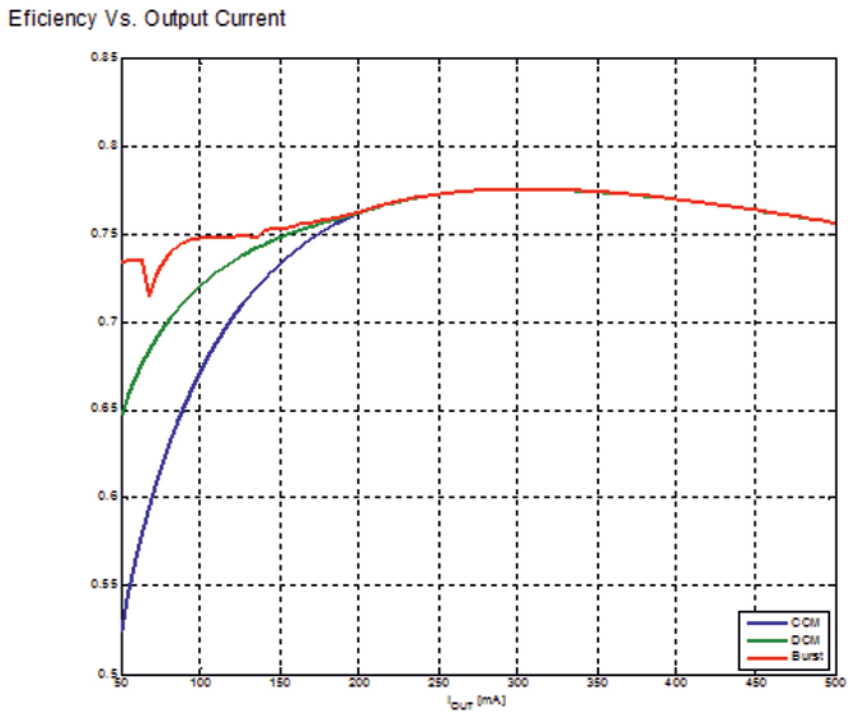

Figure 1.67. *Efficiency versus output current for different light load modulation strategies: CCM (blue), DCM (green), BURST mode (red). For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

Based on this useful information, the designer can choose to operate at 8 MHz due to the lower requirements in the power management IC, knowing that the penalty on efficiency will be only 1%.

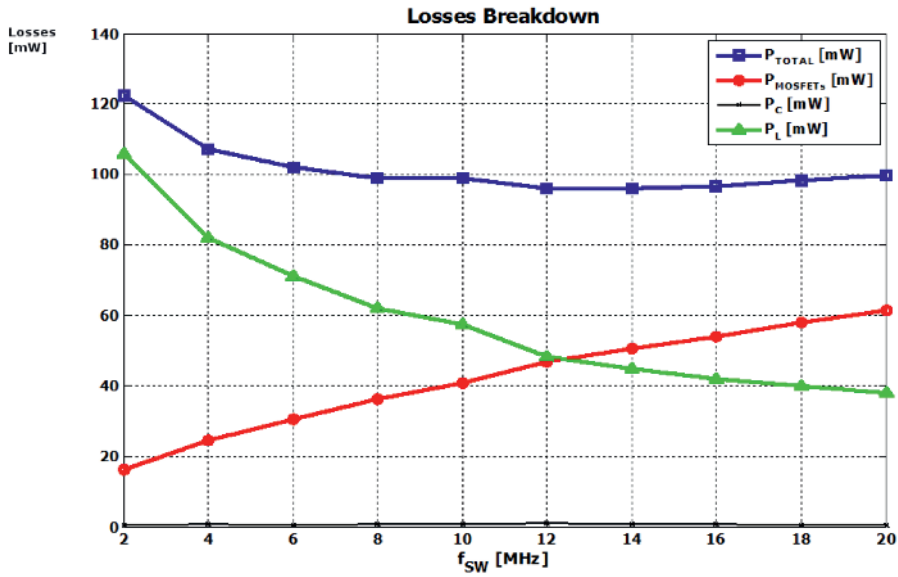

Figure 1.68. *Optimized design loss breakdown as a function of the switching frequency: total losses (blue), MOSFET losses (red), capacitor losses (black) and inductor losses (green). For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

There are other plots that also provide very useful information, such as the breakdown of losses for individual technologies, shown in Figure 1.69, as a function of the switching frequency and the breakdown of losses for all the components at a given frequency, shown in Figure 1.70. In the first case, as expected, it is shown that the higher the switching frequency, the higher the losses in the MOSFETs. It can be noted that at a low frequency (2 MHz), the difference between the total losses in the PMOS or NMOS and the switching losses is about 3mW; however, at a high frequency (20 MHz), this difference is about 10 mW, i.e. conduction losses increase with frequency. This is because all of them are optimized designs at each switching frequency and at low frequency where switching losses are lower, the size of the MOSFETs can be made large to reduce conduction losses, but as the switching frequency is increased and their influence becomes more important, the optimum size of the MOSFETs is reduced to balance conduction and switching losses.

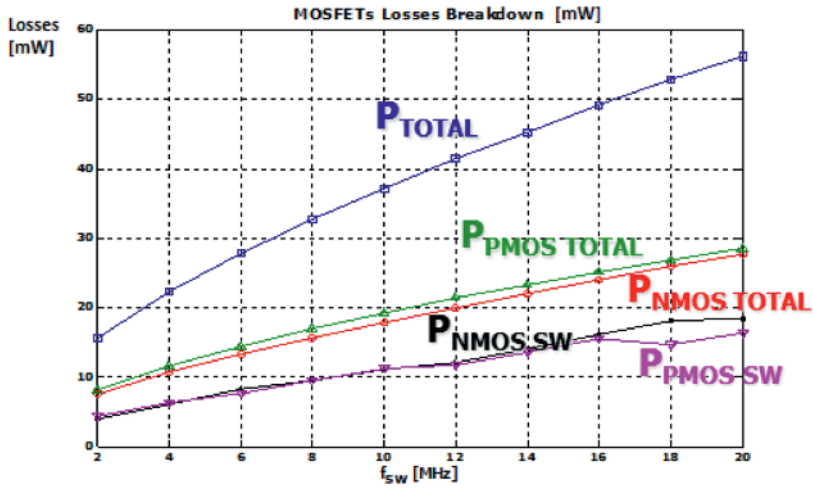

Figure 1.69. *MOSFET loss breakdown: total semiconductor losses (blue), PMOS total losses (green), NMOS total losses (red), PMOS switching losses (black) and NMOS switching losses (pink). For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

The plot in Figure 1.70 shows the detailed loss breakdown of a given design at a given switching frequency, providing information about individual MOSFET losses divided into conduction, turn-on and turn-off, and driving losses and inductor losses broken down into copper losses (DC and AC) and core losses, and input and output capacitor losses. In this case, inductor losses represent close to 50% of the total losses and the other 50% is divided equally between the high-side and low-side MOSFET.

1.6.5. *Impact of technology*

One of the outcomes of the optimization algorithm is the possibility to basically evaluate the impact of technology improvements on the overall system level metrics (efficiency, area). It is possible to evaluate different scenarios to analyze where should the main efforts be placed to get the maximum improvement. For example, it is possible to evaluate the effect of having ideal semiconductor devices (with no losses), keeping the technology of the magnetics and the integrated capacitors, or the case when the inductors are ideal (the inductor occupies no space and has no losses) so the limits will be given by the Si devices.

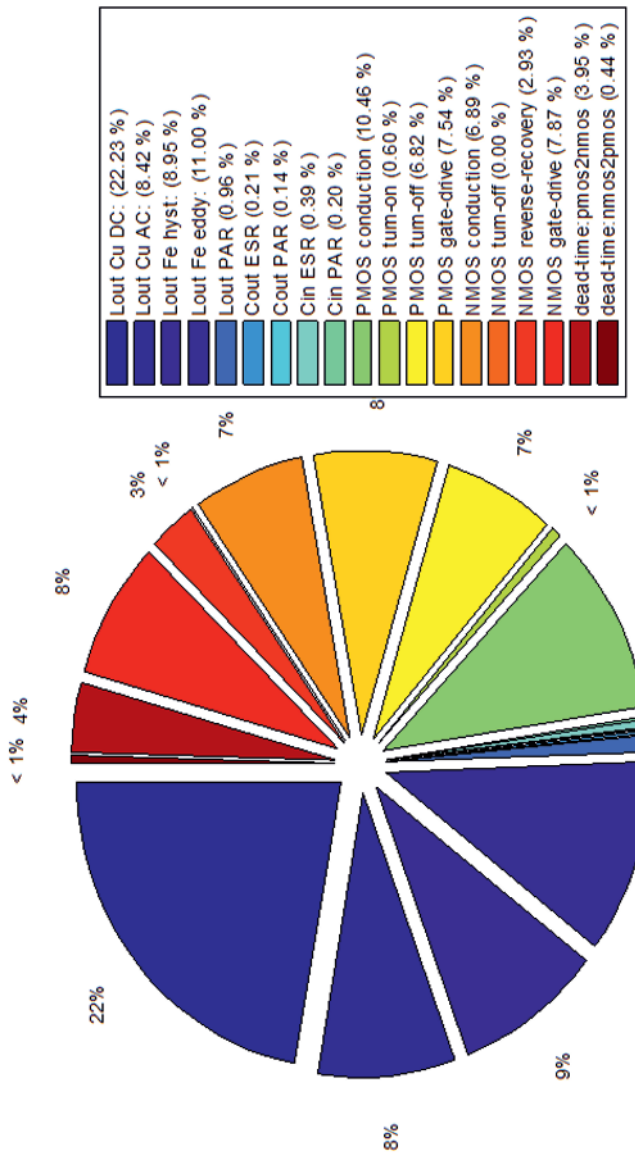

Figure 1.70. *Losses breakdown for the optimized buck converter at a typical load (270 mA) and a switching frequency of 12 MHz. Efficiency (77.5%). For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

It is also possible to analyze the impact on current designs if the technology of the power devices is improved by a factor of two (for a given semiconductor width, the conduction losses and the switching losses are divided by a factor of $\sqrt{2}$). It is interesting to analyze the case when ideal integrated magnetic inductors (without losses and occupying no space) are available but the rest of the components, Si devices and capacitors keep their current limitations. The impact on the efficiency is shown in Figure 1.71, where the efficiency of the converter is plotted against the switching frequency. In this plot, for each frequency, an optimized design is obtained (a single design is not evaluated as a function of the frequency).

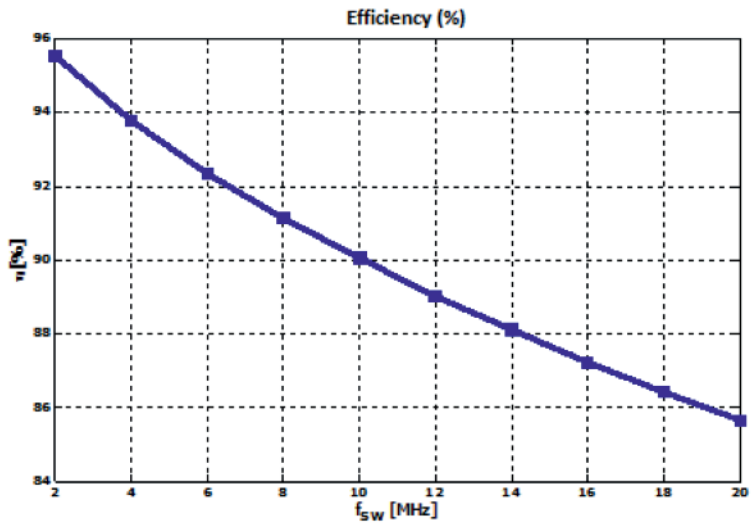

Figure 1.71. *Efficiency as a function of the switching frequency assuming ideal inductors (designs optimized at each switching frequency)*

It can be seen how the higher the frequency, the lower the efficiency as switching losses in the semiconductors increase proportionally with frequency. The result is that the better the technology of the magnetic components, the lower the switching frequency, which benefits the switching devices.

Another interesting analysis is to observe what will happen if silicon technology is improved by a factor of two, meaning that a device with the same width will have $\sqrt{2}$ lower conduction losses and $\sqrt{2}$ lower switching

losses under the same operating conditions. The results are shown in Figure 1.72, where the efficiency of the optimized designs, as a function of the switching frequency, for both Si technologies is shown. Two facts can be noted: first, the differences are lower at low frequency since the switching losses have a lower impact; second, although the improvement on the technology is significant (two times), the impact on the efficiency at 12 MHz, for example, is barely 2%.

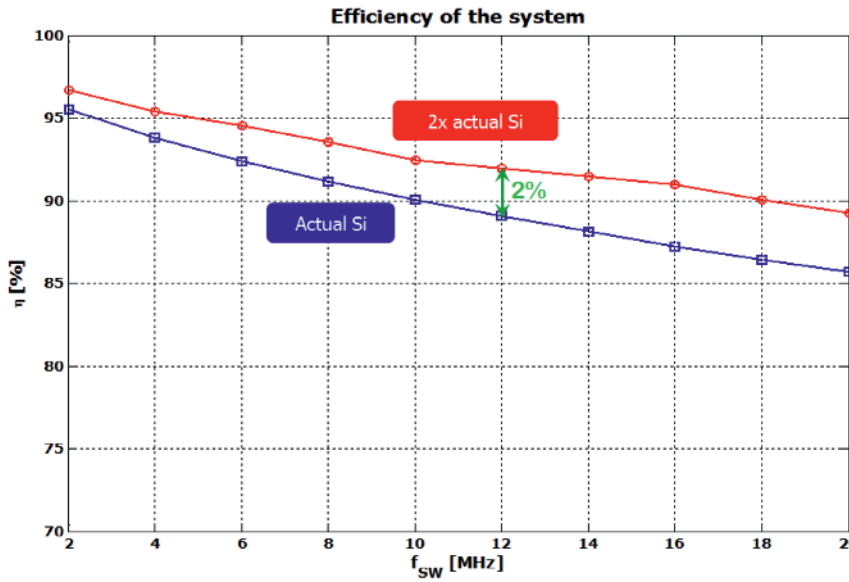

Figure 1.72. *Impact of improving Si technology by a factor of two on the efficiency: actual Si (blue), improved x2 Si (Red). For the color version of this figure, see www.iste.co.uk/allard/systems.zip*

Another interesting analysis is the impact of the integrated magnetic component technology with current Si devices shown in Figure 1.73. In the order of 10 MHz to 12 MHz, the current technology penalizes 5% of the efficiency of the converter with respect to an ideal integrated magnetic component. In this case, the comparison is not done with the same switches driving an ideal inductor and a real inductor; for each switching frequency, an optimized design with an ideal inductor and current inductor technology is carried out, so the semiconductor widths will not be the same.

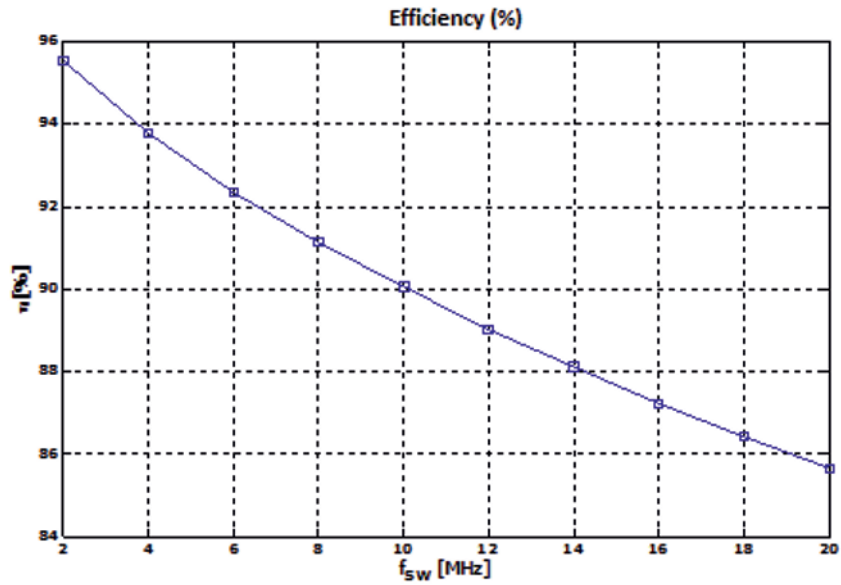

Figure 1.73. *Impact of inductor technology on efficiency: ideal inductor (blue), actual inductor technology (red)*

1.7. Conclusion

The previous section introduced the necessity for a high-level, global approach of design to decide for a trade-off between efficiency, quality of output DC energy and transient performances of a given converter architecture. Given a specification, multiple architectures may be considered and should be compared with major figures. The penalty in number of passive components and silicon area is a cursor the designer has to put somewhere in the design process but being aware of the cost on the trade-off quality.

Static metrics of the converter performances are generally put in the front at an early stage in the design process. This chapter attempted to emphasize the extreme importance of the control strategy. When more integration means higher switching frequency, it should not be forgotten that transient performances should improve as well.

This chapter has not discussed analogue versus digital implementation of controllers. Examples of both kinds are given in the following chapters.

Probably ripple-based control provides a new territory to analogue control as improved performances can be achieved using circuit complexity similar to that of the existing standard control approach. The last chapter of this book intends to show that the converter architecture complexity does not allow a choice and that digital control is the best candidate.