1

Fabrication of Nanowires

1.1. Introduction

Several fabrication processes of silicon nanowires have been developed in the research community. They can be divided into bottom-up or top-down approaches. The earliest reports of silicon nanowire fabrication often used bottom-up approaches (e.g. the vapor–liquid–solid (VLS) or similar mechanisms) to realize silicon nanowires. These methods are based on the fact that a seed particle on the silicon surface acts as a sink for the silicon atoms in the liquid phase and silicon nanowires grow out of the surface with the seed particle on the top. With these bottom-up approaches, it is relatively easy to realize nanowires at a low cost. However, one of the major drawbacks of these approaches is that the placement of the nanowires is determined by the position of the seed particle, and the exact position of the seed particle is difficult to precisely control. Also normally the bottom-up methods result in a random network of silicon nanowires on the silicon surface. Because of the random placement and the out-of-plane growth, it is not straightforward to integrate the bottom-up fabrication methods with the traditional approach used to manufacture electronics, such as complementary metal–oxide–semiconductor (CMOS) circuits, which relies on lithographic methods to transfer patterns into layers on a silicon wafer.

In the research community, the most common top-down technique to pattern sub-100 nm dimensions, needed for silicon nanowire fabrication, is electron beam lithography (EBL). With EBL, feature sizes below 100 nm are easy to achieve and patterns below 10 nm have been realized. There is no mask required since the method relies on the precision of an electron beam that is programmed to expose areas in a resist. This makes the method highly flexible and fast prototyping can be

Chapter written by Jens BOLTEN, Per-Erik HELLSTRÖM, Mikael ÖSTLING, Céline TERNON and Pauline SERRE.

made without the need for mask fabrication. The combination of being a maskless technique and having high resolution is the fundamental reason for the widespread use of EBL in the research community. The major drawback of this technique is that the writing process is serial in nature and thus extremely time-consuming. Therefore, wafer-scale fabrication is challenging with write times of several hours per wafer depending on the amount of features to be written.

With the overall goal of integrating silicon nanowires with CMOS circuits, a viable approach is to use conventional top-down techniques, used in CMOS manufacturing, to realize a vast amount of silicon nanowires on a silicon wafer. From a technological point of view, this is straightforward but a major challenge is to achieve a low-cost solution that is suitable for sensor applications. Conventional top-down optical patterning techniques, such as deep-ultraviolet (UV) and immersion deep-UV photolithography, are currently the industry standard for leading-edge semiconductor manufacturing. However, these techniques are extremely tool expensive (e.g. an immersion 193 nm wavelength tool with resolution less than 80 nm can cost more than € 15 m) and demand a high-volume application in order to be cost-effective. Generally, they are only accessible to large-scale integrated circuit manufacturers. For low-volume applications, conventional I-line (wavelength of 365 nm) optical stepper lithography is much less capital intensive with tool prices in the range of approximately € 0.2 m to € 0.3 m. However, I-line lithography tools can only print pattern resolutions of about 350 nm in the resist which is not adequate for pattern silicon nanowires with less than 100 nm feature sizes. With advanced techniques such as sidewall transfer lithography (STL), which is nowadays used by the semiconductor industry and referred to as self-aligned-double-patterning (SADP), it is possible to pattern deca-nanometer size silicon nanowires with I-line lithography and achieve high wafer scale throughput.

This chapter is organized as follows: section 1.2 describes top-down fabrication of silicon nanowires using EBL, which combined with optical lithography can be a viable approach if not too many silicon nanowires need to be patterned on a wafer. Section 1.3 describes the STL technique using I-line stepper lithography to pattern a vast amount of silicon nanowires on a silicon wafer. In section 1.4, we describe how bottom-up Si nanowires synthesized by VLS – CVD can be assembled at low cost in an efficient way for further use as a sensing material.

1.2. Silicon nanowire fabrication with electron beam lithography

1.2.1. *Key requirements*

As discussed above, one key route toward sensitive nanoscale sensor devices is the creation of large surface-to-volume ratio sensing areas. Hence, dense arrays of

nanowire structures with a high length-to-width ratio are favorable building blocks for such devices. In Figure 1.1, a semi-dense array of silicon nanowire features is presented as an example. It is obvious that the relatively high aspect ratio – the height of the features is roughly three times their width – significantly contributes to a large surface-to-volume ratio. These long quasi-one-dimensional nanowires have to be fabricated with good critical dimension (CD) control as well as low line edge and line width roughness (LER and LWR), which pose special challenges on the lithographic processes used to define these structures.

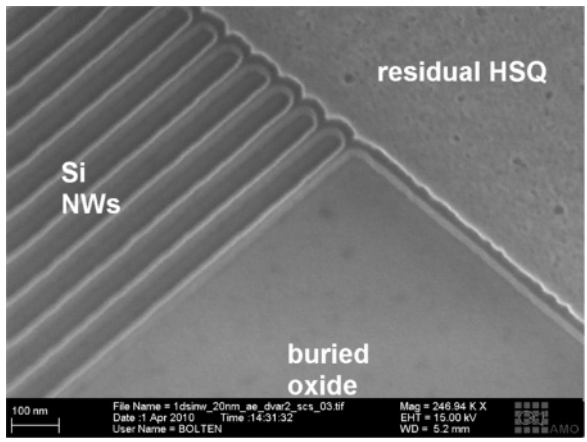


Figure 1.1. *Array of silicon nanowire features after dry etching and partial removal of residual HSQ resist*

Especially in a research and development (R&D) environment where the influence of design variations such as nanowire width, height, length and the number of parallel nanowires per device on device performance is investigated, it is crucial to guarantee a very high degree of control over CDs, LER and LWR.

1.2.2. *Why electron beam lithography?*

One lithographic technique which offers the high resolution needed for the fabrication of nanowire devices and which is capable of fulfilling the requirements discussed above is EBL.

Using EBL, silicon nanowires with widths of 10 nm and below can be fabricated as being comparably fast, flexible, efficient, reproducible and with good quality, as can be seen in Figure 1.2 where some parallel sub-10 nm features in 40 nm hydrogen silsesquioxane (HSQ) resist are shown.

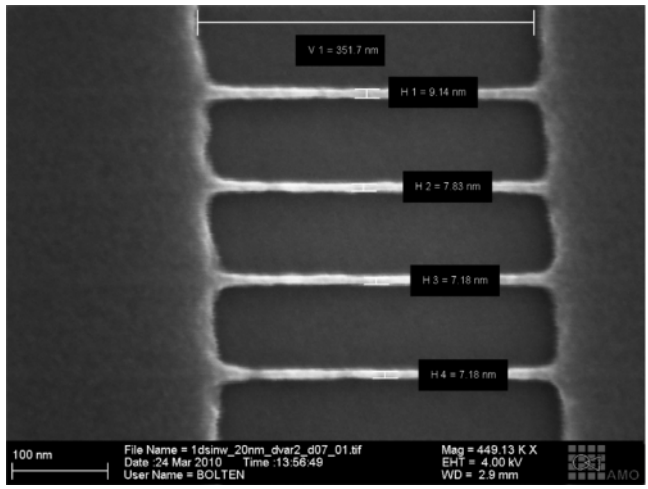


Figure 1.2. *Sub-10 nm lines in 40 nm HSQ resist, defined by EBL using a Vistec EBPG 5200 system operated at 100 kV*

Speed, flexibility and efficiency are mainly achieved due to the fact that EBL is a maskless lithographic technique, allowing the direct exposure of the design on a sample or wafer without the need to first fabricate a mask. This not only helps to reduce the time between design and a first exposure run dramatically – in an ideal scenario, the design can be exposed literally minutes after it has been finalized – but also offers the flexibility to routinely adapt the design if the first results suggest such changes without the cost of a new mask and the time delay of a mask fabrication. Hence, EBL is ideally suitable as a prototyping technique for novel device concepts such as nanoscale sensors. Furthermore, using the right tools, materials and processes, EBL offers resolution well below 10 nm at a quality level and with a reproducibility which can be hardly challenged by other lithographic techniques.

1.2.3. *Lithographic requirements*

For sensing devices, dense quasi-one-dimensional arrays of nanostructures fabricated with a high degree of CD control and low LER and LWR are needed. Translated into requirements for lithography, this means that:

– resist materials must offer smooth resist profiles;

– resist materials must offer resolution of 10 nm and better;

– resist masks must be suitable as a mask for dry etching;

– resist material and development processes need to offer high contrast to resolve dense nanowire features;

– the overall lithographic process must be robust enough to guarantee good CD control and a reasonable degree of reproducibility even for feature sizes of ~10 nm.

1.2.4. *Tools, resist materials and development processes*

When aiming to fulfill such demanding lithographic requirements as listed above, the choice of EBL tool is essential for the results that can be achieved. With EBL systems mainly based on a converted scanning electron microscope, such as the RAITH 150 line of EBL tools, the acceleration voltage limits the resolution for dense nanostructures at a given resist thickness due to forward scattering of the electrons within the resist layer. EBL systems like the Vistec EBPG series or the tools fabricated by JEOL offer acceleration voltages up to 100 kV, significantly reducing the forward scattering and hence increasing the achievable resolution for dense structures.

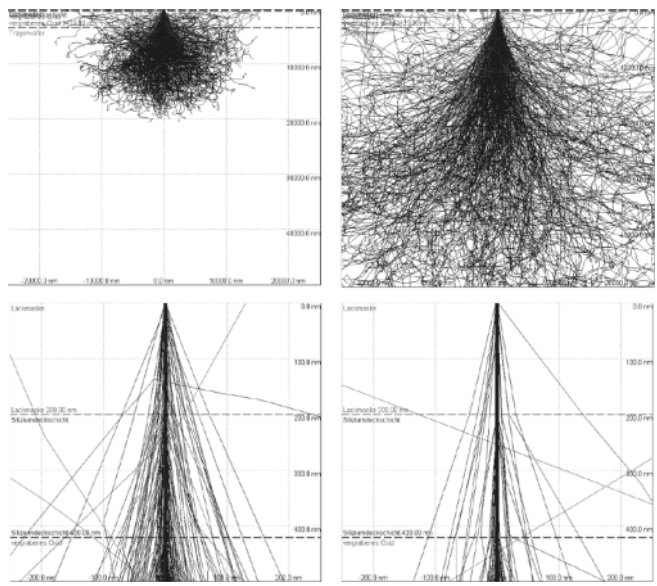


Figure 1.3. *Monte-Carlo simulations of electron scattering. Left-hand side images: 50 kV acceleration voltage; right-hand side image: 100 kV acceleration voltage. Top row: overview; bottom row: detailed view of resist layer, in this case 200 nm thick. For a color version of this figure, see www.iste.co.uk/balestra/nanodevice1.zip*

In Figure 1.3, this is demonstrated using trajectories of Monte-Carlo simulations for two acceleration voltages: 50 and 100 kV. It is clearly obvious that the forward scattering in the resist layer and the upper substrate stack layers is reduced with increasing acceleration voltage. At the same time, the higher acceleration voltage causes an increased backscattering.

Inorganic negative tone resist materials such as HSQ offer the potential to exploit the theoretically almost unlimited resolution of EBL. Such materials also yield smooth resist profiles and hence help to minimize LER and LWR. As the features have not just to be defined in a resist material but also need to be transferred into the substrate material via dry etching, the resist mask must have a sufficient thickness for this subsequent etching process; hence, resist masks with an initial thickness of less than 40–50 nm are not suitable for fabrication purposes.

In order to better use the potential of HSQ, a high contrast development process, either based on highly concentrated tetramethylammonium hydroxide (TMAH) developer solutions or developers that contain sodium hydroxide (NaOH) and sodium chloride (NaCl), is necessary. The latter are not compatible with standard CMOS processing environments but offer slightly better contrast; hence, higher resolution for dense features while TMAH is fully compatible with CMOS technology. Under optimized processing conditions feasible for a reliable fabrication of dense HSQ nanometer-scale features, the resolution which can reproducibly be achieved with TMAH is almost identical to the one demonstrated for NaOH/NaCl.

1.2.5. *Exposure strategies and proximity effect correction*

Another important aspect in the process of defining dense nanometer-scale structures by EBL is the choice of an appropriate exposure strategy and the application of an efficient proximity effect correction (PEC).

Regarding the exposure strategy, multipass grayscale exposure techniques, which basically divide the exposure into n sub-exposures with an exposure dose of roughly $1/n$ of the nominal exposure dose for the structure, can significantly reduce the LER and LWR. The slight misalignments between the sub-exposures lead to an increased overlap of the EBL exposure shots, stitching errors can be improved using overlaps between the sub-exposures and the effect of shot noise is reduced to the division of each shot into the sub-exposure shots. Especially for dense nanostructures a multipass exposure strategy with a reasonable number of sub-exposures does not significantly increase the overall exposure time, in contrast to what one might expect at first glance. Due to the nature of the design consisting of dense nanometer-scale features, low beam currents are used for such exposures.

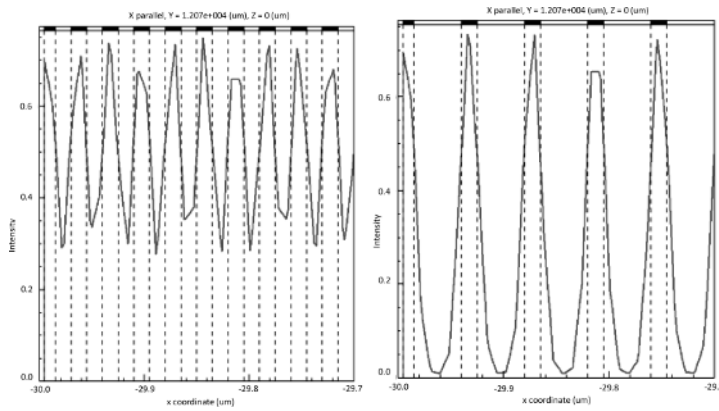
With a low beam current, the shot frequency is, for state-of-the-art EBL systems with maximum writing frequencies of 50 MHz and above, usually well below this maximum. Hence, a multipass exposure strategy can often be applied using the same exposure parameters such as beam step size and beam current, and it simply makes better use of the speed potential of the system. An increase in exposure time by applying such techniques is therefore mainly caused by the increase of stage movements, beam blanking operations and similar operations' contribution to the exposure overhead.

As shown in Figure 1.3, the use of a high acceleration voltage minimizes forward scattering at the cost of increased backscattering. While forward scattering directly reduces the achievable resolution, the influence of the backscattered electrons on the overall exposure result can be minimized by applying a PEC. The amount of dose contribution due to forward scattered and backscattered electrons for each part of a design is calculated and the primary exposure dose for each shot is carefully adjusted taking those additional dosage contributions into account. In addition to changing the exposure dose for each area of the design, it is also possible to apply slight changes to the design itself to compensate for the proximity dosage.

1.2.6. *Technology limitations and how to circumvent them*

Using state-of-the-art EBL systems and processes, nanostructures with feature sizes well below 10 nm can be realized with reasonable reproducibility and quality. Using HSQ and an initial resist thickness of ~40 nm, resist features significantly below 8 nm tend to collapse due to their mechanical instability caused by their high aspect ratio of 5 and above. Thinner resist layers are usually not suitable for pattern transfer into an silicon-on-insulator (SOI) substrate with a top silicon thickness of 50 nm. Using thinner, substrate material can be helpful to enable a further reduction of the resist thickness and hence the feature size. Employing standard CMOS-compatible processing techniques, features with widths less than ~30 nm can be realized as 1:1 line/space structures. To achieve a 1:1 line/space ration below 30 nm, either other, non-compatible developer solutions or special double exposure techniques need to be used.

One such approach has been developed and realized within the framework of the Nanofunction project. As shown in Figure 1.4, even after applying a fine-tuned PEC the modulation depth of the intensity profile of the exposure dose will quickly become insufficient to resolve ultra-dense features if feature size and feature spacing are reduced to 20 nm and below.



a) b)

Figure 1.4. *Simulated effective exposure intensity profile for 15 nm line/space structures. Gray line: intensity profile. Black and white boxes on top of plot and dashed lines: line/space regions and desired intensity profile. Simulated using the LayoutBEAMER software. a) Line/space ratio 1:1 and b) line/space ratio 1:3*

An efficient way to overcome this limitation is to utilize the excellent overlay accuracy offered by state-of-the-art EBL systems and to use a divide-and-conquer approach to replace the challenging task of fabricating such ultra-dense nanoscale features by the challenge of fabricating two sets of less densely packed but well-aligned nanowire features. This strategy is depicted in Figure 1.5. To create a line/space structure with 15 nm 1:1 features, the problem is divided into two exposures, each consisting of 15 nm wide line features with a 60 nm period, hence a 1:3 line/space ratio. As shown in Figure 1.4, such features can be easily defined. After the first exposure, shown in dark grey in Figure 1.5, the substrate is unloaded from the EBL system and developed. Subsequently, the substrate is recoated with resist and reloaded into the system, and the second exposure, shown in light gray, is performed after a very careful alignment of the substrate and with a fine-tuned dose to compensate effects caused by the existence of the first set of line features adjacent to the features that have to be defined during the second exposure.

The importance of a very precise control of the overlay between both sub-exposures can be seen in Figure 1.6, which shows the resulting line features for the case of a slight misalignment in the range of 5 nm between both exposures. The effect of the misalignment does not only effect the positioning of both sets of lines with respect to each other but also leads to a significant increase in LER and LWR as well as to areas where the resist is not completely removed between the lines.

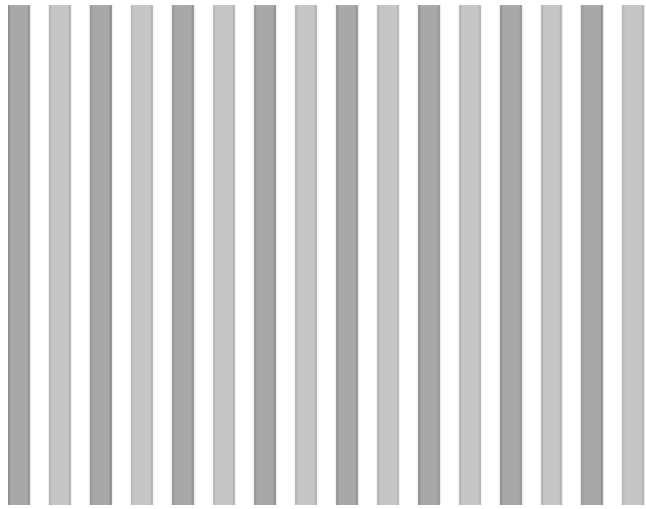


Figure 1.5. *Detail of the design of the exposed 15 nm half pitch grating. First exposure layer in dark gray and second layer in light gray*

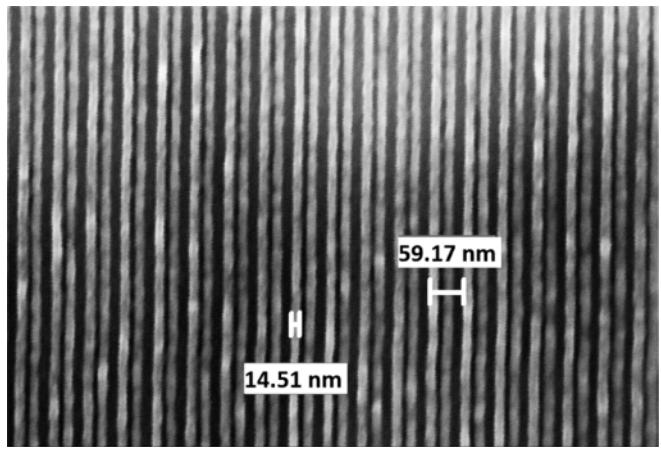


Figure 1.6. *Slightly misaligned 15 nm wide HSQ resist features*

If an alignment accuracy better than 5 nm can be achieved, no such effects occur and 20 nm and 15 nm 1:1 line/space ratio features can be defined using standard fully CMOS-compatible processing, as shown in Figure 1.7.

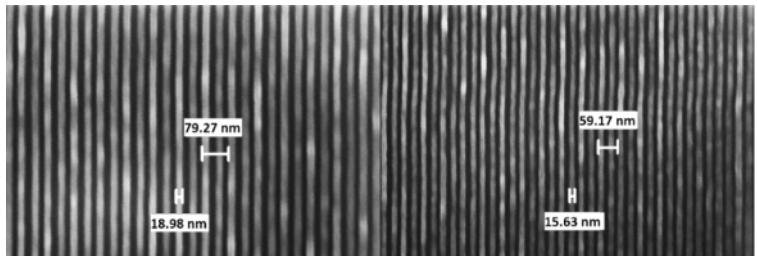


Figure 1.7. *Exposure result for dense nanoline structure in 40 nm HSQ resist. Left hand side: 20 nm half pitch, right hand side: 15 nm half pitch*

Dense nanowire features, defined in a 40 nm thick resist layer with excellent etching properties and hence being easily transferable to a substrate material by means of dry etching, can offer excellent surface-to-volume ratios and are, therefore, well suited for a large variety of sensing applications.

1.3. Silicon nanowire fabrication with sidewall transfer lithography

Optical stepper lithography is a top-down standard patterning technique developed for the semiconductor industry to print patterns in a resist layer over a full wafer scale with a high throughput of more than 50 wafers/h. Optical lithography is used to pattern the different layers in the fabrication of CMOS circuits and it is thus attractive to use the same optical lithography for fabrication of silicon nanowires. STL enables pattern lines of arbitrary small line width using conventional I-line lithography [CHO 02, HÅL 06]. The final silicon nanowire width is determined by the deposition and etching techniques rather than the resolution limit of the optical lithography. Figure 1.8 shows the STL method for patterning of silicon nanowires in the silicon layer of a silicon-on-insulator wafer. The basic principle is simple and straightforward; first deposition of a hard mask and a support material is followed by patterning of the support material. In this step, it is important to achieve vertical sidewalls of the support material with as low sidewall surface roughness as possible. Then a spacer material is deposited and etched back leaving the spacer material on the sidewall of the support material. The thickness of the spacer material will determine the final silicon nanowire width, hence the name STL. The key to achieving the final targeted nanowire width is that the deposition of the spacer material is conformal and that the etch-back is anisotropic. The support material is etched and a high selectivity to the spacer material and to the hard mask is mandatory. Finally, the hard mask is patterned by optical lithography and the spacer material together with the resist is used as masks to transfer the patterned to the underlying hard mask. After removal of the spacer material and the resist, a third mask can be used to cut part of the lines created in the hard mask if it is desirable.

This could be necessary if only one nanowire is desired since the first mask that creates an opening in the support material always creates a closed ring, and therefore without the third cut mask the formed nanowires will always be in a closed loop. The final step is to etch the silicon layer to form the silicon nanowires using the hard mask as a mask. The STL process can thus produce planar nanowires on wafer scale using conventional I-line optical lithography with three lithography masks and deposition and etching process technology.

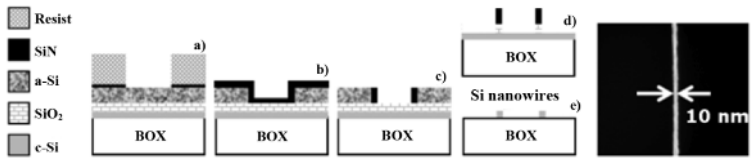


Figure 1.8. *Schematic of the STL process using SiO_2 hard mask, amorphous-Si as support layer, SiN as hard mask for etching the support layer and SiN as the spacer material. Silicon nanowires are formed in the silicon layer of a silicon-on-insulator wafer where BOX is the buried oxide. The top view SEM picture to the right shows a 10 nm wide silicon nanowire fabricated by STL with a line width roughness of 1.5 nm*

The STL process can be implemented with various material combinations. In the following, we describe a process using only common and compatible materials in a CMOS process technology such as SiO2, Si and SiN as depicted in Figure 1.8 [GUD 11]. SiO2 as a hard mask is attractive because reactive ion etching of Si using Cl2/HBr/O2 chemistry has a very high selectivity of >100:1 between Si and SiO2. The high selectivity allows the SiO2 hard mask to be relatively thin and still acts as a mask for Si etching. A thin hard mask is beneficial for the transfer of the narrow width spacer material into the hard mask. In STL, the line edge roughness is determined by the patterning of the support material and it is thus important to reduce the sidewall roughness of the resist and remove any resist residuals at the bottom of the resist, e.g. by a light O2 plasma ashing before patterning the support material. It is also important that the support material itself does not induce a sidewall roughness. Figure 1.9 depicts the sidewall surface roughness measured by atomic force microscope or microscopy (AFM) for different spacer materials. The relatively large grains of poly-SiGe inflict a high sidewall roughness [GUD 08] and it is thus preferable to use crystalline or rather amorphous support materials to minimize the sidewall roughness. An important aspect of an STL process with an amorphous support material is that the line edge roughness is determined by the sidewall roughness of the support material, and since the final silicon nanowire width is determined by the deposited thickness of the spacer material the roughness of the two silicon nanowire edges is correlated and it is actually possible to achieve lower line width roughness than the line edge roughness. This would not be possible using direct patterning of the resist since the two edges will be uncorrelated in that

case. In [GUD 11], it was demonstrated that silicon nanowires with line edge roughness of 3 nm and a line width roughness of less than 2 nm can be achieved using an amorphous Si spacer material. Using Si as support materials also allows the use of highly anisotropic Cl2/HBr/O2 reactive ion etching chemistry with high selectivity to both SiN (hard mask for amorphous Si etching) and the SiO2 hard mask under the support material. Furthermore, the Si support material can be wet stripped in TMAH with extreme selectivity toward SiO2 and SiN. Finally, the SiO2 hard mask should be etched using SiN spacers as a mask. This etch is a delicate step when implementing STL with the SiO2/Si/SiN material combination. Commonly used reactive ion etching with CHF3/CF4 chemistry only provides an etch rate of SiO2 a few times higher compared to SiN; so care must be taken not to erode the SiN spacer while etching SiO2 hard mask. There is a delicate trade-off in the SiO2 hard mask thickness given the targeted silicon nanowire width. A thicker SiO2 hard mask will cause more erosion of the SiN spacer and thus put a lower limit on how thin SiN spacer materials can be and therefore limit the minimum silicon nanowire width that can be achieved. A thinner SiO2 hard mask will allow for thinner SiN spacers to be used, therefore allowing for thinner silicon nanowire widths, but too thin an SiO2 hard mask will not work as a proper mask for the reactive ion etching of silicon. Especially, the first step in silicon etching employs a relatively low selectivity etch toward SiO2 in order to break through any native oxide on the silicon surface. The selectivity in the breakthrough etch sets a minimum thickness of the SiO2 hard mask. By a proper choice of materials and layer thicknesses together with conformal deposition and well-controlled reactive ion etching, the STL process can be fast and can achieve a high yield as indicated in Figure 1.10 where a top view of several 60 nm wide nanowires can be seen. The inset in Figure 1.10 is a SEM showing a single 60 nm wide silicon nanowire fabricated in the silicon layer of an SOI wafer.

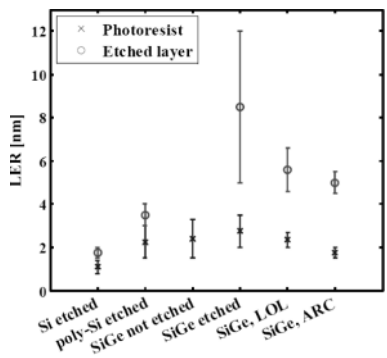


Figure 1.9. *Line edge roughness of etched spacer support materials. Polycrystalline materials exhibit a higher sidewall surface roughness after anisotropic etching. Polycrystalline SiGe support material has a line edge roughness more than 5 nm, and with silicon support material as low as 2 nm in line edge roughness can be achieved*

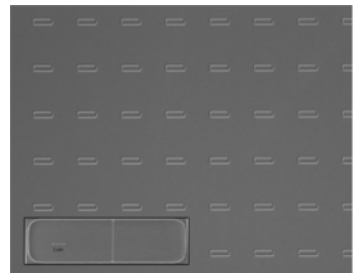


Figure 1.10. *Top view optical microscope picture showing 60 nm wide SiN spacer material fabricated using STL. In total, 48 out of 1,024 nanowires in a matrix are seen in the picture. More than 100 chips each with 1,024 nanowires were patterned on a single SOI wafer. The inset displays an individual Si nanowire after transfer into the Si layer*

1.4. Si nanonet fabrication

A nanostructured network (nanonet) is defined as a random network of high aspect ratio nanostructures (nanowires (NWs) or nanotubes (NTs)) [GRU 07, ZHA 12]. When its thickness is of the same order of magnitude than the length scale of its individual component, the nanonet is considered as three-dimensional (3D) because the percolation properties of such networks show 3D-typical characteristics. On the opposite, network that is significantly thinner will show two-dimensional (2D) percolation properties (see Chapter 3). Examples of such 2D and 3D nanonets are shown in Figure 1.11.

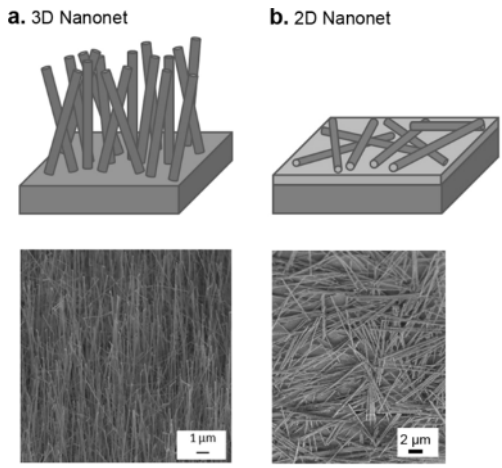


Figure 1.11. *3D nanonet: schematic representation and top-view SEM image of 3D Si nanonet a). 2D nanonet: schematic representation and top-view SEM image of 2D Si nanonet b)*

On the one hand, as explained in section 1.1, several drawbacks make the 3D nanonet integration more complex. On the other hand, and as described in detail in Chapter 2 (section 2.3), 2D nanonets have several unique properties which arise either from the individual components, the NWs or NTs, or from the structural properties of the network itself that facilitate the integration as a sensor.

In the literature, 2D nanonets are mainly fabricated by solution-based assembly of the NWs or NTs (e.g. spray coating [FER 04, KAE 05], Langmuir–Blodgett [ACH 06, PAR 08, TAO 03] and vacuum filtration [LI 06, WU 04]), which enables the fabrication of nanonets having a wide range of thicknesses, from sub-monolayer coverage to over 1 μm thickness. In the recent years, such nanonets based on carbon NTs have been studied and integrated into chemical and biological sensors that exhibit high sensitivity to gas or biological molecules [BYO 06, STA 05, WOO 07]. However, very little literature has been reported for Si nanonets.

Among the solution-based assembly methods for the nanonet fabrication, the vacuum filtration method is highly simple, versatile, low cost and scalable to large areas [DAL 08, DE 09, HU 04, MAD 10, WOO 07, WU 04]. The process itself guarantees the film homogeneity. The nanonets assembled by this method can be easily deposited at room temperature onto various types of substrates: transparent or opaque, conductor or insulating, flexible or rigid.

1.4.1. *Si NWs fabrication*

For this work, the silicon nanowires were grown on silicon <1 1 1> substrates by reduced pressure chemical vapor deposition (RP-CVD) using the Au-catalyzed VLS mechanism [WAG 64]. The growth was performed in a CVD furnace Easy TubeTM 3000 from first nano at 650°C under a pressure of 3 torr. Silane (SiH4) was used as the silicon precursor with flow of 40 sccm. Hydrogen chloride (HCl) was also added during the growth in order to inhibit the gold diffusion and the lateral growth [GEN 12, POT 11]. Phosphine (PH3) was added to dope the SiNWs with phosphorus.

The as-grown vertically standing SiNWs in the <1 1 1> direction (Figure 1.11a) are typically 10 μm in length with a diameter between 70 and 100 nm leading to an aspect ratio (length over diameter) above 100. Such an aspect ratio is necessary to favor the nanonet cohesion and the interconnection between the nanowires. Indeed, we experimentally demonstrated that in the case of too small an aspect ratio (around 10–20), the resulting network is inhomogeneous and of bad quality.

1.4.2. *Si nanonet assembling*

The 2D Si nanonets are assembled by the vacuum filtration method [SER 13]. First, silicon nanowires are dispersed in deionized water by ultrasonication for 5 min. Then, the nanowire solution is characterized by absorption spectroscopy using a Tecan Infinite 1000 in order to determine qualitatively the nanowire concentration in the solution. The absorbance scans are carried out from 230 to 1,000 nm with a 2 nm step to analyze the spectral properties of the nanowire solution. Further dilutions of the solution are done until its absorbance at 400 nm equal to 0.06. Thus, the nanowire amount in the solution can be reproducible from one solution to another even if the nanowire concentration is not quantitatively determined. After the dilution, the SiNW solution is filtered through a 0.1 μm porous nitrocellulose membrane (47 mm in diameter). As the solvent goes through the pores, the nanowires are trapped on the membrane surface forming subsequently an interconnected random network: the 2D Si nanonet (Figure 1.11(b)). Different volumes of SiNW solution are filtered in order to prepare thin networks of controllable thickness and density. Finally, the network is transferred onto various substrates by membrane dissolution due to a treatment with an acetone liquid bath for 30 min.

1.4.3. *Si nanonet morphology and properties*

Once the NW concentration in the solution is fixed by absorption intensity at 400 nm, the network density depends on the volume of the SiNW solution filtered as shown in Figure 1.12. Figures 1.12(a) and (b) display the SEM images of 2D Si nanonets with different NW density. We can notice the nanonet homogeneity that is in fact guaranteed by the filtration method. Indeed, when a network area on the membrane becomes thicker, the filtration speed in that region decreases although it increases in other regions that maintain the homogeneity. By analyzing the SEM images, the SiNW density on the surface is determined and it is shown in Figure 1.12(c) as a function of the volume of solution filtered for a given absorption intensity at 400 nm (0.06).

The observed linear dependence in Figure 1.12(c) demonstrates that the density of nanowires in the network can be monitored by simply controlling the volume of solution filtered through the membrane for a given absorbance at a specific wavelength.

In this condition (Absorbance 0.06 at 400 nm; volume 30–160 mL), each fabricated Si nanonet with density lower than 100×10^6 NW.cm^{-2} is, on the one hand, sufficiently thin to guarantee a good adhesion on the substrate even after

further immersions in solution for functionalization steps (see Chapter 2). On the other hand, such nanonets have been successfully deposited on numerous substrates: glass, polyethylene, silicon, silicon dioxide and silicon nitride over surfaces of around 1 cm^2.

Moreover, the so-assembled Si nanonets are well above the percolation threshold allowing conduction across the system: two-probe measurements at room temperature for most of these devices show non-linear, symmetric *I–V* characteristics with high current level despite the numerous inter-NW junctions in the network. Indeed, as described in Chapter 2 (Figure 2.9), even for the wider devices (1,000 µm) that contain several hundreds of NW–NW junctions per percolation path, the current is not negligible [TER 13].

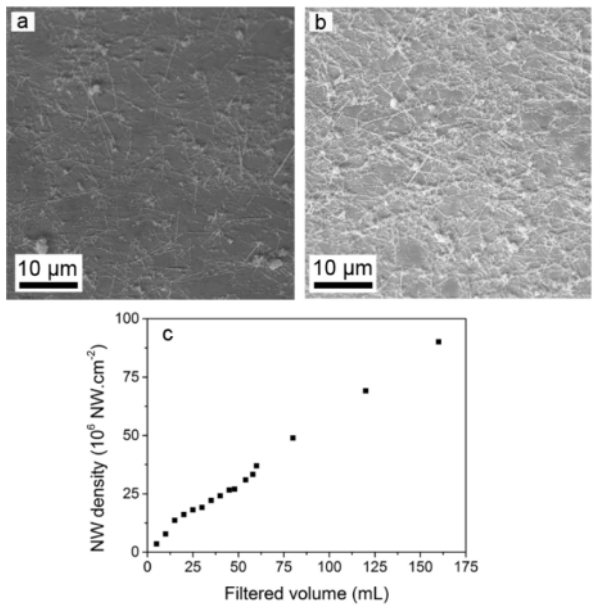


Figure 1.12. *Si nanonets assembled by the vacuum filtration method. SEM images of Si nanonets assembled using solution of same absorbance at 400 nm using different filtered volumes leading to different NW densities: a) 45 mL, 27 × 10^6 $NW.cm^{-2}$; b) 60 mL, 37 × 10^6 $NW.cm^{-2}$; c) SiNW density as a function of the SiNW solution volume for a given absorbance at 400 nm (0.06). The NW density is determined from SEM images of nanonets elaborated from different volume filtered of SiNW solution. For each volume studied, several images are analyzed at different locations on the nanonet leading to the mean density*

Considering the observed properties, including the precise control over NW density in the nanonet enabled by the filtration method, the enhanced specific area of these materials, the good adhesion on various substrates, the reproducibility and the very interesting electrical behavior, such 2D random networks are particularly well designed for integration into innovative gas- and biosensing devices with an improved sensitivity, using a low-cost fabrication method compatible with large-scale applications. As a result, the Si nanonets represent a bottom-up, low-cost alternative for the design of field-effect sensors that could be integrated above IC.

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