PRINCIPLES OF TESTING ELECTRONIC SYSTEMS

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A Wiley-Interscience Publication
JOHN WILEY & SONS, INC.
New York • Chichester • Weinheim • Brisbane • Singapore • Toronto

This book is printed on acid-free paper. ♾

Published simultaneously in Canada.

For ordering and customer service, call 1-800-CALL-WILEY.

Library of Congress Cataloging-in-Publication Data:

Mourad, Samiha.
Principles of testing electronic systems/Samiha Mourad, Yervant Zorian.
p. cm.
"A Wiley-Interscience publication."
Includes bibliographical references and index.
ISBN 0-471-31931-7
1. Electronic circuits—Testing. I. Zorian, Yervant. II. Title.
TK7867 .M697 2000
621.3815′48–dc21 99-052179

Printed in the United States of America

10 9 8 7 6 5 4 3 2 1

CONTENTS

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PREFACE

The challenge of testing electronic systems has grown rapidly over the last decade. This is due to the complexity of designing easily testable circuits. As the technology feature size decreases and designers keep increasing chip size, testing encounters difficult challenges. Along with this evolution in electronic systems, there is an evolution in design automation tools. Practically every phase of the design process is presently automated, including high-level synthesis. Earlier testability used to be considered only at the gate level. However, the complexity of present circuits and the advent of systems on a chip (SOCs) makes it mandatory to start considering testing early in the design process. All these factors pose many challenges to the design and test engineers. These challenges include, but are not limited to, development of more accurate failure modeling, examining testability on a higher level of design representation, and embedding more effective test constructs prior or during synthesis. Another major challenge to VLSI testing is the large volume of testing data that has to go through the IC.

The rapid change in technology and the growing need for efficient solutions to the problems encountered in design and test are still not matched with an increase in the number of qualified engineers to handle these tasks. Many practicing engineers are involved in testing and design for test, but they rarely have the opportunity to study the field in a systematic fashion. All their learning is mainly on the job. Although learning by doing is an acceptable mode of acquiring knowledge, it is much more productive if before being immersed in testing, these engineers are knowledgeable of its foundation. It is for these engineers that the book is mainly written. The major features of this book include:

- Relevant discussion throughout the book of where the test is situated in the design process
- Detailed discussion of issues related to scan path and ordering of scan chain registers
- Self-test methodologies for random logic and memories
- Test methodologies for RAM-based FPGAs
- Chapter on testing a system on chip

To have a good foundation in testing, one must understand five basic disciplines: (1) physical defects and their manifestation on the circuit level, (2) test pattern generation for detecting faults, (3) the relationship of testing to the design cycle, (4) design for test practice, and (5) testing the manufactured chip.

The first four disciplines are detailed in the book. The approach followed is not theoretical. The intent here is to sacrifice theoretical elegance in favor of a phenomenological understanding of the topic. For example, it is possible to use solely a mathematical basis to explain the D-algorithm for test pattern generation. However, a flowchart explanation of the algorithm is sufficient and more appropriate for its implementation in software tools. This pragmatic approach does not exclude giving the readers the opportunity to explore the theoretical foundation in depth. For this, the book includes a bibliography of specialized testing books, a list of magazines and archival journals, and a list of Web sites.

The book is organized into five main parts. Part I consists of four chapters. It is the road map for the book. From the onset it relates design and testing for obtaining reliable electronic products. Chapter 1 is an introduction to the objectives of the book in which we distinguish design verification from testing. Whereas design verification checks the compliance of the design to specifications, the intent of testing is to show that the design implementation on silicon is error-free. In this chapter we also briefly describe the preparation needed to test the final product and the processes and tools used in this preparation: test pattern generation and design to facilitate testability of the product.

Before detailing the topics presented in Chapter 1, it is important to know the causes of product failures. In Chapter 2 we provide a thorough description of the possible defects encountered in electronic products and explain the need for mapping these defects to faults on the structural and behavioral levels of the design. Most of the failures of an electronic product are due to manufacturing defects, but they may also be due to noise induced by operation of the product. Since the overwhelming majority of VLSI systems utilize CMOS, the emphasis will be on MOS technology.

Preparation for testing the product starts from its inception as a design idea. It is thus very important to learn how the design is represented at different stages of its life cycle. Toward this end, we present in Chapter 3 a taxonomy of design that is used to explain the various activities of the design cycle in Chapter 4. The automated design processes are known as synthesis and follow

algorithms that operate primarily on graphs. The knowledge gained in this part has a twofold benefit. First, it will facilitate the understanding of the following parts of the book. Second, it will mold a mind-set on why design and test can no longer be independent topics.

Part II comprises three chapters. Although much effort at present is put to use formal verification techniques in CAD tools, simulation is still the main vehicle for design verification. It plays an indispensable role in product design and testing. In addition, fault simulation helps in assessing the quality of the test pattern generated to test the products. In Chapter 5 we show how fault simulation evolved to facilitate the verification of today's very dense and large circuits.

In Chapter 6 we address what is known as deterministic test pattern generation. In general, test pattern generation relied on fault detection by measuring the voltage signal at the circuit outputs. Today, in addition to voltage measurement, current measurement is also used. This approach, which is known as I_{DDQ} testing, is possible only for CMOS circuits that constitute most present-day electronic circuits. In Chapter 7 we present current testing, which is very effective at uncovering many defects that voltage testing cannot detect. A new paradigm of *defect detection* is becoming very relevant and is utilized in addition to traditional fault detection. Moreover, current testing facilitates *defect diagnosis*.

In Part III we utilize the knowledge presented in the preceding seven chapters and pave the way to designs that facilitate testing. This part of the book consists of four chapters. In Chapter 8 we outline common sense approaches to DFT. As simple as they are, these ad hoc techniques can be very powerful. For example, a divide-and-conquer approach may make quite a difference in testing a product. The next three chapters cover structured techniques. In Chapter 9 we describe a way that helps reduce the complexity of mainly synchronous sequential circuits. Scan-path design is very widely used and is becoming a standard feature in electronic circuits. It has also been practiced on asynchronous circuits. Chapter 10 is on boundary-scan design, a technique initially thought to be used for printed circuit boards, which, however, is also becoming very useful for integrated circuits. This DFT technique follows IEEE Standard 1149.1 and is used for debugging and diagnosis. Chapter 11 is the last chapter in this part. Built-in self-test (BIST) technique is effectively applied to random logic. It is also used for memory testing, microprocessors, and FPGAs. After its principles are explained, its use in conjunction with scan design for random logic is also described.

In Part IV, which comprises two chapters, we investigate how testing is performed or applied to the ubiquitous RAMs, FPGAs, and microprocessors. Each of the three structures presented makes use of a functional fault model, since the use of structural fault models would make their testing untraceable. Testing based on the functional model also detects failures on the associated circuitry: decoding logic and the attached registers.

In Chapter 12 we investigate RAMs that have regular structures but are very dense and cause a whole set of problems in their testing. These problems are compounded when the RAM is embedded in logic chip or in a SOC. In Chapter 13 we address another two commonly used circuits. FPGAs come in different varieties, but the main interest here is in RAM-based ones. They also have regular array structures and are much less dense than RAMs. Their regular structure is exploited to make them C-testable. Microprocessors are some of the most used designs, but their testability is not explored sufficiently. Few models are used for testing microprocessors. Most embedded testability constructs, such as scan path and BIST, are widely used in microprocessor testing.

Part V is a synthesis of all the main topics covered in earlier chapters. As we advocated there, the design cycle should incorporate test preparation and design for testability constructs and be thought of as the design for a testability cycle. The two-pass approach that first completes the design then adds on these constructs and usually yields a lower-than-desirable circuit performance. Instead, a one-pass approach that includes the testability issues from the onset of the design cycle results in a circuit that is optimized for area, performance, and testability. In Chapter 14 we illustrate how constraints are placed on the synthesis process to achieve this one-pass approach. All knowledge acquired so far is utilized in Chapter 15. However, now additional problems are encountered, which are caused by embedding a variety of pre-designed blocks on the same IC. The volume of testing data increases but the throughput is still low. Testing SOCs is presenting a challenge to the testing community.

The presentation in the book combines the long teaching experience of one of the authors and the intensive industrial experience of the other author. In selecting and presenting the topics, we strove for a balance between the educational merits and the practical reality of testing.

ACKNOWLEDGMENTS

This book has been motivated and shaped by several friends, colleagues, and students. We are grateful to all of them and, in particular, Sunil Das, University of Toronto, Toronto, Canada; Yacoub M. EIZiq, SUN Microsystems, Menlo Park, California; F. Joel Ferguson, University of California at Santa Cruz, California; Suresh Gopalakrishnan, Cabeltron, Santa Clara, California; Daryl Hoot, Marvell, Sunnyvale, California; London Jin, Toshiba, Sunnyvale, California; Samy Makar, Transmeta, Santa Clara, California; Rafic Makki, University of North Carolina at Charlotte, North Carolina; Takashi Nanya, University of Tokyo, Tokyo, Japan; Kenneth P. Parker, Hewlett Packard, Fort Collins, Colorado; Prachi Sathe, Santa Clara University, Santa Clara, California; and A. J. van de Goor, Delft University of Technology, The Netherlands.

We also thank George Telecki and Cassie Craig for their helpful suggestions and their patience with our several delays in submitting the manuscript. The preparation of the manuscript would not have been possible without the help of

Martha Giannini, Mike Daly, and Amit Hakoo. The authors also acknowledge the benefits received from the comments of many Santa Clara students who used the first draft of this book. We are extremely grateful to everyone who contributed to our endeavor.

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