

HIGH-SPEED DIGITAL SYSTEM DESIGN

— |

| —

— |

| —

HIGH-SPEED DIGITAL SYSTEM DESIGN

A HANDBOOK OF INTERCONNECT
THEORY AND DESIGN PRACTICES

Stephen H. Hall
Garrett W. Hall
James A. McCall



A Wiley-Interscience Publication

JOHN WILEY & SONS, INC.

New York • Chichester • Weinheim • Brisbane • Singapore • Toronto

This book is printed on acid-free paper. ∞

Copyright © 2000 by John Wiley & Sons, Inc. All rights reserved.

Published simultaneously in Canada.

No part of this publication may be reproduced, stored in a retrieval system or transmitted in any form or by any means, electronic, mechanical, photocopying, recording, scanning or otherwise, except as permitted under Sections 107 or 108 of the 1976 United States Copyright Act, without either the prior written permission of the Publisher, or authorization through payment of the appropriate per-copy fee to the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923, (978) 750-8400, fax (978) 750-4744. Requests to the Publisher for permission should be addressed to the Permissions Department, John Wiley & Sons, Inc., 605 Third Avenue, New York, NY 10158-0012, (212) 850-6011, fax (212) 850-6008, E-Mail: PERMREQ@WILEY.COM.

For ordering and customer service, call 1-800-CALL-WILEY.

Library of Congress Cataloging-in-Publication Data:

Hall, Stephen H.

High-speed digital system design: a handbook of interconnect theory and design practices/Stephen H. Hall, Garrett W. Hall, James A. McCall p. cm.

ISBN 0-471-36090-2 (cloth)

1. Electronic digital computers—Design and construction. 2. Very high speed integrated circuits—Design and construction. 3. Microcomputers—Buses. 4. Computer interfaces. I. Hall, Garrett W. II. McCall, James A. III. Title.

TK7888.3 H315 2000
621.39'8—dc21

00-025717

Printed in the United States of America

10 9 8 7 6 5 4 3 2 1

CONTENTS

Preface	xi
1. The Importance of Interconnect Design	1
1.1 The Basics	2
1.2 The Past and the Future	4
2. Ideal Transmission Line Fundamentals	7
2.1 Transmission Line Structures on a PCB or MCM	7
2.2 Wave Propagation	8
2.3 Transmission Line Parameters	9
2.3.1 Characteristic Impedance	11
2.3.2 Propagation Velocity, Time, and Distance	14
2.3.3 Equivalent Circuit Models for SPICE Simulation	15
2.4 Launching Initial Wave and Transmission Line Reflections	18
2.4.1 Initial Wave	18
2.4.2 Multiple Reflections	19
2.4.3 Effect of Rise Time on Reflections	26
2.4.4 Reflections From Reactive Loads	28
2.4.5 Termination Schemes to Eliminate Reflections	32
2.5 Additional Examples	36
2.5.1 Problem	36
2.5.2 Goals	36
2.5.3 Calculating the Cross-Sectional Geometry of the PCB	37
2.5.4 Calculating the Propagation Delay	38
2.5.5 Determining the Wave Shape Seen at the Receiver	39
2.5.6 Creating an Equivalent Circuit	40
3. Crosstalk	42
3.1 Mutual Inductance and Mutual Capacitance	42
3.2 Inductance and Capacitance Matrix	43
3.3 Field Simulators	45
	v

3.4	Crosstalk-Induced Noise	45
3.5	Simulating Crosstalk Using Equivalent Circuit Models	51
3.6	Crosstalk-Induced Flight Time and Signal Integrity Variations	52
3.6.1	Effect of Switching Patterns on Transmission Line Performance	53
3.6.2	Simulating Traces in a Multiconductor System Using a Single-Line Equivalent Model	59
3.7	Crosstalk Trends	62
3.8	Termination of Odd- and Even-Mode Transmission Line Pairs	65
3.8.1	Pi Termination Network	65
3.8.2	T Termination Network	66
3.9	Minimization of Crosstalk	67
3.10	Additional Examples	68
3.10.1	Problem	69
3.10.2	Goals	70
3.10.3	Determining the Maximum Crosstalk-Induced Impedance and Velocity Swing	70
3.10.4	Determining if Crosstalk Will Induce False Triggers	72
4.	Nonideal Interconnect Issues	74
4.1	Transmission Line Losses	74
4.1.1	Conductor DC Losses	75
4.1.2	Dielectric DC Losses	75
4.1.3	Skin Effect	76
4.1.4	Frequency-Dependent Dielectric Losses	87
4.2	Variations in the Dielectric Constant	91
4.3	Serpentine Traces	92
4.4	Intersymbol Interference	95
4.5	Effects of 90° Bends	97
4.6	Effect of Topology	99
5.	Connectors, Packages, and Vias	102
5.1	Vias	102
5.2	Connectors	104
5.2.1	Series Inductance	104
5.2.2	Shunt Capacitance	105
5.2.3	Connector Crosstalk	105
5.2.4	Effects of Inductively Coupled Connector Pin Fields	106
5.2.5	EMI	109
5.2.6	Connector Design Guidelines	110

5.3	Chip Packages	112
5.3.1	Common Types of Packages	113
5.3.2	Creating a Package Model	117
5.3.3	Effects of a Package	121
5.3.4	Optimal Pin-Outs	127
6.	Nonideal Return Paths, Simultaneous Switching Noise, and Power Delivery	129
6.1	Nonideal Current Return Paths	129
6.1.1	Path of Least Inductance	129
6.1.2	Signals Traversing a Ground Gap	130
6.1.3	Signals That Change Reference Planes	134
6.1.4	Signals Referenced to a Power or a Ground Plane	135
6.1.5	Other Nonideal Return Path Scenarios	140
6.1.6	Differential Signals	140
6.2	Local Power Delivery Networks	141
6.2.1	Determining the Local Decoupling Requirements for High-Speed I/O	144
6.2.2	System-Level Power Delivery	147
6.2.3	Choosing a Decoupling Capacitor	149
6.2.4	Frequency Response of a Power Delivery System	150
6.3	SSO/SSN	151
6.3.1	Minimizing SSN	154
7.	Buffer Modeling	156
7.1	Types of Models	157
7.2	Basic CMOS Output Buffer	157
7.2.1	Basic Operation	157
7.2.2	Linear Modeling of the CMOS Buffer	164
7.2.3	Behavioral Modeling of the Basic CMOS Buffer	172
7.3	Output Buffers That Operate in the Saturation Region	175
7.4	Conclusions	177
8.	Digital Timing Analysis	178
8.1	Common-Clock Timing	178
8.1.1	Common-Clock Timing Equations	180
8.2	Source Synchronous Timing	183
8.2.1	Source Synchronous Timing Equations	186
8.2.2	Deriving Source Synchronous Timing Equations from an Eye Diagram	189
8.2.3	Alternative Source Synchronous Schemes	191

8.3	Alternative Bus Signaling Techniques	192
8.3.1	Incident Clocking	192
8.3.2	Embedded Clock	192
9.	Design Methodologies	194
9.1	Timings	195
9.1.1	Worst-Case Timing Spreadsheet	196
9.1.2	Statistical Spreadsheets	198
9.2	Timing Metrics, Signal Quality Metrics, and Test Loads	200
9.2.1	Voltage Reference Uncertainty	200
9.2.2	Simulation Reference Loads	202
9.2.3	Flight Time	206
9.2.4	Flight-Time Skew	207
9.2.5	Signal Integrity	209
9.3	Design Optimization	210
9.3.1	Paper Analysis	211
9.3.2	Routing Study	212
9.4	Sensitivity Analysis	215
9.4.1	Initial Trend and Significance Analysis	215
9.4.2	Ordered Parameter Sweeps	221
9.4.3	Phase 1 Solution Space	224
9.4.4	Phase 2 Solution Space	225
9.4.5	Phase 3 Solution Space	228
9.5	Design Guidelines	229
9.6	Extraction	230
9.7	General Rules of Thumb to Follow When Designing a System	230
10.	Radiated Emissions Compliance and System Noise Minimization	232
10.1	FCC Radiated Emission Specifications	233
10.2	Physical Mechanisms of Radiation	233
10.2.1	Differential-Mode Radiation	234
10.2.2	Common-Mode Radiation	241
10.2.3	Wave Impedance	245
10.3	Decoupling and Choking	246
10.3.1	High-Frequency Decoupling at the System Level	248
10.3.2	Choking Cables and Localized Power and Ground Planes	253
10.3.3	Low-Frequency Decoupling and Ground Isolation	261
10.4	Additional PCB Design Criteria, Package Considerations, and Pin-Outs	263
10.4.1	Placement of High-Speed Components and Traces	263

10.4.2	Crosstalk	263
10.4.3	Pin Assignments and Package Choice	264
10.5	Enclosure (Chassis) Considerations	265
10.5.1	Shielding Basics	265
10.5.2	Apertures	267
10.5.3	Resonances	272
10.6	Spread Spectrum Clocking	273
11.	High-Speed Measurement Techniques	276
11.1	Digital Oscilloscopes	276
11.1.1	Bandwidth	277
11.1.2	Sampling	278
11.1.3	Other Effects	281
11.1.4	Statistics	283
11.2	Time-Domain Reflectometry	283
11.2.1	TDR Theory	284
11.2.2	Measurement Factors	287
11.3	TDR Accuracy	289
11.3.1	Launch Parasitics	290
11.3.2	Probe Types	292
11.3.3	Reflections	293
11.3.4	Interface Transmission Loss	293
11.3.5	Cable Loss	294
11.3.6	Amplitude Offset Error	294
11.4	Impedance Measurement	295
11.4.1	Accurate Characterization of Impedance	295
11.4.2	Measurement Region in TDR Impedance Profile	297
11.5	Odd- and Even-Mode Impedance	299
11.6	Crosstalk Noise	299
11.7	Propagation Velocity	300
11.7.1	Length Difference Method	301
11.7.2	Y-Intercept Method	301
11.7.3	TDT Method	302
11.8	Vector Network Analyzer	303
11.8.1	Introduction to S Parameters	304
11.8.2	Equipment	305
11.8.3	One-Port Measurements (Z_O, L, C)	305
11.8.4	Two-Port Measurements (T_d , Attenuation, Crosstalk)	310
11.8.5	Calibration	314
11.8.6	Calibration for One-Port Measurements	315
11.8.7	Calibration for Two-Port Measurements	316
11.8.8	Calibration Verification	316

Appendix A: Alternative Characteristic Impedance Formulas	318
A.1 Microstrip	318
A.2 Symmetric Stripline	319
A.3 Offset Stripline	319
Appendix B: GTL Current-Mode Analysis	321
B.1 Basic GTL Operation	321
B.2 GTL Transitions When a Middle Agent Is Driving	323
B.3 GTL Transitions When an End Agent With a Termination Is Driving	325
B.4 Transitions When There is a Pull-Up at the Middle Agent	327
Appendix C: Frequency-Domain Components in a Digital Signal	329
Appendix D: Useful S-Parameter Conversions	332
D.1 $ABCD$, Z , and Y Parameters	332
D.2 Normalizing the S Matrix to a Different Characteristic Impedance	335
D.3 Derivation of the Formulas Used to Extract the Mutual Inductance and Capacitance from a Short Structure Using S_{21} Measurements	336
D.4 Derivation of the Formula to Extract Skin Effect Resistance from a Transmission Line	337
Appendix E: Definition of the Decibel	338
Appendix F: FCC Emission Limits	340
Bibliography	342
Index	345

PREFACE

This book covers the practical and theoretical aspects necessary to design modern high-speed digital systems at the platform level. The book walks the reader through every required concept, from basic transmission line theory to digital timing analysis, high-speed measurement techniques, as well as many other topics. In doing so, a unique balance between theory and practical applications is achieved that will allow the reader not only to understand the nature of the problem, but also provide practical guidance to the solution. The level of theoretical understanding is such that the reader will be equipped to see beyond the immediate practical application and solve problems not contained within these pages. Much of the information in this book has not been needed in past digital designs but is absolutely necessary today. Most of the information covered here is not covered in standard college curricula, at least not in its focus on digital design, which is arguably one of the most significant industries in electrical engineering.

The focus of this book is on the design of robust high-volume, high-speed digital products such as computer systems, with particular attention paid to computer busses. However, the theory presented is applicable to any high-speed digital system. All of the techniques covered in this book have been applied in industry to actual digital products that have been successfully produced and sold in high volume.

Practicing engineers and graduate and undergraduate students who have completed basic electromagnetic or microwave design classes are equipped to fully comprehend the theory presented in this book. At a practical level, however, basic circuit theory is all the background required to apply the formulas in this book.

Chapter 1 describes why it is important to comprehend the lessons taught in this book. (Authored by Garrett Hall)

Chapter 2 introduces basic transmission line theory and terminology with specific digital focus. This chapter forms the basis of much of the material that follow. (Authored by Stephen Hall)

Chapters 3 and 4 introduce crosstalk effects, explain their relevance to digital timings, and explore nonideal transmission line effects. (Authored by Stephen Hall)

Chapter 5 explains the impact of chip packages, vias, connectors, and many other aspects that affect the performance of a digital system. (Authored by Stephen Hall)

Chapter 6 explains elusive effects such as simultaneous switching noise and nonideal current return path distortions that can devastate a digital design if not properly accounted for. (Authored by Stephen Hall)

Chapter 7 discusses different methods that can be used to model the output buffers that are used to drive digital signals onto a bus. (Authored by Garrett Hall)

Chapter 8 explains in detail several methods of system level digital timing. It describes the theory behind different timing schemes and relates them to the high-speed digital effects described throughout the book. (Authored by Stephen Hall)

Chapter 9 addresses one of the most far-reaching challenges that is likely to be encountered: handling the very large number of variables affecting a system and reducing them to a manageable methodology. This chapter explains how to make an intractable problem tractable. It introduces a specific design methodology that has been used to produce very high performance digital products. (Authored by Stephen Hall)

Chapter 10 covers the subject of radiated emissions, which causes great fear in the hearts of system designers because radiated emission problems usually cannot be addressed until a prototype has been built, at which time changes can be very costly and time-constrained. (Authored by Garrett Hall)

Chapter 11 covers the practical aspects of making precision measurements in high-speed digital systems. (Authored by James McCall)

Acknowledgments

Many people have contributed directly or indirectly to this book. We have been fortunate to keep the company of excellent engineers and fine peers. Among the direct, knowing contributors to this book are:

Dr. Maynard Falconer, Intel Corporation

Mike Degerstrom, Mayo Foundation, Special Purpose Processor Development Group

Dr. Jason Mix, Intel Corporation

Dorothy Hall, PHI Incorporated

We would also like to recognize the following people for their continuing collaboration over the years, which have undoubtedly affected the outcome of this book. They have our thanks.

Howard Heck, Intel Corporation; Oregon Graduate Institute

Michael Leddige, Intel Corporation

Dr. Tim Schreyer, Intel Corporation

Harry Skinner, Intel Corporation

Alex Levin, Intel Corporation

Rich Melitz, Intel Corporation

Wayne Walters, Mayo Foundation, Special Purpose Processor Development Group

Pat Zabinski, Mayo Foundation, Special Purpose Processor Development Group

Dr. Barry Gilbert, Mayo Foundation, Special Purpose Processor Development Group

Dr. Melinda Picket-May, Colorado State University

Special thanks are also given to Jodi Hall, Stephen's wife, without whose patience and support this book would not have been possible.

— |

| —

— |

| —