Nodal and Loop Analysis Techniques

3

In Chapter 2 we analyzed the simplest possible circuits, those containing only a single-node pair or a single loop. We found that these circuits can be completely analyzed via a single algebraic equation. In the case of the single-node-pair circuit (i.e., one containing two nodes, one of which is a reference node), once the node voltage is known, we can calculate all the currents. In a single-loop circuit, once the loop current is known, we can calculate all the voltages.

In this chapter we extend our capabilities in a systematic manner so that we can calculate all currents and voltages in circuits that contain multiple nodes and loops. Our analyses are based primarily on two laws with which we are already familiar: Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL). In a nodal analysis we employ KCL to determine the node voltages, and in a loop analysis we use KVL to determine the loop currents.

We present and discuss a very important commercially available circuit known as the operational amplifier, or op-amp. Op-amps are used in literally thousands of applications, including such things as compact disk (CD) players, random access memories (RAMs), analog-to-digital (A/D) and digital-to-analog (D/A) converters, headphone amplifiers, and electronic instrumentation of all types. Finally, we discuss the terminal characteristics of this circuit and demonstrate its use in practical applications as well as circuit design.

LEARNING Goals

3.1 Nodal Analysis An analysis technique in which one node in an *N*-node network is selected as the reference node and Kirchhoff's current law is applied at the remaining $N - 1$ nonreference nodes. The resulting $N - 1$ linearly independent simultaneous equations are written in terms of the $N - 1$ unknown node voltages. The solution of the $N - 1$ linearly independent equations yields the $N - 1$ unknown node voltages, which in turn can be used with Ohm's law to find all currents in the circuit...*Page 62*

3.2 Loop Analysis An analysis technique in which Kirchhoff's voltage law is applied to a network containing *N* independent loops. A loop current is assigned to each independent loop, and the application of KVL to each loop yields a set of *N* independent simultaneous equations in the *N* unknown loop currents. The solution of these equations yields the *N* unknown loop currents, which in turn can be used with Ohm's law to find all voltages in the circuit...*Page 76*

3.3 Circuits with Operational Amplifiers The operational amplifier, or op-amp as it is commonly known, is an extremely important electronic circuit. Its characteristics are high input resistance, low output resistance, and very high gain. It is used in a wide range of electronic circuits...*Page 83*

3.1 Nodal Analysis

In a nodal analysis the variables in the circuit are selected to be the node voltages. The node voltages are defined with respect to a common point in the circuit. One node is selected as the reference node, and all other node voltages are defined with respect to that node. Quite often this node is the one to which the largest number of branches are connected. It is commonly called *ground* because it is said to be at ground-zero potential, and it sometimes represents the chassis or ground line in a practical circuit.

We will select our variables as being positive with respect to the reference node. If one or more of the node voltages are actually negative with respect to the reference node, the analysis will indicate it.

In order to understand the value of knowing all the node voltages in a network, we consider once again the network in Fig. 2.30, which is redrawn in Fig. 3.1. The voltages, V_S, V_a, V_b, and V_c, are all measured with respect to the bottom node, which is selected as the reference and labeled with the ground symbol ⏚. Therefore, the voltage at node 1 is $V_S = 12$ V with respect to the reference node 5; the voltage at node 2 is $V_a = 3$ V with respect to the reference node 5, and so on. Now note carefully that once these node voltages are known, we can immediately calculate any branch current or the power supplied or absorbed by any element, since we know the voltage across every element in the network. For example, the voltage V_1 across the left-most 9-kΩ resistor is the difference in potential between the two ends of the resistor; that is,

$$\begin{aligned} V_1 &= V_S - V_a \\ &= 12 - 3 \\ &= 9 \text{ V} \end{aligned}$$

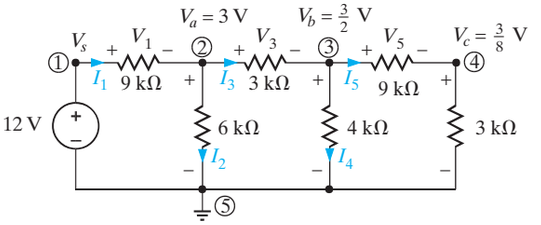


Figure 3.1
Circuit with known node voltages.

This equation is really nothing more than an application of KVL around the left-most loop; that is,

$$-V_S + V_1 + V_a = 0$$

In a similar manner, we find that

$$V_3 = V_a - V_b$$

and

$$V_5 = V_b - V_c$$

Then the currents in the resistors are

$$I_1 = \frac{V_1}{9\text{k}} = \frac{V_S - V_a}{9\text{k}}$$

$$I_3 = \frac{V_3}{3\text{k}} = \frac{V_a - V_b}{3\text{k}}$$

$$I_5 = \frac{V_5}{9\text{k}} = \frac{V_b - V_c}{9\text{k}}$$

In addition,

$$I_2 = \frac{V_a - 0}{6\text{k}}$$
$$I_4 = \frac{V_b - 0}{4\text{k}}$$

since the reference node 5 is at zero potential.

Thus, as a general rule, if we know the node voltages in a circuit, we can calculate the current through any resistive element using Ohm's law; that is,

$$i = \frac{v_m - v_N}{R} \qquad \textbf{3.1}$$

as illustrated in Fig. 3.2.

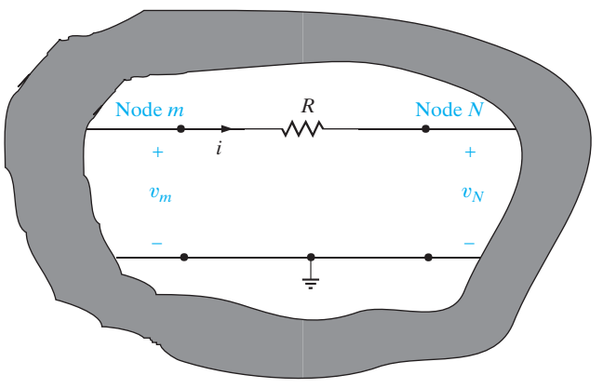


Figure 3.2
Circuit used to illustrate Ohm's law in a multiple-node network.

In Example 2.3 we illustrated that the number of linearly independent KCL equations for an N-node network was $N - 1$. Furthermore, we found that in a two-node circuit, in which one node was the reference node, only one equation was required to solve for the unknown node voltage. What is illustrated in this simple case is true in general; that is, in an N-node circuit one linearly independent KCL equation is written for each of the $N - 1$ nonreference nodes, and this set of $N - 1$ linearly independent simultaneous equations, when solved, will yield the $N - 1$ unknown node voltages.

It is instructive to treat nodal analysis by examining several different types of circuits and illustrating the salient features of each. We begin with the simplest case. However, as a prelude to our discussion of the details of nodal analysis, experience indicates that it is worthwhile to digress for a moment to ensure that the concept of node voltage is clearly understood.

At the outset it is important to specify a reference. For example, to state that the voltage at node A is 12 V means nothing unless we provide the reference point; that is, the voltage at node A is 12 V with respect to what. The circuit in Fig. 3.3 illustrates a portion of a network containing three nodes, one of which is the reference node.

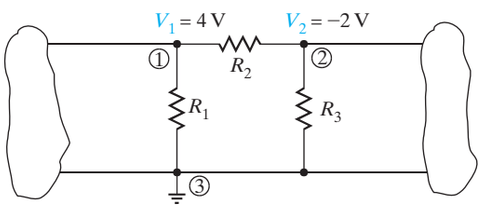


Figure 3.3
An illustration of node voltages.

The voltage $V_1 = 4$ V is the voltage at node 1 with respect to the reference node 3. Similarly, the voltage $V_2 = -2$ V is the voltage at node 2 with respect to node 3. In addition, however, the voltage at node 1 with respect to node 2 is +6 V and the voltage at node 2 with respect to node 1 is −6 V. Furthermore, since the current will flow from the node of higher potential to the node of lower potential, the current in R_1 is from top to bottom, the current in R_2 is from left to right, and the current in R_3 is from bottom to top.

These concepts have important ramifications in our daily lives. If a man were hanging in midair with one hand on one line and one hand on another and the dc line voltage of each line was exactly the same, the voltage across his heart would be zero and he would be safe. If, however, he let go of one line and let his feet touch the ground, the dc line voltage would then exist from his hand to his foot with his heart in the middle. He would probably be dead the instant his foot hit the ground.

In the town where I live, a young man tried to retrieve his parakeet that had escaped its cage and was outside sitting on a power line. He stood on a metal ladder and with a metal pole reached for the parakeet; when the metal pole touched the power line, the man was killed instantly. Electric power is vital to our standard of living, but it is also very dangerous. The material in this book *does not* qualify you to handle it safely. Therefore, always be extremely careful around electric circuits.

Now as we begin our discussion of nodal analysis, our approach will be to begin with simple cases and proceed in a systematic manner to those that are more challenging. Numerous examples will be the vehicle used to demonstrate each facet of this approach. Finally, at the end of this section, we will outline a strategy for attacking any circuit using nodal analysis.

CIRCUITS CONTAINING ONLY INDEPENDENT CURRENT SOURCES

Consider the network shown in Fig. 3.4. There are three nodes, and the bottom node is selected as the reference node. The branch currents are assumed to flow in the directions indicated in the figures. If one or more of the branch currents are actually flowing in a direction opposite to that assumed, the analysis will simply produce a branch current that is negative.

Applying KCL at node 1 yields

$$-i_A + i_1 + i_2 = 0$$

LEARNING Hint

Employing the passive sign convention.

Using Ohm's law ($i = Gv$) and noting that the reference node is at zero potential, we obtain

$$-i_A + G_1(v_1 - 0) + G_2(v_1 - v_2) = 0$$

or

$$(G_1 + G_2)v_1 - G_2v_2 = i_A$$

KCL at node 2 yields

$$-i_2 + i_B + i_3 = 0$$

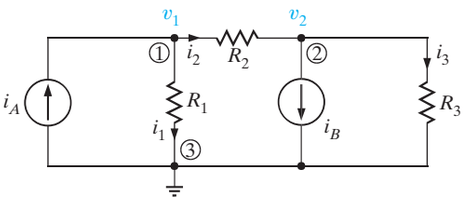


Figure 3.4
A three-node circuit.

or

$$-G_2(v_1 - v_2) + i_B + G_3(v_2 - 0) = 0$$

which can be expressed as

$$-G_2 v_1 + (G_2 + G_3)v_2 = -i_B$$

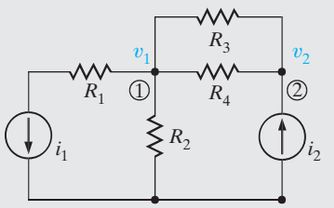
Therefore, the two equations for the two unknown node voltages v_1 and v_2 are

$$\begin{aligned}(G_1 + G_2)v_1 - G_2 v_2 &= i_A \\ -G_2 v_1 + (G_2 + G_3)v_2 &= -i_B\end{aligned} \qquad \textbf{3.2}$$

Note that the analysis has produced two simultaneous equations in the unknowns v_1 and v_2. They can be solved using any convenient technique, and modern calculators and personal computers are very efficient tools for their application.

LEARNING by Doing

D 3.1 For the following network, write the KCL equations for nodes 1 and 2.



ANSWER

$$i_1 + \frac{v_1}{R_2} + \frac{v_1 - v_2}{R_3} + \frac{v_1 - v_2}{R_4} = 0$$

$$i_2 + \frac{v_1 - v_2}{R_3} + \frac{v_1 - v_2}{R_4} = 0$$

In what follows, we will demonstrate three techniques for solving linearly independent simultaneous equations: Gaussian elimination, matrix analysis, and the MATLAB mathematical software package. A brief refresher that illustrates the use of both Gaussian elimination and matrix analysis in the solution of these equations is provided in the Problem-Solving Companion for this text. The use of the MATLAB software is straightforward, and we will demonstrate its use as we encounter the application.

The KCL equations at nodes 1 and 2 produced two linearly independent simultaneous equations:

$$-i_A + i_1 + i_2 = 0$$

$$-i_2 + i_B + i_3 = 0$$

The KCL equation for the third node (reference) is

$$+i_A - i_1 - i_B - i_3 = 0$$

Note that if we add the first two equations, we obtain the third. Furthermore, any two of the equations can be used to derive the remaining equation. Therefore, in this $N = 3$ node circuit, only $N - 1 = 2$ of the equations are linearly independent and required to determine the $N - 1 = 2$ unknown node voltages.

Note that a nodal analysis employs KCL in conjunction with Ohm's law. Once the direction of the branch currents has been *assumed*, then Ohm's law, as illustrated by Fig. 3.2 and expressed by Eq. (3.1), is used to express the branch currents in terms of the unknown node voltages. We can assume the currents to be in any direction. However, once we assume a particular direction, we must be very careful to write the currents correctly in terms of the node voltages using Ohm's law.

LEARNING Example 3.1

Suppose that the network in Fig. 3.4 has the following parameters: $I_A = 1$ mA, $R_1 = 12$ kΩ, $R_2 = 6$ kΩ, $I_B = 4$ mA, and $R_3 = 6$ kΩ. Let us determine all node voltages and branch currents.

SOLUTION For purposes of illustration we will solve this problem using Gaussian elimination, matrix analysis, and MATLAB. Using the parameter values Eq. (3.2) becomes

$$V_1\left[\frac{1}{12\text{k}} + \frac{1}{6\text{k}}\right] - V_2\left[\frac{1}{6\text{k}}\right] = 1 \times 10^{-3}$$

$$-V_1\left[\frac{1}{6\text{k}}\right] + V_2\left[\frac{1}{6\text{k}} + \frac{1}{6\text{k}}\right] = -4 \times 10^{-3}$$

where we employ capital letters because the voltages are constant. The equations can be written as

$$\frac{V_1}{4\text{k}} - \frac{V_2}{6\text{k}} = 1 \times 10^{-3}$$

$$-\frac{V_1}{6\text{k}} + \frac{V_2}{3\text{k}} = -4 \times 10^{-3}$$

Using Gaussian elimination, we solve the first equation for V_1 in terms of V_2:

$$V_1 = V_2\left(\frac{2}{3}\right) + 4$$

This value is then substituted into the second equation to yield

$$\frac{-1}{6\text{k}}\left(\frac{2}{3}V_2 + 4\right) + \frac{V_2}{3\text{k}} = -4 \times 10^{-3}$$

or

$$V_2 = -15 \text{ V}$$

This value for V_2 is now substituted back into the equation for V_1 in terms of V_2, which yields

$$V_1 = \frac{2}{3}V_2 + 4$$

$$= -6 \text{ V}$$

The circuit equations can also be solved using matrix analysis. The general form of the matrix equation is

$$\mathbf{GV} = \mathbf{I}$$

where in this case

$$\mathbf{G} = \begin{bmatrix} \frac{1}{4\text{k}} & -\frac{1}{6\text{k}} \\ -\frac{1}{6\text{k}} & \frac{1}{3\text{k}} \end{bmatrix}, \mathbf{V} = \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \text{ and } \mathbf{I} = \begin{bmatrix} 1 \times 10^{-3} \\ -4 \times 10^{-3} \end{bmatrix}$$

The solution to the matrix equation is

$$\mathbf{V} = \mathbf{G}^{-1}\mathbf{I}$$

and therefore,

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} \frac{1}{4\text{k}} & \frac{-1}{6\text{k}} \\ \frac{-1}{6\text{k}} & \frac{1}{3\text{k}} \end{bmatrix}^{-1} \begin{bmatrix} 1 \times 10^{-3} \\ -4 \times 10^{-3} \end{bmatrix}$$

To calculate the inverse of **G**, we need the adjoint and the determinant. The adjoint is

$$\text{Adj } \mathbf{G} = \begin{bmatrix} \frac{1}{3\text{k}} & \frac{1}{6\text{k}} \\ \frac{1}{6\text{k}} & \frac{1}{4\text{k}} \end{bmatrix}$$

and the determinant is

$$|\mathbf{G}| = \left(\frac{1}{3\text{k}}\right)\left(\frac{1}{4\text{k}}\right) - \left(\frac{-1}{6\text{k}}\right)\left(\frac{-1}{6\text{k}}\right)$$

$$= \frac{1}{18\text{k}^2}$$

Therefore,

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = 18\text{k}^2 \begin{bmatrix} \frac{1}{3\text{k}} & \frac{1}{6\text{k}} \\ \frac{1}{6\text{k}} & \frac{1}{4\text{k}} \end{bmatrix} \begin{bmatrix} 1 \times 10^{-3} \\ -4 \times 10^{-3} \end{bmatrix}$$

$$= 18\text{k}^2 \begin{bmatrix} \frac{1}{3\text{k}^2} - \frac{4}{6\text{k}^2} \\ \frac{1}{6\text{k}^2} - \frac{1}{\text{k}^2} \end{bmatrix}$$

$$= \begin{bmatrix} -6 \\ -15 \end{bmatrix}$$

The MATLAB solution begins with the set of equations expressed in matrix form as

```
G*V=I
```

where the symbol * denotes the multiplication of the voltage vector **V** by the coefficient matrix **G**. Then once the MATLAB software is loaded into the PC, the coefficient matrix **(G)** and the vector **V** can be expressed in MATLAB notation by typing in the rows of the matrix or vector at the prompt >>. Use semicolons to separate rows and spaces to separate columns. Brackets are used to denote vectors or matrices. When the matrix **G** and the vector **I** have been defined, then the solution equation

```
V=inv(G)*I
```

which is also typed in at the prompt >>, will yield the unknown vector **V.**

The matrix equation for our circuit expressed in decimal notation is

$$\begin{bmatrix} 0.00025 & -0.00016666 \\ -0.00016666 & 0.0003333 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 0.001 \\ -0.004 \end{bmatrix}$$

If we now input the coefficient matrix **G**, then the vector **I** and finally the equation V = inv(G)*I, the computer screen containing these data and the solution vector **V** appears as follows:

```
>> G = [0.00025 -0.000166666;
-0.000166666 0.000333333]
   G =
        1.0e-003 *
        0.2500      -0.1667
       -0.1667       0.3333
>> I = [0.001 ; -0.004]
   I =
        0.0010
       -0.0040
>> V = inv(G)*I
   V =
       -6.0001
      -15.0002
```

Knowing the node voltages, we can determine all the currents using Ohm's law:

$$I_1 = \frac{V_1}{R_1} = \frac{-6}{12\text{k}} = -\frac{1}{2}\,\text{mA}$$

$$I_2 = \frac{V_1 - V_2}{6\text{k}} = \frac{-6 - (-15)}{6\text{k}} = \frac{3}{2}\,\text{mA}$$

and

$$I_3 = \frac{V_2}{6\text{k}} = \frac{-15}{6\text{k}} = -\frac{5}{2}\,\text{mA}$$

Figure 3.5 illustrates the results of all the calculations. Note that KCL is satisfied at every node.

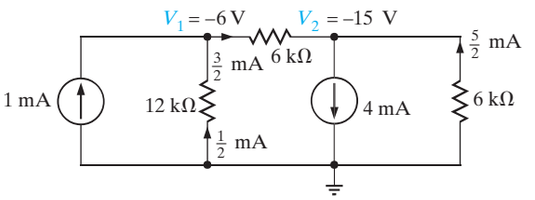


Figure 3.5 *Circuit used in Example 3.1.*

Let us now examine the circuit in Fig. 3.6. The current directions are assumed as shown in the figure.

At node 1, KCL yields

$$i_1 - i_A + i_2 - i_3 = 0$$

or

$$\frac{v_1}{R_1} - i_A + \frac{v_1 - v_2}{R_2} - \frac{v_3 - v_1}{R_3} = 0$$

$$v_1\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) - v_2\frac{1}{R_2} - v_3\frac{1}{R_3} = i_A$$

At node 2, KCL yields

$$-i_2 + i_4 - i_5 = 0$$

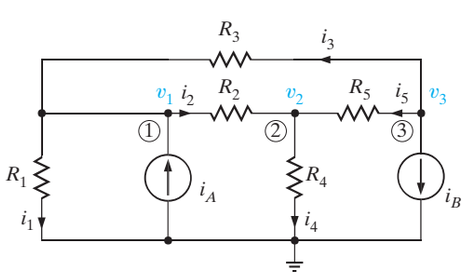


Figure 3.6
A four-node circuit.

or

$$-\frac{v_1 - v_2}{R_2} + \frac{v_2}{R_4} - \frac{v_3 - v_2}{R_5} = 0$$

$$-v_1\frac{1}{R_2} + v_2\left(\frac{1}{R_2} + \frac{1}{R_4} + \frac{1}{R_5}\right) - v_3\frac{1}{R_5} = 0$$

At node 3, the equation is

$$i_3 + i_5 + i_B = 0$$

or

$$\frac{v_3 - v_1}{R_3} + \frac{v_3 - v_2}{R_5} + i_B = 0$$

$$-v_1\frac{1}{R_3} - v_2\frac{1}{R_5} + v_3\left(\frac{1}{R_3} + \frac{1}{R_5}\right) = -i_B$$

Grouping the node equations together, we obtain

$$\begin{aligned} v_1\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) - v_2\frac{1}{R_2} - v_3\frac{1}{R_3} &= i_A \\ -v_1\frac{1}{R_2} + v_2\left(\frac{1}{R_2} + \frac{1}{R_4} + \frac{1}{R_5}\right) - v_3\frac{1}{R_5} &= 0 \\ -v_1\frac{1}{R_3} - v_2\frac{1}{R_5} + v_3\left(\frac{1}{R_3} + \frac{1}{R_5}\right) &= -i_B \end{aligned} \qquad \textbf{3.3}$$

Note that our analysis has produced three simultaneous equations in the three unknown node voltages v_1, v_2, and v_3. The equations can also be written in matrix form as

$$\begin{bmatrix} \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} & -\frac{1}{R_2} & -\frac{1}{R_3} \\ -\frac{1}{R_2} & \frac{1}{R_2} + \frac{1}{R_4} + \frac{1}{R_5} & -\frac{1}{R_5} \\ -\frac{1}{R_3} & -\frac{1}{R_5} & \frac{1}{R_3} + \frac{1}{R_5} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} i_A \\ 0 \\ -i_B \end{bmatrix} \qquad \textbf{3.4}$$

At this point it is important that we note the symmetrical form of the equations that describe the two previous networks. Equations (3.2) and (3.3) exhibit the same type of symmetrical form. The **G** matrix for each network is a symmetrical matrix. This symmetry is not accidental. The node equations for networks containing only resistors and independent current sources can always be written in this symmetrical form. We can take advantage of this fact and learn to write the equations by inspection. Note in the first equation of (3.2) that the coefficient of v_1 is the sum of all the conductances connected to node 1 and the coefficient of v_2 is the negative of the conductances connected between node 1 and node 2. The right-hand side of the equation is the sum of the currents entering node 1 through current sources. This equation is KCL at node 1. In the second equation in (3.2), the coefficient of v_2 is the sum of all the conductances connected to node 2, the coefficient of v_1 is the negative of the conductance connected between node 2 and node 1, and the right-hand side of the equation is the sum of the currents entering node 2 through current sources. This equation is KCL at node 2. Similarly, in the first equation in (3.3) the coefficient of v_1 is the sum of the conductances connected to node 1, the coefficient of v_2 is the negative of the conductance connected between node 1 and node 2, the coefficient of v_3 is the negative of the conductance connected between node 1 and node 3, and the right-hand side of the equation is the sum of the currents entering node 1 through current sources. The other

two equations in (3.3) are obtained in a similar manner. In general, if KCL is applied to node j with node voltage v_j, the coefficient of v_j is the sum of all the conductances connected to node j and the coefficients of the other node voltages (e.g., v_{j-1}, v_{j+1}) are the negative of the sum of the conductances connected directly between these nodes and node j. The right-hand side of the equation is equal to the sum of the currents entering the node via current sources. Therefore, the left-hand side of the equation represents the sum of the currents leaving node j and the right-hand side of the equation represents the currents entering node j.

LEARNING Example 3.2

Let us apply what we have just learned to write the equations for the network in Fig. 3.7 by inspection. Then given the following parameters, we will determine the node voltages using MATLAB: $R_1 = R_2 = 2\ \text{k}\Omega$, $R_3 = R_4 = 4\ \text{k}\Omega$, $R_5 = 1\ \text{k}\Omega$, $i_A = 4$ mA, and $i_B = 2$ mA.

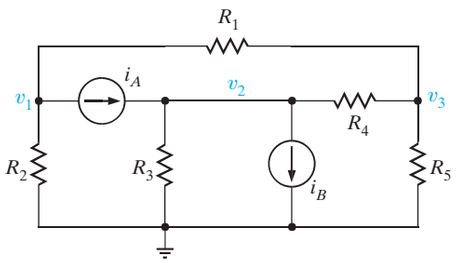


Figure 3.7 *Circuit used in Example 3.2.*

SOLUTION The equations are

$$v_1\left(\frac{1}{R_1}+\frac{1}{R_2}\right) - v_2(0) - v_3\left(\frac{1}{R_1}\right) = -i_A$$

$$-v_1(0) + v_2\left(\frac{1}{R_3}+\frac{1}{R_4}\right) - v_3\left(\frac{1}{R_4}\right) = i_A - i_B$$

$$-v_1\left(\frac{1}{R_1}\right) - v_2\left(\frac{1}{R_4}\right) + v_3\left(\frac{1}{R_1}+\frac{1}{R_4}+\frac{1}{R_5}\right) = 0$$

which can also be written directly in matrix form as

$$\begin{bmatrix} \frac{1}{R_1}+\frac{1}{R_2} & 0 & -\frac{1}{R_1} \\ 0 & \frac{1}{R_3}+\frac{1}{R_4} & -\frac{1}{R_4} \\ -\frac{1}{R_1} & -\frac{1}{R_4} & \frac{1}{R_1}+\frac{1}{R_4}+\frac{1}{R_5} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} -i_A \\ i_A - i_B \\ 0 \end{bmatrix}$$

Both the equations and the **G** matrix exhibit the symmetry that will always be present in circuits that contain only resistors and current sources.

If the component values are now used, the matrix equation becomes

$$\begin{bmatrix} \frac{1}{2\text{k}}+\frac{1}{2\text{k}} & 0 & -\frac{1}{2\text{k}} \\ 0 & \frac{1}{4\text{k}}+\frac{1}{4\text{k}} & -\frac{1}{4\text{k}} \\ -\frac{1}{2\text{k}} & -\frac{1}{4\text{k}} & \frac{1}{2\text{k}}+\frac{1}{4\text{k}}+\frac{1}{1\text{k}} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} -0.004 \\ 0.002 \\ 0 \end{bmatrix}$$

or

$$\begin{bmatrix} 0.001 & 0 & -0.0005 \\ 0 & 0.0005 & -0.00025 \\ -0.0005 & -0.00025 & 0.00175 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} -0.004 \\ 0.002 \\ 0 \end{bmatrix}$$

If we now employ these data with the MATLAB software, the computer screen containing the data and the results of the MATLAB analysis is as shown next.

```
>> G = [0.001 0 -0.0005 ; 0 0.0005
-0.00025 ; -0.0005 -0.00025 0.00175]

   G =

       0.0010            0   -0.0005
            0       0.0005   -0.0003
      -0.0005      -0.0003    0.0018

>> I = [-0.004 ; 0.002 ; 0]

   I =

      -0.0040
       0.0020
            0

>> V = inv(G)*I

   V =

      -4.3636
       3.6364
      -0.7273
```

LEARNING EXTENSIONS

E3.1 Write the node equations for the circuit in Fig. E3.1.

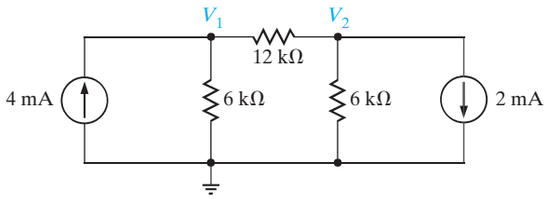


Figure E3.1

ANSWER

$$\frac{1}{4\text{k}}V_1 - \frac{1}{12\text{k}}V_2 = 4 \times 10^{-3},$$
$$\frac{-1}{12\text{k}}V_1 + \frac{1}{4\text{k}}V_2 = -2 \times 10^{-3}.$$

E3.2 Find all the node voltages in the network in Fig. E3.2 using MATLAB.

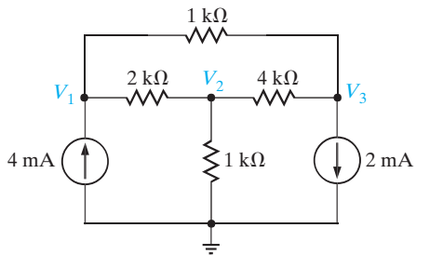


Figure E3.2

ANSWER $V_1 = 5.4286$ V, $V_2 = 2.000$ V, $V_3 = 3.1429$ V.

CIRCUITS CONTAINING DEPENDENT CURRENT SOURCES The presence of a dependent source may destroy the symmetrical form of the nodal equations that define the circuit. Consider the circuit shown in Fig. 3.8, which contains a current-controlled current source. The KCL equations for the nonreference nodes are

$$\beta i_o + \frac{v_1}{R_1} + \frac{v_1 - v_2}{R_2} = 0$$

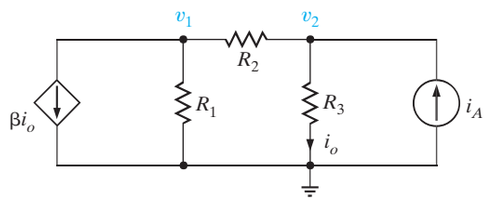


Figure 3.8
Circuit with a dependent source.

and

$$\frac{v_2 - v_1}{R_2} + i_o - i_A = 0$$

where $i_o = v_2/R_3$. Simplifying the equations, we obtain

$$(G_1 + G_2)v_1 - (G_2 - \beta G_3)v_2 = 0$$
$$-G_2 v_1 + (G_2 + G_3)v_2 = i_A$$

or in matrix form

$$\begin{bmatrix} (G_1 + G_2) & -(G_2 - \beta G_3) \\ -G_2 & (G_2 + G_3) \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 0 \\ i_A \end{bmatrix}$$

Note that the presence of the dependent source has destroyed the symmetrical nature of the node equation.

LEARNING Example 3.3

Let us determine the node voltages for the network in Fig. 3.8 given the following parameters:

$$\beta = 2 \qquad R_2 = 6\ \text{k}\Omega \qquad i_A = 2\ \text{mA}$$
$$R_1 = 12\ \text{k}\Omega \qquad R_3 = 3\ \text{k}\Omega$$

SOLUTION Using these values with the equations for the network yields

$$\frac{1}{4\text{k}} V_1 + \frac{1}{2\text{k}} V_2 = 0$$

$$-\frac{1}{6\text{k}} V_1 + \frac{1}{2\text{k}} V_2 = 2 \times 10^{-3}$$

Solving these equations using any convenient method yields $V_1 = -24/5$ V and $V_2 = 12/5$ V. We can check these answers by determining the branch currents in the network and then using that information to test KCL at the nodes. For example, the current from top to bottom through R_3 is

$$I_o = \frac{V_2}{R_3} = \frac{12/5}{3\text{k}} = \frac{4}{5\text{k}}\ \text{A}$$

Similarly, the current from right to left through R_2 is

$$I_2 = \frac{V_2 - V_1}{R_2} = \frac{12/5 - (-24/5)}{6\text{k}} = \frac{6}{5\text{k}}\ \text{A}$$

All the results are shown in Fig. 3.9. Note that KCL is satisfied at every node.

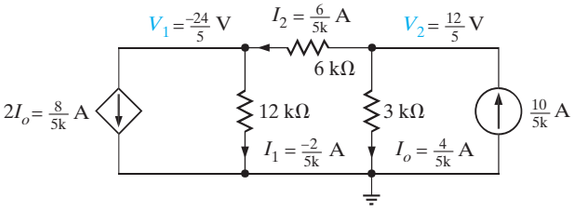


Figure 3.9 *Circuit used in Example 3.3.*

LEARNING Example 3.4

Let us determine the set of linearly independent equations that when solved will yield the node voltages in the network in Fig. 3.10. Then given the following component values, we will compute the node voltages using MATLAB: $R_1 = 1\ \text{k}\Omega$, $R_2 = R_3 = 2\ \text{k}\Omega$, $R_4 = 4\ \text{k}\Omega$, $i_A = 2$ mA, $i_B = 4$ mA, and $\alpha = 2$.

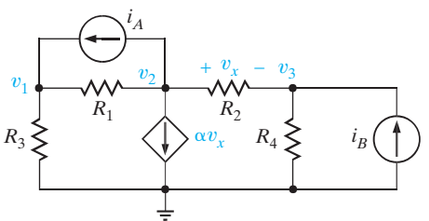


Figure 3.10 *Circuit containing a voltage-controlled current source.*

SOLUTION Applying KCL at each of the nonreference nodes yields the equations

$$G_3 v_1 + G_1(v_1 - v_2) - i_A = 0$$
$$i_A + G_1(v_2 - v_1) + \alpha v_x + G_2(v_2 - v_3) = 0$$
$$G_2(v_3 - v_2) + G_4 v_3 - i_B = 0$$

where $v_x = v_2 - v_3$. Simplifying these equations, we obtain

$$(G_1 + G_3)v_1 - G_1 v_2 = i_A$$
$$-G_1 v_1 + (G_1 + \alpha + G_2)v_2 - (\alpha + G_2)v_3 = -i_A$$
$$-G_2 v_2 + (G_2 + G_4)v_3 = i_B$$

Given the component values, the equations become

$$\begin{bmatrix} \frac{1}{1\text{k}} + \frac{1}{2\text{k}} & -\frac{1}{\text{k}} & 0 \\ -\frac{1}{\text{k}} & \frac{1}{\text{k}} + 2 + \frac{1}{2\text{k}} & -\left(2 + \frac{1}{2\text{k}}\right) \\ 0 & -\frac{1}{2\text{k}} & \frac{1}{2\text{k}} + \frac{1}{4\text{k}} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} 0.002 \\ -0.002 \\ 0.004 \end{bmatrix}$$

or

$$\begin{bmatrix} 0.0015 & -0.001 & 0 \\ -0.001 & 2.0015 & -2.0005 \\ 0 & -0.0005 & 0.00075 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} 0.002 \\ -0.002 \\ 0.004 \end{bmatrix}$$

The MATLAB input and output listings are shown next.

```
>> G = [0.0015 -0.001 0 ; -0.001
2.0015 -2.0005 ; 0 -0.0005 0.00075]

   G =

    0.0015   -0.0010         0
   -0.0010    2.0015   -2.0005
         0   -0.0005    0.0008
```

```
>> I = [0.002 ; -0.002 ; 0.004]
   I =
       0.0020
      -0.0020
       0.0040
```

```
>> V = inv(G)*I
   V =
      11.9940
      15.9910
      15.9940
```

LEARNING EXTENSIONS

E3.3 Find the node voltages in the circuit in Fig. E3.3.

ANSWER $V_1 = 16$ V, $V_2 = -8$ V.

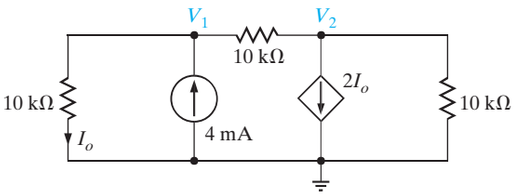


Figure E3.3

E3.4 Find the voltages V_o in the network in Fig. E3.4.

ANSWER $V_o = 4$ V.

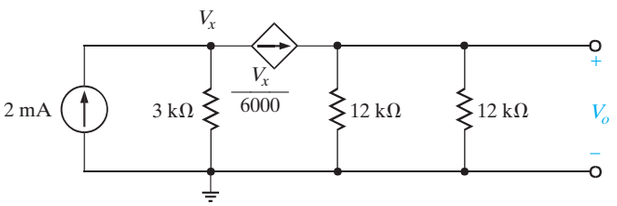


Figure E3.4

CIRCUITS CONTAINING INDEPENDENT VOLTAGE SOURCES As is our practice, in our discussion of this topic we will proceed from the simplest case to those that are more complicated. The simplest case is that in which an independent voltage source is connected to the reference node. The following example illustrates this case.

LEARNING Example 3.5

Consider the circuit shown in Fig. 3.11a. Let us determine all node voltages and branch currents.

SOLUTION This network has three nonreference nodes with labeled node voltages V_1, V_2, and V_3. Based on our previous discussions, we would assume that in order to find all the node voltages we would need to write a KCL equation at each of the nonreference nodes. The resulting three linearly independent simultaneous equations would produce the unknown node voltages. However, note that V_1 and V_3 are known quantities because an independent voltage source is connected directly between the nonreference node and each of these nodes. Therefore, $V_1 = 12$ V and $V_3 = -6$ V. Furthermore, note that the current through the 9-kΩ resistor is $[12 - (-6)]/9\text{k} = 2$ mA from left to right. We do not know V_2 or the current in the remaining resistors. However, since only one node voltage is unknown, a single-node equation will produce it. Applying KCL to this center node yields

$$\frac{V_2 - V_1}{12\text{k}} + \frac{V_2 - 0}{6\text{k}} + \frac{V_2 - V_3}{12\text{k}} = 0$$

or

$$\frac{V_2 - 12}{12\text{k}} + \frac{V_2}{6\text{k}} + \frac{V_2 - (-6)}{12\text{k}} = 0$$

from which we obtain

$$V_2 = \frac{3}{2}\text{ V}$$

Once all the node voltages are known, Ohm's law can be used to find the branch currents shown in Fig. 3.11b. The diagram illustrates that KCL is satisfied at every node.

Note that the presence of the voltage sources in this example has simplified the analysis, since two of the three linear independent equations are $V_1 = 12$ V and $V_3 = -6$ V. We will find that as a general rule, any time voltage sources are present between nodes, the node voltage equations that describe the network will be simpler.

LEARNING Hint

Any time an independent voltage source is connected between the reference node and a nonreference node, the nonreference node voltage is known.

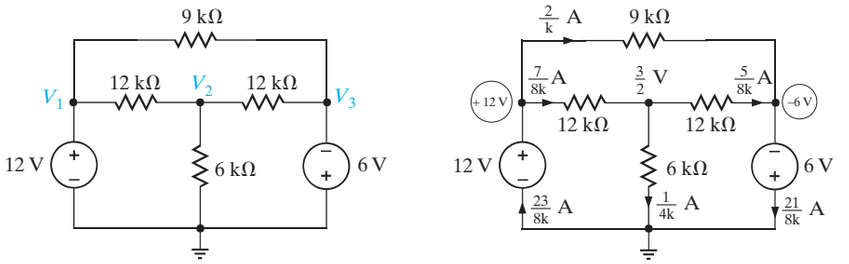


Figure 3.11
Circuit used in Example 3.5.

LEARNING EXTENSION

E3.5 Use nodal analysis to find the current I_o in the network in Fig. E3.5.

ANSWER $I_o = \frac{3}{4}$ mA.

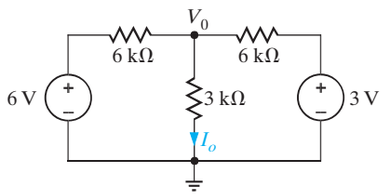


Figure E3.5

Next let us consider the case in which an independent voltage source is connected between two nonreference nodes. Once again, we will use an example to illustrate the approach.

LEARNING Example 3.6

We wish to find the currents in the two resistors in the circuit in Fig. 3.12a.

SOLUTION If we try to attack this problem in a brute force manner, we immediately encounter a problem. Thus far, branch currents were either known source values or could be expressed as the branch voltage divided by the branch resistance. However, the branch current through the 6-V source is certainly not known and cannot be directly expressed using Ohm's law. We can, of course, give this current a name and write the KCL equations

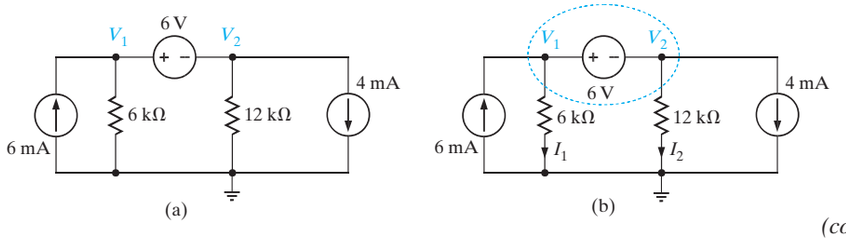


Figure 3.12
Circuits used in Example 3.6.

(continued)

at the two nonreference nodes in terms of this current. However, this approach is no panacea because this technique will result in *two* linearly independent simultaneous equations in terms of *three* unknowns; that is, the two node voltages and the current in the voltage source.

To solve this dilemma, we recall that $N - 1$ linearly independent equations are required to determine the $N - 1$ nonreference node voltages in an N-node circuit. Since our network has three nodes, we need two linearly independent equations. Now note that if somehow one of the node voltages is known, we immediately know the other; that is, if V_1 is known, then $V_2 = V_1 - 6$. If V_2 is known, then $V_1 = V_2 + 6$. Therefore, the difference in potential between the two nodes is *constrained* by the voltage source and, hence,

$$V_1 - V_2 = 6$$

This constraint equation is one of the two linearly independent equations needed to determine the node voltages.

Next consider the network in Fig. 3.12b, in which the 6-V source is completely enclosed within the dashed surface. The constraint equation governs this dashed portion of the network. The remaining equation is obtained by applying KCL to this dashed surface, which is commonly called a *supernode*. Recall that in Chapter 2 we demonstrated that KCL must hold for a surface, and this technique eliminates the problem of dealing with a current through a voltage source. KCL for the supernode is

$$-6 \times 10^{-3} + \frac{V_1}{6\text{k}} + \frac{V_2}{12\text{k}} + 4 \times 10^{-3} = 0$$

Solving these equations yields $V_1 = 10$ V and $V_2 = 4$ V and, hence, $I_1 = 5/3$ mA and $I_2 = 1/3$ mA. A quick check indicates that KCL is satisfied at every node.

LEARNING Hint

The supernode technique

- Use it when a branch between two nonreference nodes contains a voltage source.
- First encircle the voltage source and the two connecting nodes to form the supernode.
- Write the equation that defines the voltage relationship between the two nonreference nodes as a result of the presence of the voltage source.
- Write the KCL equation for the supernode.
- If the voltage source is dependent, then the controlling equation for the dependent source is also needed.

LEARNING Example 3.7

Let us determine the current I_o in the network in Fig. 3.13a.

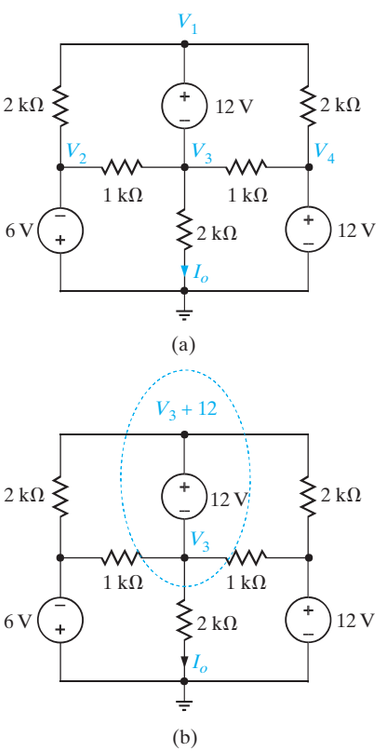


Figure 3.13
Example circuit with supernodes.

SOLUTION Examining the network, we note that node voltages V_2 and V_4 are known and the node voltages V_1 and V_3 are constrained by the equation

$$V_1 - V_3 = 12$$

The network is redrawn in Fig. 3.13b.

Since we want to find the current I_o, V_1 (in the supernode containing V_1 and V_3) is written as $V_3 + 12$. The KCL equation at the supernode is then

$$\frac{V_3 + 12 - (-6)}{2\text{k}} + \frac{V_3 + 12 - 12}{2\text{k}} + \frac{V_3 - (-6)}{1\text{k}} + \frac{V_3 - 12}{1\text{k}} + \frac{V_3}{2\text{k}} = 0$$

Solving the equation for V_3 yields

$$V_3 = -\frac{6}{7}\text{ V}$$

I_o can then be computed immediately as

$$I_o = \frac{-\frac{6}{7}}{2\text{k}} = -\frac{3}{7}\text{ mA}$$

LEARNING EXTENSION

E3.6 Use nodal analysis to find I_o in the network in Fig. E3.6.

ANSWER $I_o = 3.8$ mA.

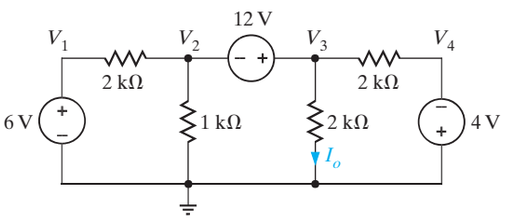


Figure E3.6

CIRCUITS CONTAINING DEPENDENT VOLTAGE SOURCES As the following examples will indicate, networks containing dependent (controlled) sources are treated in the same manner as described earlier.

LEARNING Example 3.8

We wish to find I_o in the network in Fig. 3.14.

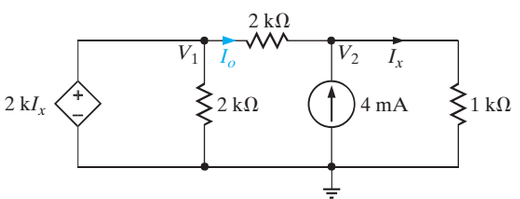


Figure 3.14 Circuit used in Example 3.8.

SOLUTION Since the dependent voltage source is connected between the node labeled V_1 and the reference node,

$$V_1 = 2kI_x$$

KCL at the node labeled V_2 is

$$\frac{V_2 - V_1}{2k} - \frac{4}{k} + \frac{V_2}{1k} = 0$$

where

$$I_x = \frac{V_2}{1k}$$

Solving these equations yields $V_2 = 8$ V and $V_1 = 16$ V. Therefore

$$I_o = \frac{V_1 - V_2}{2k}$$

$$= 4 \text{ mA}$$

LEARNING Example 3.9

Let us find the current I_o in the network in Fig. 3.15.

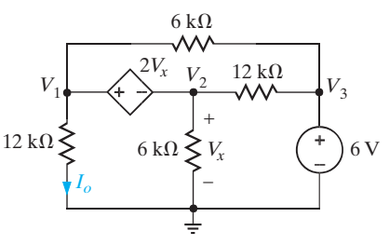


Figure 3.15 Circuit used in Example 3.9.

SOLUTION This circuit contains both an independent voltage source and a voltage-controlled voltage source. Note that $V_3 = 6$ V, $V_2 = V_x$, and a supernode exists between the nodes labeled V_1 and V_2.

Applying KCL to the supernode, we obtain

$$\frac{V_1 - V_3}{6k} + \frac{V_1}{12k} + \frac{V_2}{6k} + \frac{V_2 - V_3}{12k} = 0$$

where the constraint equation for the supernode is

$$V_1 - V_2 = 2V_x$$

The final equation is

$$V_3 = 6$$

Solving these equations, we find that

$$V_1 = \frac{9}{2} \text{ V}$$

and, hence,

$$I_o = \frac{V_1}{12k} = \frac{3}{8} \text{ mA}$$

LEARNING EXTENSION

E3.7 Use nodal analysis to find I_o in the circuit in Fig. E3.7.

ANSWER $I_o = \frac{4}{3}$ mA.

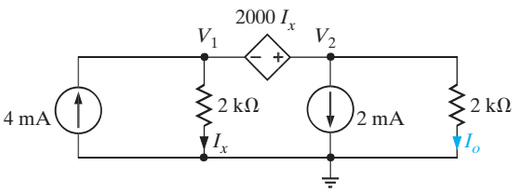


Figure E3.7

Problem-Solving Strategy Nodal Analysis

- Select one node in the N-node circuit as the reference node. Assume that the node voltage is zero and measure all node voltages with respect to this node.
- If only independent current sources are present in the network, write the KCL equations at the $N - 1$ nonreference nodes. If dependent current sources are present, write the KCL equations as is done for networks with only independent current sources; then write the controlling equations for the dependent sources.
- If voltage sources are present in the network, they may be connected (1) between the reference node and a nonreference node or (2) between two nonreference nodes. In the former case, if the voltage source is an independent source, then the voltage at one of the nonreference nodes is known. If the source is dependent, it is treated as an independent source when writing the KCL equation, but an additional constraint equation is necessary, as described previously.

  In the latter case, if the source is independent, the voltage between the two nodes is constrained by the value of the voltage source, and an equation describing this constraint represents one of the $N - 1$ linearly independent equations required to determine the N-node voltages. The surface of the network described by the constraint equation (i.e., the source and two connecting nodes) is called a supernode. One of the remaining $N - 1$ linearly independent equations is obtained by applying KCL at this supernode. If the voltage source is dependent, it is treated as an independent source when writing the KCL equations, but an additional constraint equation is necessary, as described previously.

3.2 Loop Analysis

In a nodal analysis the unknown parameters are the node voltages, and KCL is employed to determine them. In contrast to this approach, a loop analysis uses KVL to determine currents in the circuit. Once the currents are known, Ohm's law can be used to calculate the voltages. Recall that, in Chapter 2, we found that a single equation was sufficient to determine the current in a circuit containing a single loop. If the circuit contains N independent loops, we will show that N independent simultaneous equations will be required to describe the network. For now we will assume that the circuits are planar, which simply means that we can draw the circuit on a sheet of paper in a way such that no conductor crosses another conductor.

Our approach to loop analysis will mirror that used in nodal analysis (i.e., we will begin with simple cases and systematically proceed to those that are more difficult). Then at the end of this section we will outline a general strategy for employing loop analysis.

CIRCUITS CONTAINING ONLY INDEPENDENT VOLTAGE SOURCES To begin our analysis, consider the circuit shown in Fig. 3.16. Let us also identify two loops, *A-B-E-F-A* and *B-C-D-E-B*. We now define a new set of current variables called *loop currents*, which can be used to find the physical currents in the circuit. Let us assume that current i_1 flows in the first loop and that current i_2 flows in the second loop. Then the branch current flowing from B to E through R_3 is $i_1 - i_2$. The directions of the currents have been assumed. As was the case in the nodal analysis, if the actual currents are not in the direction indicated, the values calculated will be negative.

Applying KVL to the first loop yields

$$+v_1 + v_3 + v_2 - v_{S1} = 0$$

KVL applied to loop 2 yields

$$+v_{S2} + v_4 + v_5 - v_3 = 0$$

where $v_1 = i_1R_1$, $v_2 = i_1R_2$, $v_3 = (i_1 - i_2)R_3$, $v_4 = i_2R_4$, and $v_5 = i_2R_5$.

Substituting these values into the two KVL equations produces the two simultaneous equations required to determine the two loop currents; that is,

$$i_1(R_1 + R_2 + R_3) - i_2(R_3) = v_{S1}$$
$$-i_1(R_3) + i_2(R_3 + R_4 + R_5) = -v_{S2}$$

or in matrix form

$$\begin{bmatrix} R_1 + R_2 + R_3 & -R_3 \\ -R_3 & R_3 + R_4 + R_5 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} v_{S1} \\ -v_{S2} \end{bmatrix}$$

At this point it is important to define what is called a *mesh*. A mesh is a special kind of loop that does not contain any loops within it. Therefore, as we traverse the path of a mesh, we do not encircle any circuit elements. For example, the network in Fig. 3.16 contains two meshes defined by the paths *A-B-E-F-A* and *B-C-D-E-B*. The path *A-B-C-D-E-F-A* is a loop, but it is not a mesh. Since the majority of our analysis in this section will involve writing KVL equations for meshes, we will refer to the currents as mesh currents and the analysis as a *mesh analysis*.

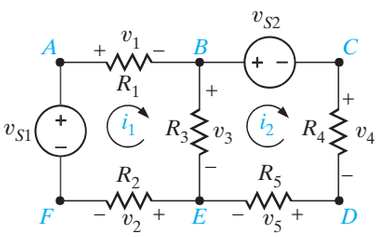


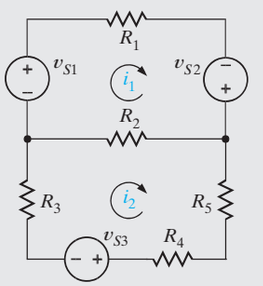
Figure 3.16
A two-loop circuit.

LEARNING Hint

The equations employ the passive sign convention.

LEARNING by Doing

D 3.2 Write the mesh equations for the following circuit.



ANSWER

$-v_{S1} + i_1R_1 - v_{S2}$
$+ (i_1 - i_2)R_2 = 0$

$i_2R_3 + (i_2 - i_1)R_2$
$+ i_2R_S + i_2R_4 + v_{S3} = 0$

LEARNING Example 3.10

Consider the network in Fig. 3.17a. We wish to find the current I_o.

SOLUTION We will begin the analysis by writing mesh equations. Note that there are no + and − signs on the resistors. However, they are not needed, since we will apply Ohm's law to each resistive element as we write the KVL equations. The equation for the first mesh is

$$-12 + 6\text{k}I_1 + 6\text{k}(I_1 - I_2) = 0$$

The KVL equation for the second mesh is

$$6\text{k}(I_2 - I_1) + 3\text{k}I_2 + 3 = 0$$

where $I_o = I_1 - I_2$.

Solving the two simultaneous equations yields $I_1 = 5/4$ mA and $I_2 = 1/2$ mA. Therefore, $I_o = 3/4$ mA. All the voltages and currents in the network are shown in Fig. 3.17b. Recall from nodal analysis that once the node voltages were determined, we could

(continued)

check our analysis using KCL at the nodes. In this case we know the branch currents and can use KVL around any closed path to check our results. For example, applying KVL to the outer loop yields

$$-12 + \frac{15}{2} + \frac{3}{2} + 3 = 0$$
$$0 = 0$$

Since we want to calculate the current I_o, we could use loop analysis, as shown in Fig. 3.17c. Note that the loop current I_1 passes through the center leg of the network and, therefore, $I_1 = I_o$. The two loop equations in this case are

$$-12 + 6\text{k}(I_1 + I_2) + 6\text{k}I_1 = 0$$

and

$$-12 + 6\text{k}(I_1 + I_2) + 3\text{k}I_2 + 3 = 0$$

Solving these equations yields $I_1 = 3/4$ mA and $I_2 = 1/2$ mA. Since the current in the 12-V source is $I_1 + I_2 = 5/4$ mA, these results agree with the mesh analysis.

Finally, for purposes of comparison, let us find I_o using nodal analysis. The presence of the two voltage sources would indicate that this is a viable approach. Applying KCL at the top center node, we obtain

$$\frac{V_o - 12}{6\text{k}} + \frac{V_o}{6\text{k}} + \frac{V_o - 3}{3\text{k}} = 0$$

and hence,

$$V_o = \frac{9}{2}\text{ V}$$

and then

$$I_o = \frac{V_o}{6\text{k}} = \frac{3}{4}\text{ mA}$$

Note that in this case we had to solve only one equation instead of two.

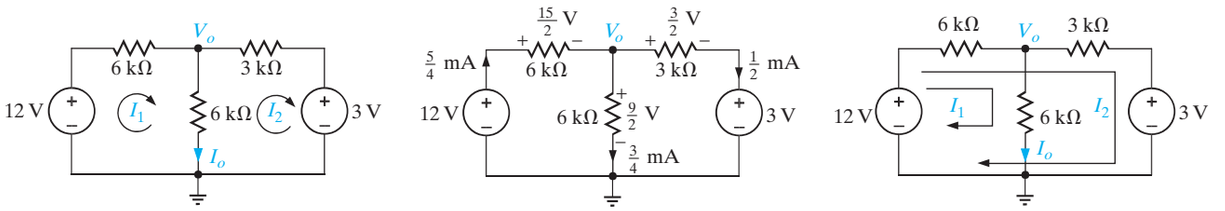


Figure 3.17 *Circuits used in Example 3.10.*

Once again we are compelled to note the symmetrical form of the mesh equations that describe the circuit in Fig. 3.16. Note that the coefficient matrix for this circuit is symmetrical.

Since this symmetry is generally exhibited by networks containing resistors and independent voltage sources, we can learn to write the mesh equations by inspection. In the first equation, the coefficient of i_1 is the sum of the resistances through which mesh current 1 flows, and the coefficient of i_2 is the negative of the sum of the resistances common to mesh current 1 and mesh current 2. The right-hand side of the equation is the algebraic sum of the voltage sources in mesh 1. The sign of the voltage source is positive if it aids the assumed direction of the current flow and negative if it opposes the assumed flow. The first equation is KVL for mesh 1. In the second equation, the coefficient of i_2 is the sum of all the resistances in mesh 2, the coefficient of i_1 is the negative of the sum of the resistances common to mesh 1 and mesh 2, and the right-hand side of the equation is the algebraic sum of the voltage sources in mesh 2. In general, if we assume all of the mesh currents to be in the same direction (clockwise or counterclockwise), then if KVL is applied to mesh j with mesh current i_j, the coefficient of i_j is the sum of the resistances in mesh j and the coefficients of the other mesh currents $(\text{e.g., } i_{j-1}, i_{j+1})$ are the negatives of the resistances common to these meshes and mesh j. The right-hand side of the equation is equal to the algebraic sum of the voltage sources in mesh j. These voltage sources have a positive sign if they aid the current flow i_j and a negative sign if they oppose it.

LEARNING Example 3.11

Let us write the mesh equations by inspection for the network in Fig. 3.18. Then we will use MATLAB to solve for the mesh currents.

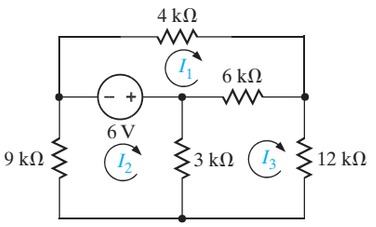


Figure 3.18 *Circuit used in Example 3.11.*

SOLUTION The three linearly independent simultaneous equations are

$$(4\text{k} + 6\text{k})I_1 - (0)I_2 - (6\text{k})I_3 = -6$$
$$-(0)I_1 + (9\text{k} + 3\text{k})I_2 - (3\text{k})I_3 = 6$$
$$-(6\text{k})I_1 - (3\text{k})I_2 + (3\text{k} + 6\text{k} + 12\text{k})I_3 = 0$$

or in matrix form

$$\begin{bmatrix} 10\text{k} & 0 & -6\text{k} \\ 0 & 12\text{k} & -3\text{k} \\ -6\text{k} & -3\text{k} & 21\text{k} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} -6 \\ 6 \\ 0 \end{bmatrix}$$

Note the symmetrical form of the equations. The general form of the matrix equation is

$$\mathbf{RI} = \mathbf{V}$$

and the solution of this matrix equation is

$$\mathbf{I} = \mathbf{R}^{-1}\mathbf{V}$$

The input/output data for a MATLAB solution are as follows:

```
>> R = [10e3 0 -6e3; 0 12e3 -3e3;
-6e3 -3e3 21e3]
   R =
          10000           0   -6000
              0       12000   -3000
          -6000       -3000    21000
>> V = [ -6 ; 6 ; 0]
   V =
      -6
       6
       0
>> I = inv(R)*V
   I =
     1.0e-003 *
      -0.6757
       0.4685
      -0.1261
```

CIRCUITS CONTAINING INDEPENDENT CURRENT SOURCES

Just as the presence of a voltage source in a network simplified the nodal analysis, the presence of a current source simplifies a loop analysis. The following examples illustrate the point.

LEARNING EXTENSION

E3.8 Use mesh equations to find V_o in the circuit in Fig. E3.8.

ANSWER $V_o = \frac{33}{5}$ V.

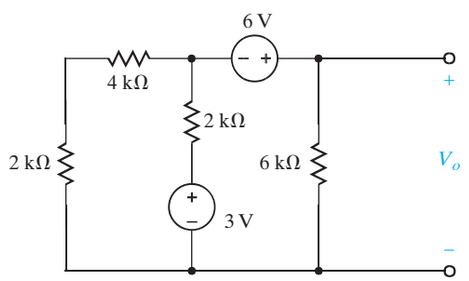


Figure E3.8

LEARNING Example 3.12

We wish to find V_o in the network in Fig. 3.19.

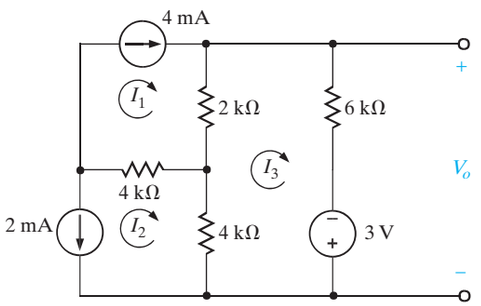


Figure 3.19 *Circuit used in Example 3.12.*

SOLUTION Since the currents I_1 and I_2 pass directly through a current source, two of the three required equations are

$$I_1 = 4 \times 10^{-3}$$
$$I_2 = -2 \times 10^{-3}$$

The third equation is KVL for the mesh containing the voltage source; that is,

$$4\text{k}(I_3 - I_2) + 2\text{k}(I_3 - I_1) + 6\text{k}I_3 - 3 = 0$$

These equations yield

$$I_3 = \frac{1}{4}\text{ mA}$$

and hence,

$$V_o = 6\text{k}I_3 - 3 = \frac{-3}{2}\text{ V}$$

What we have demonstrated in the previous example is the general approach for dealing with independent current sources when writing KVL equations; that is, use one loop through each current source. The number of "window panes" in the network tells us how many equations we need. Additional KVL equations are written to cover the remaining circuit elements in the network. The following example illustrates this approach.

LEARNING Example 3.13

Let us find I_o in the network in Fig. 3.20a.

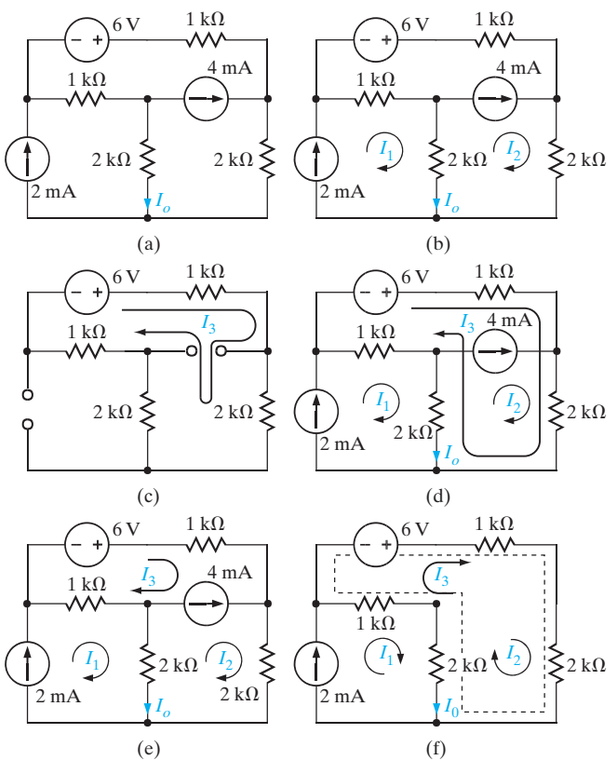


Figure 3.20 *Circuits used in Example 3.13.*

LEARNING Hint

In this case the 4-mA current source is located on the boundary between two meshes. Thus we will demonstrate two techniques for dealing with this type of situation. One is a special loop technique and the other is known as the supermesh approach.

SOLUTION First, we select two loop currents I_1 and I_2 such that I_1 passes directly through the 2-mA source, and I_2 passes directly through the 4-mA source, as shown in Fig. 3.20b. Therefore, two of our three linearly independent equations are

$$I_1 = 2 \times 10^{-3}$$
$$I_2 = 4 \times 10^{-3}$$

The remaining loop current I_3 must pass through the circuit elements not covered by the two previous equations and cannot, of course, pass through the current sources. The path for this remaining loop current can be obtained by open-circuiting the current sources, as shown in Fig. 3.20c. When all currents are labeled on the original circuit, the KVL equation for this last loop, as shown in Fig. 3.20d, is

$$-6 + 1\text{k}I_3 + 2\text{k}(I_2 + I_3) + 2\text{k}(I_3 + I_2 - I_1) + 1\text{k}(I_3 - I_1) = 0$$

Solving the equations yields

$$I_3 = \frac{-2}{3}\text{ mA}$$

and therefore,

$$I_o = I_1 - I_2 - I_3 = \frac{-4}{3}\text{ mA}$$

Next consider the supermesh technique. In this case the three mesh currents are specified as shown in Fig. 3.20e, and since the voltage across the 4-mA current source is unknown, it is assumed to be V_x. The mesh currents constrained by the current sources are

$$I_1 = 2 \times 10^{-3}$$
$$I_2 - I_3 = 4 \times 10^{-3}$$

The KVL equations for meshes 2 and 3, respectively, are

$$2\text{k}I_2 + 2\text{k}(I_2 - I_1) - V_x = 0$$
$$-6 + 1\text{k}I_3 + V_x + 1\text{k}(I_3 - I_1) = 0$$

Adding the last two equations yields

$$-6 + 1\text{k}I_3 + 2\text{k}I_2 + 2\text{k}(I_2 - I_1) + 1\text{k}(I_3 - I_1) = 0$$

Note that the unknown voltage V_x has been eliminated. The two constraint equations, together with this latter equation, yield the desired result.

The purpose of the supermesh approach is to avoid introducing the unknown voltage V_x. The supermesh is created by mentally removing the 4-mA current source, as shown in Fig. 3.20f. Then writing the KVL equation around the dotted path, which defines the supermesh, using the original mesh currents as shown in Fig. 3.20e, yields

$$-6 + 1\text{k}I_3 + 2\text{k}I_2 + 2\text{k}(I_2 - I_1) + 1\text{k}(I_3 - I_1) = 0$$

Note that this supermesh equation is the same as that obtained earlier by introducing the voltage V_x.

LEARNING EXTENSIONS

E3.9 Find V_o in the network in Fig. E3.9.

ANSWER $V_o = \frac{33}{5}$ V.

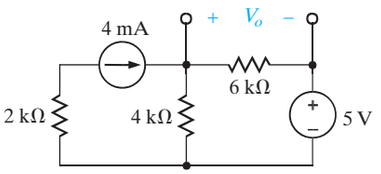


Figure E3.9

3.10 Find V_o in the network in Fig. E3.10.

ANSWER $V_o = \frac{32}{5}$ V.

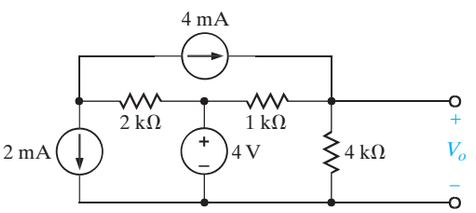


Figure E3.10

CIRCUITS CONTAINING DEPENDENT SOURCES We deal with circuits containing dependent sources just as we have in the past. First, we treat the dependent source as though it were an independent source when writing the KVL equations. Then we write the controlling equation for the dependent source. The following examples illustrate the point.

LEARNING Example 3.14

The network in Fig. 3.21 contains both a current-controlled voltage source and a voltage-controlled current source. Let us use MATLAB to determine the loop currents.

SOLUTION The equations for the loop currents shown in the figure are

$$I_1 = \frac{4}{\text{k}}$$
$$I_2 = \frac{V_x}{2\text{k}}$$
$$-1\text{k}I_x + 2\text{k}(I_3 - I_1) + 1\text{k}(I_3 - I_4) = 0$$
$$1\text{k}(I_4 - I_3) + 1\text{k}(I_4 - I_2) + 12 = 0$$

(continued)

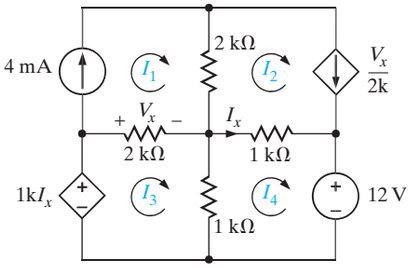


Figure 3.21
Circuit used in Example 3.14.

where

$$V_x = 2k(I_3 - I_1)$$

$$I_x = I_4 - I_2$$

Combining these equations yields

$$I_1 = \frac{4}{k}$$

$$I_1 + I_2 - I_3 = 0$$

$$1kI_2 + 3kI_3 - 2kI_4 = 8$$

$$1kI_2 + 1kI_3 - 2kI_4 = 12$$

In matrix form the equations are

$$\begin{bmatrix} 1 & 0 & 0 & 0 \\ 1 & 1 & -1 & 0 \\ 0 & 1k & 3k & -2k \\ 0 & 1k & 1k & -2k \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} \frac{4}{k} \\ 0 \\ 8 \\ 12 \end{bmatrix}$$

The input and output data for the MATLAB solution are as follows:

```
>> R = [ 1 0 0 0 ; 1 1 -1 0;
0 1000 3000 -2000;
0 1000 1000 -2000]

R =

     1     0     0     0
     1     1    -1     0
     0  1000  3000 -2000
     0  1000  1000 -2000

>> V = [ 0.004; 0; 8; 12]

V =

    0.0040
         0
    8.0000
   12.0000

>> I = inv(R)*V

I =

    0.0040
   -0.0060
   -0.0020
   -0.0100
```

As a final point, it is very important to examine the circuit carefully before selecting an analysis approach. One method could be much simpler than another, and a little time invested up front may save a lot of time in the long run.

LEARNING EXTENSION

E3.11 Use mesh analysis to find V_o in the circuit in Fig. E3.11.

ANSWER $V_o = 12$ V.

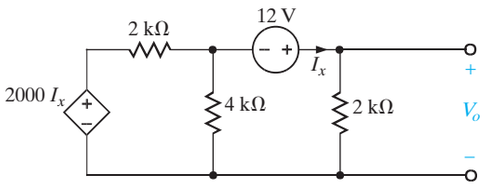


Figure E3.11

Problem-Solving Strategy Loop Analysis

- One loop current is assigned to each independent loop in a circuit that contains N independent loops.
- If only independent voltage sources are present in the network, write the N linearly independent KVL equations, one for each loop. If dependent voltage sources are present, write the KVL equation as is done for circuits with only independent voltage sources; then write the controlling equations for the dependent sources.
- If current sources are present in the network, either of two techniques can be used. In the first case, one loop current is selected to pass through one of the current sources. This is done for each current source in the network. The remaining loop currents (N − the number of current sources) are determined by open-circuiting the current sources in the network and using this modified network to select them. Once all these currents are defined in the original network, the N loop equations can be written. The second approach is similar to the first with the exception that if two mesh currents pass through a particular current source, a supermesh is formed around this source. The two required equations for the meshes containing this source are the constraint equations for the two mesh currents that pass through the source and the supermesh equation. As indicated earlier, if dependent current sources are present, the controlling equations for these sources are also necessary.

LEARNING EXTENSIONS

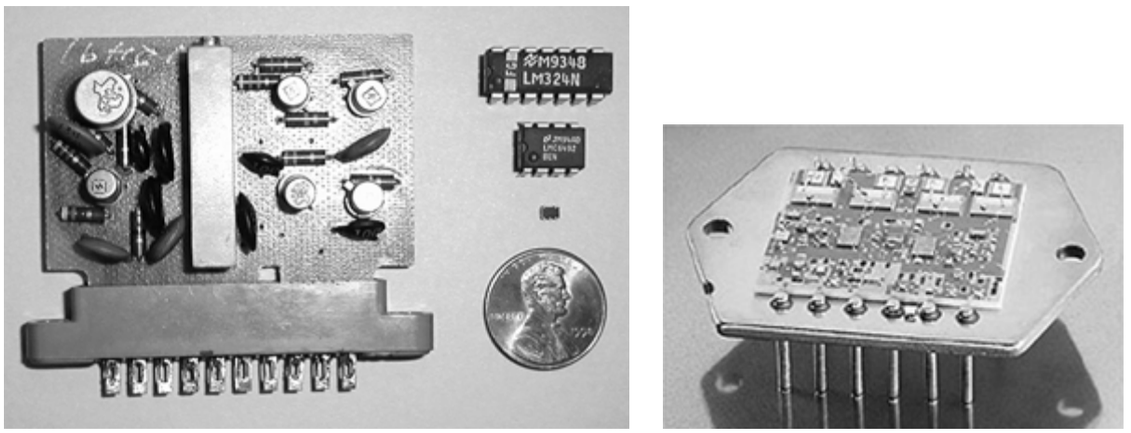
E3.12 Use loop analysis to solve the network in Example 3.5 and compare the time and effort involved in the two solution techniques.

E3.13 Use nodal analysis to solve the circuit in Example 3.12 and compare the time and effort involved in the two solution strategies.

3.3 Circuits with Operational Amplifiers

It can be argued that the operational amplifier, or op-amp as it is commonly known, is the single most important integrated circuit for analog circuit design. It is a versatile interconnection of transistors and resistors that vastly expands our capabilities in circuit design, from engine control systems to cellular phones. Early op-amps were built with vacuum tubes, making them bulky and power hungry. The invention of the transistor at Bell Labs in 1947 allowed engineers to create op-amps that were much smaller and more efficient. Still, the op-amp itself consisted of individual transistors and resistors interconnected on a printed circuit board (PCB). When the manufacturing process for integrated circuits (ICs) was developed around 1970, engineers could finally put all of the op-amps transistors and resistors onto a single IC chip. Today, it is common to find as many as four high quality op-amps on a single IC for as little as $0.40. A sample of commercial op-amps is shown in Fig. 3.22.

Let us first examine the origin of the term operational amplifier. Originally, the op-amp was designed to perform mathematical operations such as addition, subtraction, differentiation, and integration. By adding simple networks to the op-amp, we can create these "building blocks" as well as other functions such as voltage scaling, current-to-voltage conversion, and a myriad of more complex applications.

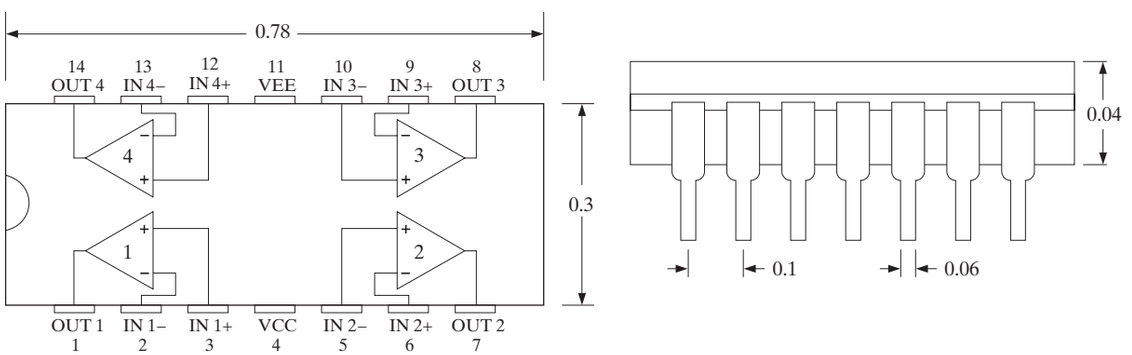


(a) (b)

Figure 3.22 *A selection of op-amps. On the left in (a) is a discrete op-amp assembled on a printed circuit board (PCB). On the right from top to bottom, a LM324 DIP (dual in-line pack), LMC6294 DIP, and MAX4240 in a SO-5 package (small outline/5 pins). A penny is shown for purposes of comparison. In (b) is the APEX PA03 with its lid removed showing individual transistors and resistors.*

How can we, understanding only sources and resistors, hope to comprehend the performance of the op-amp? The answer is modeling. When all the bells and whistles are removed, an op-amp is simply a very good voltage amplifier. In other words, the output voltage is a scaled replica of the input voltage. Modern op-amps are such good amplifiers that it is easy to create an accurate, first-order model. As mentioned earlier, the op-amp is very popular and is used extensively in circuit design at all levels. We should not be surprised to find that op-amps are available for every application—low voltage, high voltage, micro-power, high speed, high current, and so forth. Fortunately, the topology of our model is independent of these issues.

We begin our discussion with the general purpose LM324 quad (four in a pack) op-amp from National Semiconductor. The pinout for the LM324 is shown in Fig. 3.23 for a DIP (dual in-



(a) (b)

Figure 3.23 *(a) The pinout and (b) the dimensional diagram of one side of the LM324 quad op-amp. Note the pin pitch (distance pin-to-pin) is 0.1 inches, a standard for DIP packages.*

line pack) style package with the dimensions specified in inches. Recognizing there are four identical op-amps in the package, we will focus on amplifier 1. Pins 3 and 2 are the input pins, IN_+ and IN_-, and are called the noninverting and inverting inputs, respectively. The output is at pin 1. The relationship that exists between the output and input voltages is

$$V_o = A_o(IN_+ - IN_-) \qquad \textbf{3.5}$$

where all voltages are measured with respect to ground and A_o is the gain of the op-amp. From Eq. (3.5), we see that when IN_+, increases, so will V_o. However, if IN_- increases, then V_o will decrease—hence the names noninverting and inverting inputs. We mentioned earlier that op-amps are very good voltage amplifiers. How good? Typical values for A_o are between 10,000 and 1,000,000!

To provide amplification, we need power. This power is obtained from dc voltage sources connected to pins 4 and 11, called V_{CC} and V_{EE}, respectively. Actual values for these power supplies can vary widely depending on the application, from as little as one volt up to several hundred volts. Traditionally, V_{CC} is a positive dc voltage with respect to ground and V_{EE} is either a negative voltage or ground itself.

We can model the input/output relationship of the op-amp, as specified in Eq. (3.5), using a dependent voltage source. The currents into and out of the op-amp terminals (pins 3, 2, and 1) are fairly proportional to the pin voltages; that is, the relationship is essentially that specified by Ohm's law. Thus, we model the I-V performance with two resistors, one at the input terminals (R_i) and another at the output (R_o). The resultant circuit is shown in Fig. 3.24.

Let us now examine the values for A_o, R_i, and R_o. Consider the network in Fig. 3.25, where we have modeled the driving circuit with V_S and a resistance R_{Th1}, and the output load with a resistor R_L.

Since the op-amp is designed to be an excellent voltage amplifier, let us write an equation for the overall gain of the circuit V_{out}/V_{in}. Using voltage division at the input and again at the output, we quickly produce the expression

$$\frac{V_{out}}{V_{in}} = \left[\frac{R_i}{R_i + R_{Th1}}\right] A_o \left[\frac{R_L}{R_o + R_L}\right]$$

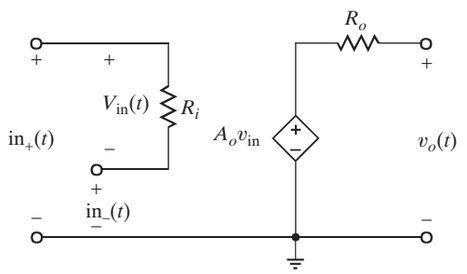


Figure 3.24
A simple model of the gain characteristics of an op-amp.

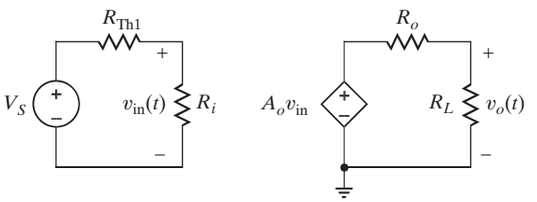


Figure 3.25
A network that depicts an op-amp circuit. V_S and R_{Th1} model the driving circuit, while the load is modeled by R_L.

Table 3.1 A list of commercial op-amps and their model values

Manufacturer	Part No.	A_o (V/V)	R_i (MV)	R_o (Ω)	Comments
National	LM324	100,000	1.0	20	General purpose, up to ±16 V supplies, very inexpensive
National	LMC6492	50,000	10^7	150	Low voltage, rail-to-rail inputs and outputs
Maxim	MAX4240	20,000	45	160	Micro-power (1.8 V supply @ 10 μA), rail-to-rail in inputs and outputs
Apex	PA03	125,000	10^5	2	High voltage, ±75 V, and high output current capability, 30 A. That's 2 kW!

To maximize the gain, regardless of the input resistance and load values, we make A_o very large and the voltage division ratios as close to unity as possible. The ideal scenario requires A_o be infinite, R_i to be infinite, and R_o to be zero, yielding a large overall gain of A_o. Table 3.1 shows the actual values of A_o, R_i, and R_o for a sampling of commercial op-amps intended for very different applications. Although A_o, R_i, and R_o are not ideal, they do approximate the ideal conditions.

The power supplies affect performance in two ways. First, each op-amp has minimum and maximum supply ranges, sometimes called rail-to-rail (a trademark of Motorola Corporation) over which the op-amp is guaranteed to function. Second, for proper operation, the input and output voltages are limited to no more than the supply voltages (Op-amps are available that have input and/or output voltage ranges beyond the supply rails: however, these devices constitute a very small percentage of the op-amp market and will not be discussed here). If the inputs and output can reach within a few dozen millivolts of the supplies, then the inputs and output are called rail-to-rail. Otherwise, the inputs/output limits are more severe—usually a volt or so away from the supply values. Combining the model in Fig. 3.25, the values in Table 3.1, and these I/O limitations, we can produce the graphs in Fig. 3.26, which show the output–input relationship for each op-amp outlined in Table 3.1. From the graph we see that the LM6492 and MAX 4240 have rail-to-rail outputs and the LM324 and PA03 do not.

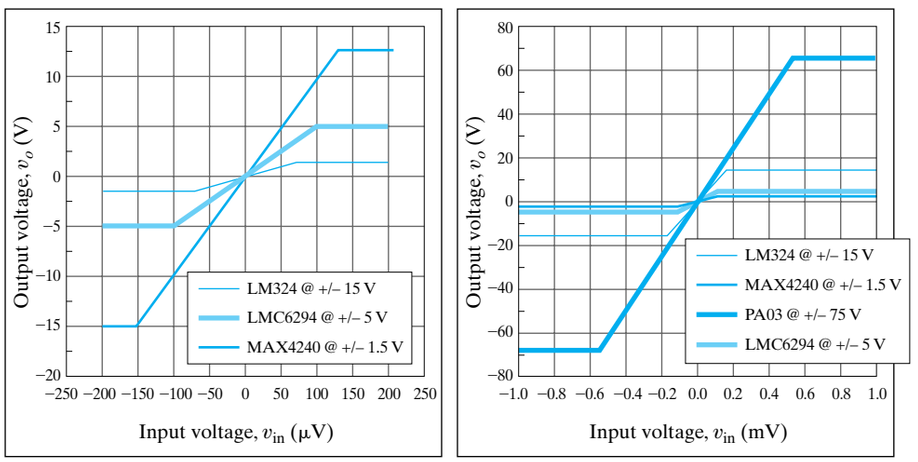


Figure 3.26
Transfer plots for the op-amps listed in Table 3.1. The supply voltages are listed in the plot legends. Note that the LMC6492 and MAX4240 have rail-to-rail output voltages, and the LM324 and PA03 do not.

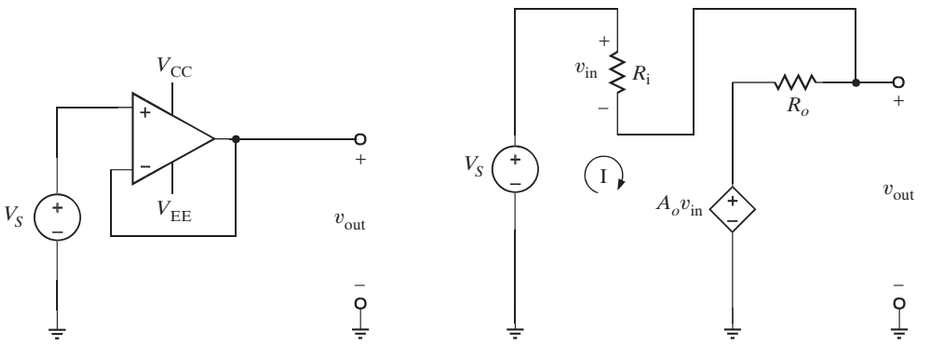


Figure 3.27
Circuit (a) and model (b) for the unity gain buffer.

In order to examine the performance of the op-amp in a practical circuit, consider the network shown in Fig. 3.27a called a unity-gain buffer. Note that the op-amp schematic symbol includes the power supplies. Employing the model in Fig. 3.25 yields the circuit in Fig. 3.27b, containing just resistors and dependent sources, which we can easily analyze. The loop equations for the network are

$$V_S = IR_i + IR_o + A_o V_{\text{in}}$$
$$V_{\text{out}} = IR_o + A_o V_{\text{in}}$$
$$V_{\text{in}} = IR_i$$

Solving for the gain, V_{out}/V_S, we find

$$\frac{V_{\text{out}}}{V_S} = \frac{1}{1 + \dfrac{R_i}{R_o + A_o R_i}}$$

For $R_o \ll R_i$, we have

$$\frac{V_{\text{out}}}{V_S} \approx \frac{1}{1 + \dfrac{1}{A_o}}$$

And, if A_o is indeed $\gg 1$,

$$\frac{V_{\text{out}}}{V_S} \approx 1$$

Thus, the origin of the name, unity gain buffer, should be apparent. Table 3.2 shows the actual gain values for $V_S = 1$ V using the op-amps listed in Table 3.1. Note how close the gain is to unity and how small the input voltage and current are. These results lead us to simplify

Table 3.2 Unity gain buffer performance for the op-amps listed in Table 3.1

Op-Amp	Buffer Gain	V_{in} (μV)	I (pA)
LM324	0.999990	9.9999	9.9998
LMC6492	0.999980	19.999	1.9999×10^{-6}
MAX4240	0.999950	49.998	1.1111
PA05	0.999992	7.9999	7.9999×10^{-5}

Table 3.3 Consequences of the ideal op-amp model on input terminal I/V values

Model Assumption	Terminal Result
$A_o \to \infty$	Input voltage $\to$ 0 V
$R_i \to \infty$	Input current $\to$ 0 A

the op-amp in Fig. 3.24 significantly. Hence, we introduce the *ideal op-amp model*, where A_o and R_i are infinite and R_o is zero. This selection of parameter values produces two important results for analyzing op-amp circuits, which are listed in Table 3.3.

From Table 3.3 we find that the ideal model for the op-amp is reduced to that shown in Fig. 3.28. The important characteristics of the model are as follows: (1) Since R_i is extremely large, the input currents to the op-amp are approximately zero (i.e., $i_+ \approx i_- \approx 0$); and (2) if the output voltage is to remain bounded, then as the gain becomes very large and approaches infinity, the voltage across the input terminals must simultaneously become infinitesimally small so that as $A \to \infty$, $v_+ - v_- \to 0$ (i.e., $v_+ - v_- = 0$ or $v_+ = v_-$). The difference between these input voltages is often called the *error signal* for the op-amp (i.e., $v_+ - v_- = v_e$).

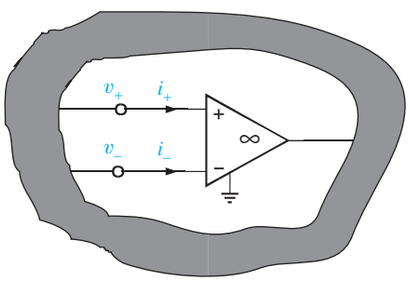


Figure 3.28
Ideal model for an operational amplifier. Model parameters: $i_+ = i_- = 0$, $v_+ = v_-$.

The ground terminal ⏚ shown on the op-amp is necessary for signal current return, and it guarantees that Kirchhoff's current law is satisfied at both the op-amp and the ground node in the circuit.

In summary, then, our ideal model for the op-amp is simply stated by the following conditions:

$$i_+ = i_- = 0 \qquad \textbf{3.6}$$
$$v_+ = v_-$$

These simple conditions are extremely important because they form the basis of our analysis of op-amp circuits.

Let us now use the ideal model to re-examine the unity gain buffer, redrawn again in Fig. 3.29, where the input voltage and currents are shown as zero. Given that $v_{\text{in}} = v_+ - v_-$

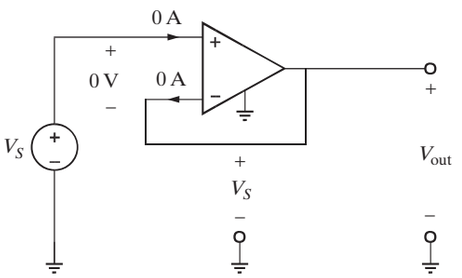


Figure 3.29
As ideal op-amp configured as a unity gain buffer.

is zero, the voltage at both op-amp inputs is V_S. Since the inverting input is physically connected to the output, V_{out} is also V_S—therefore, unity gain!

An obvious question at this point is this: If $v_o = v_S$, why not just connect v_S to v_o via two parallel connection wires; why do we need to place an op-amp between them? The answer to this question is fundamental and provides us with some insight that will aid us in circuit analysis and design.

Consider the circuit shown in Fig. 3.30a. In this case v_o is not equal to v_S because of the voltage drop across R_S:

$$v_o = v_S - iR_S$$

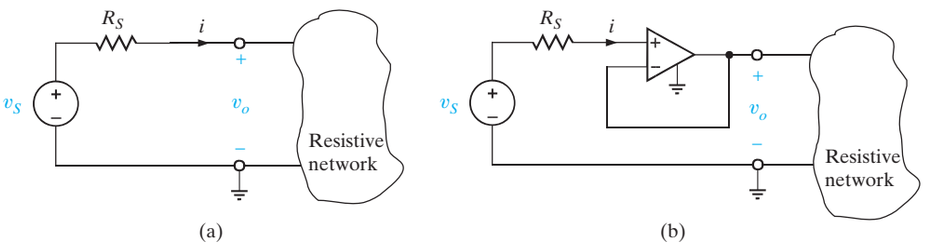


Figure 3.30
Illustration of the isolation capability of a voltage follower.

However, in Fig. 3.30b, the input current to the op-amp is zero and, therefore, v_S appears at the op-amp input. Since the gain of the op-amp configuration is 1, $v_o = v_S$. In Fig. 3.30a the resistive network's interaction with the source caused the voltage v_o to be less than v_S. In other words, the resistive network loads the source voltage. However, in Fig. 3.30b the op-amp isolates the source from the resistive network, and therefore the voltage follower is referred to as a *buffer amplifier* because it can be used to isolate one circuit from another. The energy supplied to the resistive network in the first case must come from the source v_S, whereas in the second case it comes from the power supplies that supply the amplifier, and little or no energy is drawn from v_S.

As a general rule, when analyzing op-amp circuits we write nodal equations at the op-amp input terminals, using the ideal op-amp model conditions. The following example demonstrates the simplicity of this approach.

LEARNING Example 3.15

Let us determine the gain of the basic inverting op-amp configuration shown in Fig. 3.31.

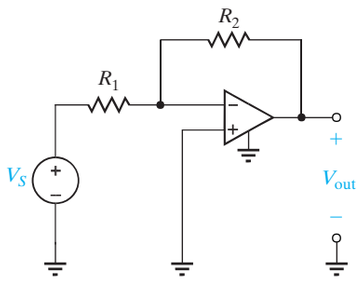


Figure 3.31
The basic inverting gain stage.

SOLUTION Using the ideal op-amp model conditions, we see that $v_+ = 0$ and, therefore $v_- = 0$. If we now write a node equation at the negative terminal of the op-amp, we obtain

$$\frac{v_S - 0}{R_1} + \frac{v_o - 0}{R_2} = 0$$

or

$$\frac{v_o}{v_S} = -\frac{R_2}{R_1}$$

Note that the gain is a simple resistor ratio. This fact makes the amplifier very versatile in that we can control the gain accurately and alter its value by changing only one resistor. Also, the gain is essentially independent of op-amp parameters. Since the precise values of A, R_i, and R_o are sensitive to such factors as temperature, radiation, and age, their elimination results in a gain that is stable regardless of the immediate environment. Since it is much easier to employ the ideal op-amp model rather than the nonideal model, unless otherwise stated we will use the ideal op-amp assumptions to analyze circuits that contain operational amplifiers.

LEARNING Example 3.16

Consider the op-amp circuit shown in Fig. 3.32. Let us determine an expression for the output voltage.

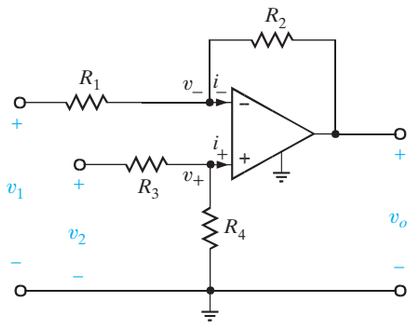


Figure 3.32 Differential amplifier operational amplifier circuit.

SOLUTION The node equation at the inverting terminal is

$$\frac{v_1 - v_-}{R_1} + \frac{v_o - v_-}{R_2} = i_-$$

At the noninverting terminal KCL yields

$$\frac{v_2 - v_+}{R_3} = \frac{v_+}{R_4} + i_+$$

However, $i_+ = i_- = 0$ and $v_+ = v_-$. Substituting these values into the two preceding equations yields

$$\frac{v_1 - v_-}{R_1} + \frac{v_o - v_-}{R_2} = 0$$

and

$$\frac{v_2 - v_-}{R_3} = \frac{v_-}{R_4}$$

Solving these two equations for v_o results in the expression

$$v_o = \frac{R_2}{R_1}\left(1 + \frac{R_1}{R_2}\right)\frac{R_4}{R_3 + R_4}v_2 - \frac{R_2}{R_1}v_1$$

Note that if $R_4 = R_2$ and $R_3 = R_1$, the expression reduces to

$$v_o = \frac{R_2}{R_1}(v_2 - v_1)$$

Therefore, this op-amp can be employed to subtract two input voltages.

LEARNING Example 3.17

The circuit shown in Fig. 3.33a is a precision differential voltage-gain device. It is used to provide a single-ended input for an analog-to-digital converter. We wish to derive an expression for the output of the circuit in terms of the two inputs.

SOLUTION To accomplish this, we draw the equivalent circuit shown in Fig. 3.33b. Recall that the voltage across the input terminals of the op-amp is approximately zero and the currents into the op-amp input terminals are approximately zero. Note that we can write node equations for node voltages v_1 and v_2 in terms of v_o and v_a. Since we are interested in an expression for v_o in terms of the voltages v_1 and v_2, we simply eliminate the v_a terms from the two node equations. The node equations are

$$\frac{v_1 - v_o}{R_2} + \frac{v_1 - v_a}{R_1} + \frac{v_1 - v_2}{R_G} = 0$$

$$\frac{v_2 - v_a}{R_1} + \frac{v_2 - v_1}{R_G} + \frac{v_2}{R_2} = 0$$

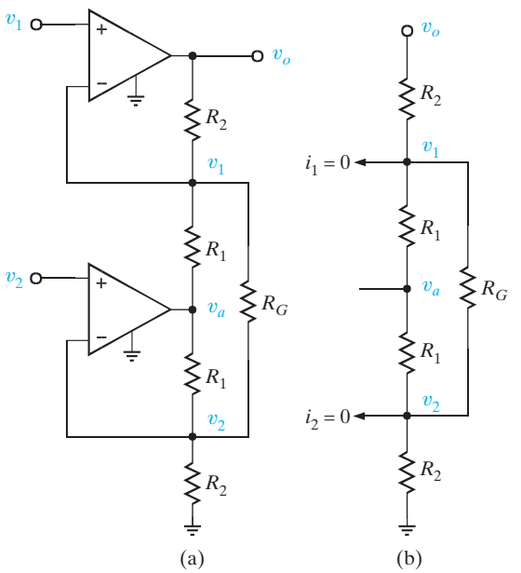


Figure 3.33 Instrumentation amplifier circuit.

Combining the two equations to eliminate v_a, and then writing v_o in terms of v_1 and v_2, yields

$$v_o = (v_1 - v_2)\left(1 + \frac{R_2}{R_1} + \frac{2R_2}{R_G}\right)$$

LEARNING EXTENSIONS

E3.14 Find I_o in the network in Fig. E3.14.

ANSWER $I_o = 8.4$ mA.

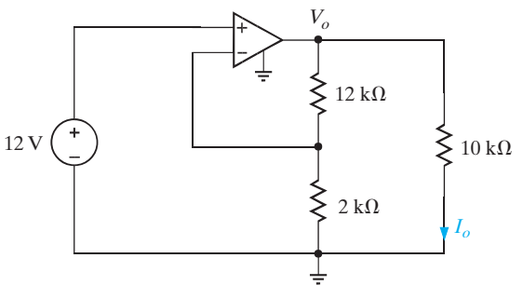


Figure E3.14

E3.15 Determine the gain of the op-amp circuit in Fig. E3.15.

ANSWER $\dfrac{V_o}{V_S} = 1 + \dfrac{R_2}{R_1}$.

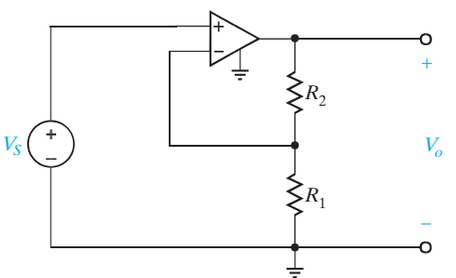


Figure E3.15

LEARNING EXTENSION

E3.16 Determine both the gain and the output voltage of the op-amp configuration shown in Fig. E3.16.

ANSWER $V_o = 0.101$ V, gain $= 101$.

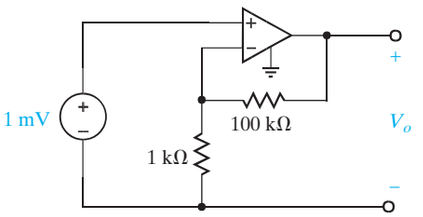
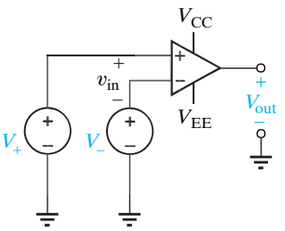
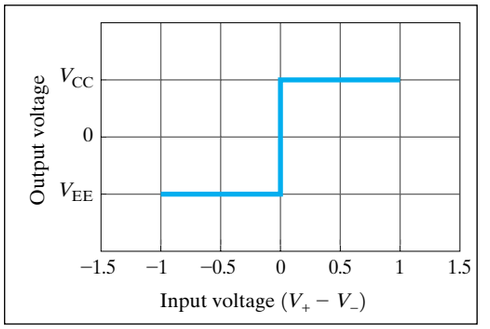


Figure E3.16

COMPARATORS A comparator, a variant of the op-amp, is designed to compare the noninverting and inverting input voltages. As shown in Fig. 3.34, when the noninverting input voltage is greater, the output goes as high as possible, at or near V_{CC}. On the other hand, if the inverting input voltage is greater, the output goes as low as possible, at or near V_{EE}. Of course, an ideal op-amp can do the same thing, that is, swing the output voltage as far as possible. However, op-amps are not designed to operate with the outputs saturated; whereas comparators are. As a result, comparators are faster and less expensive than op-amps.



(a)



(b)

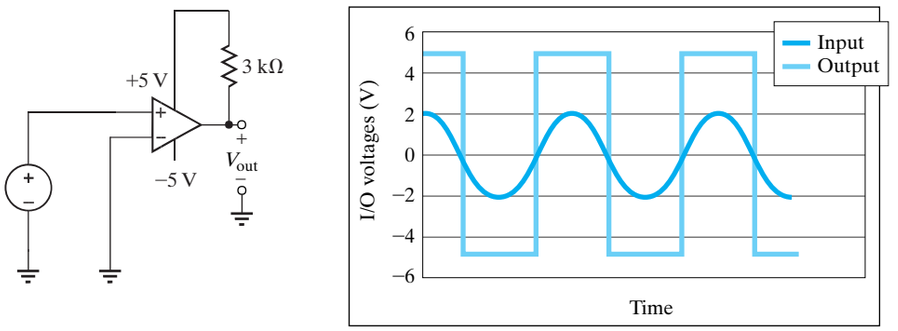
Figure 3.34
(a) An ideal comparator and (b) its transfer curve.

We will present two very different quad comparators in this text, National Semiconductor's LM339 and Maxim's MAX917. Note that the LM339 requires a resistor, called a pull-up resistor, connected between the output pin and V_{CC}. The salient features of these products are listed in Table 3.4. From Table 3.4, it is easy to surmise that the LM339 is a general purpose comparator whereas the MAX917 is intended for low-power applications such as hand-held products.

A common comparator application is the zero-crossing detector, shown in Fig. 3.35a using a LM339 with ±5 V supplies. As seen in Fig. 3.35b, when V_S is positive, V_{out} should be near +5 V and when V_S is negative, V_{out} should be near −5 V. The output changes value on every zero crossing!

Table 3.4 A listing of some of the features of the LM339 and MAX917 comparators

Product	Min. Supply	Max. Supply	Supply Current	Max. Output Current	Typical $R_{PULL\text{-}UP}$
LM339	2 V	36 V	3 mA	50 mA	3 kΩ
MAX919	1.8 V	5.5 V	0.8 μA	8 mA	NA



(a) (b)

Figure 3.35
(a) A zero-crossing detector and (b) the corresponding input/output waveforms.

Learning by Application

At this point, we have a new element, the op-amp, which we can effectively employ in both applications and circuit design. This device is an extremely useful element that vastly expands our capability in these areas. Because of its ubiquitous nature, the addition of the op-amp to our repertoire of circuit elements permits us to deal with a wide spectrum of practical circuits. Thus, we will employ it here, and also use it throughout this text.

LEARNING Example 3.18

The circuit in Fig. 3.36 is an electronic ammeter. It operates as follows: The unknown current, I through R_I produces a voltage, V_I. V_I is amplified by the op-amp to produce a voltage, V_o, which is proportional to I. The output voltage is measured with a simple voltmeter. We want to find the value of R_2 such that 10 V appears at V_o for each milliamp of unknown current.

SOLUTION Since the current into the op-amp + terminal is zero, the relationship between V_I and I is

$$V_I = IR_I$$

The relationship between the input and output voltages is

$$V_o = V_I\left(1 + \frac{R_2}{R_1}\right)$$

or, solving the equation for V_o/I, we obtain

$$\frac{V_o}{I} = R_I\left(1 + \frac{R_2}{R_1}\right)$$

Using the required ratio V_o/I of 10^4 and resistor values from Fig. 3.36, we can find that

$$R_2 = 9\ \text{k}\Omega$$

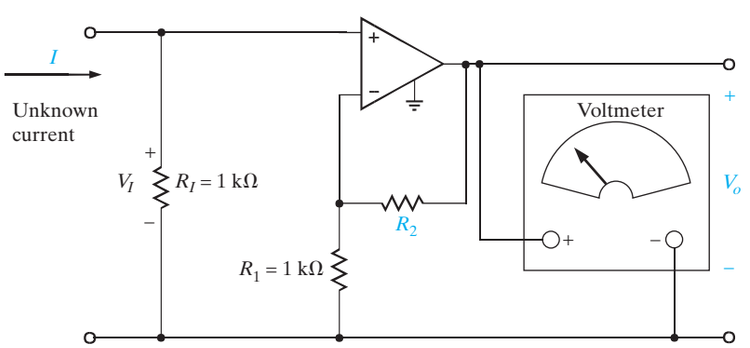


Figure 3.36
Electronic ammeter.

Learning by Design

LEARNING Example 3.19

A typical stereo system is shown in block form in Fig. 3.37a. The phonograph output signal is only about 2 μV. The standard input voltage for stereo power amplifiers is about 2 mV. Therefore, the phonograph signal must be amplified by a factor of 1000 before it reaches the poweramp. To accomplish this, a special-purpose amp, called the phono preamp, is used. Stereo manufacturers place them within the preamplifier cabinet, as shown in Fig. 3.37a.

Let us design a phono preamp using an ideal op-amp that has an input resistance of at least 1 MΩ and a voltage gain of 1000. All resistors must be less than 10 MΩ to limit noise.

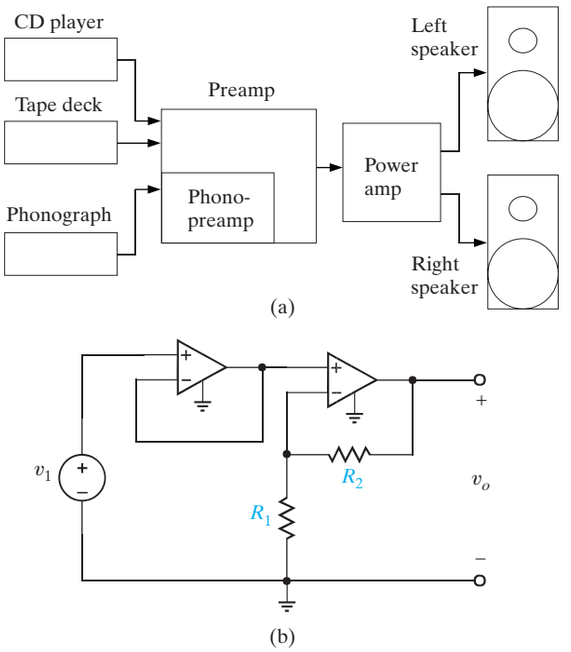


Figure 3.37 *Multistage phonograph amplifier.*

SOLUTION One possible network is shown in Fig. 3.37b. The input resistance requirement can be easily met with a voltage follower as the first stage of the amplifier. The second stage, or gain stage, can be a noninverting op-amp configuration. We will show in later chapters that the overall voltage gain is the product of the gains of the two stages,

$$A_V = A_{V1}A_{V2} = (1)\left(1 + \left(R_2/R_1\right)\right)$$

To achieve a gain of 1000, we select $R_1 = 1\ \text{k}\Omega$ and $R_2 = 999\ \text{k}\Omega$.

LEARNING Example 3.20

Let us design a temperature sensor that operates from a 3-V supply, and has a visual display consisting of five LEDs—that is, light-emitting diodes. Only one LED should be on at any time, indicating one of the following temperature ranges: less than 65, 65 to 70, 70 to 75, 75 to 80, and greater than 80°F.

SOLUTION In our proposed sensor, shown in Fig. 3.38, resistor R_X and a thermistor, R_T (a temperature sensitive resistor), form a voltage divider to produce the voltage V_T.

$$V_T = 3\left[\frac{R_X}{R_T + R_X}\right] \qquad \textbf{3.6}$$

In the temperature range of interest, a curve fit to a particular commercial thermistor's *R-T* data yields

$$R_T = 57.45e^{-0.0227T} \qquad \textbf{3.7}$$

with R_T in kΩ and T in degrees Fahrenheit. From Eqs. (3.6) and (3.7), we see that increasing temperature causes R_T to decrease and V_T to increase. The voltage V_T appears at the unity gain buffer output, where it is divided between R_1, R_2, R_3, and R_4, yielding intermediate voltages V_2, V_3, and V_4. All four comparators and the dc voltage reference, V_{ref}, are contained in the MAX919 package listed in Table 3.4. In this package, $V_{\text{ref}} = 1.245$ V.

Based on fundamental comparator operation, when $V_T < V_{\text{ref}}$, the output voltage of comparator C_1 will be low, near zero volts. Since $V_4 < V_3 < V_2 < V_T$, all the other comparator output voltages will be low as well. Thus, there is no voltage difference across LED_2, LED_3, LED_4, or LED_5, and these LEDs are off. However, the voltage across LED_1 is not zero. Current will flow from the 3-V supply, through R_{LED} and LED_1, into the output terminal of C_1, through its on-chip circuitry, out of the MAX 919 ground pin and back to the 3-V source, turning on LED_1. This is the desired display for $T < 65$°F.

Then, at exactly 65°F, LED_1 should turn off and LED_2 should turn on. This requires the output of C_1 to go high, near 3 V, while all other comparator outputs remain low. Now, only LED_2 has a nonzero voltage across it. This can be seen in the plots in Fig. 3.39.

Both display scenarios (<65° and 65°-70°) will occur properly if $V_T = V_{\text{ref}}$ precisely at $T = 65$°F. Thus, we must find R_X such that $V_T = V_{\text{ref}}$ at 65°F. From Eqs. (3.6) and (3.7),

$$1.245 = 3\left[\frac{R_X}{57.45e^{-0.0227(65)} + R_X}\right]$$

which yields $R_X = 9.32$ kΩ. This is the case until T reaches 70°F, where the output of C_2 must go high, turning off LED_2 and turning on LED_3. Thus, we require $V_2 = V_{\text{ref}}$ at exactly $T = 70$°F. Now, $V_4 < V_3 < V_2 = V_{\text{ref}}$ and $V_T > V_{\text{ref}}$. Repeating this idea at $T = 75$ and 80°F yields the voltage division equations

$$V_2|_{T=70} = 1.245 = \left[\frac{R_2 + R_3 + R_4}{R_\Sigma}\right]V_T|_{T=70}$$

$$V_3|_{T=75} = 1.245 = \left[\frac{R_3 + R_4}{R_\Sigma}\right]V_T|_{T=75}$$

$$V_4|_{T=80} = 1.245 = \left[\frac{R_4}{R_\Sigma}\right]V_T|_{T=80}$$

where $R_\Sigma = R_1 + R_2 + R_3 + R_4$. Arbitrarily selecting R_Σ to be 100 kΩ and using Eqs. (3.6) and (3.7), the required resistor values are $R_4 = 83.11$ kΩ, $R_3 = 5.01$ kΩ, $R_2 = 5.60$ kΩ, and $R_1 = 6.28$ kΩ.

The LEDs employed in this design have a voltage of 2 V when on and a desired current of 1 mA. Consider again the case where LED_1 is on; that is, the output of comparator C_1 is zero. By KVL, we have

$$3 = I_{\text{LED}}R_{\text{LED}} + V_{\text{LED}} = (0.001)R_{\text{LED}} + 2.0$$

yielding $R_{\text{LED}} = 1$ kΩ. Since only one LED is on at any time, there is exactly one resistor, R_{LED}, for every possible display scenario.

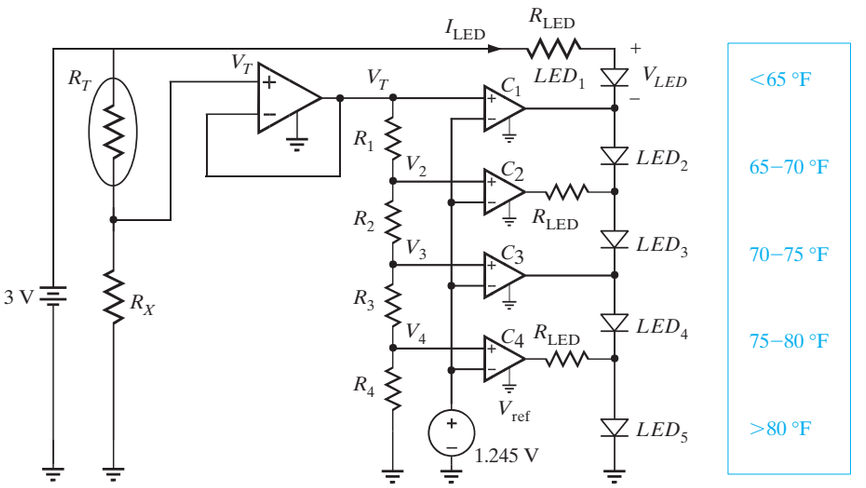


Figure 3.38
The temperature sensor schematic diagram.

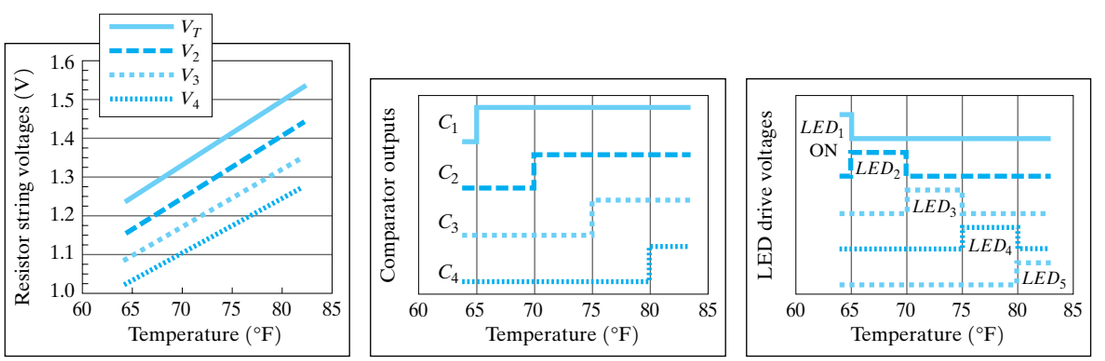


Figure 3.39
Critical voltages in the temperature sensor of Fig. 3.38. Resistor string voltages (a) are compared to V_{ref} to produce the comparator output voltages in (b). Resistors R_X and R_1–R_4 have been selected such that the comparator outputs change exactly at the desired temperature boundaries. The LEDs drive voltages (c) are such that only one LED is on at any time.

LEARNING Check

Summary

- ***Nodal analysis for an N-node circuit***
- Select one node in the N-node circuit as the reference node. Assume that the node voltage is zero and measure all node voltages with respect to this node.
- If only independent current sources are present in the network, write the KCL equations at the $N - 1$ nonreference nodes. If dependent current sources are present, write the KCL equations as is done for networks with only independent current sources; then write the controlling equations for the dependent sources.
- If voltage sources are present in the network, they may be connected (1) between the reference node and a nonreference node or (2) between two nonreference nodes. In the former case, if the voltage source is an independent source, then the voltage at one of the nonreference nodes is known. If the source is dependent, it is treated as an independent source when writing the KCL equations, but an additional constraint equation is necessary.

  In the latter case, if the source is independent, the voltage between the two nodes is constrained by the value of the voltage source and an equation describing this constraint represents one of the $N - 1$ linearly independent equations required to determine the N-node voltages. The surface of the network described by the constraint equation (i.e., the source and two connecting nodes) is called a supernode. One of the remaining $N - 1$ linearly independent equations is obtained by applying KCL at this supernode. If the voltage source is dependent, it is treated as an independent source when writing the KCL equations, but an additional constraint equation is necessary.

- ***Loop analysis for an N-loop circuit***
- One loop current is assigned to each independent loop in a circuit that contains N independent loops.
- If only independent voltage sources are present in the network, write the N linearly independent KVL equations, one for each loop. If dependent voltage sources are present, write the KVL equations as is done for circuits with only independent voltage sources; then write the controlling equations for the dependent sources.
- If current sources are present in the network, either of two techniques can be used. In the first case, one loop current is selected to pass through one of the current sources. This is done for each current source in the network. The remaining loop currents (N − the number of current sources) are determined by open-circuiting the current sources in the network and using this modified network to select them. Once all these currents are defined in the original network, the N-loop equations can be written. The second approach is similar to the first with the exception that if two mesh currents pass through a particular current source, a supermesh is formed around this source. The two required equations for the meshes containing this source are the constraint equations for the two mesh currents that pass through the source and the supermesh equation. If dependent current sources are present, the controlling equations for these sources are also necessary.
- ***Ideal op-amp model*** For an ideal op-amp, $i_x = i_- = 0$ and $v_x = v_-$. Both nodal and loop analysis are useful in solving circuits containing operational amplifiers.

Problems

SECTION 3.1

3.1 Find I_o in the circuit in Fig. P3.1 using nodal analysis.

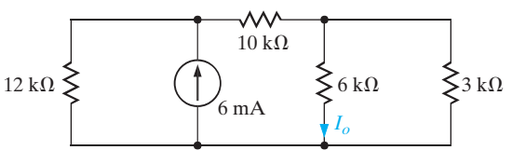


Figure P3.1

3.2 Find I_o in the circuit in Fig. P3.2 using nodal analysis.

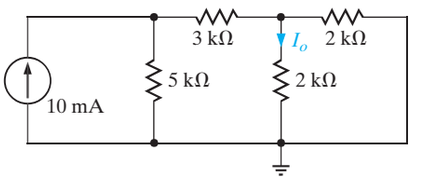


Figure P3.2

3.3 Find V_2 in the circuit in Fig. P3.3 using nodal analysis.

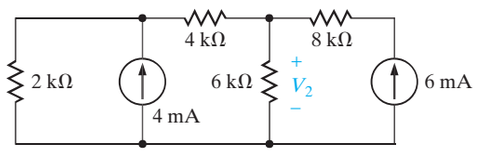


Figure P3.3

3.4 Use nodal analysis to find V_o in the circuit in Fig. P3.4.

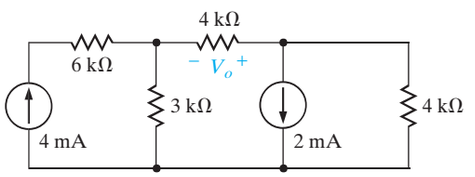


Figure P3.4

3.5 Find I_o in the circuit in Fig. P3.5 using nodal analysis.

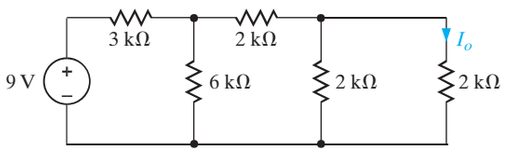


Figure P3.5

3.6 Use nodal analysis to find both V_1 and V_o in the circuit in Fig. P3.6.

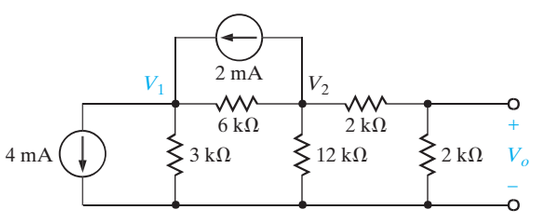


Figure P3.6

3.7 Find V_1 and V_2 in the circuit in Fig. P3.7 using nodal analysis. Then solve the problem using MATLAB and compare your answers.

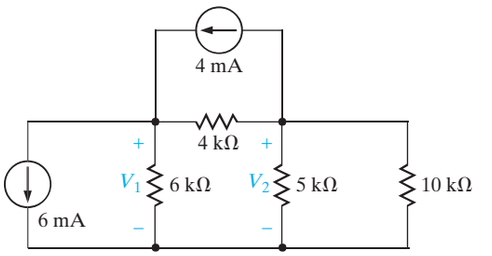


Figure P3.7

3.8 Find I_o in the network in Fig. P3.8 using nodal analysis.

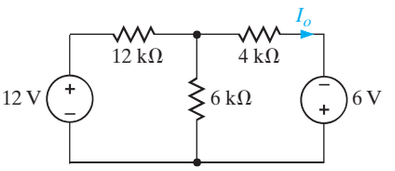


Figure P3.8

3.9 Find V_o in the network in Fig. P3.9 using nodal analysis.

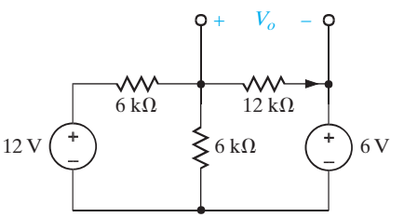


Figure P3.9

3.10 Use nodal analysis to find I_o and I_1 in the network in Fig. P3.10.

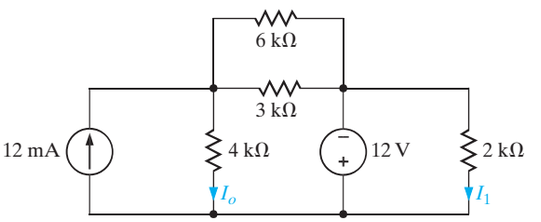


Figure P3.10

3.11 Find I_o in the circuit in Fig. P3.11 using nodal analysis.

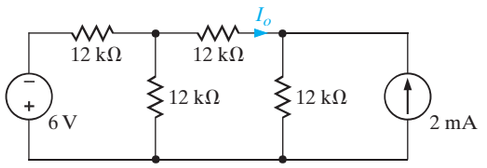


Figure P3.11

3.12 Use nodal analysis to find V_o in the network in Fig. P3.12. Then solve the problem using MATLAB and compare your answers.

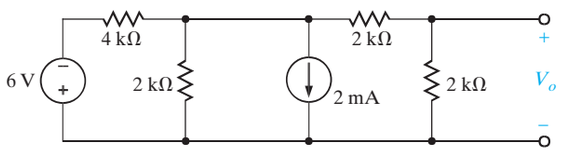


Figure P3.12

3.13 Find I_o in the network in Fig. P3.13.

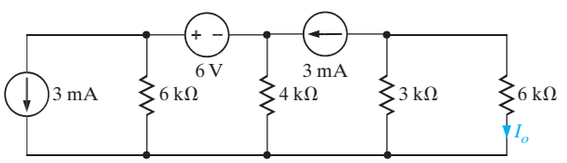


Figure P3.13

3.14 Find V_o in the network in Fig. P3.14.

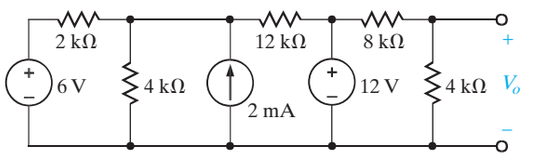


Figure P3.14

3.15 Use nodal analysis to find V_o in the circuit in Fig. P3.15.

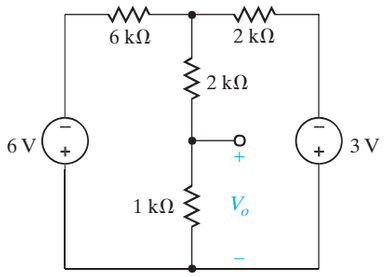


Figure P3.15

3.16 Write the node equations for the circuit in Fig. P3.16 in matrix form, and find all the node voltages using MATLAB.

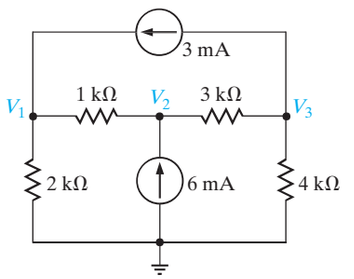


Figure P3.16

3.17 Find I_1 in the network in Fig. P3.17.

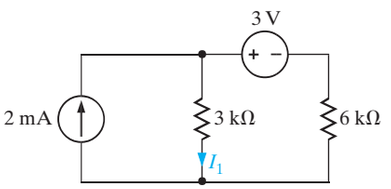


Figure P3.17

3.18 Find I_o in the network in Fig. P3.18.

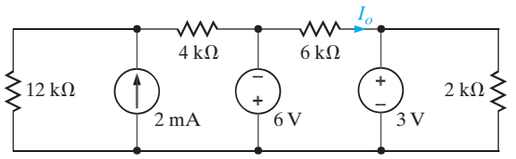


Figure P3.18

3.19 Find I_o in the circuit in Fig. P3.19.

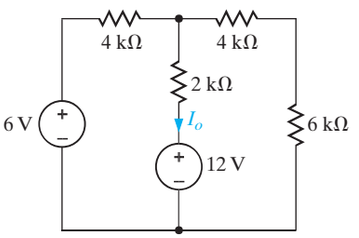


Figure P3.19

3.20 Find I_o in the network in Fig. P3.20 using nodal analysis.

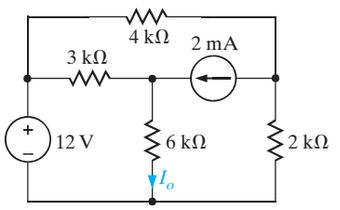


Figure P3.20

3.21 Use nodal analysis to find V_o in the network in Fig. P3.21. Then solve this problem using MATLAB and compare your answers.

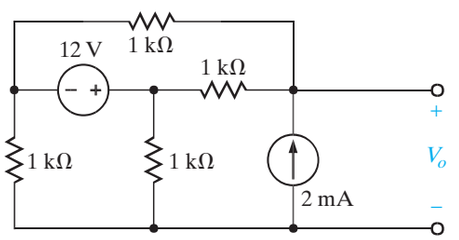


Figure P3.21

3.22 Find V_o in the circuit in Fig. P3.22 using nodal analysis.

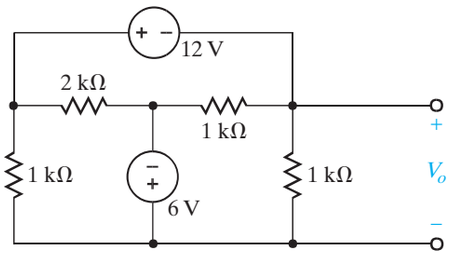


Figure P3.22

3.23 Use nodal analysis to find I_o in the network in Fig. P3.23.

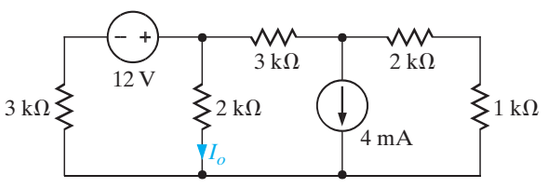


Figure P3.23

3.24 Find I_o in the network in Fig. P3.24 using nodal analysis.

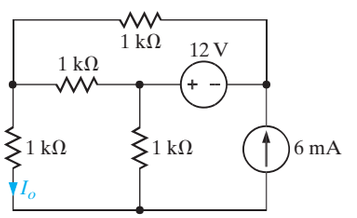


Figure P3.24

3.25 Use nodal analysis to find V_o in the circuit in Fig. P3.25.

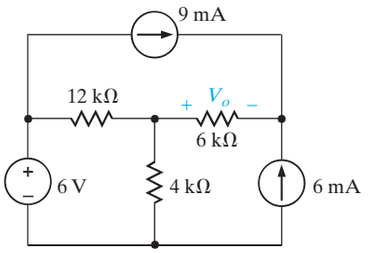


Figure P3.25

3.26 Find V_o in the circuit in Fig. P3.26 using nodal analysis.

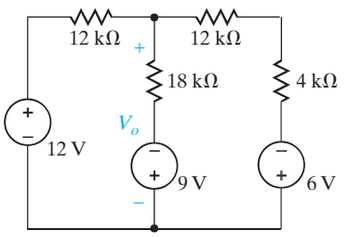


Figure P3.26

3.27 Find V_o in the network in Fig. P3.27 using nodal analysis.

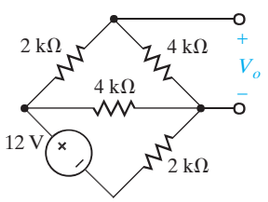


Figure P3.27

3.28 Find V_o in the network in Fig. P3.28 using nodal analysis.

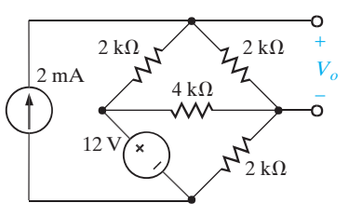


Figure P3.28

3.29 Find V_o in the network in Fig. P3.29 using nodal analysis.

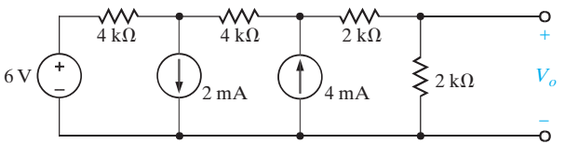


Figure P3.29

3.30 Find I_o in the circuit in Fig. P3.30 using nodal analysis.

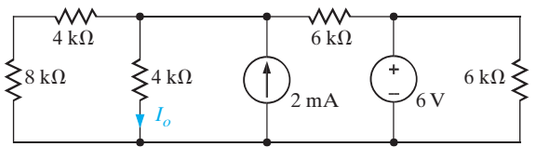


Figure P3.30

3.31 Find V_o in the circuit in Fig. P3.31 using nodal analysis.

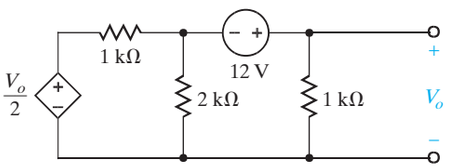


Figure P3.31

3.32 Use nodal analysis to find V_o in the network in Fig. P3.32.

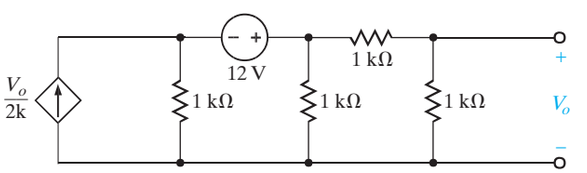


Figure P3.32

3.33 Find V_o in the circuit in Fig. P3.33 using nodal analysis. Then solve the problem using MATLAB and compare your answers.

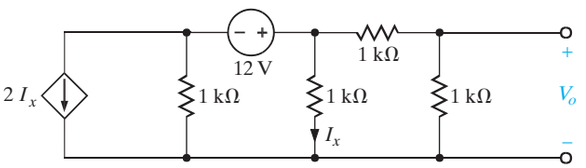


Figure P3.33

3.34 Find I_o in the network in Fig. P3.34.

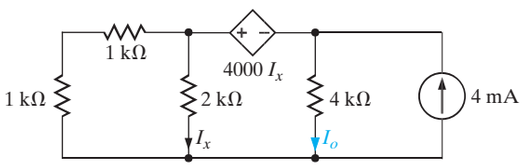


Figure P3.34

3.35 Find V_o in the circuit in Fig. P3.35 using nodal analysis.

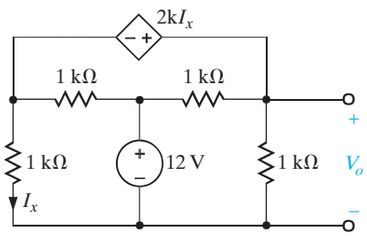


Figure P3.35

3.36 Find I_o in the circuit in Fig. P3.36 using nodal analysis.

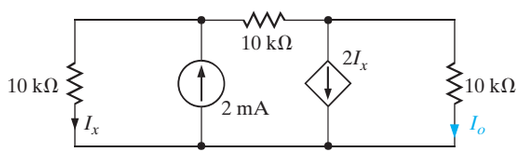


Figure P3.36

3.37 Find V_o in the network in Fig. P3.37 using nodal analysis.

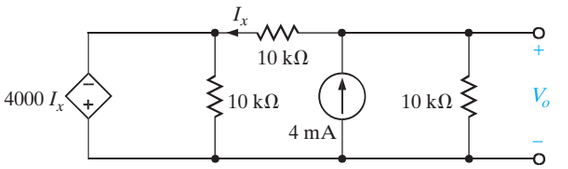


Figure P3.37

3.38 Use nodal analysis to find V_o in the network in Fig. P3.38. In addition, determine all branch currents and check KCL at every node.

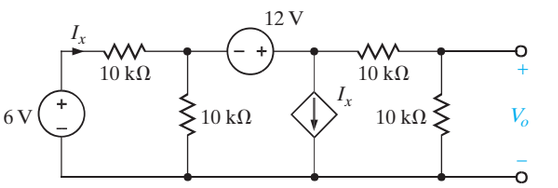


Figure P3.38

3.39 Use nodal analysis to find V_o in the circuit in Fig. P3.39.

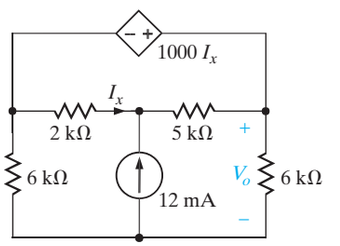


Figure P3.39

3.40 Use nodal analysis to find V_o in the circuit in Fig. P3.40.

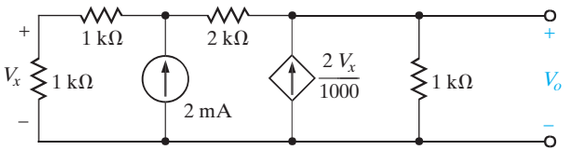


Figure. P3.40

3.41 Use MATLAB to find the node voltages in the network in Fig. P3.41.

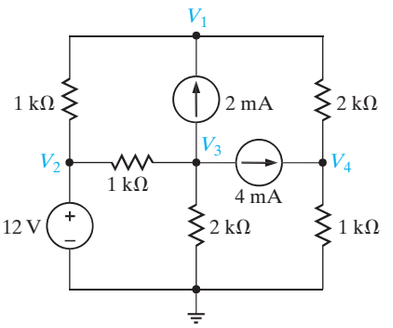


Figure P3.41

SECTION 3.2

3.42 Use mesh equations to find V_o in the circuit in Fig. P3.42.

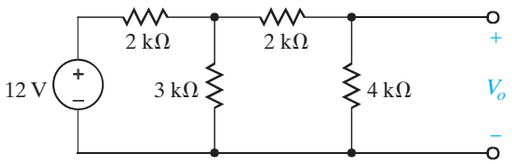


Figure P3.42

3.43 Find V_o in the network in Fig. P3.43 using mesh equations.

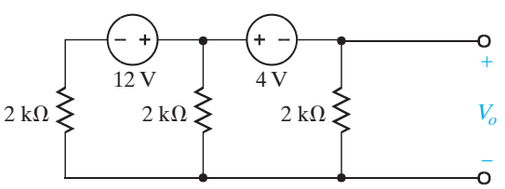


Figure P3.43

3.44 Use mesh analysis to find V_o in the circuit in Fig. P3.44.

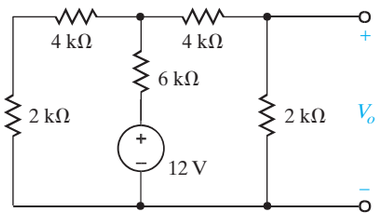


Figure P3.44

3.45 Use mesh analysis to find V_o in the network in Fig. P3.45.

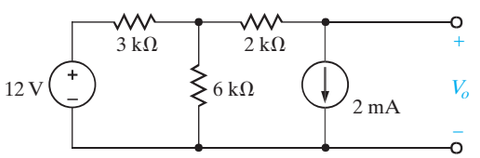


Figure P3.45

3.46 Use loop analysis to find V_o in the circuit in Fig. P3.46.

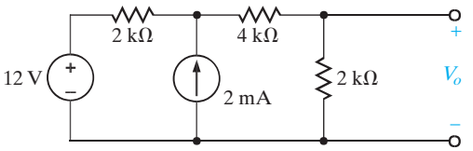


Figure P3.46

3.47 Use loop analysis to find I_o in the circuit in Fig. P3.47.

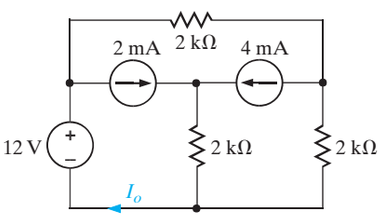


Figure P3.47

3.48 Use both nodal analysis and mesh analysis to find I_o in the circuit in Fig. P3.48.

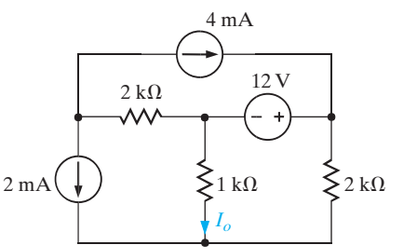


Figure P3.48

3.49 Find I_o in the network in Fig. P3.49 using mesh analysis.

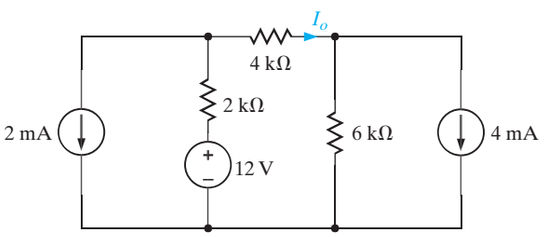


Figure P3.49

3.50 Find I_o in the network in Fig. P3.50 using mesh analysis.

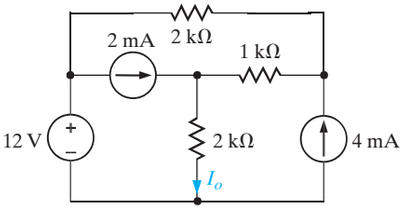


Figure P3.50

3.51 Find V_o in the circuit in Fig. P3.51 using mesh analysis.

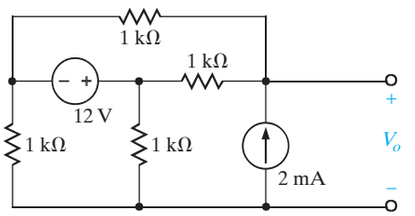


Figure P3.51

3.52 Use loop analysis to find V_o in the network in Fig. P3.52.

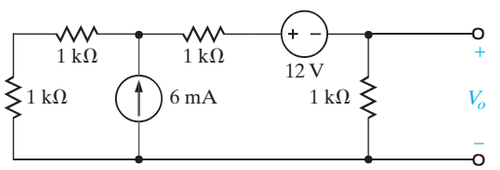


Figure P3.52

3.53 Find I_o in the network in Fig. P3.53 using loop analysis. Then solve the problem using MATLAB and compare your answers.

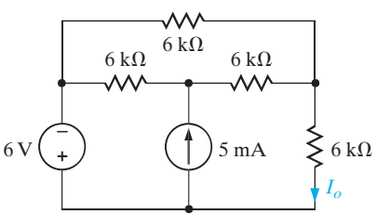


Figure P3.53

3.54 Use loop analysis to find I_o in the circuit in Fig. P3.54.

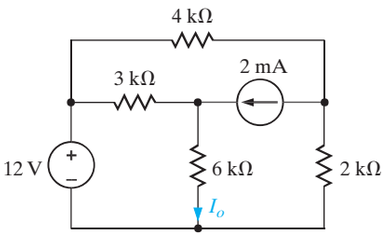


Figure P3.54

3.55 Find V_o in the network in Fig. P3.55 using both mesh and nodal analyses.

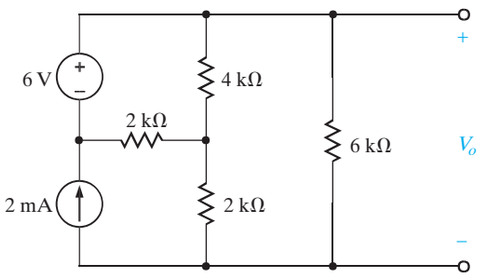


Figure P3.55

3.56 Use loop analysis to find V_o in the circuit in Fig. P3.56.

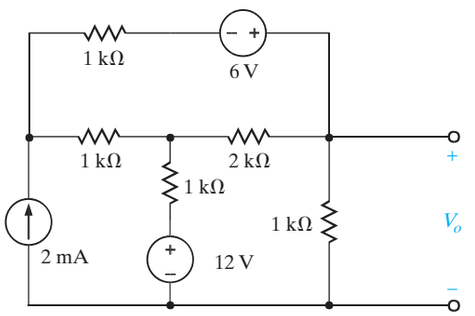


Figure P3.56

3.57 Use loop analysis to find I_o in the network in Fig. P3.57.

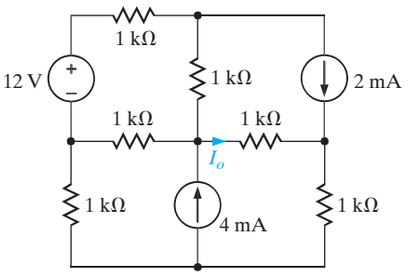


Figure P3.57

3.58 Use loop analysis to find V_o in the network in Fig. P3.58.

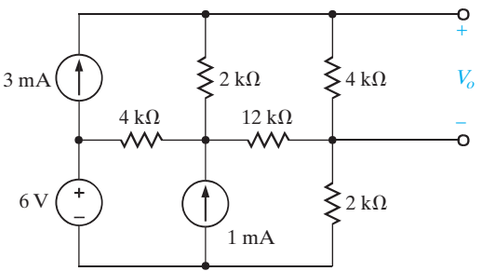


Figure P3.58

3.59 Find V_o in the network in Fig. P3.59.

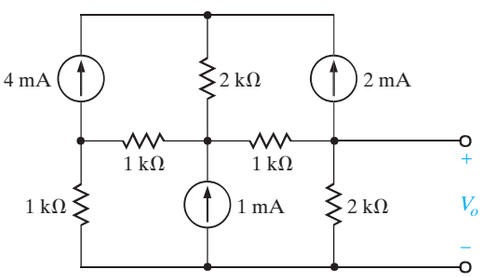


Figure P3.59

3.60 Find V_o in the circuit in Fig. P3.60.

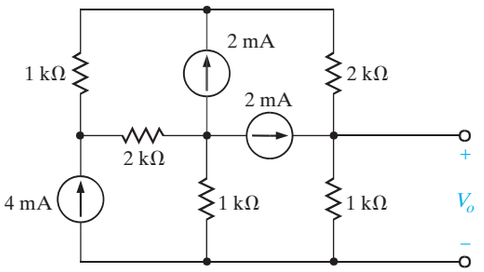


Figure P3.60

3.61 Find I_o in the circuit in Fig. P3.61.

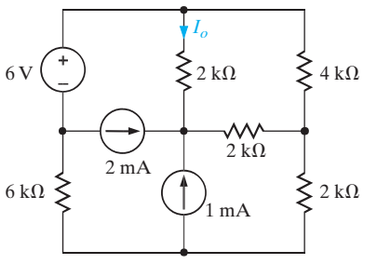


Figure P3.61

3.62 Use loop analysis to find V_o in the network in Fig. P3.62.

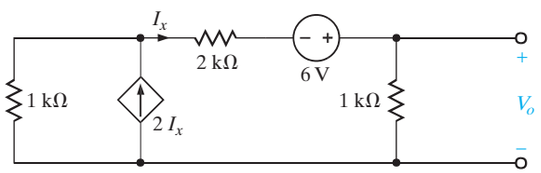


Figure P3.62

3.63 Use mesh analysis to find V_o in the circuit in Fig. P3.63.

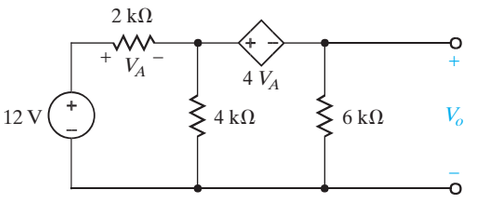


Figure P3.63

3.64 Use loop analysis to find V_o in the circuit in Fig. P3.64.

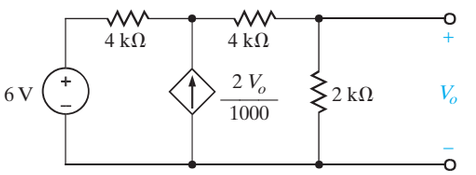


Figure P3.64

3.65 Find V_o in the circuit in Fig. P3.65 using mesh analysis.

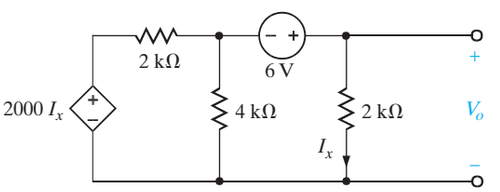


Figure P3.65

3.66 Use both nodal analysis and mesh analysis to find V_o in the circuit in Fig. P3.66.

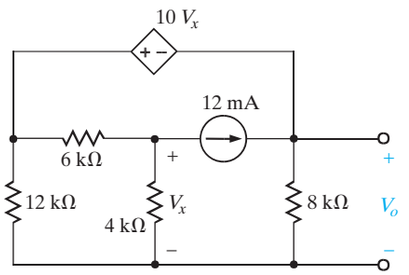


Figure P3.66

3.67 Using mesh analysis, find V_o in the circuit in Fig. P3.67.

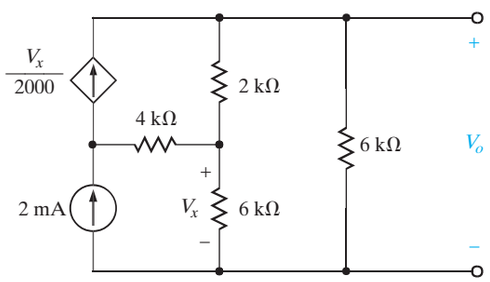


Figure P3.67

3.68 Find V_o in the network in Fig. P3.68.

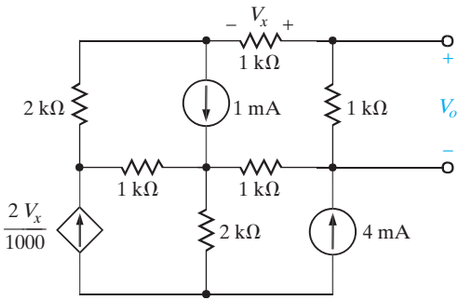


Figure P3.68

3.69 Use MATLAB to find the mesh currents in the network in Fig. P3.69.

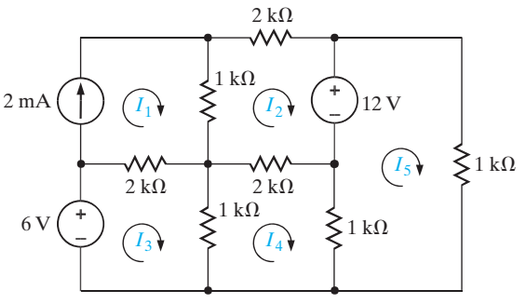


Figure P3.69

SECTION 3.3

Assume that all op-amps in this section are ideal.

3.70 Find V_o in the circuit in Fig. P3.70.

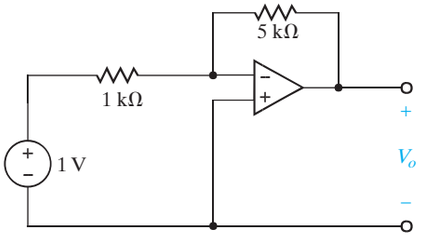


Figure P3.70

3.71 Find V_o in the network in Fig. P3.71 and explain what effect R_1 has on the output.

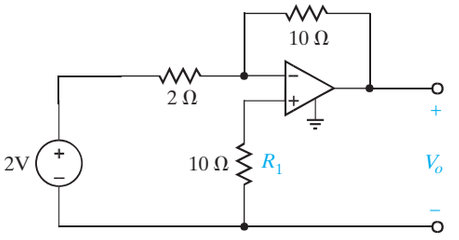


Figure P3.71

3.72 Find V_o in the network in Fig. P3.72.

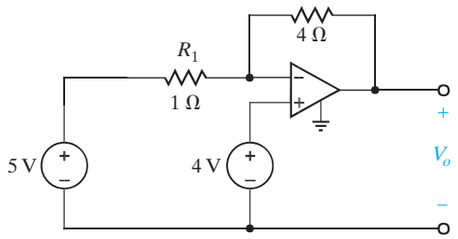


Figure P3.72

3.73 The network in Fig. P3.73 is a current-to-voltage converter or transresistance amplifier. Find v_o/i_S for this network.

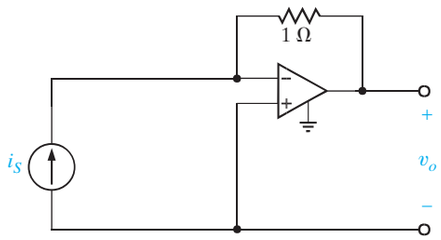


Figure P3.73

3.74 Find V_o in the circuit in Fig. P3.74.

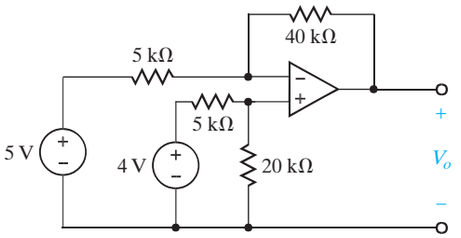


Figure P3.74

3.75 Find V_o in the circuit in Fig. P3.75.

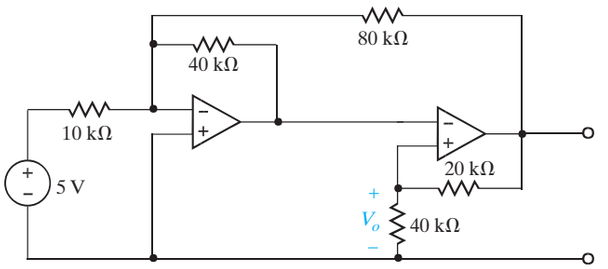


Figure P3.75

Typical Problems Found on the FE Exam

3FE-1 Find V_o in the circuit in Fig. 3PFE-1.

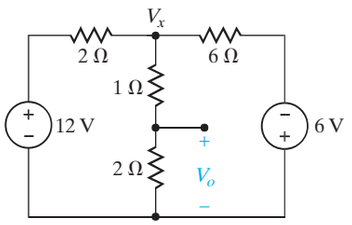


Figure 3PFE-1

3FE-2 Determine the power dissipated in the 6-ohm resistor in the network in Fig. 3PFE-2.

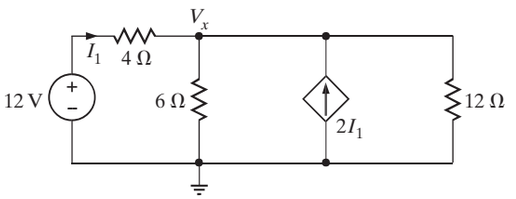


Figure 3PFE-2

3FE-3 Find the current I_x in the 4-ohm resistor in the circuit in Fig. 3PFE-3.

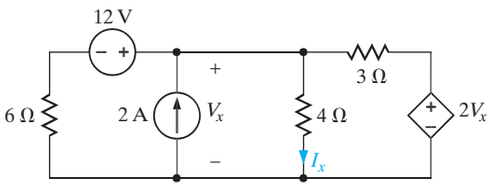


Figure 3PFE-3

3FE-4 Determine the voltage V_o in the circuit in Fig. 3PFE-4.

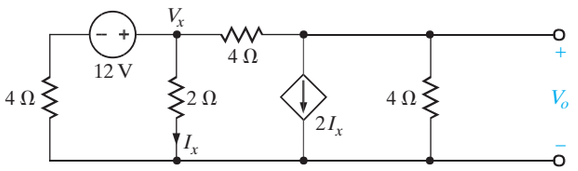


Figure 3PFE-4

3FE-5 Given the summing amplifier shown in Fig. 3PFE-5, select the values of R_2 that will produce an output voltage of −3 V.

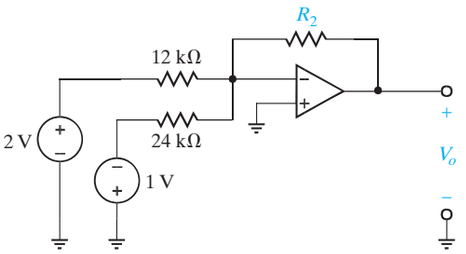


Figure 3PFE-5

3FE-6 Determine the output voltage V_o of the summing op-amp circuit shown in Fig. 3PFE-6.

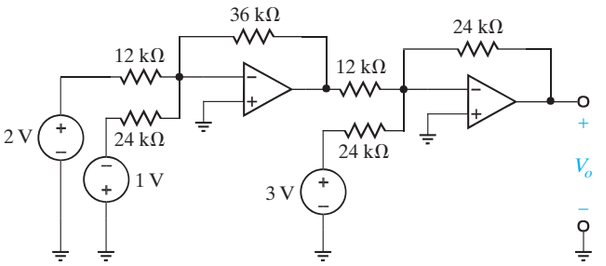


Figure 3PFE-6