

Integrated Circuit Design with the MOSFET

9

The MOSFET has become more popular in circuit design in the last decade, especially for mixed-signal circuits that combine both digital and analog circuits on a single chip. With the improvements in high-frequency performance, the MOSFET can compete with the BJT up to frequencies in the low GHz range. Of course, the heterojunction BJT can operate at much higher frequencies than this, approaching frequencies of 100 GHz.

This chapter will consider several configurations of amplifying stages used in MOSFET amplifier design. Each configuration is analyzed in terms of midband voltage gain, upper corner frequency, and the size of the output active region.

Design of MOSFET circuits is considerably different from the design of BJT circuits. For example, the dimensions of the channel are used as part of the design procedure in MOSFET circuits. The width of the channel affects the transconductance, the output resistance and capacitance, and the midband voltage gain of the stage. The specification of channel width is often one step in the design of a MOSFET amplifier stage. In digital circuits, the width and the length are generally of the same order of magnitude. In amplifier design, the dimension of channel width may be hundreds of times greater than the channel length to achieve high values of voltage gain. Such considerations are not necessary in BJT amplifier design, which provides one reason for covering BJT design in a separate chapter. The next chapter will consider the BJT.

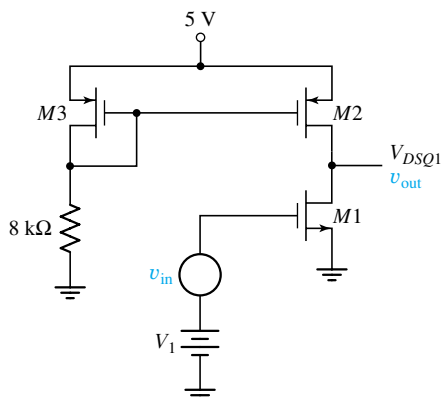
One circuit that is very significant in IC design is the current mirror. This circuit not only provides bias for amplifier stages, it also provides an incremental resistive load for various amplifier stages. The first section of this chapter will discuss some basic configurations of this important circuit, before moving to various amplifier configurations.

9.1 MOSFET Current Mirrors

9.2 Amplifier Configurations for MOSFET Integrated Circuits

DEMONSTRATION PROBLEM

The circuit shown is a common-source amplifier with a current mirror load. If $K_n = \mu_n C_{ox} W_n / 2L_n = 0.12 \text{ mA/V}^2$, $K_p = \mu_p C_{ox} W_p / 2L_p = 0.1 \text{ mA/V}^2$, $\lambda_n = \lambda_p = 0.01 \text{ V}^{-1}$, and $V_{Tn} = -V_{Tp} = 1 \text{ V}$, find V_1 to set $V_{DSQ1} = 2.5 \text{ V}$. Calculate the midband voltage gain of the amplifier.



Amplifier for Demonstration Problem

This problem requires a knowledge of the dc current versus voltage relationships of the MOSFETs to find the bias voltage, V_1 . A knowledge of the incremental equivalent circuit for the MOSFET is needed to calculate the midband voltage gain.

9.1 MOSFET Current Mirrors

IMPORTANT Concepts

1. A simple MOSFET current mirror is constructed in the same configuration as that of the BJT current mirror.
2. The ratio of output to input current can be determined by the aspect ratios of the two devices.
3. The Wilson current mirror can be used to achieve higher output impedance for the output device.

The BJT current mirror was developed in the 1960s for use in op amp circuits. As the MOSFET increased in capability, the MOSFET current mirror evolved from the BJT circuit. MOSFET current mirrors operate on similar principles to the BJT mirrors to be discussed in Chapter 10 and use similar configurations. One advantage of MOSFET current mirrors over BJT mirrors is that the MOS devices draw zero control current. The BJT stages exhibit small errors due to the finite base currents required. On the other hand, the matching of threshold voltages on MOS devices is generally not as good as the V_{BE} matching of bipolar devices. Since BJT mirrors require additional considerations beyond those of MOSFET mirrors, a more thorough discussion of this circuit appears in Chapter 10.

Figure 9.1 shows a simple nMOS current mirror consisting of two matched devices, $M1$ and $M2$. This current mirror may be used to create a constant bias current for an IC amplifier stage. Integrated circuits provide the capability of matching device characteristics quite closely and the current mirror takes advantage of this capability. In the circuit of Fig. 9.1, the current I_o is intended to be equal to I_{in} . Although not shown in the figure, the external circuit through which I_o flows connects to the drain of $M2$. The current I_{in} equals the drain current of $M1$ whereas I_o is the drain current of $M2$.

Device $M1$ is in its active region, since drain current is flowing and the drain voltage equals the gate voltage. With V_{DS2} sufficiently positive to put $M2$ in the active region, the

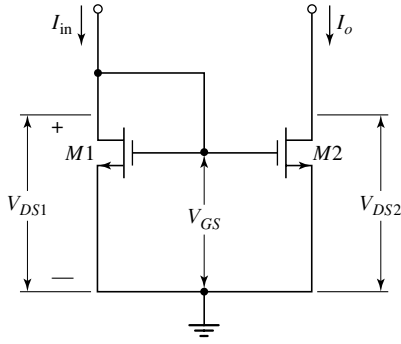


Figure 9.1
A simple nMOS current mirror (sink).

ratio of output current, I_o , to input current, I_{in} , can be expressed as

$$\frac{I_o}{I_{in}} = \left[\frac{L_1 W_2}{L_2 W_1} \right] \left[\frac{V_{GS} - V_{T2}}{V_{GS} - V_{T1}} \right]^2 \left[\frac{1 + \lambda_2(V_{DS2} - V_{DSP2})}{1 + \lambda_1(V_{DS1} - V_{DSP1})} \right] \left[\frac{\mu_2 C_{ox2}}{\mu_1 C_{ox1}} \right] \quad (9.1)$$

In ICs, it is possible to match devices so that $\mu_1 C_{ox1} = \mu_2 C_{ox2}$, $V_{T1} = V_{T2}$, and $\lambda_1 \approx \lambda_2$. With these conditions satisfied, Eq. (9.1) can be written as

$$\frac{I_o}{I_{in}} = \left[\frac{L_1 W_2}{L_2 W_1} \right] \left[\frac{1 + \lambda(V_{DS2} - V_{DSP2})}{1 + \lambda(V_{DS1} - V_{DSP1})} \right] \quad (9.2)$$

As a result of the connection between gate and source of $M1$, $V_{DS1} = V_{GS}$ and, since $V_{DSP1} = V_{GS} - V_{T1}$, we can simplify the denominator of Eq. (9.2) further. We can express $[1 + \lambda(V_{DS1} - V_{DSP1})]$ as

$$[1 + \lambda(V_{GS} - V_{GS} + V_{T1})] = 1 + \lambda V_{T1}$$

Finally, if we limit the output voltage such that $V_{DS2} = V_{DS1}$, Eq. (9.2) reduces to

$$\frac{I_o}{I_{in}} = \frac{L_1 W_2}{L_2 W_1} \quad (9.3)$$

This equation indicates that in the simple MOSFET current mirror, the ratio of I_o to I_{in} may be scaled to any desired value by scaling the aspect ratios (W/L) of the devices.

There are three effects that cause the MOSFET current mirror performance to differ from that predicted by Eq. (9.3). These are:

1. Channel length modulation as V_{DS2} changes, as predicted by Eq. (9.2)
2. Threshold voltage mismatch
3. Imperfect geometrical matching

EXAMPLE 9.1

Assume that a matched pair of MOSFETs are used in the current mirror of Fig. 9.1 with values of $\lambda = 0.032 \text{ V}^{-1}$, $\mu C_{ox} = 70 \text{ } \mu\text{A}/\text{V}^2$, $W/2L = 10$, and $V_T = 0.9 \text{ V}$. If a 5-V source in series with a resistor, R , is connected to the drain of $M1$ to create the input current, calculate the value of R needed to create an input current of $100 \text{ } \mu\text{A}$. Calculate the output current when $V_{DS2} = 3 \text{ V}$.

SOLUTION From the equation for drain current in the active region we write

$$I_{D1} = \frac{\mu C_{ox} W}{2L} [V_{GS} - V_T]^2 [1 + \lambda(V_{DS1} - V_{DSP1})]$$

Since $V_{DS1} = V_{GS}$ and $V_{DSP1} = V_{GS} - V_T$, this equation can be expressed as

$$I_{D1} = 100 = 700 [V_{GS} - 0.9]^2 [1 + 0.032 \times 0.9]$$

We can now solve for the value of V_{GS} to result in the specified drain current. This value is $V_{GS} = 1.27$ V. The resistance needed to create 100 μ A of drain current is

$$R = \frac{5 - V_{DS1}}{I_{D1}} = \frac{5 - 1.27}{0.1} = 37.3 \text{ k}\Omega$$

The output current is calculated from

$$I_{D2} = \frac{\mu C_{ox} W}{2L} [V_{GS} - V_T]^2 [1 + \lambda(V_{DS2} - V_{DSP2})]$$

In this case, $V_{DS2} - V_{DSP2} = V_{DS2} - (V_{GS} - V_T) = 3 - 1.27 + 0.9 = 2.63$ V. The output current is then $I_o = 104 \mu\text{A}$.

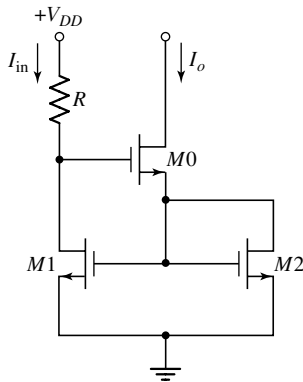


Figure 9.2
nMOS version of the Wilson current mirror.

A MOSFET version of the BJT Wilson current mirror, discussed in Chapter 10, may be used to reduce the output compliance error of the mirror. Figure 9.2 illustrates such an nMOS mirror.

For matched devices, the current I_{in} may be expressed as

$$I_{in} = \frac{V_{DD} - 2V_{GS}}{R} \quad (9.4)$$

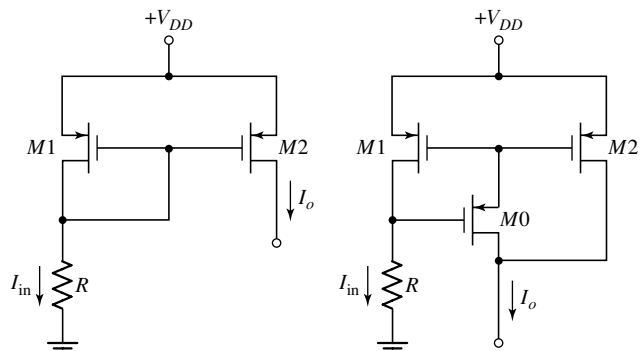
where V_{GS} is the gate-to-source voltage of all three devices. The output current is then

$$I_o = I_{in} \left[\frac{L_1 W_2}{L_2 W_1} \right] \quad (9.5)$$

The voltage at the drain of $M2$ remains constant at a value of V_{GS} , keeping I_o constant, as the output voltage at the drain of $M0$ varies over a large range. This stage has a higher output impedance than that of the simple current mirror because it has a source impedance. Device $M2$ presents an impedance between drain and ground that equals $1/g_{m2}$, thus increasing the output impedance of $M0$. A higher output impedance leads to a smaller current change with output voltage.

It is also possible to create current mirror sources with almost identical performance to these sinks by using pMOS devices. Figure 9.3 shows a simple mirror and a Wilson-type mirror using pMOS devices.

Figure 9.3
Current sources: (a) simple mirror, (b) Wilson mirror.



PRACTICE Problems

9.1 For the finished design of Example 9.1, calculate the output current when $V_{DS2} = 4$ V. *Ans:* 107 μ A.

9.2 At what voltage must V_{DS2} be in the current mirror of Example 9.1 to cause an output current of 102 μ A? *Ans:* 2.37 V.

9.3 Using the device parameters of Example 9.1, select the resistance R of this example to lead to an output current of 180 μ A when $V_{DS2} = 4$ V. *Ans:* $R = 22.3 \text{ k}\Omega$.

in critical circuit design, the remainder of this chapter will apply the simple mirror of this section.

9.2 Amplifier Configurations for MOSFET Integrated Circuits

IMPORTANT Concepts

1. Most MOSFET IC amplifier stages do not use a resistor as the load for the amplifying stage.
2. The load is generally created by one or more other MOS devices. These devices are called active loads.
3. Active load stages can lead to very high voltage gains.
4. The ratio of channel width to channel length, called the aspect ratio, is quite significant in MOSFET circuit design.

In amplifier design, MOS circuits have become increasingly important, but not to the extent of CMOS digital circuits. Many of the MOSFET designs are nMOS or pMOS circuits rather than CMOS circuits, but may be referred to as CMOS designs, because an established CMOS process is used to create the design even though no devices appear in the complementary or CMOS configuration.

Whereas digital circuit design almost eliminates the need for resistors or capacitors, analog circuit design may use resistors or capacitors in the design of amplifiers. It is useful to minimize the need for these elements, since they may occupy spaces in which tens or hundreds of MOS devices may fit. In the next few subsections we will discuss MOSFET amplifier configurations. Before proceeding to these amplifiers, some useful relations for the MOSFET will be tabulated. These are written in terms of an nMOS device in Table 9.1 and were derived in Chapter 6.

9.2.1 SIMPLE AMPLIFIER STAGES

A simple stage that can produce a controlled voltage gain is the diode-connected load stage, shown in Fig. 9.4. The numbers in circles represent the node numbers to be used in a later

PRACTICE Problem

9.4 A MOSFET has values of $g_m = 500 \mu\text{A/V}$ and $r_{ds} = 130 \text{ k}\Omega$ at $I_D = 120 \mu\text{A}$. Approximate the values of g_m and r_{ds} for this device at $I_D = 1 \text{ mA}$.
Ans: $g_m = 1.44 \text{ mA/V}$,
 $r_{ds} = 15.6 \text{ k}\Omega$.

Table 9.1 Useful Relations for an nMOS Device

DC Equations

$V_{\text{eff}} = V_{GS} - V_T$	Positive for triode or active region
$V_{DSP} = V_{GS} - V_T = V_{\text{eff}}$	Zero or negative for subthreshold or cutoff
$I_D = \frac{\mu C_{\text{ox}} W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$	Drain-source pinchoff voltage
$I_D = \frac{\mu C_{\text{ox}} W}{2L} [V_{GS} - V_T]^2 [1 + \lambda(V_{DS} - V_{\text{eff}})]$	Borders triode and active region
	Triode region
	Active region

Small-Signal Equations

$g_m = \sqrt{2\mu C_{\text{ox}}(W/L)I_D} = \frac{2I_D}{V_{\text{eff}}}$	Transconductance
$r_{ds} = \frac{1}{\lambda I_{DP}}$	Drain-source resistance

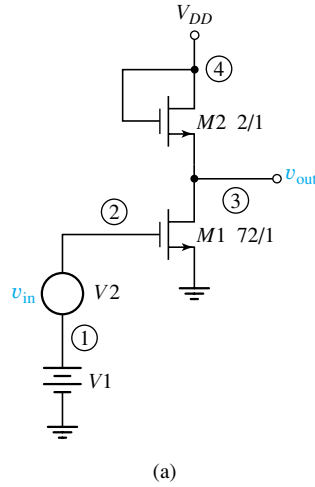
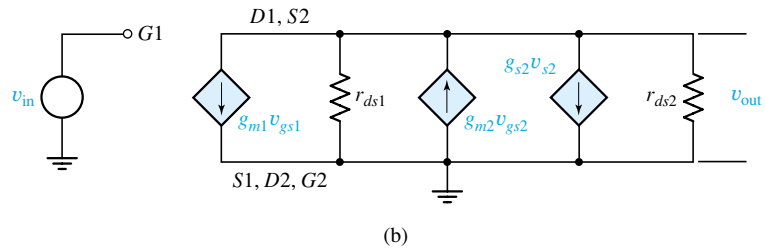


Figure 9.4
 (a) An amplifier with a diode-connected load.
 (b) Equivalent circuit.



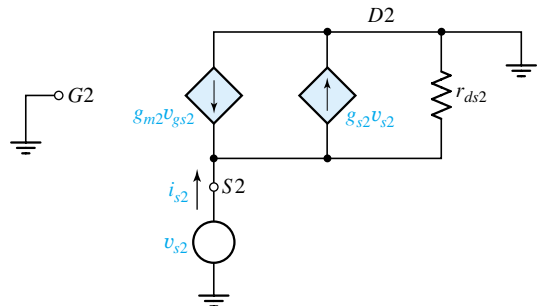
simulation. This amplifier configuration demonstrates several important points relating to general MOSFET IC amplifier design. The transconductance term, g_{s2} , accounts for the body effect as the source to body voltage changes in device $M2$.

The amplifier can be treated as a gain stage, $M1$, driving a load impedance where the load impedance is that looking into the source of $M2$. Figure 9.5 shows the model for $M2$ used to calculate the impedance at the source terminal. The impedance, R_{S2} , looking into $S2$ can be found by assuming that a voltage, v_{s2} , is applied to $S2$. The resulting current is calculated and divided into v_{s2} to find R_{S2} .

With the gate voltage of $M2$ tied to ground, the gate-to-source voltage reduces to $v_{gs2} = v_{g2} - v_{s2} = -v_{s2}$. When v_{s2} is applied to the source of $M2$, the current into this terminal is

$$i_{s2} = g_{m2}v_{s2} + g_{s2}v_{s2} + \frac{v_{s2}}{r_{ds2}}$$

Figure 9.5
 Circuit used for impedance calculation.



The impedance looking into this terminal is then

$$R_{S2} = \frac{v_{s2}}{i_{s2}} = \frac{1}{g_{m2} + g_{s2} + g_{ds2}} \quad (9.6)$$

where $g_{ds2} = 1/r_{ds2}$.

The midband voltage gain is found by recognizing that device $M1$ sees this load in parallel with its own output impedance, r_{ds1} . This parallel resistance is the output resistance, R_{out} , which can be expressed as

$$R_{out} = r_{ds1} \parallel R_{S2} = \frac{1}{g_{m2} + g_{s2} + g_{ds2} + g_{ds1}} \quad (9.7)$$

The midband voltage gain is then

$$A_{MB} = -g_{m1} R_{out} = -\frac{g_{m1}}{g_{m2} + g_{s2} + g_{ds2} + g_{ds1}} \quad (9.8)$$

Typically, the largest term in the denominator will be g_{m2} , which allows the gain to be approximated by

$$A_{MB} \approx -\frac{g_{m1}}{g_{m2}} \quad (9.9)$$

For example, a $1\text{-}\mu$ device ($L = 1\mu$) may have values of $g_m = 0.2$ mA/V, $g_s = 0.022$ mA/V, and $g_{ds} = 0.001$ mA/V, which leads to a 12% error in the approximation of Eq. (9.9).

Examination of Eq. (9.9) shows that, for higher gains, g_{m1} must be much larger than g_{m2} , which can be accomplished by controlling the aspect ratios (W/L) of the two devices. The approximate variation of gain with device scaling can be derived from a consideration of the equation for transconductance in the active region. This equation is found from Table 9.1 and is

$$g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D} \quad (9.10)$$

Since the drain currents of both devices are equal, the voltage gain approximation of Eq. (9.9) can now be written as

$$A_{MB} \approx -\frac{\sqrt{2\mu_n C_{ox}(W_1/L_1)I_D}}{\sqrt{2\mu_n C_{ox}(W_2/L_2)I_D}} = -\left[\frac{(W_1/L_1)}{(W_2/L_2)}\right]^{1/2} \quad (9.11)$$

It can be seen from Eq. (9.11) that the magnitude of the voltage gain varies as the square root of the ratio of aspect ratios. If a gain of -6 is required, both devices can have the same channel length with device $M1$ using a channel width that is 36 times that of $M2$.

We recognize that the actual gain may be slightly lower than the value indicated by Eq. (9.11), but the approximation is sufficient to begin a design that can be “tweaked” during simulation.

One consideration that becomes more important as power-supply voltages are lowered in value is that of *headroom*. This term is used to indicate how much of the output voltage swing cannot be used if serious distortion is to be avoided. If a stage that uses a 5-V dc power supply has a headroom of 1.2 V, then the maximum usable output voltage range is $5 - 1.2 = 3.8$ V. For the circuit of Fig. 9.4, the output can be driven to within a few tenths of a volt of ground by a positive input signal. The drain voltage can swing to its pinchoff

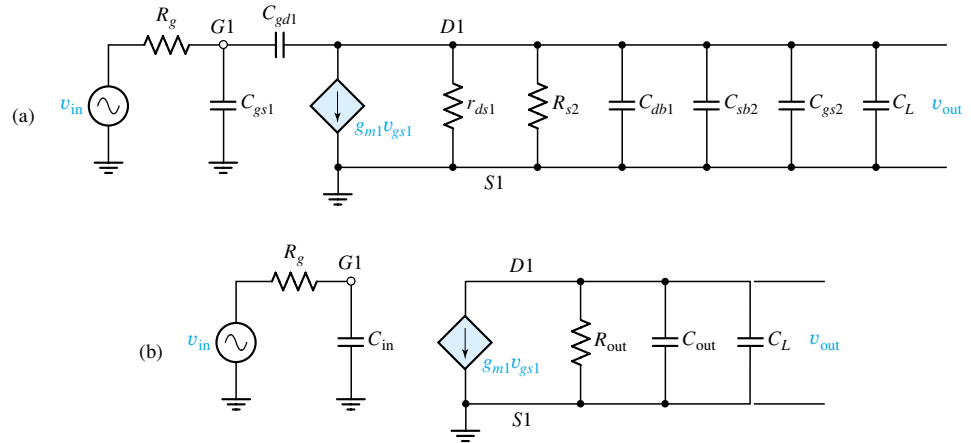


Figure 9.6
 (a) High-frequency model of diode-connected load stage.
 (b) Simplified high-frequency model.

value, which is $V_{GS1} - V_{Tn} = V_{eff1}$. This value is often near 200–300 mV. When the output swings positive, the load device must continue to conduct current; thus the gate-to-source voltage must equal or exceed the threshold voltage plus the effective voltage. The headroom for this stage is then a few tenths of a volt, perhaps 0.3 V, plus the threshold voltage of $M2$. This headroom voltage is approximately V_{GS1} .

The upper corner frequency of an amplifier stage is often significant, but depends on generator resistance and load capacitance as well as on the stage itself. Figure 9.6(a) shows the high-frequency model for this stage including a load capacitance and a generator resistance. Capacitor C_{gd} is gate-to-drain capacitance, C_{gs} is gate-to-source capacitance, C_{db} is drain-to-bulk capacitance, and C_{sb} is the source-to-bulk capacitance. The capacitance C_{gd1} bridges the input and output nodes and can be reflected to the input and output terminals using the Miller effect. The input capacitance of Fig. 9.6(b) is $C_{in} = C_{gs1} + (1 + |A_{MB}|)C_{gd1}$, and the output capacitance is $C_{out} = C_{gd1} + C_{db1} + C_{sb2} + C_{gs2}$.

From Eq. (9.7), the output resistance seen by the output capacitance is

$$R_{out} = \frac{1}{g_{m2} + g_{ds1} + g_{s2} + g_{ds2}} \approx \frac{1}{g_{m2} + g_{s2}} \quad (9.12)$$

The amplifying stage has two upper corner frequencies; one caused by the input circuit and one caused by the output circuit. These frequencies are calculated by

$$f_{in-high} = \frac{1}{2\pi R_g C_{in}} \quad (9.13)$$

$$f_{out-high} = \frac{1}{2\pi R_{out}(C_{out} + C_L)} \quad (9.14)$$

Depending on circuit values, these frequencies may be widely or narrowly separated. If widely separated—for example, if the higher one is at least 5 times the lower frequency—then the lower frequency approximates the overall upper corner frequency, $f_{2\phi}$. If the two frequencies are less than a factor of five different, the method of Chapter 3 must be used to calculate the overall upper corner frequency.

The circuit of Fig. 9.4, implemented on a 0.5- μ process, but with gate lengths of 1 μ , is simulated by PSpice[®] to demonstrate several of the points made in this section. The Spice netlist file is shown in Table 9.2. A 5-V power supply is used.

Table 9.2 Spice Netlist File for Amplifier with Diode-Connected Load

```

CH9.CIR

V1 1 0 1.0V
V2 2 1 AC 0.005V
V3 4 0 5V
M1 3 2 0 0 N L=1U W=72U AD=360P AS=360P PD=82U PS=82U
M2 4 4 3 0 N L=1U W=2U AD=10P AS=10P PD=12U PS=12U
.AC DEC 10100 1000MEG
.OP
.PROBE
.LIB C5X.LIB
.END

```

This program uses a model for the MOSFETs named C5X.LIB.

PRACTICAL Considerations

In specifying a MOSFET device for analysis by Spice, the length and width of the channel are first specified. The surface area of the drain and source follow, then the external perimeters of the drain and source are specified. For device $M1$, the channel length in microns is 1 and the width is 72. The area of the drain is determined by W_1 and the layout length of the drain region. For this device, the width is 72; thus the length of the drain region must be 5 to result in an area of $72 \times 5 = 360$ square microns. The perimeter used for the drain is not equal to $2W_1 + 2L_D$. Rather it is the perimeter of the drain region minus the width of the channel: $PD = W_1 + 2L_D = 72 + 10 = 82$. Certain capacitances are based on the external perimeter of the associated region, but the capacitance associated with the side of the region that abuts the channel is accounted for in a separate calculation. The same considerations apply to the source terminal also.

The circuit is first simulated with neither source resistance nor load capacitance. The results of this simulation are $A_{MBsim} = -7.15$ V/V, $f_{2o-sim} = 202.1$ MHz, with a headroom of about 2.5 V. The headroom is found by doing a dc scan of the input voltage and watching the output voltage for departures from linearity.

From calculation the midband voltage gain is found to be

$$|A_{MB}| \approx \left[\frac{(W_1/L_1)}{(W_2/L_2)} \right]^{1/2} = \sqrt{36} = 6 \text{ V/V}$$

The capacitance values given by the Spice simulation are

$$C_{in} = C_{gs1} + (1 + |A_{MB}|)C_{gd1} = 168 + (1 + 6)21.6 = 319.2 \text{ fF}$$

and

$$C_{out} = C_{gd1} + C_{db1} + C_{sb2} + C_{gs2} = 21.6 + 141 + 7.5 + 5 = 175.1 \text{ fF}$$

The output resistance, calculated from Eq. (9.12) using parameters from the simulation, is $R_{out} = 4.35$ k Ω . The upper corner frequency with no source resistance and no load

Table 9.3 Summary of Simulation Results for the Diode-Connected Load Stage

$A_{MBsim} = -7.15 \text{ V/V}$		
$C_L, \text{ pF}$	$R_g, \text{ k}\Omega$	$f_{2o-sim}, \text{ MHz}$
0	0	202
1	0	30.1
0	339	1.52
1	339	1.48

capacitance is then

$$f_{2o} = \frac{1}{2\pi R_{out} C_{out}} = \frac{1}{2\pi \times 4350 \times 175.1 \times 10^{-15}} = 209 \text{ MHz}$$

When a load capacitance of 1 pF is added across the output terminals, the simulation shows an upper corner frequency of 30 MHz, and the calculation leads to a value of 31.1 MHz.

If a rather large signal generator resistance of 339 k Ω , which will also be used in succeeding circuits for comparison purposes, is added to the circuit along with the 1-pF output capacitance, the simulated value of upper corner frequency is 1.48 MHz. The upper corner frequency is lowered from 30 MHz to 1.48 MHz, due to the generator resistance and input capacitance. The overall upper corner frequency must then be caused primarily by the input circuit; thus, we calculate a value of

$$f_{2o} = \frac{1}{2\pi R_g C_{in}} = \frac{1}{2\pi \times 339 \times 10^3 \times 319.2 \times 10^{-15}} = 1.47 \text{ MHz}$$

If a generator resistance that equals the output resistance of this stage is used—that is, $R_g = 4.35 \text{ k}\Omega$ —the upper corner frequency is 83.7 MHz without C_L and 26.1 MHz with $C_L = 1 \text{ pF}$ added. Table 9.3 summarizes these results for the diode-connected load stage.

PRACTICAL Considerations

Several practical points relating to IC design can be based on this analysis.

1. Although the load is not a resistor, the same techniques used in the analysis of discrete circuits are still valid. The equivalent resistance of the MOSFET load is first found and substituted for the load resistance.
2. The aspect ratio is important in determining the performance of the circuit. Very large aspect ratios often result in analog design, while high-frequency digital circuits generally keep this ratio at a low value to minimize capacitance and required *real estate* or chip volume. Schematics of analog MOSFET circuits label the width and length of each device near the device, as shown in Fig. 9.4.
3. Approximate results are useful to provide a starting point for circuit simulations that are a necessity before an IC chip is laid out. Fabrication runs are very expensive and mistakes must be avoided to minimize cost. Thus, the simulation step is never omitted in the IC design process. This step will use parameters for the MOS devices that are based on the actual process to be used in fabrication.
4. Headroom may be an important consideration, since IC chips often use low-voltage dc supplies.

There are some disadvantages to the stage discussed in this section that limit its usefulness. Larger channel areas lead to increased capacitance, so the bandwidth of high-gain stages will be less than that of lower-gain stages for the diode-connected load stage. On the other hand, it is a simple stage that has a low output impedance and is, therefore, not affected to a great extent by load capacitance.

In the following chapter we will see that the BJT never uses the configuration of Fig. 9.4, since the impedance looking into the emitter is r_e . This load impedance is too low to achieve a significant voltage gain. We will also see that the load impedance cannot be increased by scaling the areas of a BJT, since r_e is not a function of area. This difference is very significant in BJT design and MOSFET design, the latter of which uses aspect ratio as a critical design parameter.

The load device of Fig. 9.4 can be replaced by a pMOS device, as shown in Fig. 9.7. This configuration eliminates the body effect of the load device and increases the resistance due to a smaller value of μ_p compared to μ_n . The value of μ_n is about three times that of μ_p . The approximation of Eq. (9.9) becomes more accurate, and the voltage gain can be written as

$$|A_{MB}| = \left[\frac{\mu_n C_{oxn}(W_1/L_1)}{\mu_p C_{oxp}(W_2/L_2)} \right]^{1/2} \approx \left[\frac{3(W_1/L_1)}{(W_2/L_2)} \right]^{1/2} \quad (9.15)$$

To approximate the upper corner frequency of the diode-connected pMOS stage, the capacitances of Fig. 9.8 are added. It is generally true that $C_{ds} \ll C_{db}$, giving a total capacitance from output to ground of

$$C_{out} = C_{db1} + C_{gd1} + C_{db2} + C_{gs2}$$

The output resistance can be found as

$$R_{out} = \frac{1}{g_{m2} + g_{ds2} + g_{ds1}} \approx \frac{1}{g_{m2}}$$

It is left as an exercise for the reader to derive this expression for output impedance.

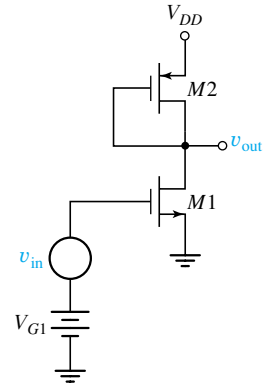


Figure 9.7
A diode-connected pMOS load.

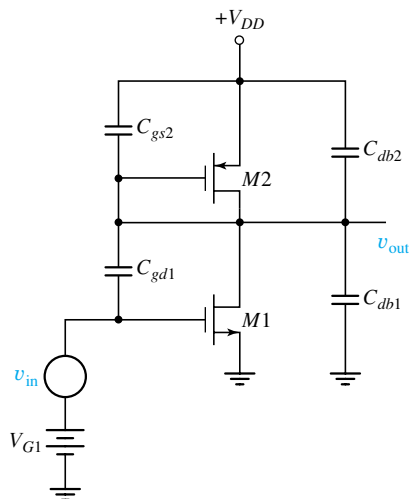


Figure 9.8
Parasitic capacitances determining the upper 3-dB frequency.

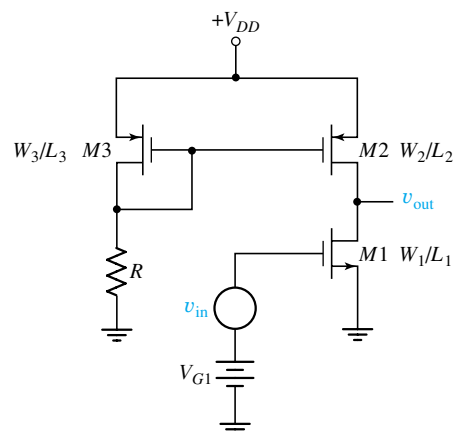


Figure 9.9
A MOSFET stage with an active current source load.

PRACTICE Problem

9.5 Two n -devices are used in a diode-connected amplifier stage similar to that of Fig. 9.4(a). If $L_1 = L_2 = 0.6 \mu$, calculate W_1/W_2 for a midband voltage gain of -4.3 V/V.
Ans: 18.5.

The upper corner frequency is then

$$f_{2o} = \frac{1}{2\pi C_{out} R_{out}} \quad (9.16)$$

This value is approximately

$$f_{2o} = \frac{g_{m2}}{2\pi(C_{db1} + C_{db2} + C_{gs2} + C_{gd1})} \quad (9.17)$$

In many cases, the load capacitance or input capacitance to the next stage will lower f_{2o} from this value, as seen earlier in this section.

9.2.2 ACTIVE LOAD STAGE

A stage used often in IC design is the active load stage. Typically, the active load is a current source, often based on the current mirror. A simple MOSFET active load stage appears in Fig. 9.9.

There is a compelling reason to use active load stages in IC design. The device that acts as the load for the amplifying stage can present a large incremental load while allowing a reasonable drain current to flow. This large incremental load leads to a high gain for the stage, while the dc current can lead to acceptable values of transconductance and bias current. If a fixed resistor with a large value were used to achieve high gain, the dc drop across this element would be prohibitive for normal bias currents.

PRACTICAL Considerations

A simple current mirror might provide $100 \mu\text{A}$ of current to an amplifying stage while presenting $60 \text{ k}\Omega$ of incremental resistance to the stage. If a simple $60\text{-k}\Omega$ resistance replaced the current mirror, the same incremental resistance would prevail, but the dc voltage drop across the resistor would be

$$V_R = 0.1 \times 60 = 6 \text{ V}$$

The dc power supply for many MOSFET IC amplifiers is 5 V or less; thus, using a simple resistor is out of the question.

The difference between an active load and a simple resistor becomes even more apparent when a more complex current mirror is used to produce a resistive load of several hundred kilohms or greater. The dc drop across a several hundred kilohm resistor, conducting a typical bias current, might be over 100 V.

The pMOS current mirror of Fig. 9.9 provides bias current to the amplifying device, $M1$. This device also sees an incremental resistive load that equals

$$R_{\text{out}} = r_{ds1} \parallel r_{ds2} = \frac{1}{g_{ds1} + g_{ds2}} \quad (9.18)$$

The midband voltage gain is now

$$A_{MB} = -g_{m1} R_{\text{out}} \quad (9.19)$$

Since the values of r_{ds} can be high for both devices, the voltage gain for a single stage can also be reasonably high.

The output voltage can be driven positive to the point that $M2$ reaches its pinchoff value for V_{DS} . This voltage may be $V_{DD} - V_{\text{eff}2} = V_{DD} - 0.4$ V. In the negative direction, the output can be driven to the point that $M1$ reaches pinchoff, which is equal to $V_{\text{eff}1} = 0.4$ V. The headroom is perhaps 0.6–0.8 V.

The output capacitance for the amplifier of Fig. 9.9 is

$$C_{\text{out}} = C_{db1} + C_{db2} + C_{gd1} + C_{gd2}$$

which gives an upper corner frequency of

$$f_{2o} = \frac{(g_{ds1} + g_{ds2})}{2\pi(C_{db1} + C_{db2} + C_{gd1} + C_{gd2})} \quad (9.20)$$

Again, we emphasize that a load capacitance or input capacitance of a following stage will lower this value.

EXAMPLE 9.2

The current mirror of Fig. 9.10 supplies a current of $50 \mu\text{A}$ to the amplifying stage. The dc output voltage is adjusted by voltage source, V_1 , to be 2.4 V. If $g_{m1} = 0.19 \text{ mA/V}$, $g_{ds1} = 0.95 \mu\text{A/V}$, $g_{ds2} = 2 \mu\text{A/V}$, $C_{db1} = 11.0 \text{ fF}$, $C_{db2} = 32.0 \text{ fF}$, $C_{gd1} = 1.5 \text{ fF}$, and $C_{gd2} = 4.5 \text{ fF}$,

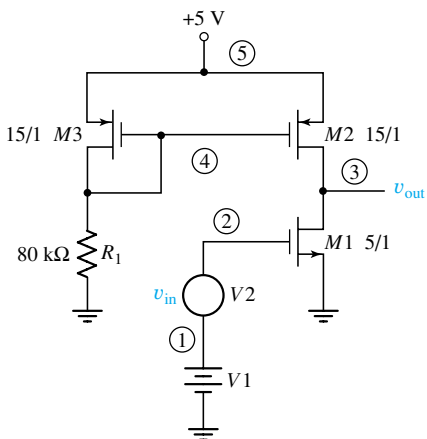


Figure 9.10
Amplifier for Example 9.2.

- (a) Calculate the midband voltage gain, A_{MB} .
- (b) Calculate the upper corner frequency, f_{2o} .
- (c) Verify results with a Spice simulation.

SOLUTION The output resistance for this stage is

$$R_{out} = \frac{1}{g_{ds1} + g_{ds2}} = \frac{10^6}{2.95} = 339 \text{ k}\Omega$$

Using Eq. (9.19) allows the voltage gain to be found as

$$A_{MB} = -g_{m1}R_{out} = -0.19 \times 10^{-3} \times 339 \times 10^3 = -64.4 \text{ V/V}$$

The output capacitance is

$$C_{out} = C_{db1} + C_{db2} + C_{gd1} + C_{gd2} = 11.0 + 32.0 + 1.5 + 4.5 = 49 \text{ fF}$$

From Eq. (9.20), this gives an upper corner frequency of

$$f_{2o} = \frac{1}{2\pi C_{out}R_{out}} = \frac{1}{2\pi \times 49 \times 10^{-15} \times 339 \times 10^3} = 9.58 \text{ MHz}$$

The Spice netlist file is listed in Table 9.4. Corresponding node and element numbers are shown in Fig. 9.10.

Table 9.4 Spice Netlist File for Example 9.2

```
EX9-2.CIR

R1 0 4 80K
V1 1 0 1.275V
V2 2 1 AC 0.005V
V3 5 0 5V
M1 3 2 0 0 N L=1U W=5U AD=25P AS=25P PD=15U PS=15U
M2 3 4 5 5 P L=1U W=15U AD=75P AS=75P PD=25U PS=25U
M3 4 4 5 5 P L=1U W=15U AD=75P AS=75P PD=25U PS=25U
.AC DEC 10 100 10MEG
.OP
.PROBE
.LIB C5X.LIB
.END
```

The results of this simulation are $A_{MBsim} = -63.6 \text{ V/V}$ and $f_{2o-sim} = 8.53 \text{ MHz}$, which compare well with the calculated results. A dc scan on the input voltage allows the active region of the output voltage to be evaluated. For this circuit, the active region extends from 0.4 V to 4.6 V, which also agrees well with theory.

Adding Generator Impedance and Load Impedance Only the output capacitance was used in developing Eq. (9.20) for upper corner frequency. As mentioned in connection with the diode-connected load stage, there are two other considerations that must be made for the practical circuit. One is the additional capacitance added between output and ground due to the input capacitance of the following stage or from the output pad of an IC chip. The second is the generator resistance or output resistance of the previous stage that drives the input capacitance of this stage. Both loops must be considered to result in an accurate upper corner frequency.

Let us suppose that the output of the amplifier of Fig. 9.10 is brought to an output pad and pin of an IC chip. The capacitance associated with the pad might exceed 1 pF. If the simulation is repeated with a 1-pF load added, the upper corner frequency drops from 8.35 MHz to 431 kHz, a very large drop.

If this stage were loaded by a comparable stage rather than by 1 pF, the corner frequency might drop by a factor of two rather than a factor of 20. In order to avoid this drop, a buffer stage may be added to drive the 1-pF load without the large reduction in corner frequency. Another possibility is to increase the values of W for all the devices. Although this increases the capacitance, the output resistance decreases and g_m increases to result in a comparable voltage gain. The effect of the load capacitance on upper corner frequency will now be much less.

As mentioned earlier, the stage of Fig. 9.10 is driven by a perfect voltage generator with zero output resistance. If this stage were driven by an identical stage, the output impedance of the first stage would become the generator resistance for the second stage. To demonstrate the effect of generator resistance on upper corner frequency, a resistance of 339 k Ω is used as a generator resistance for the circuit of Fig. 9.10. This particular value of resistance will be used in succeeding examples for comparison purposes. No external load capacitance is used in this simulation. The simulated upper corner frequency is lowered in this situation from a value of 8.35 MHz to 3.08 MHz.

This value can be calculated by noting that the input circuit will now cause a corner frequency determined by the generator resistance and the input capacitance. The input capacitance equals the sum of C_{gs1} , C_{gb1} , and the Miller effect capacitance $(1 + |A_{MB}|)C_{gd1}$. From the output file of the simulation, these values are

$$|A_{MB}| = 63.6 \text{ V/V} \quad C_{gs1} = 13.35 \text{ fF} \quad C_{gd1} = 1.5 \text{ fF} \quad C_{gb1} = 0.3 \text{ fF}$$

The total input capacitance resulting is approximately 111 fF. With a value of $R_g = 339 \text{ k}\Omega$ for generator resistance, this adds a corner frequency of

$$f_{\text{in-high}} = \frac{1}{2\pi C_{\text{in}} R_g} = 4.23 \text{ MHz}$$

The amplifier now has an input corner frequency of 4.23 MHz and an output corner frequency of 8.53 MHz. We use the method of Chapter 3 to calculate the overall upper corner frequency when two single-pole upper corner frequencies make up the amplifier response. The result is a calculated overall corner frequency of $f_{2o\text{-calc}} = 3.56 \text{ MHz}$. This value exceeds the simulated value of 3.08 MHz by 15%.

If a generator resistance of 339 k Ω and a 1-pF load capacitance are both added to the amplifier, the new upper corner frequency is found from simulation to be 399 kHz. Table 9.5 summarizes the results of this simulation.

The active current source load provides a method to achieve high midband voltage gains without the large discrepancy in size required by the diode-connected load amplifier.

Table 9.5 Summary of Simulation Results for the Current-Source Load Stage

$A_{MB\text{sim}} = -63.6 \text{ V/V}$		
C_L , pF	R_g , k Ω	$f_{2o\text{-sim}}$, MHz
0	0	8.53
1	0	0.43
0	339	3.08
1	339	0.40

It suffers from poor frequency response when a large capacitive load, much larger than the output capacitance of the stage, is present.

We can note that the midband voltage gain given by Eq. (9.19) will be increased if R_{out} is increased. This resistance can be increased by using a more complex current mirror to make the output resistance much larger than the output resistance of the amplifying stage. While this increases the midband voltage gain, the upper corner frequency due to the output loop, calculated from Eq. (9.20), decreases by the same factor. If this corner frequency is the dominant one, midband voltage gain and bandwidth can be exchanged directly by varying the output resistance of the current mirror.

PRACTICAL Considerations

Although the upper corner frequency of the active load stage is significantly affected by a 1-pF capacitance, it is possible to minimize this problem. The channel width of the output stage can be increased considerably to result in an increase in output capacitance and a corresponding decrease in output resistance. The upper corner frequency with no external load can be approximately equal to that of the smaller device. However, when a 1-pF load capacitance is added, the percentage increase of capacitance is much less for the large device than for the small device. The effect on upper corner frequency is then much less for the larger device.

The effect of channel width, W , on the voltage gain can be seen in the following example.

EXAMPLE 9.3

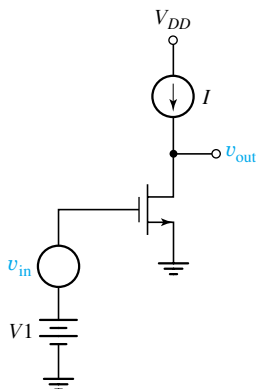


Figure 9.11
Circuit for Example 9.3.

In the circuit of Fig. 9.11, the current source generates $100 \mu\text{A}$ of current and has an incremental output resistance of $r_{cs} = 100 \text{ k}\Omega$. The device $M1$ is a $1 \mu\text{m}$ gate length device with $\mu C_{\text{ox}} = 0.06 \text{ mA/V}^2$ and $\lambda = 0.03 \text{ V}^{-1}$. Find the channel width to result in a midband voltage gain of 100 V/V .

SOLUTION The midband voltage gain of this stage is

$$A_{MB} = -g_m R_{\text{out}}$$

where

$$R_{\text{out}} = r_{cs} \parallel r_{ds1}$$

The value of r_{ds1} can be approximated by assuming that the drain pinchoff current is approximately equal to $100 \mu\text{A}$. The result is

$$r_{ds1} = \frac{1}{\lambda I_D} = \frac{1}{0.03 \times 0.1} = 333 \text{ k}\Omega$$

Using the $100\text{-k}\Omega$ impedance of the current source, the output resistance is found to be

$$R_{\text{out}} = 100 \parallel 333 = 76.9 \text{ k}\Omega$$

Recalling that

$$g_m = \sqrt{2\mu C_{\text{ox}}(W/L)I_D}$$

we can write the magnitude of the voltage gain as

$$|A_{MB}| = g_m R_{out} = \sqrt{2 \times 0.06 \times (W/L) \times 0.1} \times 76.9 = 100 \text{ V/V}$$

Solving this equation for the ratio of W/L leads to a value of 141μ for W .

9.2.3 SOURCE FOLLOWER WITH ACTIVE LOAD

The source follower provides a buffer stage, but the midband voltage gain is low, even less than the value of unity approached by the BJT emitter-follower stage. The bandwidth is quite high for both the emitter-follower and the source-follower stages. Figure 9.12 demonstrates a source follower with a current mirror load.

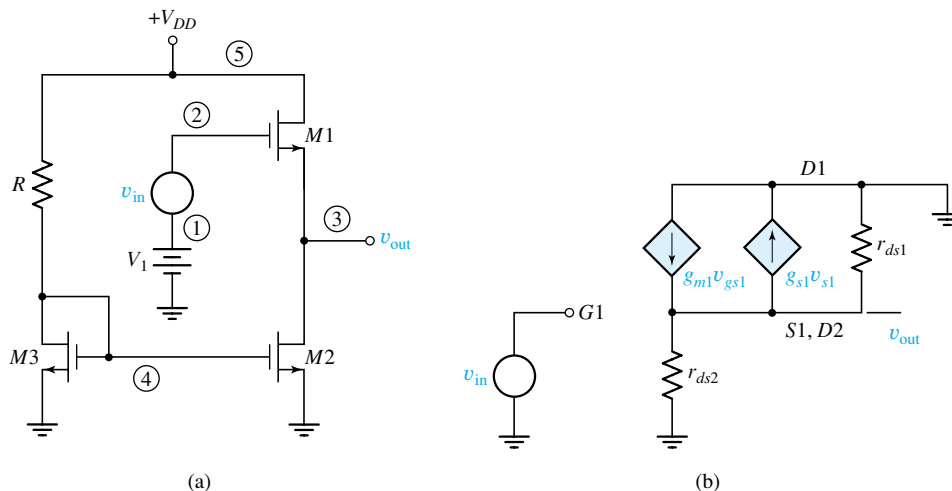
The device $M2$ presents a resistance of r_{ds2} between the source of $M1$ and ground. In addition, device $M1$ presents a resistance of r_{ds1} in parallel with $1/g_{s1}$ to the dc power supply, which is also ground for incremental signals. Again we note that the body effect in $M1$ must be included, since the source-to-substrate voltage of this device varies with the output signal. In fact, it equals the output signal.

The circuit of Fig. 9.12(b) is redrawn in Fig. 9.13 and the pertinent parasitic capacitances are added. The current source strength, $g_{m1}v_{gs1}$, can be written as $g_{m1}(v_{in} - v_{out})$. In the equivalent circuit, this current can be generated by two separate sources, as shown in Fig. 9.13. The source terminal now appears at the top of the figure while the drain terminal is grounded.

The two current sources $g_{m1}v_{out}$ and $g_{s1}v_{out}$ can be converted to conductances g_{m1} and g_{s1} , respectively. As a voltage appears at $S1$, the currents through these conductances equal the values that would be generated by the sources. Figure 9.14 shows an alternate equivalent circuit that is used to find the voltage gain as a function of frequency. This circuit results from taking a Thévenin equivalent of the current source, $g_{m1}v_{in}$, and the parallel resistance, R_{out} .

The circuit of Fig. 9.14 is analyzed to find that

$$A(j\omega) = g_{m1}R_{out} \frac{1 + j\omega C_{gs1}/g_{m1}}{1 + j\omega(C_{gs1} + C_{out})R_{out}} \quad (9.21)$$



PRACTICE Problems

9.6 Work Example 9.2 for a generator resistance of $R_g = 50 \text{ k}\Omega$.

9.7 Work Example 9.2 for a generator resistance of $R_g = 50 \text{ k}\Omega$ and an input capacitance to a following stage of $C_{in2} = 100 \text{ fF}$.

9.8 The drain current of the current mirror output stage of Fig. 9.10 is increased to $100 \mu\text{A}$. Assuming that the capacitances remain constant, calculate the new midband voltage gain and upper corner frequency for the amplifier.

Ans: $A_{MB} = -45.4 \text{ V/V}$,
 $f_{2o} = 19.2 \text{ MHz}$.

9.9 Work Example 9.3 if a midband voltage gain of 180 V/V is required.

Ans: $W = 457 \mu$.

Figure 9.12

(a) A source-follower stage with current source load.
(b) Equivalent circuit.

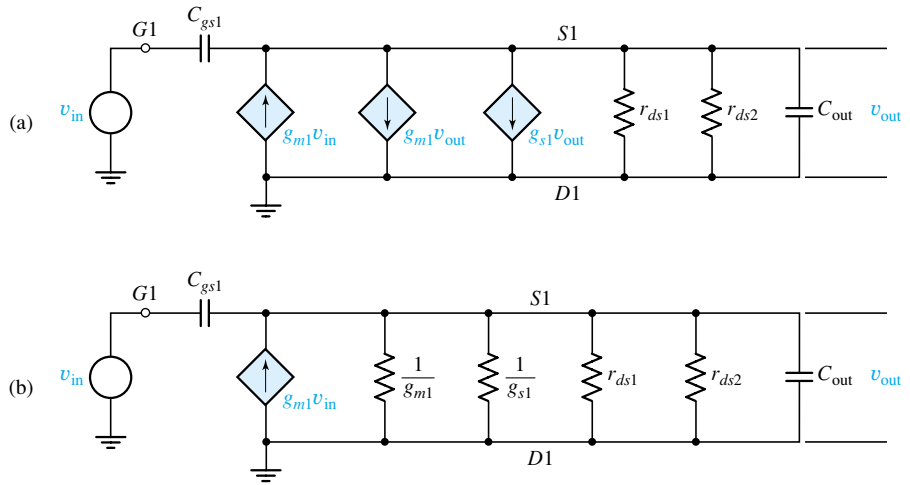


Figure 9.13
 (a) The high-frequency source follower equivalent circuit.
 (b) Using transconductances for two current sources.

where

$$R_{out} = \frac{1}{g_{m1} + g_{s1} + g_{ds1} + g_{ds2}} \tag{9.22}$$

and

$$C_{out} = C_{sb1} + C_{db2} + C_{gd2} \approx C_{sb1} + C_{db2} \tag{9.23}$$

The midband gain can be evaluated from Eqs. (9.21) and (9.22) to be

$$A_{MB} = \frac{g_{m1}}{g_{m1} + g_{s1} + g_{ds1} + g_{ds2}} \tag{9.24}$$

In many submicron processes, the value of the denominator of Eq. (9.24) might equal 1.15 to 1.2 times g_{m1} . This leads to values of midband gain ranging from about 0.8 to 0.9 V/V.

The transfer function for voltage gain as a function of frequency shows a zero at

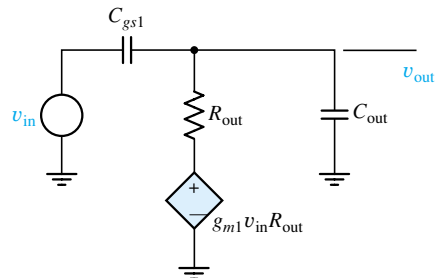
$$f_{zero} = \frac{g_{m1}}{2\pi C_{gs1}} \tag{9.25}$$

and a pole at

$$f_{pole} = \frac{g_{m1} + g_{s1} + g_{ds1} + g_{ds2}}{2\pi(C_{gs1} + C_{out})} \tag{9.26}$$

Typically, the zero frequency is higher than the pole frequency, and the asymptotic frequency response appears as in Fig. 9.15. At high frequencies the capacitor C_{gs1} feeds

Figure 9.14
 Alternate equivalent circuit of the source follower.



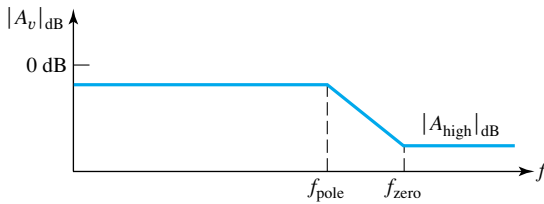


Figure 9.15
Asymptotic frequency response
of source follower.

through from input directly to output, causing a gain of

$$A_{\text{high}} = \frac{C_{gs1}}{C_{gs1} + C_{\text{out}}} \quad (9.27)$$

As we consider the large-signal operation of the source follower, we see that the output voltage can be driven positive to a value of $V_{DD} - V_{\text{eff}1} - V_{T1}$. The negative voltage can reach $V_{\text{eff}2}$ before $M2$ leaves the active region. The headroom is then $V_{T1} + V_{\text{eff}1} + V_{\text{eff}2}$.

EXAMPLE 9.4

In the source follower and current mirror of Fig. 9.12, a dc drain current of $50 \mu\text{A}$ passes through $M1$ and $M2$. The following parameters apply to the devices of the circuit at this bias point: $g_{m1} = 199 \mu\text{A/V}$, $g_{s1} = 44 \mu\text{A/V}$, $g_{ds1} = 1 \mu\text{A/V}$, $g_{ds2} = 1.6 \mu\text{A/V}$, $C_{gs1} = 7.1 \text{ fF}$, $C_{sb1} = 12.6 \text{ fF}$, $C_{db2} = 12.7 \text{ fF}$, and $C_{gd2} = 1.5 \text{ fF}$. Calculate the midband voltage gain, the pole frequency or upper corner frequency, and the zero frequency. Also calculate the high frequency gain due to capacitor feedthrough of C_{gs1} . Simulate this circuit with Spice.

SOLUTION The midband voltage gain is calculated from Eq. (9.24) as

$$A_{MB} = \frac{g_{m1}}{g_{m1} + g_{s1} + g_{ds1} + g_{ds2}} = \frac{199}{245.6} = 0.810 \text{ V/V}$$

The pole frequency that will be near the upper corner frequency is found from Eq. (9.26) to be

$$f_{\text{pole}} = \frac{g_{m1} + g_{s1} + g_{ds1} + g_{ds2}}{2\pi(C_{gs1} + C_{\text{out}})} = \frac{245.6 \times 10^{-6}}{2\pi \times 33.9 \times 10^{-15}} = 1.15 \text{ GHz}$$

From Eq. (9.25), the zero frequency is calculated to be

$$f_{\text{zero}} = \frac{g_{m1}}{2\pi C_{gs1}} = \frac{199 \times 10^{-6}}{2\pi \times 7.1 \times 10^{-15}} = 4.46 \text{ GHz}$$

The high-frequency gain is

$$A_{\text{high}} = \frac{C_{gs1}}{C_{gs1} + C_{\text{out}}} = \frac{7.1}{33.9} = 0.209 \text{ V/V}$$

The Spice simulation file is listed in Table 9.6.

The frequency response resulting from this simulation is shown in Fig. 9.16. The simulated midband gain is 0.811 V/V , which is very close to the calculated value of 0.810 V/V . The upper corner frequency from the simulation is 1.01 GHz , compared to a calculated value of 1.15 GHz . The simulated zero frequency is 6.15 GHz , and the calculated value is 4.46 MHz . The high-frequency gain had a simulated value of 0.16 V/V , whereas the calculated value was 0.21 V/V .

Table 9.6 Spice File for Example 9.4

```

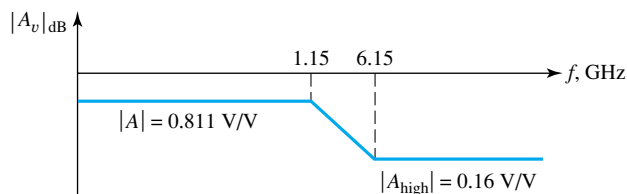
EX9-4.CIR

R1 4 5 75K
V1 1 0 3.0V
V2 2 1 AC 0.1V
V3 5 0 5V
M1 5 2 3 0 N L=1U W=5U AD=25P AS=25P PD=15U PS=15U
M2 3 4 0 0 N L=1U W=5U AD=25P AS=25P PD=15U PS=15U
M3 4 4 0 0 N L=1U W=5U AD=25P AS=25P PD=15U PS=15U
.AC DEC 10 100 10000MEG
.OP
.PROBE
.LIB C5X.LIB
.END

```

A dc scan on the input voltage shows an output active region extending from approximately 0.32 to 3.03 V. The lower voltage is approximately $V_{\text{eff}2}$, and the upper voltage should approximate $V_{DD} - V_{\text{eff}1} - V_{T1}$.

Figure 9.16
Simulated frequency response
for source follower.



We note that the upper corner frequency for the source follower is 1.01 GHz, compared to 8.53 MHz for the comparable-sized current source load stage of Example 9.2. The primary reason for this is the difference in the output resistance of the two stages. For the current source load stage, the output resistance is 339 k Ω , and the source follower output resistance is about 4 k Ω . In order to compare this stage when driven by a signal generator resistance, a 339-k Ω resistance is inserted in the input lead. This simulation leads to an overall upper corner frequency of 101.5 MHz. The corresponding value for the current source load of Example 9.2 is 3.08 MHz.

With a capacitive load of 1 pF and a generator resistance of 339 k Ω , a Spice simulation shows an upper corner frequency of 37 MHz. Although this value is much lower than the unloaded value, it is considerably more than the corresponding frequency of the current source load stage, which was 399 kHz. Table 9.7 summarizes these results.

PRACTICAL Considerations

As noted earlier, capacitive loading can be a serious problem for an output stage that connects to an IC pin, which will connect to the input of another circuit. Because of the high output resistance of configurations such as the active load stage, a small capacitance of a pF or less will decrease the upper corner frequency significantly.

Table 9.7 Summary of Simulation Results for Source Follower

$A_{MBsim} = -0.811 \text{ V/V}$		
$C_L, \text{ pF}$	$R_g, \text{ k}\Omega$	$f_{2o-sim}, \text{ MHz}$
0	0	1,010
1	0	36.6
0	339	101.6
1	339	37.2

The source follower stage is often inserted between a high-gain stage and the output pin of a chip to serve as a buffer stage. This buffer presents a rather low capacitance to the preceding stage, since there is no Miller multiplication of C_{gd} and, as seen from the simulation, a 1-pF load capacitance can result in a reasonably high upper corner frequency.

9.2.4 THE CASCODE CONNECTION

The cascode connection has been used for many years in high-frequency BJT circuits. It has become more important in IC MOSFET design in recent years. We will discuss the MOSFET cascode circuit in this section. Figure 9.17(a) shows the basic cascode circuit with a current source load.

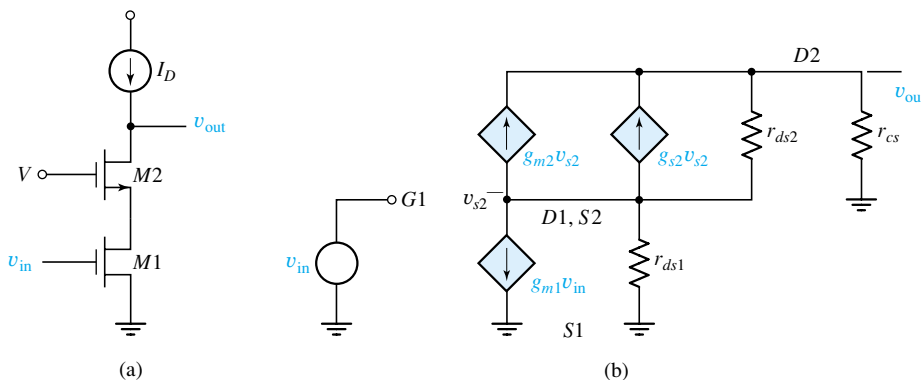
The equivalent circuit for the upper device would include a current generator of value $g_{m2}V_{gs2}$. For this connection, $v_{gs2} = -v_{s2}$; thus this current generator reverses the direction of current flow and removes the negative sign to lead to the value of $g_{m2}v_{s2}$, shown in Fig. 9.17(b).

The resistance r_{cs} is the output resistance of the current source. For a simple source, this value would be r_{ds} . For a Wilson mirror, it would be considerably larger. The equivalent circuit can be converted to a Thévenin circuit, as shown in Fig. 9.18. The output voltage is

$$v_{out} = -ir_{cs}$$

where i is the incremental drain current. Note that the upper voltage source is proportional to the source voltage of $M2$, v_{s2} . This voltage can be expressed as

$$v_{s2} = -g_{m1}r_{ds1}v_{in} + ir_{ds1}$$



PRACTICE Problems

9.10 For the source follower of Fig. 9.12, derive the output resistance looking into the source terminal of $M1$.

9.11 If g_{ds1} and g_{ds2} are considered negligible for the source follower of Example 9.4, what will the midband voltage gain be?

Ans: 0.819 V/V.

Figure 9.17
(a) The MOSFET cascode amplifier stage. (b) The equivalent circuit.

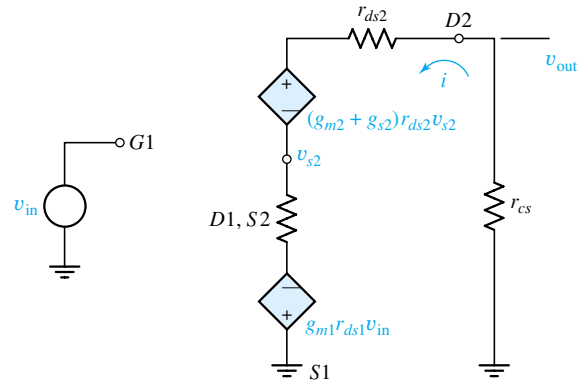


Figure 9.18
An alternate equivalent circuit for the cascode.

If the transconductance of $M2$ is added to the body effect transconductance—that is,

$$g_{t2} = g_{m2} + g_{s2}$$

the midband voltage gain can be found to be

$$A_{MB} = - \frac{(g_{m1} r_{ds1} + g_{t2} g_{m1} r_{ds1} r_{ds2}) r_{cs}}{r_{ds1} + r_{ds2} + r_{cs} + g_{t2} r_{ds1} r_{ds2}} \tag{9.28}$$

This expression represents the product of two relatively large gains. As bias current decreases, the r_{ds} terms increase faster than the g_m terms decrease. Gains of several thousand can be obtained with this circuit. However, as r_{ds} increases, the high-frequency response decreases, since the output resistance must drive the parasitic capacitance at the output of the stage.

A differential version of this stage is often used as an input stage in MOSFET op amp chips. A slightly different version of the cascode is the folded cascode that replaces $M2$ by a pMOS device with a drain connection to ground. We will not consider the folded cascode stage.

The headroom of the cascode circuit can be found to be

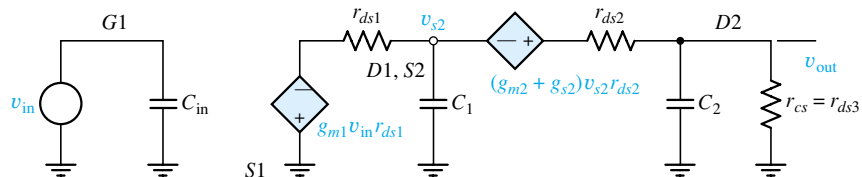
$$V_{\text{headroom}} = V_{\text{eff1}} + V_{\text{eff2}} - V_{\text{eff3}} \tag{9.29}$$

The value of V_{eff3} will be negative for the pMOS device of a simple current mirror.

The upper corner frequency of the cascode can be found from the equivalent circuit, shown in Fig. 9.19. The analysis of this circuit is somewhat complex. An accurate value of the upper corner frequency can be found by simulation, but it can be approximated rather easily from the equivalent circuit. We first note that with no signal generator resistance, the input capacitance will not influence the bandwidth. We next note that the corner frequency due to the capacitance C_1 will be affected by the parallel combination of r_{ds1} and the impedance looking into the source of $M2$. This impedance will be much less than r_{ds1} and can be approximated by

$$R_{S2} = \frac{1}{g_{m2} + g_{s2}}$$

Figure 9.19
High-frequency model of the cascode.



This corner frequency will be quite large, at least compared to that caused by C_2 . If the current source is a simple current mirror, its output impedance will be $r_{cs} = r_{ds3}$. The resistance seen by C_2 is then $r_{ds3} \parallel R_{out2}$, where R_{out2} is the impedance looking into the drain of $M2$. This latter impedance will be quite large since the source resistance of $M2$ equals r_{ds1} . This source resistance increases the output resistance of $M2$ significantly; thus, the resistance seen by C_2 is approximately r_{ds3} . The upper corner frequency of the cascode can then be approximated by

$$f_{2o} \approx \frac{1}{2\pi r_{ds3} C_2} \quad (9.30)$$

where $C_2 = C_{db2} + C_{gd2} + C_{db3} + C_{gd3}$.

EXAMPLE 9.5

The cascode circuit of Fig. 9.20 has a dc drain current for all transistors of $50 \mu\text{A}$. This current is supplied by a simple current mirror with $M3$ as the output device. With the bias voltages shown, the parameters are $g_{m1} = 181 \mu\text{A/V}$, $g_{m2} = 195 \mu\text{A/V}$, $g_{ds1} = 5.87 \mu\text{A/V}$, $g_{s2} = 57.1 \mu\text{A/V}$, $g_{ds2} = 0.939 \mu\text{A/V}$, $g_{ds3} = 3.76 \mu\text{A/V}$, $C_{db2} = 9.8 \text{ fF}$, $C_{gd2} = 1.5 \text{ fF}$, $C_{db3} = 40.9 \text{ fF}$, and $C_{gd3} = 4.5 \text{ fF}$. Calculate the midband voltage gain and the approximate upper corner frequency of this cascode stage. Verify these results with a Spice simulation.

SOLUTION The midband gain is calculated from Eq. (9.28).

$$A_{MB} = -\frac{(g_{m1}r_{ds1} + g_{t2}g_{m1}r_{ds1}r_{ds2})r_{ds3}}{r_{ds1} + r_{ds2} + r_{ds3} + g_{t2}r_{ds1}r_{ds2}} = -46.8 \text{ V/V}$$

We note that this gain can be approximated by

$$A_{MB} = -g_{m1}r_{ds3} = -\frac{181}{3.76} = -48.1 \text{ V/V}$$

Which assumes that the incremental current generated by device $M1$, $g_{m1}v_{in}$, flows through $M2$ to develop the output voltage across r_{ds3} .

This low value of voltage gain could be increased sharply by increasing the output impedance of the current mirror to something much greater than r_{ds3} .

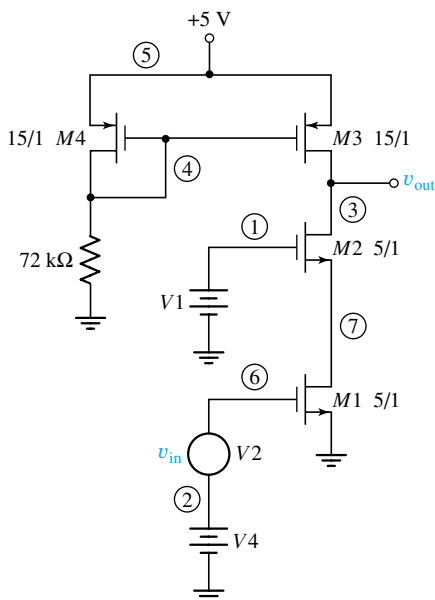


Figure 9.20
Cascode circuit for Example 9.5.

The upper corner frequency is approximated by Eq. (9.30) as

$$f_{2o} = \frac{1}{2\pi r_{ds3} C_2} = \frac{1}{2\pi \times 56.7 \times 10^{-15} \times 266 \times 10^3} = 10.6 \text{ MHz}$$

The Spice netlist is included in Table 9.8.

Table 9.8 Spice Netlist for Example 9.5

```

EX9-5.CIR

R1 0 4 72K
V1 1 0 2.1V
V2 2 6 AC 0.005V
V3 5 0 5V
V4 2 0 1.3V
M1 7 6 0 0 N L=1U W=5U AD=25P AS=25P PD=15U PS=15U
M2 3 1 7 0 N L=1U W=5U AD=25P AS=25P PD=15U PS=15U
M3 3 4 5 5 P L=1U W=15U AD=75P AS=75P PD=25U PS=25U
M4 4 4 5 5 P L=1U W=15U AD=75P AS=75P PD=25U PS=25U
.AC DEC 10 100 100MEG
.OP
.PROBE
.LIB C5X.LIB
.END

```

The results of the simulation are $A_{MB\text{sim}} = -46.9 \text{ V/V}$ and $f_{2o\text{-sim}} = 9.65 \text{ MHz}$. The calculated gain is very close to the simulated value, and the upper corner frequency is calculated to be about 10% higher than the simulated value.

In order to demonstrate the effect of current on gain and bandwidth, the dc drain current of the circuit is dropped from $50 \mu\text{A}$ to $10.7 \mu\text{A}$. For this situation, the simulated results are $A_{MB\text{sim}} = -94.1 \text{ V/V}$ and $f_{2o\text{-sim}} = 2.52 \text{ MHz}$. The gain has approximately doubled, while the bandwidth has dropped by a factor of about 4.

The effect on voltage gain can be seen from the approximation

$$A_{MB} = -g_{m1} r_{ds3}$$

Since g_m varies as the square root of drain current and r_{ds} varies approximately inversely with current, the voltage gain at a new current, I_{D2} , compares to the voltage gain at a current of I_{D1} as

$$A_{MB}(I_{D2}) = \sqrt{\frac{I_{D1}}{I_{D2}}} A_{MB}(I_{D1})$$

For this circuit, the new gain at $10.7 \mu\text{A}$ would be approximated as

$$A_{MB}(10.7) = \sqrt{\frac{50}{10.7}} A_{MB}(50) = 2.16 \times (-46.8) = -101 \text{ V/V}$$

The bandwidth decrease is due to the increase in output resistance when drain current is lowered.

Table 9.9 Summary of Simulation Results for Cascode Amplifier

$A_{MB\text{sim}} = -46.9 \text{ V/V}$		
$C_L, \text{ pF}$	$R_g, \text{ k}\Omega$	$f_{2\omega\text{-sim}}, \text{ MHz}$
0	0	9.65
1	0	0.55
0	339	8.95
1	339	0.55

If a signal generator resistance is present, a second corner frequency is added at the input due to C_{in} of Fig. 9.19. When a 339-k Ω generator resistance is added to the simulation of Table 9.8, the new upper corner frequency is 8.95 MHz. This value represents a relatively small change from the original value of 9.65 MHz, which implies that C_{in} is rather small. Thus we see one of the advantages of the cascode connection; that is, the input capacitance is small because the Miller effect is minimized by a small voltage gain from gate to drain of $M1$.

If a load capacitance of 1 pF is added but no generator resistance is present, the upper corner frequency is lowered to 552 kHz. Adding the generator resistance to this circuit leads to no further reduction of the upper corner frequency.

The headroom for the cascode circuit is simulated to be about 0.94 V. Using simulated values of the effective voltages of Eq. (9.29) gives a calculated value of

$$V_{\text{headroom}} = 0.47 + 0.45 + 0.41 = 1.33 \text{ V}$$

These results are summarized in Table 9.9.

9.2.5 THE ACTIVE CASCODE AMPLIFIER

An amplifier that behaves much like the cascode circuit, but offers slightly more headroom and requires one less bias voltage source, is the active cascode stage of Fig. 9.21. It also exhibits high gain although it has a lower bandwidth than the cascode stage with a current mirror load. The only difference between this circuit and the cascode circuit is that the gates of both nMOS amplifying stages, $M1$ and $M2$, are tied together and driven by the input signal. The load is formed by the two pMOS devices, $M3$ and $M4$, which again connect both gates together and also to a bias source. The connection of $M3$ and $M4$ is called a partial cascode stage.

The partial cascode can be found to present an output impedance, looking into the drain of $M4$, of

$$R_{o4} = r_{ds3} + r_{ds4} + g_{t4}r_{ds3}r_{ds4} \quad (9.31)$$

where $g_{t4} = g_{m4} + g_{s4}$.

The midband voltage gain is evaluated as

$$A_{MB} = - \left(\frac{g_{m1}}{g_{ds1}} + \frac{g_{m2}}{g_{ds2}} + \frac{g_{m1}g_{t2}}{g_{ds1}g_{ds2}} \frac{R_{o4}}{R_{o4} + R_{o2}} \right) \quad (9.32)$$

where

$$R_{o2} = r_{ds1} + r_{ds2} + g_{t2}r_{ds1}r_{ds2} \quad (9.33)$$

and $g_{t2} = g_{m2} + g_{s2}$.

PRACTICE Problem

9.12 Rework Example 9.5 if the current from the mirror is changed to 75 μA .

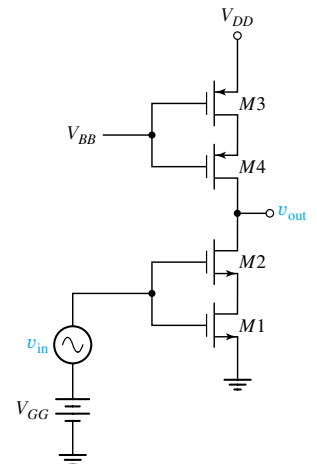


Figure 9.21 An active cascode stage with a partial cascode load.

The device $M2$ is chosen to have a larger aspect ratio than that of $M1$, and the same is true of $M4$ compared to $M3$. Thus the outer devices, $M1$ and $M3$, are forced to operate in the triode region or near the edge of the triode and the active region.

The gain expression can be reduced by using aspect ratios of the pMOS devices that are three times the corresponding nMOS devices, which will result in the following approximate transconductance relationships:

$$g_{r2} = g_{r4} \quad g_{rds1} = g_{rds3} \quad g_{ds2} = g_{ds4}$$

With some simple approximations, the voltage gain can be expressed as

$$A_{MB} \approx -\frac{g_{r2}g_{m1}}{2g_{ds1}g_{ds2}} \quad (9.34)$$

The output impedance of the active cascode for comparable devices is considerably greater than that of the cascode. Of course, additional devices could be used in the current mirror load of the cascode to increase the output impedance. For a four-transistor circuit, the active cascode has higher gain, smaller headroom, and fewer required bias voltages. The disadvantage is a smaller bandwidth.

The headroom is

$$V_{\text{headroom}} = V_{\text{eff1}} + V_{\text{eff3}} \quad (9.35)$$

which may be 0.4 to 0.5 V.

A Spice netlist file of the active cascode with drain currents equal to about $50 \mu\text{A}$ is shown in Table 9.10.

The results of this simulation are indicated in Table 9.11.

Both the cascode and active cascode will show an increased gain and decreased bandwidth as drain current decreases. For the circuits of Figs. 9.17(a) and 9.21, the drain currents are decreased to approximately $10 \mu\text{A}$. The new simulated results for the cascode circuit with no additional loading are $A_{MB\text{sim}} = -70.9 \text{ V/V}$ and $f_{2o\text{-sim}} = 3.03 \text{ MHz}$. The results for the active cascode are $A_{MB\text{sim}} = -624 \text{ V/V}$ and $f_{2o\text{-sim}} = 63 \text{ kHz}$.

All of the stages discussed in this chapter require a voltage bias on the gate of the amplifying stage. Voltage reference circuits can be constructed to provide the necessary voltage bias; however, these sources will not be considered here.

Table 9.10 Spice Netlist File for Active Cascode Amplifier

```

ACTCAS.CIR

V1 1 0 1.333V
V2 5 0 5V
V3 4 1 AC 0.001V
V4 7 0 3.52V
M1 3 4 0 0 N L=1U W=5U AD=25P AS=25P PD=15U PS=15U
M2 2 4 3 0 N L=1U W=40U AD=200P AS=200P PD=50U PS=50U
M3 6 7 5 5 P L=1U W=15U AD=75P AS=75P PD=25U PS=25U
M4 2 7 6 5 P L=1U W=120U AD=600P AS=600P PD=130U PS=130U
.AC DEC 10 100 100MEG
.OP
.PROBE
.LIB C5X.LIB
.END

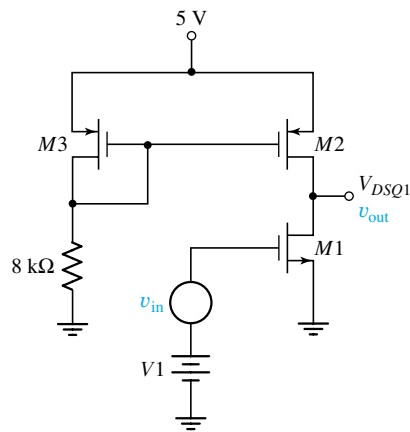
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Table 9.11 Summary of Results for Active Cascode Amplifier

C_L , pF	R_g , k Ω	$f_{2\omega\text{-sim}}$, kHz
0	0	249
1	0	69.5
0	339	87.2
1	339	45.9

DISCUSSION OF DEMONSTRATION PROBLEM

The amplifier of the Demonstration Problem is repeated here for convenience. The first part of the problem consists of solving for the current through the 8-k Ω resistance at the current mirror input, which will allow the output current from $M2$ to be equated to the current into $M1$ with an output voltage of 2.5 V.

*Amplifier for Demonstration Problem*

The drain current of $M3$ can be written as

$$I_{D3} = K_p[V_{GS3} - V_{Tp}]^2[1 - \lambda(V_{DS3} - V_{DSP3})]$$

We note that $V_{GS3} = V_{G3} - V_{DD} = 8I_{D3} - 5$ V and $V_{DS3} - V_{DSP3} = V_{Tp} = -1$ V. Writing the right side of the drain current equation in terms of I_{D3} leads to a quadratic equation. The solution of this equation results in $I_{D3} = 0.2888$ mA and $V_{G3} = 2.31$ V. The pinchoff current of both $M2$ and $M3$ is

$$I_{DP} = K_p[V_{GS} - V_{Tp}]^2 = 0.1 \times [-1.69]^2 = 0.2856 \text{ mA}$$

The pinchoff voltage is $V_{DSP} = -1.69$ V.

We now equate the current, I_{D2} , to the current I_{D1} , which allows the equation

$$I_{DSP2}[1 - \lambda(V_{DS2} - V_{DSP2})] = I_{DSP1}[1 + \lambda(V_{DS1} - V_{DSP1})]$$

to be written. The left side of this equation is I_{DS2} and the right side is I_{DS1} . Noting that

$I_{DS2} = 0.1[-1.69]^2$ leads to

$$I_{DS2} = 0.1[-1.69]^2[1 - 0.01(-2.5 + 1.69)] = 0.2879 \text{ mA}$$

This value is equated to the right side of the equation, which is

$$I_{DS1} = 0.2879 = 0.12[V_{GS1} - 1]^2[1 + 0.01(1.035 - 0.01V_{GS1})]$$

Solving for V_{GS1} gives

$$V_{GS1} = 2.54 \text{ V}$$

When this voltage is applied to the gate of $M1$, a current of 0.2879 mA and a voltage of $V_{DSQ1} = 2.5\text{V}$ result.

The incremental values of r_{ds1} and r_{ds2} can now be found from

$$r_{ds} = \frac{1}{\lambda I_{DSP}}$$

The values of r_{ds1} and r_{ds2} are equal and are both 350 k Ω . The resistance between output and ground is the parallel combination of these two resistances or 175 k Ω .

The midband voltage gain is

$$A_{MB} = -g_{m1}R_{\text{out}}$$

The value of g_m is found to be

$$g_m = \sqrt{2\mu C_{\text{ox}}(W/L)I_D}$$

For $M1$, the transconductance is 0.37 mA/V, which gives a gain of

$$A_{MB} = -0.37 \times 175 = -64.7 \text{ V/V}$$

SUMMARY

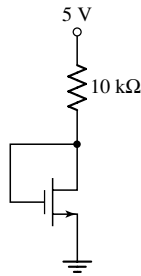
- The MOSFET amplifier designed for implementation as an IC reduces to a minimum the number of resistors required. Active loads often replace the resistors used in discrete MOSFET amplifiers.
- The current mirror is used extensively in IC design. It serves as a bias current source as well as an active load.
- The individual amplifier stage must not be analyzed as an isolated stage. The driving source resistance that may arise from a previous stage and the load capacitance that may arise from a following stage or an IC output pad must be included in the analysis of frequency response.
- The source follower has a low voltage gain but a very good frequency response.
- The cascode and partial cascode connections provide rather efficient amplifying configurations.

PROBLEMS

SECTION 9.1 MOSFET CURRENT MIRRORS

9.1 If $\mu W C_{ox}/2L = 50 \mu A/V^2$, $V_T = 0.8 V$, and $\lambda = 0.02$, calculate the drain current in the circuit shown.

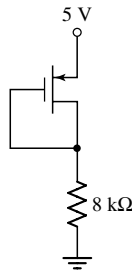
Figure P9.1



9.2 For the circuit of Problem 9.1, calculate the value of pinchoff current, I_{DP} , and pinchoff voltage, V_{DSP} .

9.3 If $\mu W C_{ox}/2L = 80 \mu A/V^2$, $V_T = -1.0 V$, and $\lambda = 0.02$, calculate the drain current in the circuit shown.

Figure P9.3



9.4 For the circuit of Problem 9.3, calculate the value of pinchoff current, I_{DP} , and pinchoff voltage, V_{DSP} .

9.5 If $\mu W C_{ox}/2L = 50 \mu A/V^2$, $V_T = 0.8 V$, and $\lambda = 0.02$, calculate the ratio I_o/I_{in} for the circuit of Fig. 9.1

SECTION 9.2.1 SIMPLE AMPLIFIER STAGES

9.8 What is the approximate midband voltage gain for the circuit of Fig. 9.4(a) if the dimensions of $M1$ are $W_1 = 24 \mu$ and $L_1 = 1 \mu$ and the dimensions of $M2$ are $W_2 = 6 \mu$ and $L_2 = 2 \mu$?

9.9 What should the value of W_1 be in Fig. 9.4(a) to lead to a midband voltage gain of $-42 V/V$? The length of the channel of $M1$ is $L_1 = 1 \mu$, and the dimensions of $M2$ are $W_2 = 2 \mu$ and $L_2 = 2 \mu$.

SECTION 9.2.2 ACTIVE LOAD STAGE

9.12 In the active load stage of Fig. 9.10, the current from the mirror is increased from $50 \mu A$ to $100 \mu A$. What would you

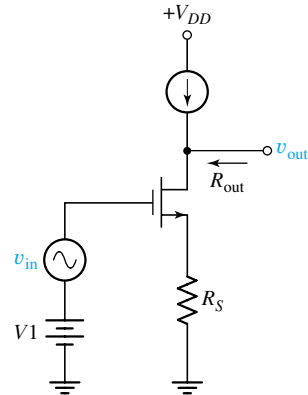
when $I_{in} = 72 \mu A$ and $V_{DS2} = 6 V$. Assume matched MOSFETs.

★ 9.6 In Fig. 9.1, the current source, I_{in} , is generated by a 12-V voltage source in series with a 60-kΩ resistor. Matched devices are used, except for V_{T2} , with values as given in Problem 9.5.

- (a) Calculate the current, I_{in} .
- (b) Calculate V_{GS} .
- (c) If I_o/I_{in} is to be unity when $V_{DS2} = 8 V$, what is the required value of V_{T2} ?
- (d) With the value of V_{T2} in part (c), what is I_o/I_{in} when $V_{DS2} = 16 V$?

9.7 Derive the output impedance, looking into the drain, for the circuit shown. Express the result in terms of r_{ds} , g_m , and R_S . Neglect body effect for this derivation. Compare this impedance to that resulting when $R_S = 0$.

Figure P9.7



D 9.10 If the circuit of Fig. 9.4(a) is to have a midband voltage gain of approximately $-4.8 V/V$, to what value should W_1 be changed?

9.11 What is the upper corner frequency of the amplifier of Fig. 9.4(a) if $C_{out} = 98 fF$, $g_{m2} = 0.4 mA/V$, and $g_{s2} = 0.05 mA/V$? Assume that the load capacitance is $50 fF$.

now expect the midband voltage gain to be? Explain your calculations.

☆ **9.13** Rework the Demonstration Problem if all parameters remain the same except $\lambda_p = 0.024 \text{ V}^{-1}$ and $\lambda_n = 0.02 \text{ V}^{-1}$.

☆ **9.14** Rework the Demonstration Problem if all parameters remain the same except $K_n = 0.16 \text{ mA/V}^2$.

9.15 In the circuit of Fig. 9.10, a resistance of value $400 \text{ k}\Omega$ is placed in series with the input signal generator. Calculate the value of load capacitance that causes the input upper corner frequency to equal the output upper corner frequency. What is the overall upper corner frequency? Use the capacitance values from the circuit simulation.

9.16 In the circuit of Fig. 9.10, a resistance is placed in series with the input signal generator. Calculate the value of this resistor to cause the input upper corner frequency to equal the output upper corner frequency. Assume a zero value for load capacitance. Use the capacitance values from the circuit simulation. What is the overall upper corner frequency?

☆ **D 9.17** In the circuit shown, the current source has infinite impedance and can be adjusted to supply whatever current is required to keep $M1$ in the active region as V_{GS} is changed. If $\lambda = 0.03 \text{ V}^{-1}$, $V_T = 1.02 \text{ V}$, and $\mu C_{ox} W/2L = 0.2 \text{ mA/V}^2$,

- Calculate A_{MB} when $V_{GS} = 2 \text{ V}$.
- Find the value of V_{GS} required to double this voltage gain. Assume that $V_{DS} = 4 \text{ V}$ for both cases.

SECTION 9.2.3 SOURCE FOLLOWER WITH ACTIVE LOAD

9.22 Rework Example 9.4 if all parameters remain the same except g_m , which becomes $g_{m1} = 300 \text{ mA/V}$.

9.23 Find the overall upper corner frequency of the source follower of Example 9.4 if a load capacitance of 0.6 pF is added.

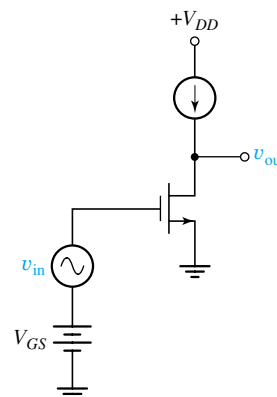
SECTION 9.2.4 THE CASCODE CONNECTION

9.25 In Example 9.5, using the cascode circuit of Fig. 9.20, the current from the mirror is increased from $50 \mu\text{A}$ to $100 \mu\text{A}$.

SECTION 9.2.5 THE ACTIVE CASCODE AMPLIFIER

9.26 Explain why the midband voltage gain increases with decreasing drain current in the active cascode amplifier.

Figure P9.17



D 9.18 If the current source in Problem D9.17 is fixed at a value of $100 \mu\text{A}$, what must V_{GS} be to result in $V_{DS} = 4 \text{ V}$? What is the value of A_{MB} for this bias?

9.19 Rework Example 9.3 for a required midband voltage gain of -76 V/V .

9.20 In the circuit of Example 9.3, the drain current is lowered to $50 \mu\text{A}$. Approximate the new value of midband voltage gain. Explain this approximation.

D 9.21 Using devices with $L = 1 \mu\text{m}$, $|V_T| = 1 \text{ V}$, $\lambda = 0.02 \text{ V}^{-1}$, and $\mu C_{ox} = 0.06 \text{ mA/V}^2$, design an active load stage with a simple current mirror load to have a midband gain of -120 V/V .

9.24 Find the overall upper corner frequency of the source follower of Example 9.4 if a load capacitance of 0.6 pF is added and a generator resistance of $100 \text{ k}\Omega$ is present. Calculate the midband voltage gain.

What would you now expect the midband voltage gain to be? Explain your calculations.