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CHAPTER 3

CIRCUIT ANALYSIS TECHNIQUES

Assuming any system of linear conductors connected in such a manner that to the extremities of each one of them there is connected at least one other, a system having electromotive forces E_1, $E_2 \ldots E_3$, no matter how distributed, we consider two points A and A′ belonging to the system and having potentials V and V′. If the points A and A′ are connected by a wire ABA′, which has a resistance r, with no electromotive forces, the potentials of points A and A′ assume different values from V and V′, but the current i flowing through this wire is given by $i = (V - V')/(r + R)$ in which R represents the resistance of the original wire, this resistance being measured between the points A and A′, which are considered to be electrodes.

Leon Charles Thévenin, 1883,
French Telegraph Engineer

Some History Behind This Chapter

Leon Charles Thévenin (1857–1926), a distinguished French telegraph engineer and teacher, was led to his theorem in 1883 following an extensive study of Kirchhoff''s laws. Norton's theorem, the dual of Thévenin's theorem, was not proposed until 1926 by Edward L. Norton, an American electrical engineer working on long-distance telephony. Curiously, it turns out that the basic concept had been discovered earlier by Herman von Helmholtz, while studying electricity in animal tissue. Electrical engineering tradition credits Thévenin and Norton, perhaps because they worked in areas that offered practical applications for their results.

Why This Chapter Is Important Today

In this chapter you advance to studying general methods of analyzing circuits and to the major theorems that describe linear circuits. These theorems are conceptual tools that give new insight into circuit behavior. Most importantly, you will be introduced to the design of interface circuits; your first exposure to devising a circuit to perform a predetermined function.

Chapter Sections

3–1 Node-Voltage Analysis
3–2 Mesh-Current Analysis
3–3 Linearity Properties
3–4 Thévenin and Norton Equivalent Circuits
3–5 Maximum Signal Transfer
3–6 Interface Circuit Design

Chapter Learning Objectives

3-1 General Circuit Analysis (Sects. 3-1 to 3-2)

Given a linear resistance circuit:
(a) (Formulation) Write node-voltage or mesh-current equations for the circuit.
(b) (Solution) Solve the equations from part (a) for selected signal variables or input-output relationships.

3-2 Linearity Properties (Sect. 3-3)

Given a linear resistance circuit:
(a) Use the proportionality principle to find selected signal variables.
(b) Use the superposition principle to find selected signal variables.

3-3 Thévenin and Norton Equivalent Circuits (Sect. 3-4)

Given a linear resistance circuit:
(a) Find the Thévenin or Norton equivalent at a specified pair of terminals.
(b) Use the Thévenin or Norton equivalent to find the signals delivered to linear or nonlinear loads.

3-4 Maximum Signal Transfer (Sect. 3-5)

Given a linear resistance circuit:
(a) Find the maximum voltage, current, and power available at a specified pair of terminals.
(b) Find the resistive loads required to obtain the maximum available signal levels.

3-5 Interface Circuit Design (Sect. 3-6)

Given the signal transfer goals at a source-load interface, design one or more two-port interface circuits to achieve the goals and evaluate the alternative design solutions.

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3–1 NODE-VOLTAGE ANALYSIS

Before describing node-voltage analysis, we first review the foundation for every method of circuit analysis. As noted in Sec. 2–3, circuit behavior is based on constraints of two types: (1) connection constraints (Kirchhoff's laws) and (2) device constraints (element *i–v* relationships). As a practical matter, however, using element voltages and currents to express the circuit constraints produces a large number of equations that must be solved simultaneously to find the circuit responses. For example, a circuit with only six devices requires us to treat 12 equations with 12 unknowns. Although this is not an impossible task using software tools like Mathcad, it is highly desirable to reduce the number of equations that must be solved simultaneously.

You should not abandon the concept of element and connection constraints. This method is vital because it provides the foundation for all methods of circuit analysis. In subsequent chapters, we use element and connection constraints many times to develop important ideas in circuit analysis.

Using node voltages instead of element voltages as circuit variables can reduce the number of equations that must be treated simultaneously. To define a set of node voltages, we first select a reference node. The **node voltages** are then defined as the voltages between the remaining nodes and the selected reference node. Figure 3–1 shows the notation used to define node-voltage variables. In this figure the reference node indicated by the ground symbol and the node voltages are identified by a voltage symbol next to all the other nodes. This notation means that the positive reference mark for the node voltage is located at the node in question while the negative mark is at the reference node. Obviously, any circuit with N nodes involves $N-1$ node voltages.

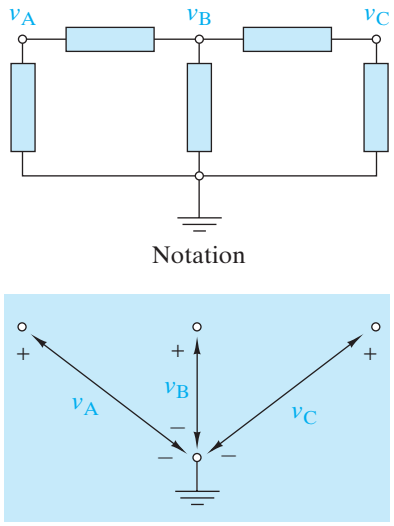

FIGURE 3–1 *Node-voltage definition and notation.*

A fundamental property of node voltages needs to be covered at the outset. Suppose we are given a two-terminal element whose element voltage is labeled v_1. Suppose further that the terminal with the plus reference mark is connected to a node, say node A. The two cases shown in Figure 3–2 are the only two possible ways the other element terminal can be connected. In case A, the other terminal is connected to the reference node, in which case KVL requires $v_1 = v_A$. In case B, the other terminal is connected to a nonreference node, say node B, in which case KVL requires $v_1 = v_A - v_B$. This example illustrates the following fundamental property of node voltages:

If the Kth two-terminal element is connected between nodes X and Y, then the element voltage can be expressed in terms of the two node voltages as

$$v_K = v_X - v_Y \tag{3–1}$$

where X is the node connected to the positive reference for element voltage v_K.

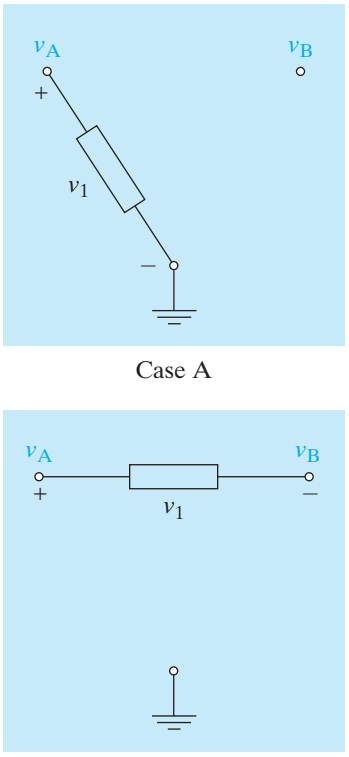

FIGURE 3–2 *Two possible connections of a two-terminal element.*

Equation (3–1) is a KVL constraint at the element level. If node Y is the reference node, then by definition $v_Y = 0$ and Eq. (3–1) reduces to $v_K = v_X$. On the other hand, if node X is the reference node, then $v_X = 0$ and therefore $v_K = -v_Y$. The minus sign occurs here because the positive reference for the element is connected to the reference node. In any case, the important fact is that the voltage across any two-terminal element can be expressed as the difference of two node voltages, one of which may be zero.

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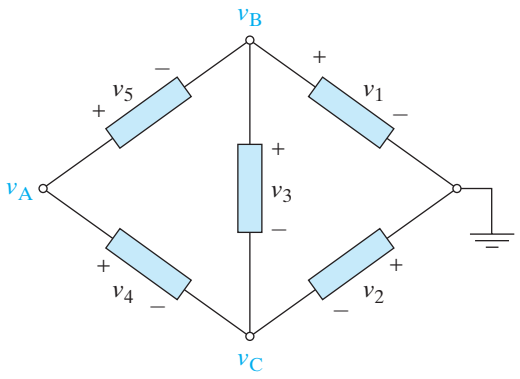
Exercise 3–1

The reference node and node voltages in the bridge circuit of Figure 3–3 are $v_A = 5$ V, $v_B = 10$ V, and $v_C = -3$ V. Find the element voltages.

FIGURE 3–3



Answers: $v_1 = 10$ V; $v_2 = 3$ V; $v_3 = 13$ V; $v_4 = 8$ V; $v_5 = -5$ V

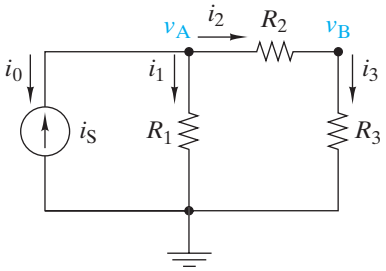


FIGURE 3–4 *Circuit for demonstrating node-voltage analysis.*

FORMULATING NODE-VOLTAGE EQUATIONS

To formulate a circuit description using node voltages, we use element and connection constraints, except that the KVL connection equations are not explicitly written. Instead we use the fundamental property of node analysis to express the element voltages in terms of the node voltages.

The circuit in Figure 3–4 will demonstrate the formulation of node-voltage equations. In Figure 3–4 we have identified a reference node (indicated by the ground symbol), four element currents (i_0, i_1, i_2, and i_3), and two node voltages (v_A and v_B).

The KCL constraints at the two nonreference nodes are

$$\text{Node A: } -i_0 - i_1 - i_2 = 0$$

$$\text{Node B: } i_2 - i_3 = 0 \tag{3–2}$$

Using the fundamental property of node analysis, we use the element equations to relate the element currents to the node voltages.

$$\text{Resistor } R_1\text{: } i_1 = G_1 v_A$$

$$\text{Resistor } R_2\text{: } i_2 = G_2(v_A - v_B)$$

$$\text{Resistor } R_3\text{: } i_3 = G_3 v_B$$

$$\text{Current Source: } i_0 = -i_S \tag{3–3}$$

We have written six equations in six unknowns—four element currents and two node voltages. The right side of the element equations in Eq. (3–3) involves unknown node voltages and the input signal i_S. Substituting the element constraints in Eq. (3–3) into the KCL connection constraints in Eq. (3–2) yields

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$$\text{Node A: } i_S - G_1 v_A - G_2(v_A - v_B) = 0$$
$$\text{Node B: } \quad G_2(v_A - v_B) - G_3 v_B = 0$$

which can be arranged in the following standard form:

$$\text{Node A: } \quad (G_1 + G_2)v_A - G_2 v_B = i_S$$
$$\text{Node B: } \quad -G_2 v_A + (G_2 + G_3)v_B = 0 \qquad (3\text{–}4)$$

In this standard form all of the unknown node voltages are grouped on one side and the independent sources on the other.

By systematically eliminating the element currents, we have reduced the circuit description to two linear equations in the two unknown node voltages. The coefficients in the equations on the left side ($G_1 + G_2$, G_2, $G_2 + G_3$) depend only on circuit parameters, while the right side contains the known input driving force i_S.

As noted previously, every method of circuit analysis must satisfy KVL, KCL, and the element *i–v* relationships. In developing the node-voltage equations in Eq. (3–4), it may appear that we have not used KVL. However, KVL is satisfied because the equations $v_1 = v_A$, $v_2 = v_A - v_B$, and $v_3 = v_B$ were used to write the right side of the element equations in Eq. (3–3). The KVL constraints do not appear explicitly in the formulation of node equations, but are implicitly included when the fundamental property of node analysis is used to write the element voltages in terms of the node voltages.

In summary, four steps are needed to develop node-voltage equations.

STEP 1 Select a reference node. Identify a node voltage at each of the remaining $N - 1$ nodes and a current with every element in the circuit.

STEP 2 Write KCL connection constraints in terms of the element currents at the $N - 1$ nonreference nodes.

STEP 3 Use the element *i–v* relationships and the fundamental property of node analysis to express the element currents in terms of the node voltages.

STEP 4 Substitute the element constraints from step 3 into the KCL connection constraints from step 2 and arrange the resulting $N - 1$ equations in a standard form.

Writing node-voltage equations leads to $N - 1$ equations that must be solved simultaneously. If we write the element and connection constraints in terms of element voltages and currents, we must solve $2E$ simultaneous equations. The reduction from $2E$ to $N - 1$ is particularly impressive in circuits with a large number of elements (large E) connected in parallel (small N).

EXAMPLE 3–1

Formulate node-voltage equations for the bridge circuit in Figure 3–5.

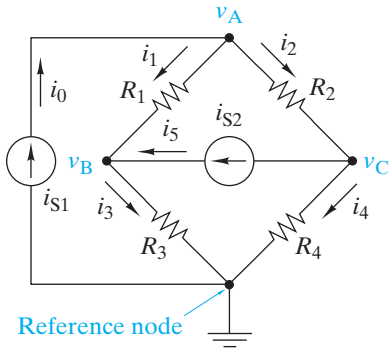

FIGURE 3–5

SOLUTION:

Step 1: The reference node, node voltages, and element currents are shown in Figure 3–5.

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Step 2: The KCL constraints at the three nonreference nodes are:

$$\text{Node A: } i_0 - i_1 - i_2 = 0$$

$$\text{Node B: } i_1 - i_3 + i_5 = 0$$

$$\text{Node C: } i_2 - i_4 - i_5 = 0$$

Step 3: We write the element equations in terms of the node voltages and input signal sources.

$$i_0 = i_{S1} \qquad i_3 = G_3 v_B$$

$$i_1 = G_1(v_A - v_B) \qquad i_4 = G_4 v_C$$

$$i_2 = G_2(v_A - v_C) \qquad i_5 = i_{S2}$$

Step 4: Substituting the element equations into the KCL constraints and arranging the result in standard form yields three equations in the three unknown node voltages.

$$\text{Node A: } (G_1 + G_2)v_A - G_1 v_B - G_2 v_C = i_{S1}$$

$$\text{Node B: } \quad -G_1 v_A + (G_1 + G_3)v_B = i_{S2}$$

$$\text{Node C: } \quad -G_2 v_A + (G_2 + G_4)v_C = -i_{S2}$$

■

WRITING NODE-VOLTAGE EQUATIONS BY INSPECTION

The node-voltage equations derived in Example 3–1 have a symmetrical pattern. The coefficient of v_B in the node A equation and the coefficient of v_A in the node B equation are both the negative of the conductance connected between the nodes ($-G_1$). Likewise, the coefficients of v_A in the node C equation and v_C in the node A equation are both $-G_2$. Finally, coefficients of v_A in the node A equation', v_B in the node B equation, and v_C in the node C equation are the sum of the conductances connected to the node in question.

The symmetrical pattern always occurs in circuits containing only resistors and independent current sources. To understand why, consider any general two-terminal conductance G with one terminal connected to, say, node A. According to the fundamental property of node analysis, there are only two possibilities. Either the other terminal of G is connected to the reference node, in which case the current *leaving* node A via conductance G is

$$i = G(v_A - 0) = Gv_A$$

or else it is connected to another nonreference node, say, node B, in which case the current *leaving* node A via G is

$$i = G(v_A - v_B)$$

The pattern for node equations follows from these observations. The sum of the currents leaving any node A via conductances involves the following terms:

1. v_A times the sum of conductances connected to node A
2. Minus v_B times the sum of conductances connected between nodes A and B and similar terms for all other nodes connected to node A by conductances

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Because of KCL, the sum of currents leaving node A via conductances plus the sum of currents directed away from node A by independent current sources must equal zero.

The aforementioned process allows us to write node-voltage equations by inspection without going through the intermediate steps involving the KCL constraints and the element equations. For example, the circuit in Figure 3–6 contains two independent current sources and four resistors. Starting with node A, the sum of conductances connected to node A is $G_1 + G_2$. The conductance between nodes A and B is G_2. The reference direction for the source current i_{S1} is into node A, while the reference direction for i_{S2} is directed away from node A. Pulling all of the observations together, we write the sum of currents directed out of node A as

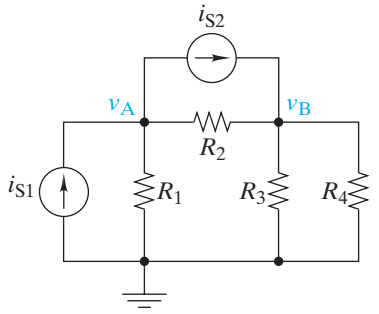

FIGURE 3–6 *Circuit for demonstrating writing node-voltage equations by inspection.*

$$\text{Node A: } (G_1 + G_2)v_A - G_2v_B - i_{S1} + i_{S2} = 0 \tag{3–5}$$

Similarly, the sum of conductances connected to node B is $G_2 + G_3 + G_4$, the conductance connected between nodes B and A is again G_2, and the source current i_{S2} is directed toward node B. These observations yield the following node-voltage equation:

$$\text{Node B: } (G_2 + G_3 + G_4)v_B - G_2v_A - i_{S2} = 0 \tag{3–6}$$

Rearranging Eqs. (3–5) and (3–6) in standard form yields

$$\begin{aligned} \text{Node A:} \quad & (G_1 + G_2)v_A - G_2v_B = i_{S1} - i_{S2} \\ \text{Node B:} \quad & -G_2v_A + (G_2 + G_3 + G_4)v_B = i_{S2} \end{aligned} \tag{3–7}$$

We have two symmetrical equations in the two unknown node voltages. The equations are symmetrical because the conductance G_2 connected between nodes A and B appears as the cross-coupling term in each equation.

EXAMPLE 3–2

Formulate node-voltage equations for the bridged-T circuit in Figure 3–7.

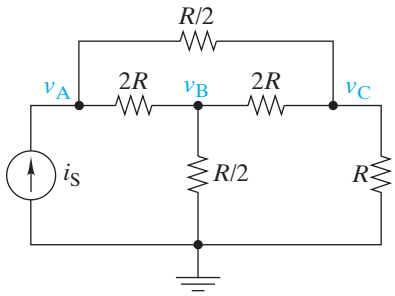

FIGURE 3–7

SOLUTION:

The total conductance connected to node A is $1/2R + 2/R = 2.5G$, to node B is $1/2R + 1/2R + 2/R = 3G$, and to node C is $1/R + 2/R + 1/2R = 3.5G$. The conductance connected between nodes A and B is $1/2R = 0.5G$, between nodes A and C is $2/R = 2G$, and between nodes B and C is $1/2R = 0.5G$. The independent current source is directed into node A. By inspection, the node-voltage equations are

$$\begin{aligned} \text{Node A:} \quad & 2.5Gv_A - 0.5Gv_B - 2Gv_C = i_S \\ \text{Node B:} \quad & -0.5Gv_A + 3Gv_B - 0.5Gv_C = 0 \\ \text{Node C:} \quad & -2Gv_A - 0.5Gv_B + 3.5Gv_C = 0 \end{aligned}$$

Written in matrix form,

$$\begin{bmatrix} 2.5G & -0.5G & -2G \\ -0.5G & 3G & -0.5G \\ -2G & -0.5G & 3.5G \end{bmatrix} \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} = \begin{bmatrix} i_S \\ 0 \\ 0 \end{bmatrix}$$

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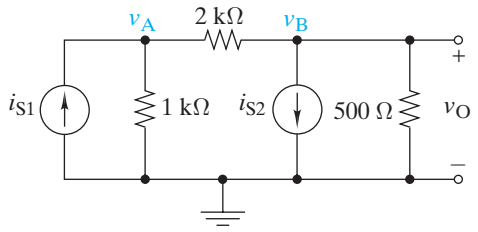
This matrix equation is of the form $\mathbf{Ax} = \mathbf{B}$, where $\mathbf{A}$ is a 3×3 square matrix describing the circuit, $\mathbf{x}$ is a 3×1 column matrix of unknown node voltages, and $\mathbf{B}$ is a 3×1 column matrix of known inputs. Note that the $\mathbf{A}$ matrix is symmetrical about its main diagonal.[1] ■

Exercise 3–2

Formulate node-voltage equations for the circuit in Figure 3–8.

FIGURE 3–8



Answers:

$$(1.5 \times 10^{-3})v_A - (0.5 \times 10^{-3})v_B = i_{S1}$$
$$-(0.5 \times 10^{-3})v_A + (2.5 \times 10^{-3})v_B = -i_{S2}$$

SOLVING LINEAR ALGEBRAIC EQUATIONS

So far, we have only dealt with the problem of formulating node-voltage equations. To complete a circuit analysis problem, we must solve these linear equations for selected responses. Cramer's rule and Gaussian elimination are standard mathematical tools commonly used for hand solution of circuit equations. These tools are assumed to be part of the reader's mathematical background. Those needing a review of these matters are referred to Appendix B.

Cramer's rule and Gaussian elimination are suitable for hand calculations involving up to three or perhaps four simultaneous equations. Cramer's rule is useful when the circuit parameters are left in symbolic form, while the Gaussian method is more efficient for numerical examples involving four or more equations. However, any problem in which Gaussian methods offer significant advantages over Cramer's rule is probably best handled using computer tools. In other words, the ready availability of computer tools makes hand solution by Gaussian elimination an obsolete skill.

At about four or five simultaneous equations, numerical solutions are best obtained using computer-aided analysis. Many scientific hand-held calculators have a built-in capability to solve five or more linear equations. Virtually all PC-based mathematical software can solve systems of linear

1 See Appendix B for a discussion of matrix algebra, including the definition of a symmetrical matrix.

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equations or, what is equivalent, perform matrix manipulations. In particular, Appendix B illustrates that both MATLAB and Mathcad can solve systems of linear equations written in matrix form.

In this book we often use Cramer's rule to solve simultaneous equations. This does not mean Cramer's rule is the optimum method, but only that it can easily handle and compactly document the solution of the class of problems treated in this book. We will also use MATLAB and Mathcad to demonstrate the use of computer tools to solve circuit equations in the matrix form. Readers needing a review of or an introduction to matrix methods are advised to study Appendix B.

Earlier in this section we formulated node-voltage equations for the circuit in Figure 3–4. [See Eq. (3–4).]

$$\text{Node A:} \quad (G_1 + G_2)v_A - G_2 v_B = i_S$$
$$\text{Node B:} \quad -G_2 v_A + (G_2 + G_3)v_B = 0$$

We use Cramer's rule to solve these equations because it easily handles the case in which the circuit parameters are left in symbolic form:

$$v_A = \frac{\Delta_A}{\Delta} = \frac{\begin{vmatrix} i_S & -G_2 \\ 0 & G_2 + G_3 \end{vmatrix}}{\begin{vmatrix} G_1 + G_2 & -G_2 \\ -G_2 & G_2 + G_3 \end{vmatrix}} = \left(\frac{G_2 + G_3}{G_1G_2 + G_1G_3 + G_2G_3} \right) i_S \qquad (3\text{–}8)$$

$$v_B = \frac{\Delta_B}{\Delta} = \frac{\begin{vmatrix} G_1 + G_2 & i_S \\ -G_2 & 0 \end{vmatrix}}{\Delta} = \left(\frac{G_2}{G_1G_2 + G_1G_3 + G_2G_3} \right) i_S \qquad (3\text{–}9)$$

These results express the two node voltages in terms of the circuit parameters and the input signal. Given the two node voltages v_A and v_B, we can now determine every element voltage and every current using Ohm's law and the fundamental property of node voltages.

$$v_1 = v_A \qquad v_2 = v_A - v_B \qquad v_3 = v_B$$
$$i_1 = G_1 v_A \qquad i_2 = G_2(v_A - v_B) \qquad i_3 = G_3 v_B$$

In solving the node equations, we left everything in symbolic form to emphasize that responses depend on the values of the circuit parameters (G_1, G_2, G_3) and the input signal (i_S). Even when numerical values are given, it is sometimes useful to leave some parameters in symbolic form to obtain input-output relationships or to reveal the effect of specific parameters on circuit response.

EXAMPLE 3–3

Given the circuit in Figure 3–9, find the input resistance R_{IN} seen by the current source and the output voltage v_O.

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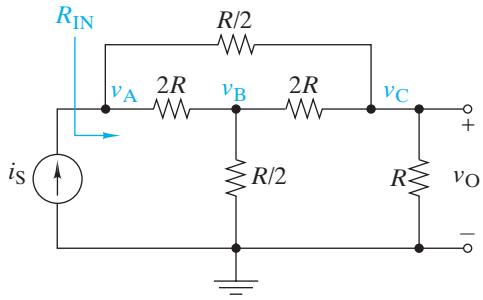
FIGURE 3–9



SOLUTION:

In Example 3–2 we formulated node-voltage equations for this circuit as follows:

$$\text{Node A:}\quad 2.5Gv_A - 0.5Gv_B - 2Gv_C = i_S$$

$$\text{Node B:}\quad -0.5Gv_A + 3Gv_B - 0.5Gv_C = 0$$

$$\text{Node C:}\quad -2Gv_A - 0.5Gv_B + 3.5Gv_C = 0$$

The input resistance is the ratio v_A/i_S, so we first solve for v_A:

$$v_A = \frac{\Delta_A}{\Delta} = \frac{\begin{vmatrix} i_S & -0.5G & -2G \\ 0 & 3G & -0.5G \\ 0 & -0.5G & 3.5G \end{vmatrix}}{\begin{vmatrix} 2.5G & -0.5G & -2G \\ -0.5G & 3G & -0.5G \\ -2G & -0.5G & 3.5G \end{vmatrix}}$$

$$= \frac{i_S \times G^2 \begin{vmatrix} 3 & -0.5 \\ -0.5 & 3.5 \end{vmatrix}}{2.5G^3 \begin{vmatrix} 3 & -0.5 \\ -0.5 & 3.5 \end{vmatrix} + 0.5G^3 \begin{vmatrix} -0.5 & -2 \\ -0.5 & 3.5 \end{vmatrix} - 2G^3 \begin{vmatrix} -0.5 & -2 \\ 3 & -0.5 \end{vmatrix}}$$

$$= \frac{10.25 i_S}{11.75G}$$

Hence the input resistance is

$$R_{IN} = \frac{v_A}{i_S} = \frac{10.25}{11.75G} = 0.872R$$

To find the output voltage, we solve for v_C:

$$v_C = \frac{\Delta_C}{\Delta} = \frac{\begin{vmatrix} 2.5G & -0.5G & i_S \\ -0.5G & 3G & 0 \\ -2G & -0.5G & 0 \end{vmatrix}}{\Delta} = \frac{i_S \times G^2 \begin{vmatrix} -0.5 & 3 \\ -2 & -0.5 \end{vmatrix}}{\Delta}$$

$$= \frac{6.25G^2 i_S}{11.75G^3} = 0.532 i_S R$$

■

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Exercise 3–3

Solve the node-voltage equations in Exercise 3–2 for v_O in Figure 3–8.

Answer: $v_O = 1000(i_{S1} - 3i_{S2})/7$

Exercise 3–4

Use node-voltage equations to solve for v_1, v_2, and i_3 in Figure 3–10.

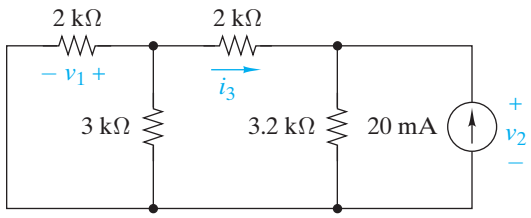

FIGURE 3–10

Answers: $v_1 = 12$ V; $v_2 = 32$ V; $i_3 = -10$ mA

NODE ANALYSIS WITH VOLTAGE SOURCES

Up to this point we have analyzed circuits containing only resistors and independent current sources. Applying KCL in such circuits is simplified because the sum of currents at a node only involves the output of current sources or resistor currents expressed in terms of the node voltages. Adding voltage sources to circuits modifies node analysis procedures because the current through a voltage source is not directly related to the voltage across it. While initially it may appear that voltage sources complicate the situation, they actually simplify node analysis by reducing the number of equations required.

Figure 3–11 shows three ways to deal with voltage sources in node analysis. Method 1 uses a source transformation to replace the voltage source and series resistance with an equivalent current source and parallel resistance. We can then formulate node equations at the remaining nonreference nodes in the usual way. The source transformation eliminates node C, so there are only $N - 2$ nonreference nodes left in the circuit. Obviously, method 1 only applies when there is a resistance in series with the voltage source.

Method 2 in Figure 3–11 can be used whether or not there is a resistance in series with the voltage source. When node B is selected as the reference node, then by definition $v_B = 0$ and the fundamental property of node voltages says that $v_A = v_S$. We do not need a node-voltage equation at node A because its voltage is known to be equal to the source voltage. We write the node equations at the remaining $N - 2$ nonreference nodes in the usual way. In the final step, we move all terms involving v_A to the right side, since it is a known input and not an unknown response. Method 2 reduces the number of node equations by 1 since no equation is needed at node A.

The third method in Figure 3–11 is needed when neither node A nor node B can be selected as the reference and the source is not connected in

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EQA

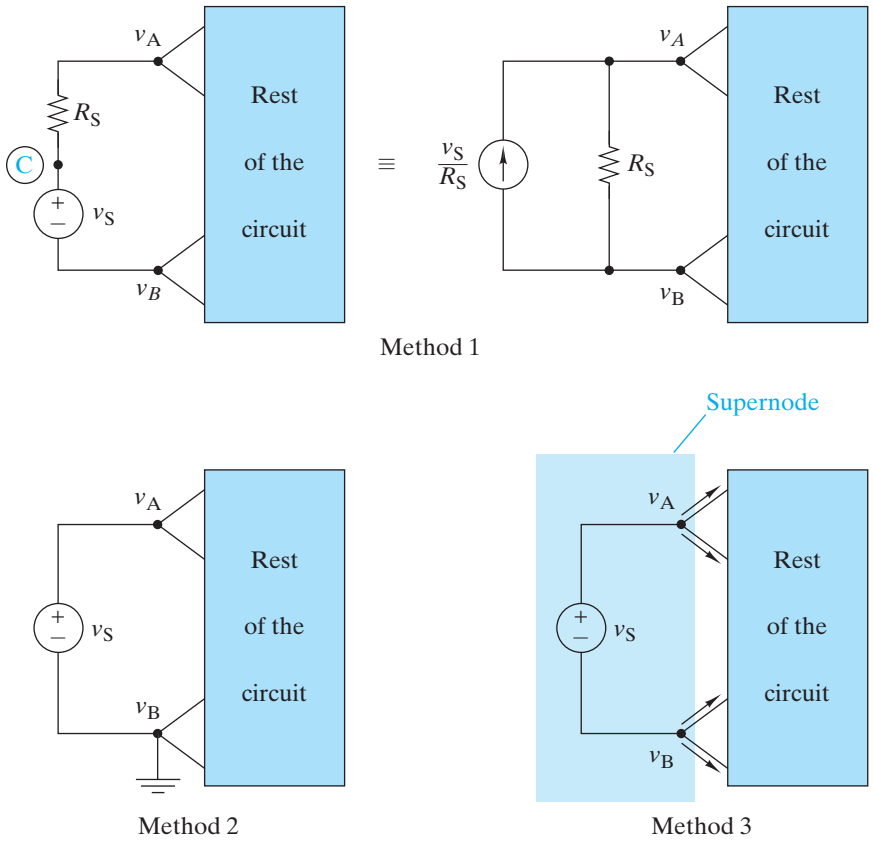

FIGURE 3–11 *Three methods of treating voltage sources in node analysis.*

series with a resistance. In this case we combine nodes A and B into a **supernode**, indicated by the boundary in Figure 3–11. We use the fact that KCL applies to the currents penetrating this boundary to write a node equation at the supernode. We then write node equations at the remaining $N-3$ nonreference nodes in the usual way. We now have $N-3$ node equations plus one supernode equation, leaving us one equation short of the $N-1$ required. Using the fundamental property of node voltages, we can write

$$v_A - v_B = v_S \tag{3–10}$$

The voltage source inside the supernode constrains the difference between the node voltages at nodes A and B. The voltage source constraint provides the additional relationship needed to write $N-1$ independent equations in $N-1$ node voltages.

For reference purposes we will call these modified node equations, since we either modify the circuit (method 1), use voltage source constraints to define node voltage at some nodes (method 2), or combine nodes to produce a supernode (method 3). The three methods are not mutually exclusive. We frequently use a combination of methods, as illustrated in the following examples.

EXAMPLE 3–4

Use node-voltage analysis to find v_O in the circuit in Figure 3–12(a).

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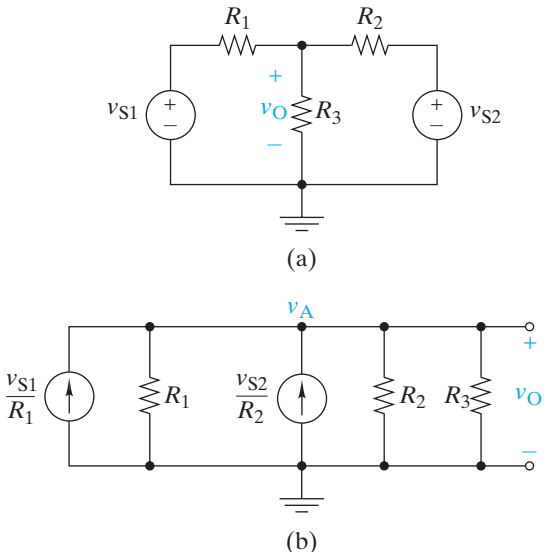

FIGURE 3–12

SOLUTION:

The given circuit in Figure 3–12(a) has four nodes, so we appear to need $N - 1 = 3$ node-voltage equations. However, applying source transformations to the two voltage sources (method 1) produces the two-node circuit in Figure 3–12(b). For the modified circuit, we need only one node equation.

$$(G_1 + G_2 + G_3)v_A = G_1v_{S1} + G_2v_{S2}$$

To find the output voltage, we solve for v_A:

$$v_O = v_A = \frac{G_1v_{S1} + G_2v_{S2}}{G_1 + G_2 + G_3}$$

Because of the two voltage sources, we need only one node equation in what appears to be a three-node circuit. The two voltage sources have a common node, so the number of unknown node voltages is reduced from three to one. The general principle illustrated is that the number of independent KCL constraints in a circuit containing N nodes and N_V voltage sources is $N - 1 - N_V$. ■

EXAMPLE 3–5

Find the input resistance of the circuit in Figure 3–13.

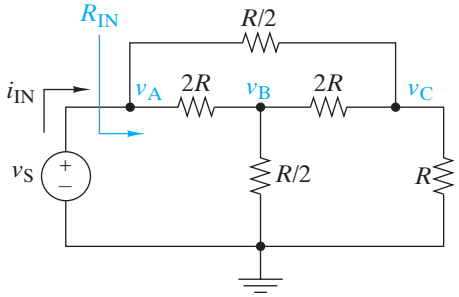

FIGURE 3–13

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EQA

SOLUTION:

Method 1 of handling voltage sources will not work here because the source in Figure 3–13 is not connected in series with a resistor. Method 2 will work in this case because the voltage source is connected to the reference node. As a result, we only need node equations at nodes B and C since the node A voltage is $v_A = v_S$. By inspection, the two required node equations are

$$\text{Node B:} \quad -0.5Gv_A + 3Gv_B - 0.5Gv_C = 0$$

$$\text{Node C:} \quad -2Gv_A - 0.5Gv_B + 3.5Gv_C = 0$$

Since $v_A = v_S$, these equations can be written in standard form as follows:

$$\text{Node B:} \quad 3Gv_B - 0.5Gv_C = 0.5Gv_S$$

$$\text{Node C:} \quad -0.5Gv_B + 3.5Gv_C = 2Gv_S$$

Solving for the two unknown node voltages yields

$$v_B = \frac{\Delta_B}{\Delta} = \frac{\begin{vmatrix} 0.5Gv_S & -0.5G \\ 2Gv_S & 3.5G \end{vmatrix}}{\begin{vmatrix} 3G & -0.5G \\ -0.5G & 3.5G \end{vmatrix}} = \frac{2.75G^2v_S}{10.25G^2} = \frac{2.75v_S}{10.25}$$

$$v_C = \frac{\Delta_C}{\Delta} = \frac{\begin{vmatrix} 3G & 0.5Gv_S \\ -0.5G & 2Gv_S \end{vmatrix}}{\Delta} = \frac{6.25G^2v_S}{10.25G^2} = \frac{6.25v_S}{10.25}$$

Given the two node voltages, we can now solve for the input current.

$$i_{IN} = \frac{v_S - v_B}{2R} + \frac{v_S - v_C}{R/2} = \frac{3.75v_S}{10.25R} + \frac{8v_S}{10.25R} = \frac{11.75v_S}{10.25R}$$

Hence, the input resistance is

$$R_{IN} = \frac{v_S}{i_{IN}} = \frac{10.25R}{11.75} = 0.872R$$

This is the same answer as in Example 3–3, where the same circuit was driven by a current source rather than a voltage source. Input resistance is an intrinsic property of a circuit that does not depend on how the circuit is driven. ■

EXAMPLE 3–6

For the circuit in Figure 3–14,

(a) Formulate node-voltage equations.
(b) Solve for the output voltage v_O using $R_1 = R_4 = 2\ \text{k}\Omega$ and $R_2 = R_3 = 4\ \text{k}\Omega$.

SOLUTION:

(a) The voltage sources in Figure 3–14 do not have a common node, and we cannot select a reference node that includes both sources. Selecting node D as the reference forces the condition $v_B = v_{S2}$ (method 2) but leaves the other source v_{S1} ungrounded. We surround the ungrounded source,

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EQA

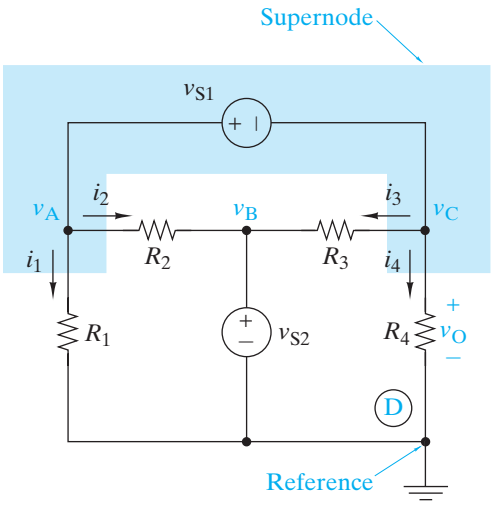

FIGURE 3–14

and all wires leading to it, by the supernode boundary shown in Figure 3–14 (method 3). KCL applies to the four element currents that penetrate the supernode boundary, and we can write

$$i_1 + i_2 + i_3 + i_4 = 0$$

These currents can easily be expressed in terms of the node voltages.

$$G_1 v_A + G_2(v_A - v_B) + G_3(v_C - v_B) + G_4 v_C = 0$$

Since $v_B = v_{S2}$, the standard form of this equation is

$$(G_1 + G_2)v_A + (G_3 + G_4)v_C = (G_2 + G_3)v_{S2}$$

We have one equation in the two unknown node voltages v_A and v_C. Applying the fundamental property of node voltages inside the supernode, we can write

$$v_A - v_C = v_{S1}$$

That is, the ungrounded voltage source constrains the difference between the two unknown node voltages inside the supernode. It thereby supplies the relationship needed to obtain two equations in two unknowns.

(b) Inserting the given numerical values yields

$$(7.5 \times 10^{-4})v_A + (7.5 \times 10^{-4})v_C = (5 \times 10^{-4})v_{S2}$$

$$v_A - v_C = v_{S1}$$

To find the output v_O, we need to solve these equations for v_C. The second equation yields $v_A = v_C + v_{S1}$, which, when substituted into the first equation, yields the required output:

$$v_O = v_C = \frac{v_{S2}}{3} - \frac{v_{S1}}{2}$$

■

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EQA

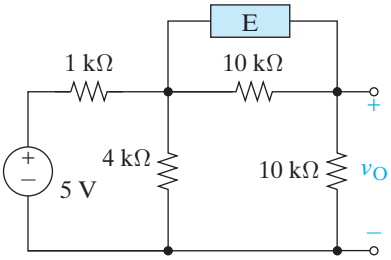

FIGURE 3–15

Exercise 3–5

Find v_O in Figure 3–15 when the element E is

(a) A 10-kΩ resistance
(b) A 4-mA independent current source with reference arrow pointing left

Answers:

(a) 2.53 V
(b) –17.3 V

Exercise 3–6

Find v_O in Figure 3–15 when the element E is

(a) An open circuit
(b) A 10-V independent voltage source with the plus reference on the right

Answers:

(a) 1.92 V
(b) 12.96 V

SUMMARY OF NODE-VOLTAGE ANALYSIS

We have seen that node-voltage equations are very useful in the analysis of a variety of circuits. These equations can always be formulated using KCL, the element constraints, and the fundamental property of node voltages. When in doubt, always fall back on these principles to formulate node equations in new situations. With practice and experience, however, we eventually develop an analysis approach that allows us to recognize shortcuts in the formulation process. The following guidelines summarize our approach and may help you develop your own analysis style:

1. Simplify the circuit by combining elements in series and parallel wherever possible.
2. If not specified, select a reference node so that as many voltage sources as possible are directly connected to the reference.
3. Node equations are required at supernodes and all other nonreference nodes except those that are directly connected to the reference by voltage sources.
4. Use KCL to write node equations at the nodes identified in step 3. Express element currents in terms of node voltages or the currents produced by independent current sources.
5. Write expressions relating the node voltages to the voltages produced by independent voltage sources.
6. Substitute the expressions from step 5 into the node equations from step 4 and arrange the resulting equations in standard form.
7. Solve the equations from step 6 for the node voltages of interest. Cramer's rule is often useful when circuit parameters are left in symbolic form. Computer tools are useful when there are four or more equations and numerical values are given.

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EQA

3–2 MESH-CURRENT ANALYSIS

Mesh currents are analysis variables that are useful in circuits containing many elements connected in series. To review terminology, a loop is a closed path formed by passing through an ordered sequence of nodes without passing through any node more than once. A mesh is a special type of loop that does not enclose any elements. For example, loops A and B in Figure 3–16 are meshes, while the loop X is not a mesh because it encloses an element.

Mesh-current analysis is restricted to planar circuits. A **planar circuit** can be drawn on a flat surface without crossovers in the "window pane" fashion shown in Figure 3–16. To define a set of variables, we associate a **mesh current** (i_A, i_B, i_C, etc.) with each window pane and assign a reference direction. The reference directions for all mesh currents are customarily taken in a clockwise sense. There is no momentous reason for this, except perhaps tradition.

We think of these mesh currents as circulating through the elements in their respective meshes, as suggested by the reference directions shown in Figure 3–16. We should emphasize that this viewpoint is not based on the physics of circuit behavior. There are not red and blue electrons running around that somehow get assigned to mesh currents i_A or i_B. Mesh currents are variables used in circuit analysis. They are only somewhat abstractly related to the physical operation of a circuit and may be impossible to measure directly. For example, there is no way to cut the circuit in Figure 3–16 to insert an ammeter that only measures i_E.

Mesh currents have a unique feature that is the dual of the fundamental property of node voltages. If we examine Figure 3–16, we see the elements around the perimeter are contained in only one mesh, while those in the interior are in two meshes. In a planar circuit any given element is contained in at most two meshes. When an element is in two meshes, the two mesh currents circulate through the element in opposite directions. In such cases KCL declares that the net current through the element is the difference of the two mesh currents.

These observations lead us to the fundamental property of mesh currents:

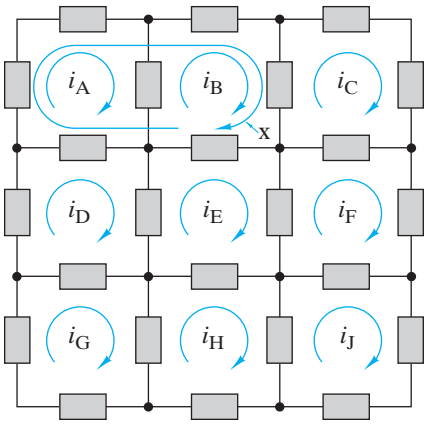

FIGURE 3–16 *Meshes in a planar circuit.*

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If the Kth two-terminal element is contained in meshes X and Y, then the element current can be expressed in terms of the two mesh currents as

$$i_K = i_X - i_Y \tag{3–11}$$

where X is the mesh whose reference direction agrees with the reference direction of i_K.

Equation (3–11) is a KCL constraint at the element level. If the element is contained in only one mesh, then $i_K = i_X$ or $i_K = -i_Y$, depending on whether the reference direction for the element current agrees or disagrees with the reference direction of the mesh current. The key idea is that the current through every two-terminal element in a planar circuit can be expressed in terms of no more than two mesh currents.

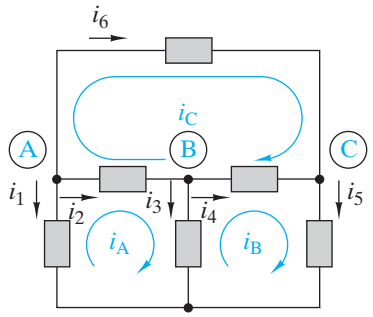


FIGURE 3–17

Exercise 3–7

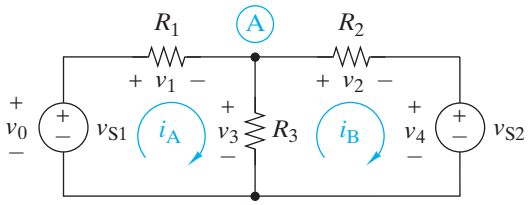
In Figure 3–17 the mesh currents are $i_A = 10$ A, $i_B = 5$ A, and $i_C = -3$ A. Find the element currents i_1 through i_6 and show that KCL is satisfied at nodes A, B, and C.

Answers: $i_1 = -10$ A; $i_2 = 13$ A; $i_3 = 5$ A; $i_4 = 8$ A; $i_5 = 5$ A; $i_6 = -3$ A.

To use mesh currents to formulate circuit equations, we use elements and connection constraints, except that the KCL constraints are not explicitly written. Instead, we use the fundamental property of mesh currents to express the element voltages in terms of the mesh currents. By doing so we avoid using the element currents and work only with the element voltages and mesh currents.

For example, the planar circuit in Figure 3–18 can be analyzed using the mesh-current method. In the figure we have defined two mesh currents

FIGURE 3–18 *Circuit for demonstrating mesh-current analysis.*



and five element voltages. We write KVL constraints around each mesh using the element voltages.

$$\text{Mesh A: } -v_0 + v_1 + v_3 = 0$$
$$\text{Mesh B: } -v_3 + v_2 + v_4 = 0 \tag{3–12}$$

Using the fundamental property of mesh currents, we write the element voltages in terms of the mesh currents and input voltages:

$$\begin{aligned} v_1 &= R_1 i_A & v_0 &= v_{S1} \\ v_2 &= R_2 i_B & v_4 &= v_{S2} \\ v_3 &= R_3(i_A - i_B) \end{aligned} \tag{3–13}$$

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EQA

We substitute these element equations into the KVL connection equations and arrange the result in standard form.

$$\begin{aligned}(R_1 + R_3)i_A - R_3 i_B &= v_{S1}\\ -R_3 i_A + (R_2 + R_3)i_B &= -v_{S2}\end{aligned} \tag{3–14}$$

We have completed the formulation process with two equations in two unknown mesh currents.

As we have previously noted, every method of circuit analysis must satisfy KCL, KVL, and the element *i–v* relationships. When formulating mesh equations, it may appear that we have not used KCL. However, writing the element constraints in the form in Eq. (3–13) requires the KCL equations $i_1 = i_A$, $i_2 = i_B$, and $i_3 = i_A - i_B$. Mesh-current analysis implicitly satisfies KCL when the element constraints are expressed in terms of the mesh currents. In effect, the fundamental property of mesh currents ensures that the KCL constraints are satisfied.

We use Cramer's rule to solve for the mesh currents in Eq. (3–14):

$$i_A = \frac{\Delta_A}{\Delta} = \frac{\begin{vmatrix} v_{S1} & -R_3 \\ -v_{S2} & R_2 + R_3 \end{vmatrix}}{\begin{vmatrix} R_1 + R_3 & -R_3 \\ -R_3 & R_2 + R_3 \end{vmatrix}} = \frac{(R_2 + R_3)v_{S1} - R_3 v_{S2}}{R_1R_2 + R_1R_3 + R_2R_3} \tag{3–15}$$

and

$$i_B = \frac{\Delta_B}{\Delta} = \frac{\begin{vmatrix} R_1 + R_3 & v_{S1} \\ -R_3 & -v_{S2} \end{vmatrix}}{\begin{vmatrix} R_1 + R_3 & -R_3 \\ -R_3 & R_2 + R_3 \end{vmatrix}} = \frac{R_3 v_{S1} - (R_1 + R_3)v_{S2}}{R_1R_2 + R_1R_3 + R_2R_3} \tag{3–16}$$

Equations (3–15) and (3–16) can now be substituted into the element constraints in Eq. (3–13) to solve for every voltage in the circuit. For instance, the voltage across R_3 is

$$v_3 = R_3(i_A - i_B) = \frac{R_2R_3v_{S1} + R_1R_3v_{S2}}{R_1R_2 + R_1R_3 + R_2R_3} \tag{3–17}$$

You are invited to show that the result in Eq. (3–17) agrees with the node analysis result obtained in Example 3–4 for the same circuit.

The mesh-current analysis approach just illustrated can be summarized in four steps:

STEP 1 Identify a mesh current with every mesh and a voltage across every circuit element.

STEP 2 Write KVL connection constraints in terms of the element voltages around every mesh.

STEP 3 Use KCL and the *i–v* relationships of the elements to express the element voltages in terms of the mesh currents.

STEP 4 Substitute the element constraints from step 3 into the connection constraints from step 2 and arrange the resulting equations in standard form.

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EQA

The number of mesh-current equations derived in this way equals the number of KVL connection constraints in step 2. When discussing combined constraints in Chapter 2, we noted that there are $E - N + 1$ independent KVL constraints in any circuit. Using the window panes in a planar circuit generates $E - N + 1$ independent mesh currents. Mesh analysis works best when the circuit has many elements (E large) connected in series (N also large).

WRITING MESH-CURRENT EQUATIONS BY INSPECTION

The mesh equations in Eq. (3–14) have a symmetrical pattern that is similar to the coefficient symmetry observed in node equations. The coefficients of i_B in the first equation and i_A in the second equation are the negative of the resistance common to meshes A and B. The coefficients of i_A in the first equation and i_B in the second equation are the sum of the resistances in meshes A and B, respectively.

This pattern will always occur in planar circuits containing resistors and independent voltage sources when the mesh currents are defined in the window panes of a planar circuit, as shown in Figure 3–16. To see why, consider a general resistance R that is contained in, say, mesh A. There are only two possibilities. Either R is not contained in any other mesh, in which case the voltage across it is

$$v = R(i_A - 0) = Ri_A$$

or else it is also contained in only one adjacent mesh, say mesh B, in which case the voltage across it is

$$v = R(i_A - i_B)$$

These observations lead to the following conclusions. The voltage across resistance in mesh A involves the following terms:

1. i_A times the sum of the resistances in mesh A
2. $-i_B$ times the sum of resistances common to mesh A and mesh B, and similar terms for any other mesh adjacent to mesh A

The sum of the voltages across resistors plus the sum of the independent voltage sources around mesh A must equal zero.

The aforementioned process makes it possible for us to write mesh-current equations by inspection without going through the intermediate steps involving the KVL connection constraints and the element constraints.

EXAMPLE 3–7

For the circuit of Figure 3–19,

(a) Formulate mesh-current equations.
(b) Find the output v_O using $R_1 = R_4 = 2\ \text{k}\Omega$ and $R_2 = R_3 = 4\ \text{k}\Omega$.

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EQA

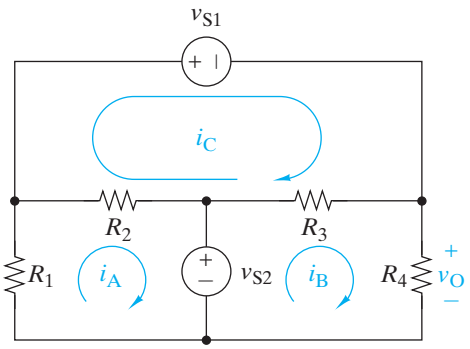

FIGURE 3–19

SOLUTION:

(a) To write mesh-current equations by inspection, we note that the total resistances in meshes A, B, and C are $R_1 + R_2$, $R_3 + R_4$, and $R_2 + R_3$, respectively. The resistance common to meshes A and C is R_2. The resistance common to meshes B and C is R_3. There is no resistance common to meshes A and B. Using these observations, we write the mesh equations as

$$\text{Mesh A: } (R_1 + R_2)i_A - 0\,i_B - R_2 i_C + v_{S2} = 0$$

$$\text{Mesh B: } (R_3 + R_4)i_B - 0\,i_A - R_3 i_C - v_{S2} = 0$$

$$\text{Mesh C: } (R_2 + R_3)i_C - R_2 i_A - R_3 i_B + v_{S1} = 0$$

The algebraic signs assigned to voltage source terms follow the passive convention for the mesh current in question. Arranged in standard form, these equations become

$$\begin{aligned} (R_1 + R_2)i_A - R_2 i_C &= -v_{S2} \\ +(R_3 + R_4)i_B - R_3 i_C &= +v_{S2} \\ -R_2 i_A - R_3 i_B + (R_2 + R_3)i_C &= -v_{S1} \end{aligned}$$

Coefficient symmetry greatly simplifies the formulation of these equations compared with the more fundamental, but time-consuming, process of writing element and connection constraints.

(b) Inserting the numerical values into these equations yields

$$\begin{aligned} 6000\,i_A - 4000\,i_C &= -v_{S2} \\ 6000\,i_B - 4000\,i_C &= v_{S2} \\ -4000\,i_A - 4000\,i_B + 8000\,i_C &= -v_{S1} \end{aligned}$$

Placing these three mesh equations in matrix form produces

$$\begin{bmatrix} 6000 & 0 & -4000 \\ 0 & 6000 & -4000 \\ -4000 & -4000 & +8000 \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} -v_{S2} \\ v_{S2} \\ -v_{S1} \end{bmatrix}$$

This is a matrix equation of the form $\mathbf{AX} = \mathbf{B}$, where

$$\mathbf{A} = \begin{bmatrix} 6000 & 0 & -4000 \\ 0 & 6000 & -4000 \\ -4000 & -4000 & +8000 \end{bmatrix} \quad \mathbf{X} = \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} \quad \mathbf{B} = \begin{bmatrix} -v_{S2} \\ v_{S2} \\ -v_{S1} \end{bmatrix}$$

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EQA

The matrix **A** is a square matrix of the coefficients on the left side of the mesh equations, **X** is a column matrix of the unknown mesh currents, and **B** is a column matrix of the input voltages on the right side of the mesh equations. To solve this matrix equation, we multiply by the inverse of the coefficient matrix ($\mathbf{A}^{-1}$). On the left side the result is $\mathbf{A}^{-1}\mathbf{AX} = \mathbf{X}$, and the right side becomes $\mathbf{A}^{-1}\mathbf{B}$. In other words, multiplying by $\mathbf{A}^{-1}$ yields the solution for the unknown mesh currents as

$$\mathbf{X} = \mathbf{A}^{-1}\mathbf{B}$$

In sum, to solve a system of linear equations by matrix methods we form the matrix product $\mathbf{A}^{-1}\mathbf{B}$. It is at this point that MATLAB comes into play.

Using MATLAB to solve for the mesh currents, we first enter the **A** matrix by the statement

```
A=[6000 0 -4000;0 6000 -4000;-4000 -4000 8000];
```

The elements in **B** matrix are the symbolic variables v_{S1} and v_{S2}. These quantities are not unknowns, but symbols that represent all possible values of the input voltages. Thus, we must first write the statement

```
syms VS1 VS2
```

which declares these identifiers to be symbolic rather than numerical quantities. We can now enter the **B** matrix as

```
B=[-VS2;VS2;-VS1];
```

and solve for the unknown mesh currents using MATLAB statement

```
X=inv(A)*B
```

which yields

```
X =

[-1/6000*VS2-1/4000*VS1]
[1/6000*VS2-1/4000*VS1]
[           -3/8000*VS1]
```

The elements of the column matrix **X** are the three unknown mesh currents expressed in terms of the input voltages. The output voltage in Figure 3–19 is written in terms of the mesh currents as $v_O = R_4 i_B$. In MATLAB notation the required mesh current is

```
iB = X(2)=1/6000*VS2-1/4000*VS1
```

Since $R_4 = 2000$ we conclude that

$$v_O = \frac{v_{S2}}{3} - \frac{v_{S1}}{2}$$

The mesh-current analysis result obtained here is the same as the node-voltage result obtained in Example 3–6. Either approach produces the same answer, but which method do you think is easier? ■

MESH EQUATIONS WITH CURRENT SOURCES

In developing mesh analysis, we assumed that circuits contain only voltage sources and resistors. This assumption simplifies the formulation process because the sum of voltages around a mesh is determined by voltage sources and the mesh currents through resistors. A current source complicates the picture because the voltage across it is not directly related to its

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current. We need to adapt mesh analysis to accommodate current sources just as we revised node analysis to deal with voltage sources.

There are three ways to handle current sources in mesh analysis:

1. If the current source is connected in parallel with a resistor, then it can be converted to an equivalent voltage source by source transformation. Each source conversion eliminates a mesh and reduces the number of equations required by 1. This method is the dual of method 1 for node analysis.

2. If a current source is contained in only one mesh, then that mesh current is determined by the source current and is no longer an unknown. We write mesh equations around the remaining meshes in the usual way and move the known mesh current to the source side of the equations in the final step. The number of equations obtained is one less than the number of meshes. This method is the dual of method 2 for node analysis.

3. Neither of the first two methods will work when a current source is contained in two meshes or is not connected in parallel with a resistance. In this case we create a **supermesh** by excluding the current source and any elements connected in series with it, as shown in Figure 3–20. We write one mesh equation around the supermesh

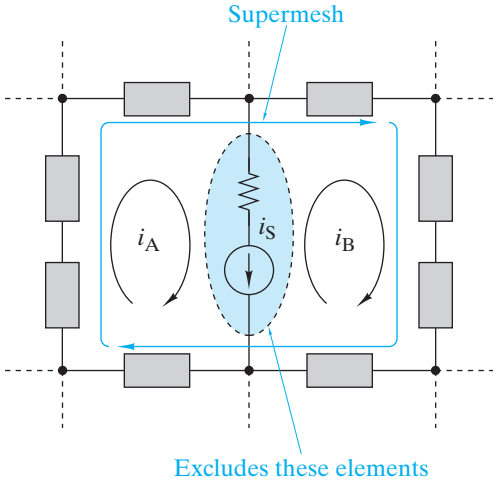

FIGURE 3–20 *Example of a supermesh.*

using the currents i_A and i_B. We then write mesh equations of the remaining meshes in the usual way. This leaves us one equation short because parts of meshes A and B are included in the supermesh. However, the fundamental property of mesh currents relates the currents i_S, i_A, and i_B as

$$i_A - i_B = i_S$$

This equation supplies the one additional relationship needed to get the requisite number of equations in the unknown mesh currents.

The aforementioned three methods are not mutually exclusive. We can use more than one method in a circuit, as the following examples illustrate.

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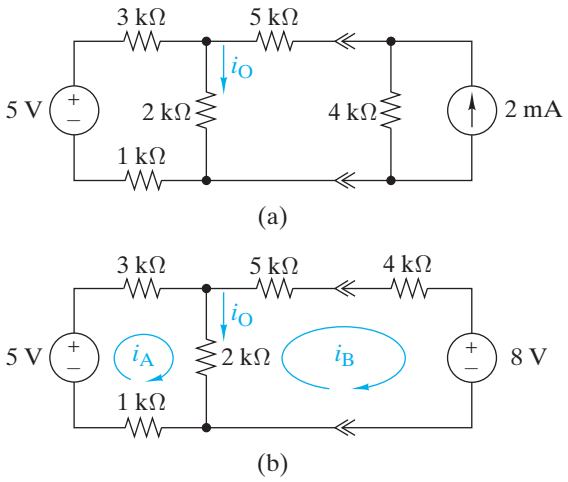
EXAMPLE 3–8

Use mesh-current equations to find i_O in the circuit in Figure 3–21(a).

FIGURE 3–21



SOLUTION:

The current source in this circuit can be handled by a source transformation (method 1). The 2-mA source in parallel with the 4-kΩ resistor in Figure 3–21(a) can be replaced by an equivalent 8-V voltage source in series with the same resistor, as shown in Figure 3–21(b). In this circuit the total resistance in mesh A is 6 kΩ, the total resistance in mesh B is 11 kΩ, and the resistance contained in both meshes is 2 kΩ. By inspection, the mesh equations for this circuit are

$$(6000)i_A - (2000)i_B = 5$$

$$-(2000)i_A + (11000)i_B = -8$$

Solving for the two mesh currents yields $i_A = 0.6290$ mA and $i_B = -0.6129$ mA. By KCL the desired current is $i_O = i_A - i_B = 1.2419$ mA. The given circuit in Figure 3–21(a) has three meshes and one current source. The source transformation leading to Figure 3–21(b) produces a circuit with only two meshes. The general principle illustrated is that the number of independent mesh equations in a circuit containing E elements, N nodes, and N_I current sources is $E - N + 1 - N_I$. ■

EXAMPLE 3–9

Use mesh-current equations to find the v_O in Figure 3–22.

SOLUTION:

Source transformation (method 1) is not possible here since neither current source is connected in parallel with a resistor. The current source i_{S2} is in both mesh B and mesh C, so we exclude this element and create the

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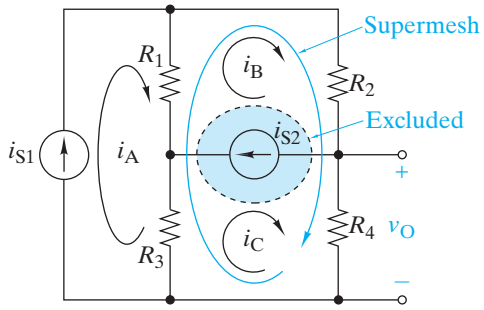

FIGURE 3–22

supermesh (method 3) shown in the figure. The sum of voltages around the supermesh is

$$R_1(i_B - i_A) + R_2(i_B) + R_4(i_C) + R_3(i_C - i_A) = 0$$

The supermesh voltage constraint yields one equation in the three unknown mesh currents. Applying KCL to each of the current sources yields

$$i_A = i_{S1}$$
$$i_B - i_C = i_{S2}$$

Because of KCL, the two current sources force constraints that supply two more equations. Using these two KCL constraints to eliminate i_A and i_B from the supermesh KVL constraint yields

$$(R_1 + R_2 + R_3 + R_4)i_C = (R_1 + R_3)i_{S1} - (R_1 + R_2)i_{S2}$$

Hence, the required output voltage is

$$v_O = R_4 i_C = R_4 \times \left[\frac{(R_1 + R_3)i_{S1} - (R_1 + R_2)i_{S2}}{R_1 + R_2 + R_3 + R_4}\right]$$ ■

Exercise 3–8

Use mesh analysis to find the current i_O in Figure 3–23 when the element E is

(a) A 5-V voltage source with the positive reference at the top
(b) A 10-kΩ resistor

Answers:

(a) –0.136 mA
(b) –0.538 mA

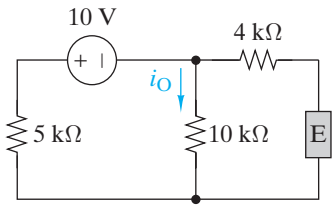

FIGURE 3–23

Exercise 3–9

Use mesh analysis to find the current i_O in Figure 3–23 when the element E is

(a) A 1-mA current source with the reference arrow directed down
(b) Two 20-kΩ resistors in parallel

Answers:

(a) –1 mA
(b) –0.538 mA

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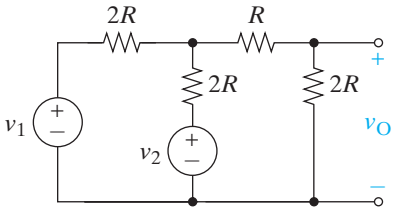

FIGURE 3–24

Exercise 3–10

Use mesh-current equations to find v_O in Figure 3–24.

Answer: $v_O = (v_1 + v_2)/4$

SUMMARY OF MESH-CURRENT ANALYSIS

Mesh-current equations can always be formulated from KVL, the element constraints, and the fundamental property of mesh currents. When in doubt, always fall back on these principles to formulate mesh equations in new situations. The following guidelines summarize an approach to formulating mesh equations for resistance circuits:

1. Simplify the circuit by combining elements in series or parallel wherever possible.
2. Mesh equations are required for supermeshes and all other meshes except those where current sources are contained in only one mesh.
3. Use KVL to write mesh equations for the meshes identified in step 2. Express element voltages in terms of mesh currents or the voltage produced by independent voltage sources.
4. Write expressions relating the mesh currents to the currents produced by independent current sources.
5. Substitute the expressions from step 4 into the mesh equations from step 3 and place the result in standard form.
6. Solve the equations from step 5 for the mesh currents of interest. Cramer's rule is often useful when circuit parameters are left in symbolic form. Computer tools are useful when there are four or more equations and numerical values are given.

3–3 LINEARITY PROPERTIES

This book treats the analysis and design of **linear circuits**. A circuit is said to be linear if it can be adequately modeled using only linear elements and independent sources. The hallmark feature of a linear circuit is that outputs are linear functions of the inputs. Circuit **inputs** are the signals produced by external sources, and **outputs** are any other designated signals. Mathematically, a function is said to be linear if it possesses two properties—homogeneity and additivity. In linear circuits, **homogeneity** means that the output is proportional to the input. **Additivity** means that the output due to two or more inputs can be found by adding the outputs obtained when each input is applied separately. Mathematically, these properties are written as follows:

$$f(Kx) = Kf(x) \quad \text{(homogeneity)} \tag{3–18}$$

and

$$f(x_1 + x_2) = f(x_1) + f(x_2) \quad \text{(additivity)} \tag{3–19}$$

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where K is a scalar constant. In circuit analysis the homogeneity property is called **proportionality**, while the additivity property is called **superposition**.

THE PROPORTIONALITY PROPERTY

The **proportionality property** applies to linear circuits with one input. For linear resistive circuits, proportionality states that every input-output relationship can be written as

$$y = Kx \tag{3–20}$$

where x is the input current or voltage, y is an output current or voltage, and K is a constant. The block diagram in Figure 3–25 describes this linear input–output relationship. In a block diagram the lines headed by arrows indicate the direction of signal flow. The arrow directed into the block indicates the input, while the output is indicated by the arrow directed out of the block. The variable names written next to these lines identify the input and output signals. The scalar constant K written inside the block indicates that the input signal x is multiplied by K to produce the output signal as $y = Kx$.

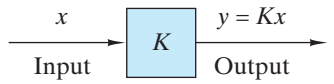


FIGURE 3–25 *Block diagram representation of the proportionality property.*

Caution: Proportionality only applies when the input and output are current or voltage. It does not apply to output power since power is equal to the product of current and voltage. In other words, output power is not linearly related to the input current or voltage.

We have already seen several examples of proportionality. For instance, using voltage division in Figure 3–26(a) produces

$$v_O = \left(\frac{R_2}{R_1 + R_2}\right) v_S$$

which means

$$x = v_S \qquad y = v_O$$

$$K = \frac{R_2}{R_1 + R_2}$$

Similarly, applying current division in Figure 3–26(b) yields

$$i_O = \left(\frac{G_2}{G_1 + G_2}\right) i_S$$

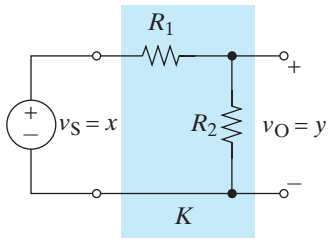
so that

$$x = i_S \qquad y = i_O$$

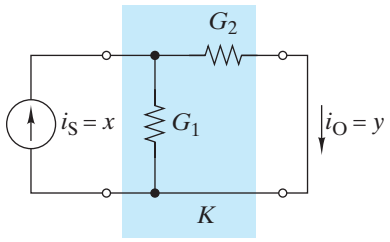
$$K = \frac{G_2}{G_1 + G_2}$$

In these two examples the proportionality constant K is dimensionless because the input and output have the same units. In other situations K could have the units of ohms or siemens when the input and output have different units.

The next example illustrates that the proportionality constant K can be positive, negative, or even zero.



(a)



(b)

FIGURE 3–26 *Examples of circuit exhibiting proportionality: (a) Voltage divider. (b) Current divider.*

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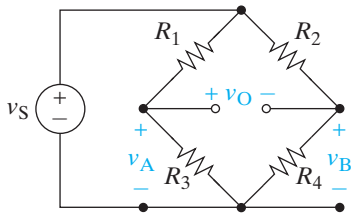

FIGURE 3–27

EXAMPLE 3–10

Given the bridge circuit of Figure 3–27,

(a) Find the proportionality constant K in the input-output relationship $v_O = Kv_S$.
(b) Find the sign of K when $R_2R_3 > R_1R_4$, $R_2R_3 = R_1R_4$, and $R_2R_3 < R_1R_4$.

SOLUTION:

(a) We observe that the circuit consists of two voltage dividers. Applying the voltage division rule to each side of the bridge circuit yields

$$v_A = \frac{R_3}{R_1 + R_3}v_S \quad \text{and} \quad v_B = \frac{R_4}{R_2 + R_4}v_S$$

The fundamental property of node voltages allows us to write

$$v_O = v_A - v_B$$

Substituting the equations for v_A and v_B into this KVL equation yields

$$\begin{aligned} v_O &= \left(\frac{R_3}{R_1 + R_3} - \frac{R_4}{R_2 + R_4}\right)v_S \\ &= \left(\frac{R_2R_3 - R_1R_4}{(R_1 + R_3)(R_2 + R_4)}\right)v_S \\ &= \qquad (K) \qquad v_S \end{aligned}$$

(b) The proportionality constant K can be positive, negative, or zero. Specifically,

$$\text{If } R_2R_3 > R_1R_4 \text{ then } K > 0$$
$$\text{If } R_2R_3 = R_1R_4 \text{ then } K = 0$$
$$\text{If } R_2R_3 < R_1R_4 \text{ then } K < 0$$

When the products of the resistances in opposite legs of the bridge are equal, then $K = 0$ and the bridge is said to be balanced. ■

UNIT OUTPUT METHOD

The **unit output method** is an analysis technique based on the proportionality property of linear circuits. The method involves finding the input-output proportionality constant K by assuming an output of one unit and determining the input required to produce that unit output. This technique is most useful when applied to ladder circuits, and it involves the following steps:

1. A unit output is assumed; that is, $v_O = 1$ V or $i_O = 1$ A.
2. The input required to produce the unit output is then found by successive application of KCL, KVL, and Ohm's law.

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3. Because the circuit is linear, the proportionality constant relating input and output is

$$K = \frac{\text{Output}}{\text{Input}} = \frac{1}{\text{Input for unit output}}$$

Given the proportionality constant K, we can find the output for any input using Eq. (3–20).

In a way, the unit output method solves the circuit response problem backwards—that is, from output to input—as illustrated by the next example.

EXAMPLE 3–11

Use the unit output method to find v_O in the circuit shown in Figure 3–28(a).

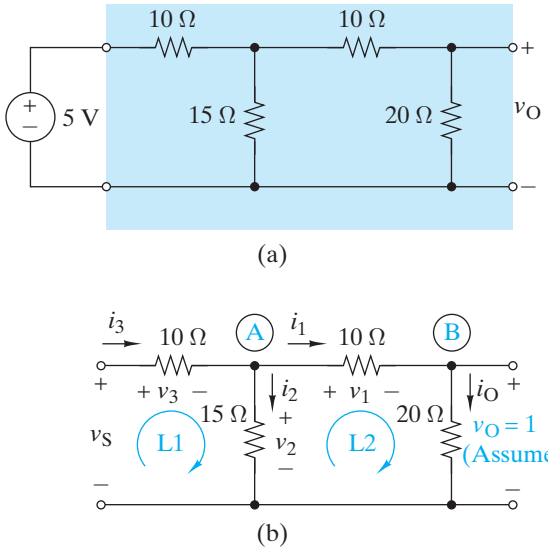

FIGURE 3–28

SOLUTION:

We start by assuming $v_O = 1$, as shown in Figure 3–28(b). Then, using Ohm's law, we find i_O.

$$i_O = \frac{v_O}{20} = 0.05 \text{ A}$$

Next, using KCL at node B, we find i_1.

$$i_1 = i_O = 0.05 \text{ A}$$

Again, using Ohm's law, we find v_1.

$$v_1 = 10i_1 = 0.5 \text{ V}$$

Then, writing a KVL equation around loop L2, we find v_2 as

$$v_2 = v_1 + v_O = 0.5 + 1.0 = 1.5 \text{ V}$$

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Using Ohm's law once more produces

$$i_2 = \frac{v_2}{15} = \frac{1.5}{15} = 0.1 \text{ A}$$

Next, writing a KCL equation at node A yields

$$i_3 = i_1 + i_2 = 0.05 + 0.1 = 0.15 \text{ A}$$

Using Ohm's law one last time,

$$v_3 = 10i_3 = 1.5 \text{ V}$$

We can now find the source voltage v_S by applying KVL around loop L1:

$$v_S\big|_{\text{for } v_O = 1\text{V}} = v_3 + v_2 = 1.5 + 1.5 = 3 \text{ V}$$

A 3-V source voltage is required to produce a 1-V output. From this result, we calculate the proportionality constant K to be

$$K = \frac{v_O}{v_S} = \frac{1}{3}$$

Once K is known, the output for the specified 5-V input is $v_O = (⅓)5 = 1.667$ V. ■

Exercise 3–11

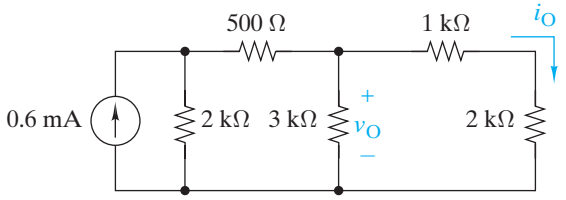
Find v_O in the circuit of Figure 3–28(a) when v_S is –5 V, 10 mV, and 3 kV.

Answers: $v_O = -1.667$ V; 3.333 mV; 1 kV

Exercise 3–12

Use the unit output method to find $K = i_O/i_{IN}$ for the circuit in Figure 3–29. Then use the proportionality constant K to find i_O for the input current shown in the figure.

FIGURE 3–29



Answers: $K = ¼$; $i_O = 0.15$ mA

Exercise 3–13

Use the unit output method to find $K = v_O/i_{IN}$ for the circuit in Figure 3–29. Then use K to find v_O for the input current shown in the figure.

Answers: $K = 750\ \Omega$; $v_O = 450$ mV

Note: In this exercise K has the dimensions of ohms because the input is a current and the output a voltage.

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ADDITIVITY PROPERTY

The **additivity property** states that any output current or voltage of a linear resistive circuit with multiple inputs can be expressed as a linear combination of the several inputs:

$$y = K_1x_1 + K_2x_2 + K_3x_3 + \ldots \tag{3–21}$$

where x_1, x_2, x_3, . . . are current or voltage inputs, and K_1, K_2, K_3 . . . are constants that depend on the circuit parameters. Figure 3–30 shows how we represent this relationship in block diagram form. Again the arrows indicate the direction of signal flow and the K's within the blocks are scalar multipliers. The circle in Figure 3–30 is a new block diagram element called a summing point that implements the operation $y = \sum K_i x_i$. Although the block diagram in Figure 3–30 is nothing more than a pictorial representation of Eq. (3–21), the diagram often helps us gain a clearer picture of how signals interact in different parts of a circuit.

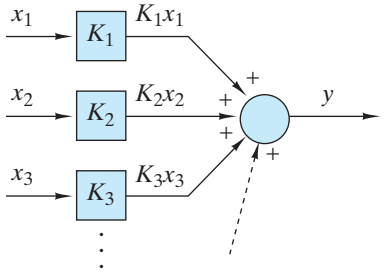

FIGURE 3–30 *Block diagram representation of the additivity property.*

To illustrate this property, we analyze the two-input circuit in Figure 3–31 using node-voltage analysis. Applying KCL at node A, we obtain

$$\frac{v_A - v_S}{R_1} - i_S + \frac{v_A}{R_2} = 0$$

Moving the inputs to the right side of this equation yields

$$\left[\frac{1}{R_1} + \frac{1}{R_2}\right]v_A = \frac{v_S}{R_1} + i_S$$

Since $v_O = v_A$, we obtain the input-output relationship in the form

$$v_O = \left[\frac{R_2}{R + R_2}\right]v_S + \left[\frac{R_1R_2}{R_1 + R_2}\right]i_S$$

$$y = [K_1]x_1 + [K_2]x_2 \tag{3–22}$$

This result shows that the output is a linear combination of the two inputs. Note that K_1 is dimensionless since its input and output are voltages, and that K_2 has the units of ohms since its input is a current and its output is a voltage.

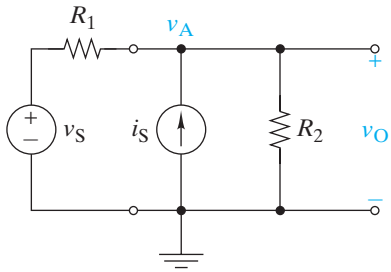

FIGURE 3–31 *Circuit used to demonstrate superposition.*

SUPERPOSITION PRINCIPLE

Since the output in Eq. (3–21) is a linear combination, the contribution of each input source is independent of all other inputs. This means that the output can be found by finding the contribution from each source acting alone and then adding the individual responses to obtain the total response. This suggests that the output of a multiple-input linear circuit can be found by the following steps:

STEP 1 "Turn off" all independent sources except one and find the output of the circuit due to that source acting alone.

STEP 2 Repeat the process in step 1 until each independent source has been turned on and the output due to that source found.

STEP 3 The total output with all independent sources turned on is the algebraic sum of the outputs caused by each source acting alone.

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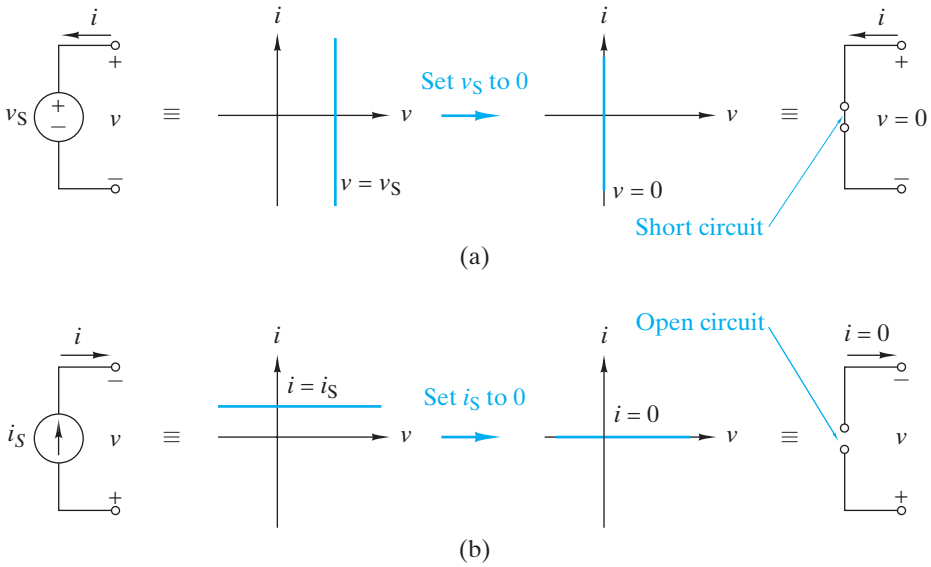

FIGURE 3–32 *Turning off an independent source: (a) Voltage source. (b) Current source.*

These steps describe a circuit analysis technique called the **superposition principle**. Before applying this method, we must discuss what happens when a voltage or current source is "turned off."

The *i–v* characteristics of voltage and current sources are shown in Figure 3–32. A voltage source is "turned off" by setting its voltage to zero ($v_S = 0$). This step translates the voltage source *i–v* characteristic to the *i*-axis, as shown in Figure 3–32(a). In Chapter 2 we found that a vertical line on the *i*-axis is the *i–v* characteristic of a short circuit. Similarly, "turning off" a current source ($i_S = 0$) in Figure 3–32(b) translates its *i–v* characteristic to the *v*-axis, which is the *i–v* characteristic of an open circuit. Therefore, when a voltage source is "turned off" we replace it by a short circuit, and when a current source is "turned off" we replace it by an open circuit.

The superposition principle is now applied to the circuit in Figure 3–31 to duplicate the response in Eq. (3–22), which was found by node analysis. Figure 3–33 shows the steps involved in applying superposition to the circuit in Figure 3–31. Figure 3–33(a) shows that the circuit has two input sources. We will first "turn off" i_S and replace it with an open circuit, as shown in Figure 3–33(b). The output of the circuit in Figure 3–33(b) is called v_{O1} and represents that part of the total output caused by the voltage source. Using voltage division in Figure 3–33(b) yields v_{O1} as

$$v_{O1} = \frac{R_2}{R_1 + R_2} v_S$$

Next we "turn off" the voltage source and "turn on" the current source, as shown in Figure 3–33(c). Using Ohm's law, we get $v_{O2} = i_{O2}R_2$. We use current division to express i_{O2} in terms of i_S to obtain v_{O2}:

$$v_{O2} = i_{O2}R_2 = \left[\frac{R_1}{R_1 + R_2} i_S\right] R_2 = \frac{R_1 R_2}{R_1 + R_2} i_S$$

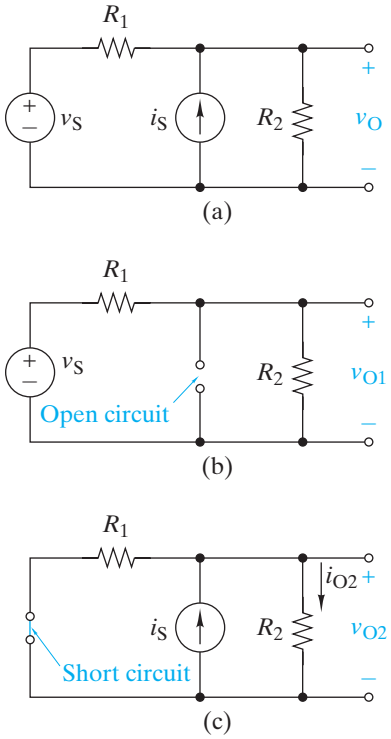

FIGURE 3–33 *Circuit analysis using superposition: (a) Current source off. (b) Voltage source off.*

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Applying the superposition principle, we find the response with both sources "turned on" by adding the two responses v_{O1} and v_{O2}.

$$v_O = v_{O1} + v_{O2}$$
$$= \left[\frac{R_2}{R_1 + R_2}\right]v_S + \left[\frac{R_1R_2}{R_1 + R_2}\right]i_S$$

This superposition result is the same as the circuit reduction result given in Eq. (3–22).

EXAMPLE 3–12

Figure 3–34(a) shows a resistance circuit used to implement a signal-summing function. Use superposition to show that the output v_O is a weighted sum of the inputs v_{S1}, v_{S2}, and v_{S3}.

SOLUTION:

To determine v_O using superposition, we first turn off sources 1 and 2 ($v_{S1} = 0$ and $v_{S2} = 0$) to obtain the circuit in Figure 3–34(b). This circuit is a voltage divider in which the output leg consists of two equal resistors in parallel. The equivalent resistance of the output leg is $R/2$, so the voltage division rule yields

$$v_{O3} = \frac{R/2}{R + R/2}v_{S3} = \frac{v_{S3}}{3}$$

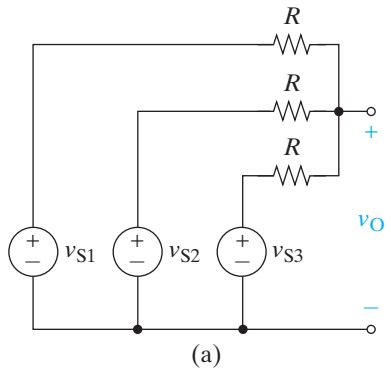
Because of the symmetry of the circuit, it can be seen that the same technique applies to all three inputs; therefore

$$v_{O2} = \frac{v_{S2}}{3} \text{ and } v_{O1} = \frac{v_{S1}}{3}$$

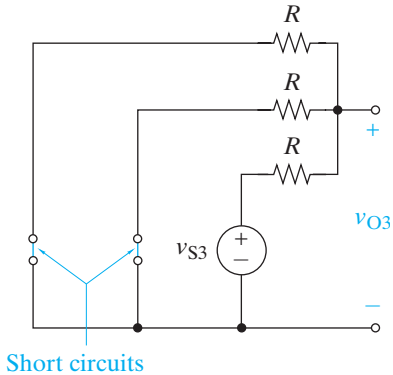
Applying the superposition principle, the output with all sources "turned on" is

$$v_O = v_{O1} + v_{O2} + v_{O3}$$
$$= \frac{1}{3}[v_{S1} + v_{S2} + v_{S3}]$$

That is, the output is proportional to the sum of the three input signals with $K_1 = K_2 = K_3 = ⅓$. ■



(a)



(b)

FIGURE 3–34

Exercise 3–14

The circuit of Figure 3–35 contains two R-$2R$ modules. Use superposition to find v_O.

Answer: $v_O = ½v_{S1} + ¼v_{S2}$

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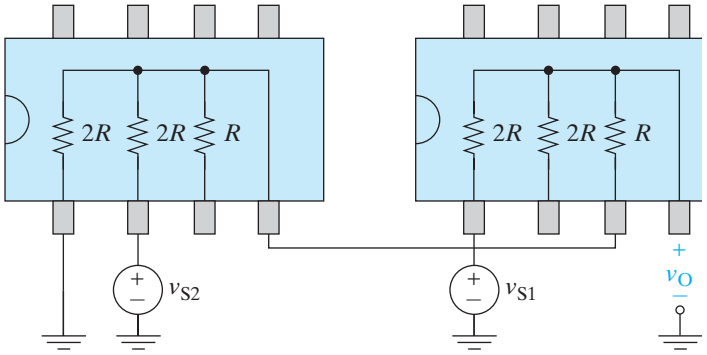
FIGURE 3–35



Exercise 3–15

Repeat Exercise 3–14 with the voltage source v_{S2} replaced by a current source i_{S2} with the current reference arrow directed toward ground.

Answer: $v_O = 3v_{S1}/5 - 4i_{S2}R/5$

The preceding examples and exercises illustrate the applications of the superposition principle. You should not conclude that superposition is used primarily to solve for the response of circuits with multiple independent sources. In fact, superposition is not a particularly attractive method of analysis since a circuit with N sources requires N different circuit analyses to obtain the final result. Unless the circuit is relatively simple, superposition does not reduce the analysis effort compared with, say, node-voltage analysis. Superposition is still an important property of linear circuits because it is often used as a conceptual tool to develop other circuit analysis techniques. For example, superposition is used in the next section to prove Thévenin's theorem.

3–4 THÉVENIN AND NORTON EQUIVALENT CIRCUITS

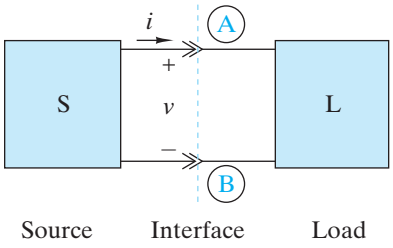


FIGURE 3–36 *A two-terminal interface.*

An *interface* is a connection between circuits. Circuit interfaces occur frequently in electrical and electronic systems, so special analysis methods are used to handle them. For the two-terminal interface shown in Figure 3–36, we normally think of one circuit as the source S and the other as the load L. We think of signals as being produced by the source circuit and delivered to the load circuit. The source-load interaction at an interface is one of the central problems of circuit analysis and design.

The Thévenin and Norton equivalent circuits shown in Figure 3–37 are valuable tools for dealing with circuit interfaces. The conditions under which these equivalent circuits exist can be stated as a theorem:

> ***If the source circuit in a two-terminal interface is linear, then the interface signals v and i do not change when the source circuit is replaced by its Thévenin or Norton equivalent circuit.***

The equivalence requires the source circuit to be linear but places no restriction on the linearity of the load circuit. Later in this section we

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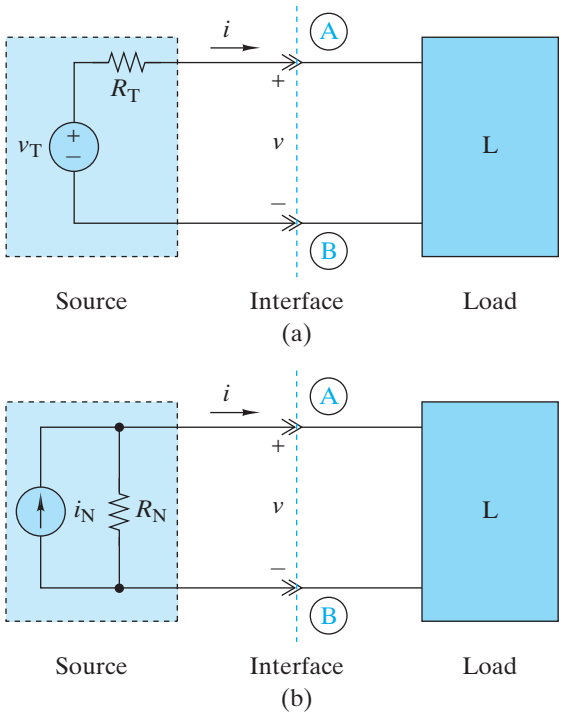

FIGURE 3–37 *Equivalent circuits for the source: (a) Thévenin equivalent. (b) Norton equivalent.*

consider cases in which the load is nonlinear. In subsequent chapters we will study circuits in which the loads are energy storage elements called capacitors and inductors.

The Thévenin equivalent circuit consists of a voltage source (v_T) in series with a resistance (R_T). The Norton equivalent circuit is a current source (i_N) in parallel with a resistance (R_N). Note that the Thévenin and Norton equivalent circuits are practical sources in the sense discussed in Chapter 2.

The two circuits have the same *i–v* characteristics, since replacing one by the other leaves the interface signals unchanged. To derive the equivalency conditions, we apply KVL and Ohm's law to the Thévenin equivalent in Figure 3–37(a) to obtain its *i–v* relationship at the terminals A and B:

$$v = v_T - iR_T \tag{3–23}$$

Next, applying KCL and Ohm's law to the Norton equivalent in Figure 3–37(b) yields its *i–v* relationship at terminals A–B:

$$i = i_N - \frac{v}{R_N} \tag{3–24}$$

Solving Eq. (3–24) for v yields

$$v = i_N R_N - iR_N \tag{3–25}$$

The Thévenin and Norton circuits have identical *i–v* relationships. Comparing Eqs. (3–23) and (3–25), we conclude that

$$R_N = R_T$$
$$i_N R_N = v_T \tag{3–26}$$

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In essence, the Thévenin and Norton equivalent circuits are related by the source transformation studied in Chapter 2. We do not need to find both equivalent circuits. Once one of them is found, the other can be determined by a source transformation. The Thévenin and Norton circuits involve four parameters (v_T, R_T, i_N, R_N), and Eq. (3–26) provides two relations between the four parameters. Therefore, only two parameters are needed to specify either equivalent circuit.

In circuit analysis problems it is convenient to use the short-circuit current and open-circuit voltage to specify Thévenin and Norton circuits. The circuits in Figure 3–38(a) show that when the load is an open circuit the interface voltage equals the Thévenin voltage; that is, $v_{OC} = v_T$, since there is no voltage across R_T when $i = 0$. Similarly, the circuits in Figure 3–38(b) show that when the load is a short circuit the interface current equals the Norton current; that is, $i_{SC} = i_N$, since all the source current i_N is diverted through the short-circuit load.

In summary, the parameters of the Thévenin and Norton equivalent circuits at a given interface can be found by determining the open-circuit voltage and the short-circuit current.

$$\begin{aligned} v_T &= v_{OC} \\ i_N &= i_{SC} \\ R_N &= R_T = v_{OC}/i_{SC} \end{aligned} \tag{3–27}$$

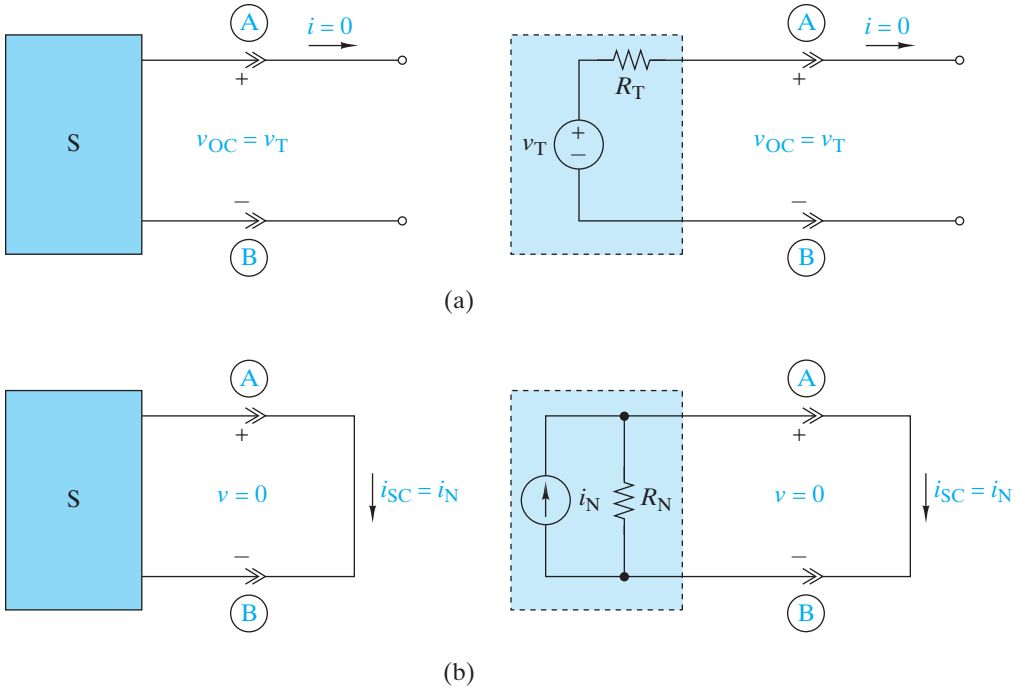

FIGURE 3–38 *Loads used to find Thévenin and Norton equivalent circuits: (a) Open circuit yields the Thévenin voltage. (b) Short circuit yields the Norton current.*

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APPLICATIONS OF THÉVENIN AND NORTON EQUIVALENT CIRCUITS

Replacing a complex circuit by its Thévenin or Norton equivalent can greatly simplify the analysis and design of interface circuits. For example, suppose we need to select a load resistance in Figure 3–39(a) so the source circuit to the left of the interface A–B delivers 4 volts to the load. This task is easily handled once we have the Thévenin or Norton equivalent for the source circuit.

To obtain the Thévenin and Norton equivalents, we need v_{OC} and i_{SC}. The open-circuit voltage v_{OC} is found by disconnecting the load at the terminals A and B, as shown in Figure 3–39(b). The voltage across the 15-Ω resistor is zero because the open circuit causes the current through the resistor to be zero. The open-circuit voltage at the interface is the same as the voltage across the 10-Ω resistor. Using voltage division, this voltage is

$$v_T = v_{OC} = \frac{10}{10 + 5} \times 15 = 10 \text{ V}$$

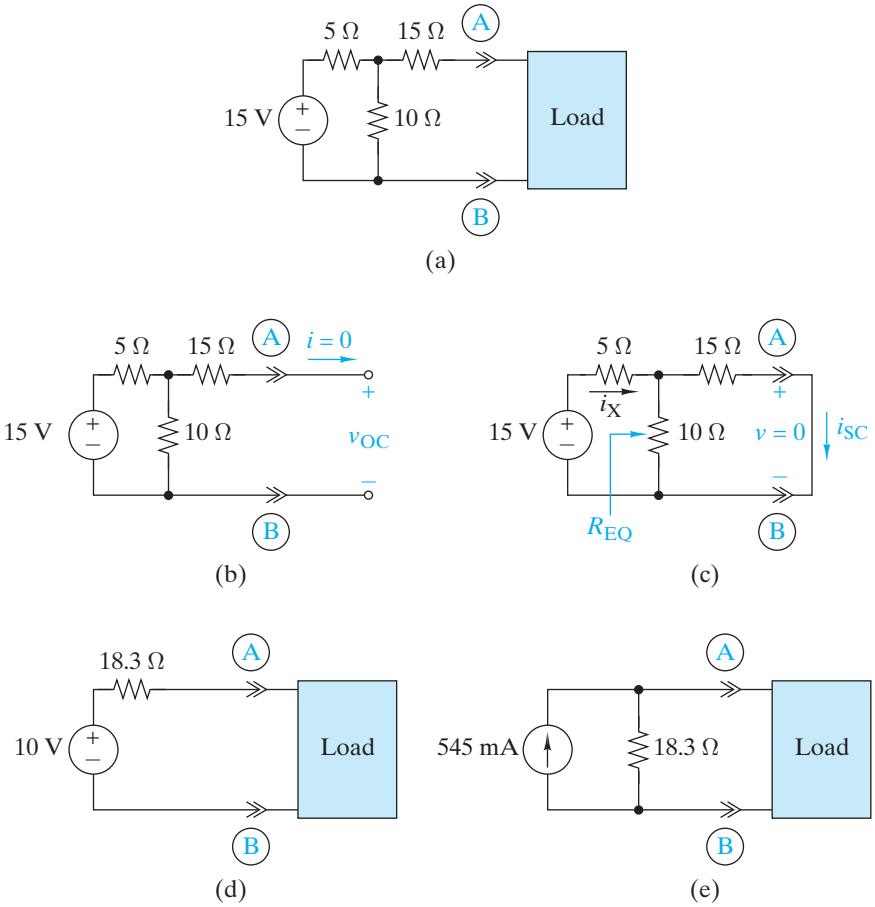

FIGURE 3–39 *Example of finding the Thévenin and Norton equivalent circuits: (a) The given circuit. (b) Open circuit yields the Thévenin voltage. (c) Short circuit yields the Norton current. (d) Thévenin equivalent circuit. (e) Norton equivalent circuit.*

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Next we find the short-circuit current i_{SC} using the circuit in Figure 3–39(c). The total current i_X delivered by the 15-V voltage source is

$$i_X = 15/R_{EQ}$$

where R_{EQ} is the equivalent resistance seen by the voltage source with a short circuit at the interface.

$$R_{EQ} = 5 + \frac{1}{\frac{1}{10} + \frac{1}{15}} = 11\ \Omega$$

We find $i_X = 15/11 = 1.36$ A. Given i_X, we now use current division to obtain the short-circuit current:

$$i_N = i_{SC} = \frac{10}{10 + 15} \times i_X = 0.545\ \text{A}$$

Finally, we compute the Thévenin and Norton resistances:

$$R_T = R_N = \frac{v_{OC}}{i_{SC}} = 18.3\ \Omega$$

The resulting Thévenin and Norton equivalent circuits are shown in Figures 3–39(d) and 3–39(e).

It now is an easy matter to select a load R_L so 4 V is supplied to the load. Using the Thévenin equivalent circuit, the problem reduces to a voltage divider:

$$\frac{R_L}{R_L + R_T} \times v_T = \frac{R_L}{R_L + 18.3} \times 10 = 4\ \text{V}$$

Solving for R_L yields $R_L = 12.2\ \Omega$.

The Thévenin or Norton equivalent can always be found from the open-circuit voltage and short-circuit current at the interface. The following examples illustrate other methods of determining these equivalent circuits.

EXAMPLE 3–13

(a) Find the Thévenin equivalent circuit of the source circuit to the left of the interface in Figure 3–40(a).
(b) Use the Thévenin equivalent to find the power delivered to two different loads. The first load is a 10-kΩ resistor and the second is a 5-V voltage source whose positive terminal is connected to the upper interface terminal.

SOLUTION:

(a) To find the Thévenin equivalent, we use the sequence of circuit reductions shown in Figure 3–40. In Figure 3–40(a) the 15-V voltage source in series with the 3-kΩ to the left of terminals A and B is replaced by a 3-kΩ resistor in parallel with an equivalent current source with i_S = 15/3000 = 5 mA. In Figure 3–40(b), looking to the left at terminals C and D, we see two resistors in parallel whose equivalent resistance is (3 kΩ)||(6 kΩ) = 2 kΩ. We also see two current sources in parallel whose equivalent is i_S = 5 mA – 2 mA = 3 mA. This equivalent current

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source is shown in Figure 3–40(c) to the left of terminals C and D. Figure 3–40(d) shows this current source converted to an equivalent voltage source v_S = 3 mA × 2 kΩ = 6 V in series with 2 kΩ. In Figure 3–40(d) the three resistors are connected in series and can be replaced by an equivalent resistance R_{EQ} = 2 kΩ + 3 kΩ + 4 kΩ = 9 kΩ. This step produces the Thévenin equivalent shown in Figure 3–40(e).

Note: The steps leading from Figure 3–40(a) to 3–40(e) involve circuit reduction techniques studied in Chapter 2, so we know that this approach only works on ladder circuits like the one in Figure 3–40(a).

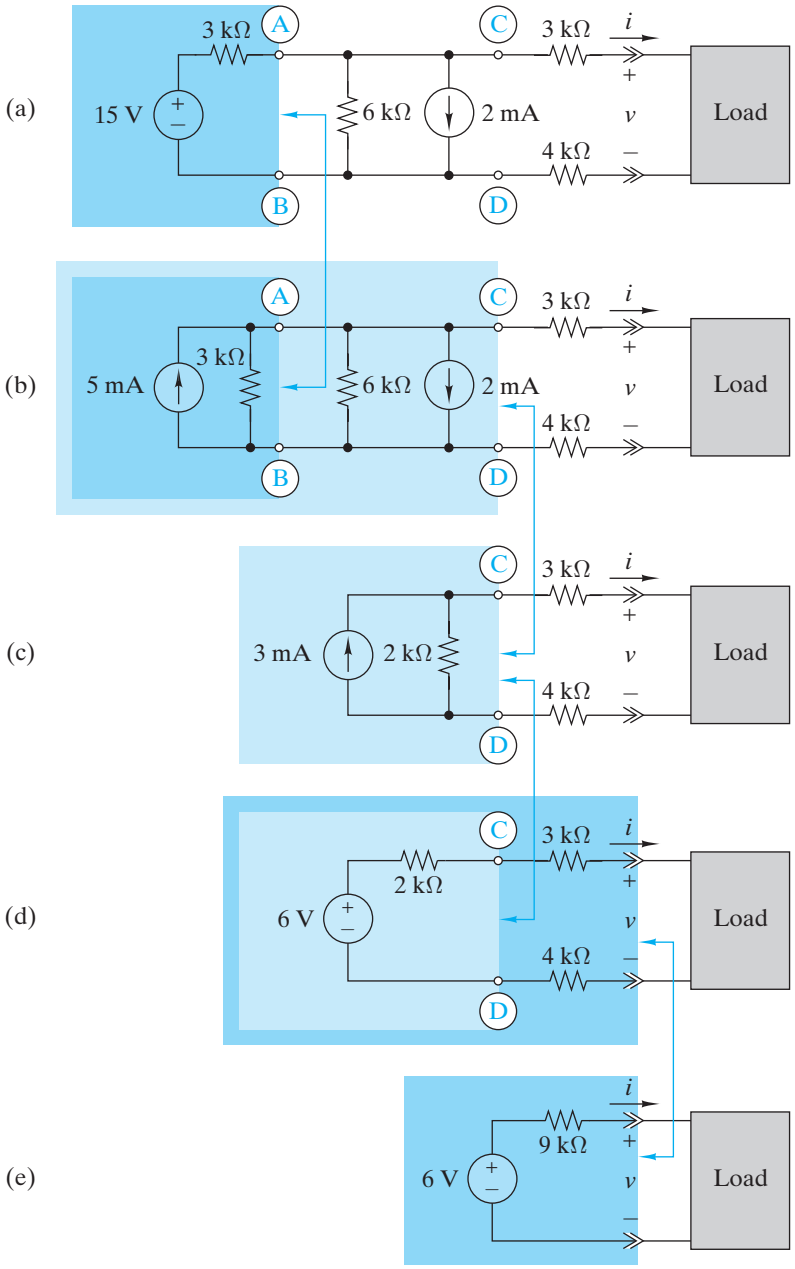

FIGURE 3–40

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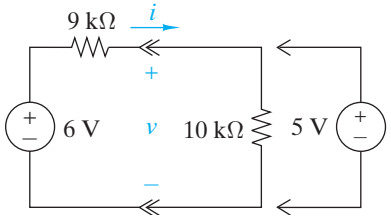


FIGURE 3–41

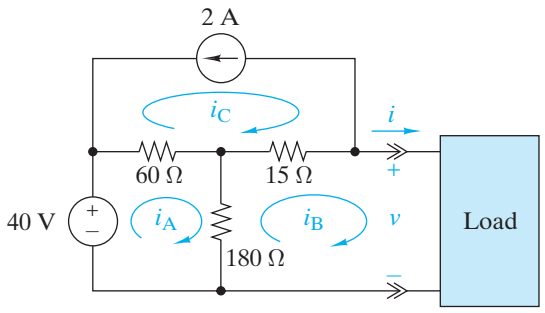
(b) Figure 3–41 shows the Thévenin equivalent found in (a) and the two loads. When the load is a 10-kΩ resistor, the interface current is $i = (6)/(9000 + 10{,}000) = 0.3158$ mA, and the power delivered to the load is $i^2R_L = 0.9973$ mW. When the load is a 5-V source, the interface voltage and current are $v = 5$ V and $i = (6 - 5)/9000 = 0.1111$ mA, and the power to the load is $vi = 0.5555$ mW. Since $p > 0$ in the latter case, we see that the voltage source load is absorbing rather than delivering power. A practical example of this situation is a battery charger.

Caution: The Thévenin equivalent allows us to calculate the power delivered to a load, but it does not tell us what power is dissipated in the source circuit. For instance, if the load in Figure 3–40(e) is an open circuit, then no power is dissipated in the Thévenin equivalent since $i = 0$. This does not mean that the power dissipated in the source circuit is zero, as we can easily see by looking back at Figure 3–40(a). The Thévenin equivalent circuit has the same i–v characteristic at the interface, but it does not duplicate the internal characteristics of the source circuit. ■

EXAMPLE 3–14

(a) Find the Norton equivalent of the source circuit to the left of the interface in Figure 3–42.
(b) Find the interface current i when the power delivered to the load is 5 W.

FIGURE 3–42



SOLUTION:

(a) The circuit reduction method will not work here since the source circuit is not a ladder. In this example we write mesh-current equations and solve directly for the source circuit i–v relationship. We only need to write equations for meshes A and B since the 2-A current source determines the mesh C current. The voltage sums around these meshes are

$$\text{Mesh A:}\quad -40 + 60(i_A - i_C) + 180(i_A - i_B) = 0$$

$$\text{Mesh B:}\quad -180(i_A - i_B) + 15(i_B - i_C) + v = 0$$

But since $i_B = i$ and the current source forces the condition $i_C = -2$, these equations have the form

$$240i_A - 180i = -80$$

$$-180i_A + 195i = -30 - v$$

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Solving for i in terms of v yields

$$i = \frac{\begin{vmatrix} 240 & -80 \\ -180 & -30 - v \end{vmatrix}}{\begin{vmatrix} 240 & -180 \\ -180 & 195 \end{vmatrix}} = \frac{-21600 - 240v}{14400}$$

$$= -1.5 - \frac{v}{60}$$

At the interface the i–v relationship of the source circuit is $i = -1.5 - v/60$. Equation (3–24) gives the i–v relationship of the Norton circuit as $i = i_N - v/R_N$. By direct comparison, we conclude that $i_N = -1.5$ A and $R_N = 60\ \Omega$. This equivalent circuit is shown in Figure 3–43.

(b) When 5 W is delivered to the load, we have $vi = 5$ or $v = 5/i$. Substituting $v = 5/i$ into the source i–v relationship $i = -1.5 - v/60$ yields a quadratic equation

$$12i^2 + 18i + 1 = 0$$

whose roots are $i = -0.05778$ A and -1.442 A. Thus, there are two values of interface current that deliver 5 W to the load. ■

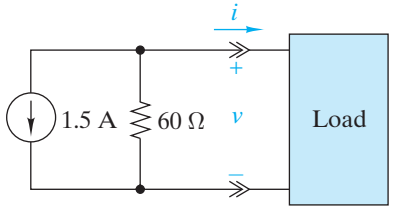

FIGURE 3–43

DERIVATION OF THÉVENIN'S THEOREM

The derivation of Thévenin's theorem is based on the superposition principle. We begin with the circuit in Figure 3–44(a), where the source circuit S is linear. Our approach is to use superposition to show that the source circuit and the Thévenin circuit have the same i–v relationship at the interface. To find the source circuit i–v relationship, we first disconnect the load and apply a current source i_{TEST}, as shown in Figure 3–44(b). Using superposition to find v_{TEST}, we first turn i_{TEST} off and leave all the sources inside S on, as shown in Figure 3–44(c). Turning a current source off leaves an open circuit, so

$$v_{TEST1} = v_{OC}$$

Next we turn i_{TEST} back on and turn off all of the sources inside S. Since the source circuit S is linear, it reduces to the equivalent resistance shown in Figure 3–44(d) when all internal sources are turned off. Using Ohm's law, we write

$$v_{TEST2} = (R_{EQ})(-i_{TEST})$$

The minus sign in this equation results from the reference directions originally assigned to i_{TEST} and v_{TEST} in Figure 3–44(b). Using the superposition principle, we find the i–v relationship of the source circuit at the interface to be

$$v_{TEST} = v_{TEST1} + v_{TEST2}$$
$$= v_{OC} - R_{EQ} i_{TEST}$$

This equation has the same form as the i–v relationship of the Thévenin equivalent circuit in Eq. (3–23) when $v_{TEST} = v$, $i_{TEST} = i$, $v_{OC} = v_T$, and $R_T = R_{EQ}$.

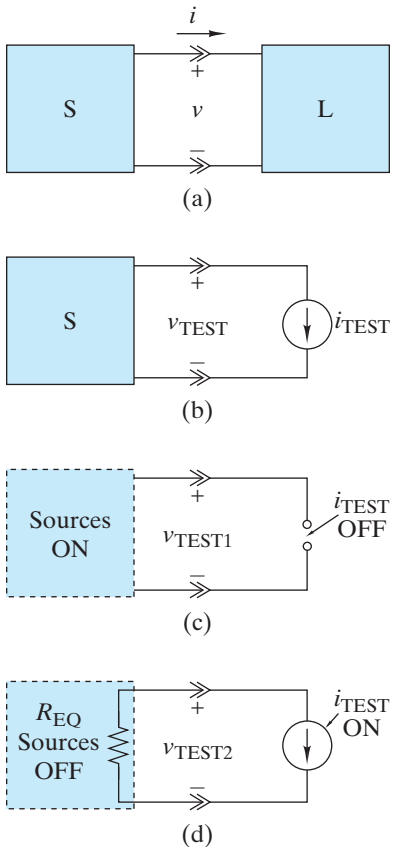

FIGURE 3–44 *Using superposition to prove Thévenin's theorem.*

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The derivation points out another method of finding the Thévenin resistance. As indicated in Figure 3–44(d), when all the sources are turned off, the i–v relationship of the source circuit reduces to $v = -iR_{EQ}$. Similarly, the i–v relationship of a Thévenin equivalent circuit reduces to $v = -iR_T$ when $v_T = 0$. We conclude that

$$R_T = R_{EQ} \tag{3–28}$$

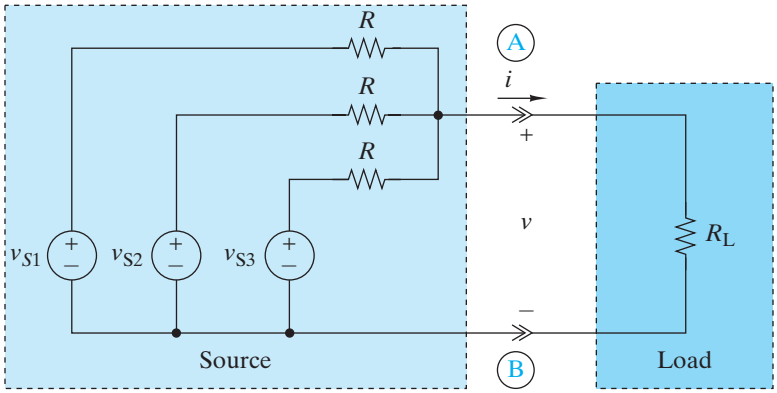
We can find the value of R_T by determining the resistance seen looking back into the source circuit with all sources turned off. For this reason the Thévenin resistance R_T is sometimes called the **lookback resistance**.

The next example shows how lookback resistance contributes to finding a Thévenin equivalent circuit.

EXAMPLE 3–15

(a) Find the Thévenin equivalent of the source circuit to the left of the interface in Figure 3–45.
(b) Use the Thévenin equivalent to find the voltage delivered to the load.

FIGURE 3–45



SOLUTION:

(a) The source circuit in Figure 3–45 is treated in Example 3–12 by using superposition to calculate the open-circuit voltage between terminals A and B. Using the results from Example 3–12, we have

$$v_T = v_{OC} = \frac{1}{3}(v_{S1} + v_{S2} + v_{S3})$$

Turning all sources off in Figure 3–45 leads to the resistance circuit in Figure 3–46. Looking back into the source circuit in Figure 3–46, we see three equal resistances connected in parallel whose equivalent resistance is $R/3$. Hence, the Thévenin resistance is

$$R_T = R_{EQ} = \frac{R}{3}$$

(b) Given the Thévenin circuit parameters v_T and R_T, we apply voltage division in Figure 3–45 to find the interface voltage.

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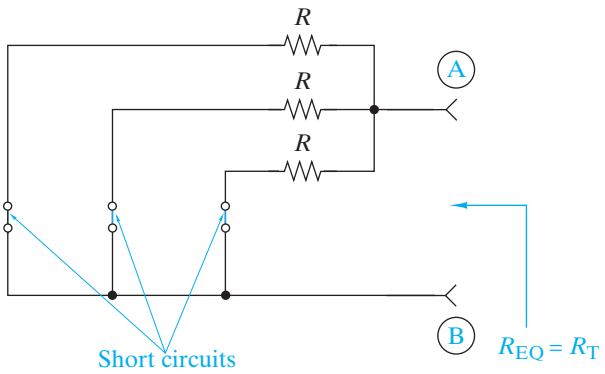

FIGURE 3–46

$$v = \frac{R_L}{R_L + R_T} v_T = \left(\frac{R_L}{R_L + R/3}\right)\left(\frac{v_{S1} + v_{S2} + v_{S3}}{3}\right)$$

$$= \left(\frac{R_L}{3R_L + R}\right)(v_{S1} + v_{S2} + v_{S3})$$

The interface voltage is proportional to the sum of the three source voltages. The proportionality constant $K = R_L/(3R_L + R)$ depends on both the source and the load since these two circuits are connected at the interface. ■

Exercise 3–16

(a) Find the Thévenin and Norton equivalent circuits seen by the load in Figure 3–47.
(b) Find the voltage, current, and power delivered to a 50-Ω load resistor.

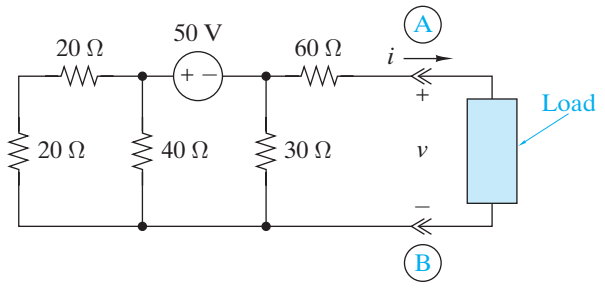

FIGURE 3–47

Answers:

(a) $v_T = -30$ V; $i_N = -417$ mA; $R_N = R_T = 72$ Ω
(b) $v = -12.3$ V; $i = -246$ mA; $p = 3.03$ W

Exercise 3–17

Find the current and power delivered to an unknown load in Figure 3–47 when $v = +6$ V.

Answers: $i = -½$A; $p = -3$ W

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APPLICATION TO NONLINEAR LOADS

Thévenin and Norton equivalent circuits can be used to find the response of a two-terminal nonlinear element (NLE). The method of analysis is a straightforward application of device and interface *i–v* characteristics. An interface is defined at the terminals of the nonlinear element, and the linear part of the circuit is reduced to the Thévenin equivalent in Figure 3–48(a). The *i–v* relationship of the Thévenin equivalent can be written with interface current as the dependent variable:

$$i = \left(-\frac{1}{R_T}\right)v + \left(\frac{v_T}{R_T}\right) \tag{3–29}$$

This is the equation of a straight line in the *i–v* plane shown in Figure 3–48(b). The line intersects the *i*-axis ($v = 0$) at $i = v_T/R_T = i_{SC}$ and intersects

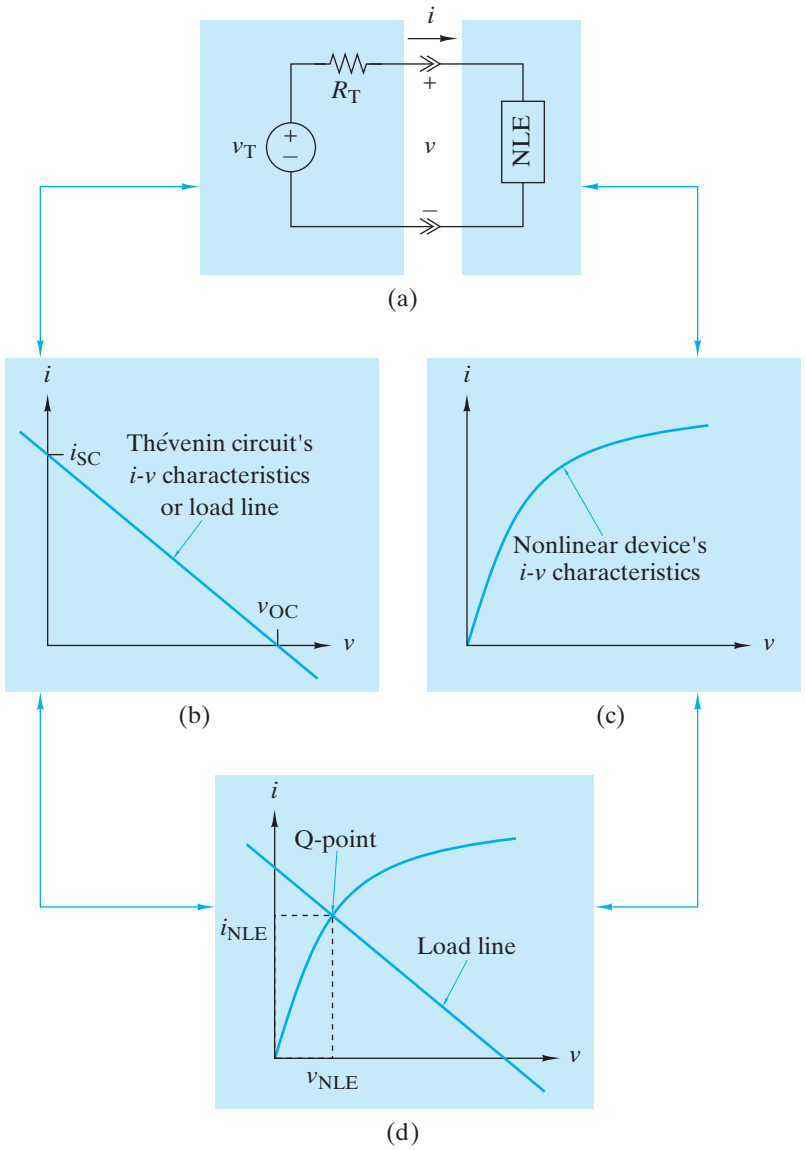

FIGURE 3–48 *Graphical analysis of a nonlinear circuit: (a) Given circuit. (b) Load line. (c) Nonlinear device i–v characteristics. (d) Q-point.*

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the v-axis ($i = 0$) at $v = v_T = v_{OC}$. This line could logically be called the source line since it is determined by the Thévenin parameters of the source circuit. Logic notwithstanding, electrical engineers call this the **load line** for reasons that have blurred with the passage of time.

The nonlinear element has the i–v characteristic shown in Figure 3–48(c). Mathematically, this nonlinear characteristic has the form

$$i = f(v) \tag{3–30}$$

To find the circuit response, we must solve Eqs. (3–29) and (3–30) simultaneously. Computer software tools like Mathcad can easily solve this problem when a numerical expression for the function $f(v)$ is known explicitly. However, in practice an approximate graphical solution is often adequate, particularly when $f(v)$ is only given in graphical form.

In Figure 3–48(d) we superimpose the load line on the i–v characteristic curve of the nonlinear element. The two curves intersect at the point $i = i_{NLE}$ and $v = v_{NLE}$, which yields the values of interface variables that satisfy both the source constraints in Eq. (3–29) and the nonlinear element constraints in Eq. (3–30). In the terminology of electronics, the point of intersection is called the operating point or **Q-point**, where Q stands for *quiescent.*

EXAMPLE 3–16

Find the voltage, current, and power delivered to the diode in Figure 3–49(a).

SOLUTION:

We first find the Thévenin equivalent of the circuit to the left of the terminals A and B. By voltage division, the open-circuit voltage is

$$v_T = v_{OC} = \frac{100}{100 + 100} \times 5 = 2.5 \text{ V}$$

When the voltage source is turned off, the lookback equivalent resistance seen between terminals A and B is

$$R_T = 10 + 100 \| 100 = 60\ \Omega$$

The source circuit load line is given by

$$i = -\frac{1}{60}v + \frac{1}{60} \times 2.5$$

This line intersects the i-axis ($v = 0$) at $i = i_{SC} = 2.5/60 = 41.7$ mA and intersects the v-axis ($i = 0$) at $v = v_{OC} = 2.5$ V. Figure 3–49(b) superimposes the source circuit load line on the diode's i–v curve. The intersection (Q-point) is at $i = i_D = 15$ mA and $v = v_D = 1.6$ V. This is the point (i_D, v_D) at which both the source and diode device constraints are satisfied. Finally, the power delivered to the diode is

$$p_D = i_D v_D = (15 \times 10^{-3})(1.6) = 24 \text{ mW}$$

Because of the nonlinear element, the proportionality and superposition properties do not apply to this circuit. For instance, if the source voltage in Figure 3–49 is decreased from 5 V to 2.5 V, the diode current and voltage do not decrease by one-half. Try it. ■

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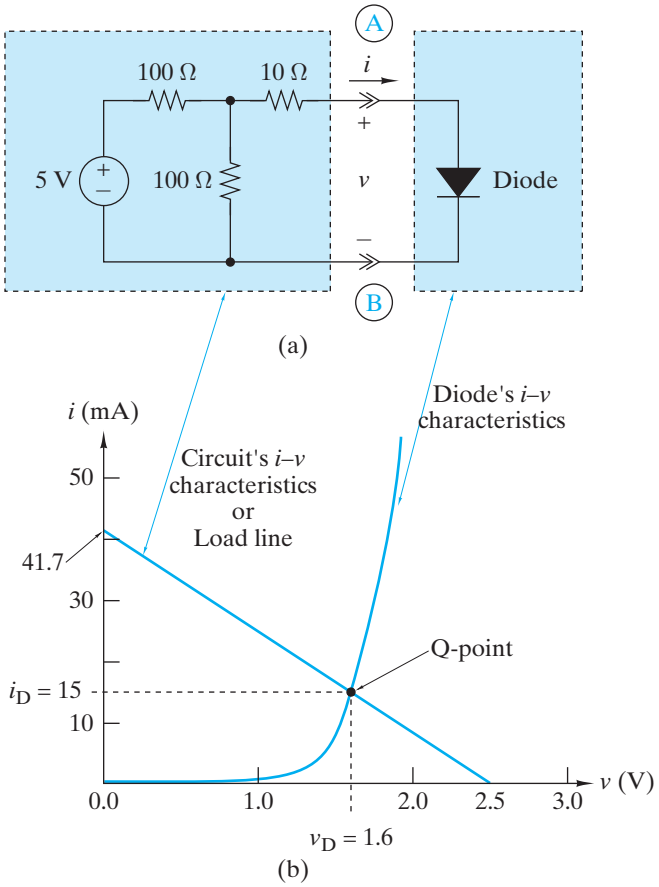
FIGURE 3–49



Exercise 3–18

Find the voltage, current, and power delivered to the diode in Figure 3–49(a) when the 10-Ω resistor is replaced by a short circuit.

Answer: $v_D = 1.7$ V; $i_D = 18$ mA; $p_D = 30.6$ mW

In summary, any two of the following parameters determine the Thévenin or Norton equivalent circuit at a specified interface:

- The open-circuit voltage at the interface
- The short-circuit current at the interface
- The source circuit lookback resistance

Alternatively, for ladder circuits the Thévenin or Norton equivalent circuit can be found by a sequence of circuit reductions (see Example 3–13). For general circuits they can always be found by directly solving for the *i–v* relationship of the source circuit using node-voltage or mesh-current equations that include the interface current and voltage as unknowns (see Example 3–14).

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EQA

3–5 MAXIMUM SIGNAL TRANSFER

An interface is a connection between two circuits at which the signal levels may be observed or specified. In this regard an important consideration is the maximum signal levels that can be transferred across a given interface. This section defines the maximum voltage, current, and power available at an interface between a *fixed source* and an *adjustable load.*

For simplicity we will treat the case in which both the source and load are linear resistance circuits. The source can be represented by a Thévenin equivalent and the load by an equivalent resistance R_L, as shown in Figure 3–50. For a fixed source, the parameters v_T and R_T are given and the interface signal levels are functions of the load resistance R_L.

By voltage division, the interface voltage is

$$v = \frac{R_L}{R_L + R_T} v_T \tag{3–31}$$

For a fixed source and a variable load, the voltage will be a maximum if R_L is made very large compared with R_T. Ideally, R_L should be made infinite (an open circuit), in which case

$$v_{MAX} = v_T = v_{OC} \tag{3–32}$$

Therefore, the maximum voltage available at the interface is the source open-circuit voltage v_{OC}.

The current delivered at the interface is

$$i = \frac{v_T}{R_L + R_T} \tag{3–33}$$

For a fixed source and a variable load, the current will be a maximum if R_L is made very small compared with R_T. Ideally, R_L should be zero (a short circuit), in which case

$$i_{MAX} = \frac{v_T}{R_T} = i_N = i_{SC} \tag{3–34}$$

Therefore, the maximum current available at the interface is the source short-circuit current i_{SC}.

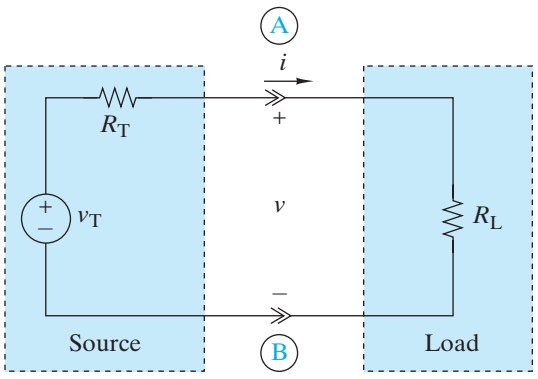

FIGURE 3–50 *Two-terminal interface for deriving the maximum signal transfer conditions.*

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EQA

The power delivered at the interface is equal to the product $v \times i$. Using Eqs. (3–31) and (3–33), the power is

$$p = v \times i = \frac{R_L v_T^2}{(R_L + R_T)^2} \tag{3–35}$$

For a given source, the parameters v_T and R_T are fixed and the delivered power is a function of a single variable R_L. The condition for maximum voltage ($R_L \to \infty$) and the condition for maximum current ($R_L = 0$) both produce zero power. The value of R_L that maximizes the power lies somewhere between these two extremes. To find this value, we differentiate Eq. (3–35) with respect to R_L and solve for the value of R_L for which $dp/dR_L = 0$.

$$\frac{dp}{dR_L} = \frac{[(R_L + R_T)^2 - 2R_L(R_L + R_T)]v_T^2}{(R_L + R_T)^4} = \frac{R_T - R_L}{(R_L + R_T)^3} v_T^2 = 0 \tag{3–36}$$

Clearly, the derivative is zero when $R_L = R_T$. Therefore, **maximum power transfer** occurs when the load resistance equals the Thévenin resistance of the source. When the condition $R_L = R_T$ exists, the source and load are said to be **matched**.

Substituting the condition $R_L = R_T$ back into Eq. (3–35) shows the maximum power to be

$$p_{MAX} = \frac{v_T^2}{4R_T} \tag{3–37}$$

Since $v_T = i_N R_T$, this result can also be written as

$$p_{MAX} = \frac{i_N^2 R_T}{4} \tag{3–38}$$

or

$$p_{MAX} = \frac{v_T i_N}{4} = \left[\frac{v_{OC}}{2}\right]\left[\frac{i_{SC}}{2}\right] \tag{3–39}$$

These equations are consequences of what is known as the **maximum power transfer theorem**:

> ***A source with a fixed Thévenin resistance R_T delivers maximum power to an adjustable load R_L when $R_L = R_T$.***[2]

To summarize, at an interface with a fixed source,

1. The maximum available voltage is the open-circuit voltage.
2. The maximum available current is the short-circuit current.
3. The maximum available power is the product of one-half the open-circuit voltage times one-half the short-circuit current.

---

2 An ideal voltage source has zero internal resistance, hence $R_T = 0$. Equation (3–37) points out that $R_T = 0$ implies an infinite p_{MAX}. Infinite power is a physical impossibility, which reminds us that all ideal circuit models have some physical limitations.

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EQA

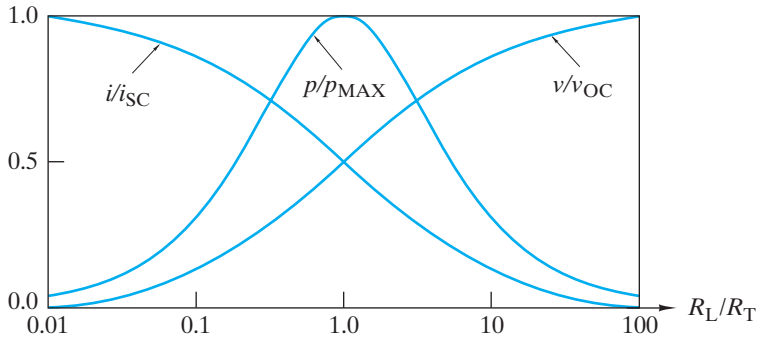

FIGURE 3–51 *Normalized plots of current, voltage, and power versus* R_L/R_T.

Figure 3–51 shows plots of the interface voltage, current, and power as functions of R_L/R_T. The plots of v/v_{OC}, i/i_{SC}, and p/p_{MAX} are normalized to the maximum available signal levels, so the ordinates in Figure 3–51 range from 0 to 1. The plot of the normalized power p/p_{MAX} in the neighborhood of the maximum is not a particularly strong function of R_L/R_T. Changing the ratio R_L/R_T by a factor of 2 in either direction from the maximum reduces p/p_{MAX} by less than 20%. The normalized voltage v/v_{OC} is within 20% of its maximum when $R_L/R_T = 4$. Similarly, the normalized current is within 20% of its maximum when $R_L/R_T = ¼$. In other words, for engineering purposes we can get close to the maximum signal levels with load resistances that only approximate the theoretical requirements.

EXAMPLE 3–17

A source circuit with $v_T = 2.5$ V and $R_T = 60\ \Omega$ drives a load with $R_L = 30\ \Omega$.

(a) Determine the maximum signal levels available from the source circuit.
(b) Determine the actual signal levels delivered to the load.

SOLUTION:

(a) The maximum available voltage and current are

$$v_{MAX} = v_{OC} = v_T = 2.5\text{ V}\ (R_L \to \infty)$$

$$i_{MAX} = i_{SC} = \frac{v_T}{R_T} = 41.7\text{ mA}\ (R_L = 0)$$

The maximum available power is found using Eq. (3–39).

$$p_{MAX} = \left[\frac{v_{OC}}{2}\right]\left[\frac{i_{SC}}{2}\right] = 26.0\text{ mW}\ (R_L = R_T = 60\ \Omega)$$

(b) The actual signal levels delivered to the 30-Ω load are

$$v_L = \frac{30}{30 + 60}2.5 = 0.833\text{ V}$$

$$i_L = \frac{2.5}{30 + 60} = 27.8\text{ mA}$$

$$p_L = v_L i_L = 23.1\text{ mW}$$

Although these levels are less than the maximum available values, the power delivered to the 30-Ω load is nearly 90% of the maximum. ■

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EQA

Exercise 3–19

A source circuit delivers 4 V when a 50-Ω resistor is connected across its output and 5 V when a 75-Ω resistor is connected. Find the maximum voltage, current, and power available from the source.

Answers: 10 V, 133 mA; 333 mW

Remember that the maximum signal levels just derived are for a fixed source resistance and an adjustable load resistance. This situation often occurs in communication systems where devices such as antennas, transmitters, and signal generators have fixed source resistances such as 50, 75, 300, or 600 ohms. In such cases the load resistance is selected to achieve the desired interface conditions, which often involves matching.

Matching source and load applies when the load resistance R_L in Figure 3–50 is adjustable and the Thévenin source resistance R_T is fixed. When R_L is fixed and R_T is adjustable, then Eqs. (3–31), (3–33), and (3–35) point out that the maximum voltage, current, and power are delivered when the Thévenin source resistance is zero. If the source circuit at an interface is adjustable, then ideally the Thévenin source resistance should be zero. In the next chapter we will see that OP AMP circuits approach this ideal.

3–6 INTERFACE CIRCUIT DESIGN

The maximum signal levels discussed in the previous section place bounds on what is achievable at an interface. However, those bounds are based on a fixed source and an adjustable load. In practice, there are circumstances in which the source or the load, or both, can be adjusted to produce prescribed interface signal levels. Sometimes it is necessary to insert a circuit between the source and the load to achieve the desired results. Figure 3–52 shows the general situations and some examples of resistive interface circuits. By its nature, the inserted circuit has two terminal pairs, or interfaces, at which voltage and current can be observed or specified. These terminal pairs are also called *ports*, and the interface circuit is referred to as a **two-port network**. The port connected to the source is called the input, and the port connected to the load is called the output. The purpose of this two-port network is to make certain that the source and load interact in a prescribed way.

BASIC CIRCUIT DESIGN CONCEPTS

Before we treat examples of different interface situations, you should recognize that we are now discussing a limited form of circuit design, as contrasted with circuit analysis. Although we use circuit analysis tools in design, there are important differences. A linear circuit analysis problem generally has a unique solution. A circuit design problem may have many solutions or even no solution. The maximum available signal levels found in the preceding section provide bounds that help us test for the existence of a solution. Generally there will be several ways to meet the interface constraints, and it then becomes necessary to evaluate the alternatives using other factors, such as cost, power consumption, or reliability.

At this point in our study, resistors are the only elements we can use to design interface circuits. In subsequent chapters we will introduce other

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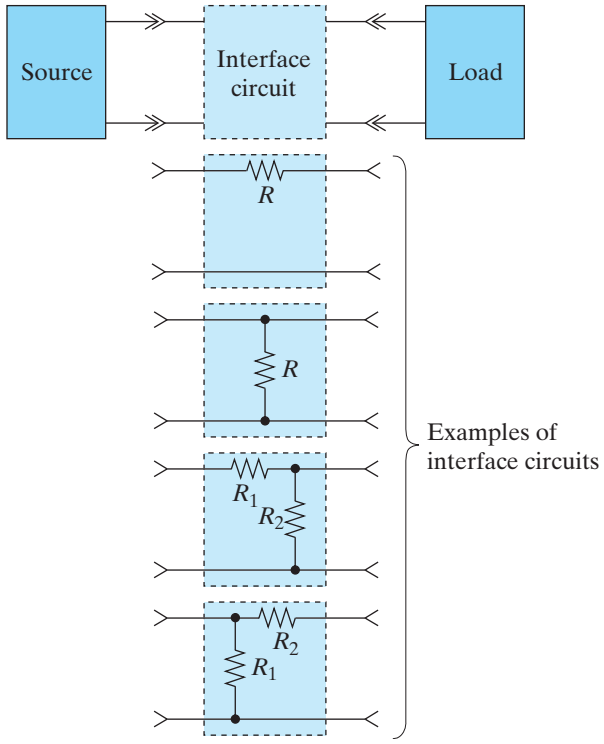

FIGURE 3–52 *A general interface circuit and some examples.*

devices, such as OP AMPs (Chapter 4) and capacitors and inductors (Chapter 6). In a design situation the engineer must choose the resistance values in a proposed circuit. This decision is influenced by a host of practical considerations, such as standard values and tolerances, power ratings, temperature sensitivity, cost, and fabrication methods. We will occasionally introduce some of these considerations into our design examples. Gaining a full understanding of these practical matters is not one of our objectives. Rather, our goal is simply to illustrate how different constraints can influence the design process.

DESIGN EXAMPLE 3–18

Select the load resistance in Figure 3–53 so that the interface signals are in the range defined by $v \geq 4$ V and $i \geq 30$ mA.

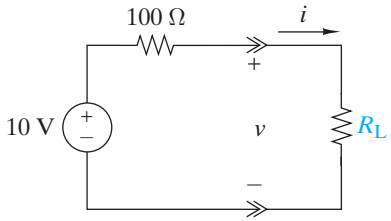

FIGURE 3–53

SOLUTION:

In this design problem, the source circuit is given and we are free to select the load. For a fixed source, the maximum signal levels available at the interface are

$$v_{MAX} = v_T = 10 \text{ V}$$

$$i_{MAX} = \frac{v_T}{R_T} = 100 \text{ mA}$$

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EQA

The bounds given as design requirements are below the maximum available signal levels, so we should be able to find a suitable resistor. Using voltage division, the interface voltage constraint requires

$$\frac{R_L}{100 + R_L} \times 10 \geq 4$$

or

$$10R_L \geq 4R_L + 400$$

This condition yields $R_L \geq 400/6 = 66.7\ \Omega$. The interface current constraint can be written as

$$\frac{10}{100 + R_L} \geq 0.03$$

or

$$10 \geq 3 + 0.03R_L$$

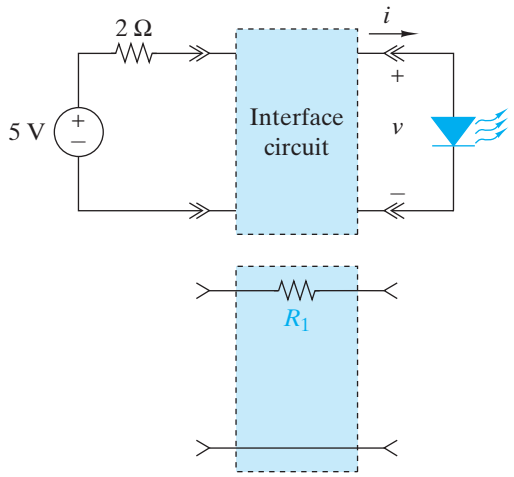
which requires $R_L \leq 7/0.03 = 233\ \Omega$. In theory, any value of R_L between 66.7 Ω and 233 Ω will work. However, to allow for parameter variations we select $R_L = 150\ \Omega$ because it lies at the arithmetic midpoint of the allowable range and is a standard value of resistance (see Table A–1, Appendix A). ■

DESIGN EXAMPLE 3–19

A light-emitting diode (LED) converts electric current into an optical signal. LEDs operate at low signal levels with voltages from about 1 V to perhaps 3 V and at currents between about 10 mA and 40 mA. Voltages or currents above these levels may damage or destroy the device.

Figure 3–54 shows an LED operating at $v = 1.5$ V and connected to a 5-V source by an interface circuit. Design the interface circuit so that the LED current is $i = 15\ \text{mA} \pm 10\%$ using one or more of the following standard resistors: 110 Ω, 160 Ω, 240 Ω, 360 Ω, and 510 Ω. These resistors all have a tolerance of ±5%, which you must account for in your design.

FIGURE 3–54



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EQA

SOLUTION:

If the source is directly connected to the LED, the delivered current would be

$$i = \frac{5 - 1.5}{2} = 1.75 \text{ A}$$

This much current would destroy (vaporize?) the device. The series resistor R_1 in the interface is needed to limit the current to the prescribed level. Applying KVL around the series loop yields

$$-5 + (2 + R_1)i + 1.5 = 0$$

Setting $i = 15$ mA and solving for R_1 yields

$$R_1 = \frac{3.5}{0.015} - 2 = 231 \ \Omega$$

The nearest standard value listed is 240 Ω ± 5%, which means that R_1 would fall in the range $228 \le R_1 \le 252$ Ω. At the end points of this range, the LED current is

$$i = \frac{3.5}{252 + 2} = 13.8 \text{ mA} \quad \text{and} \quad i = \frac{3.5}{228 + 2} = 15.2 \text{ mA}$$

Both of these values are within the 15 mA ± 10% tolerance on the LED current. ■

DE DESIGN AND EVALUATION EXAMPLE 3–20

Design two versions of the interface circuit in Figure 3–55 that deliver $v_2 = 5$ V to the 200-Ω load. Evaluate the two designs in terms of power loss in the interface circuit.

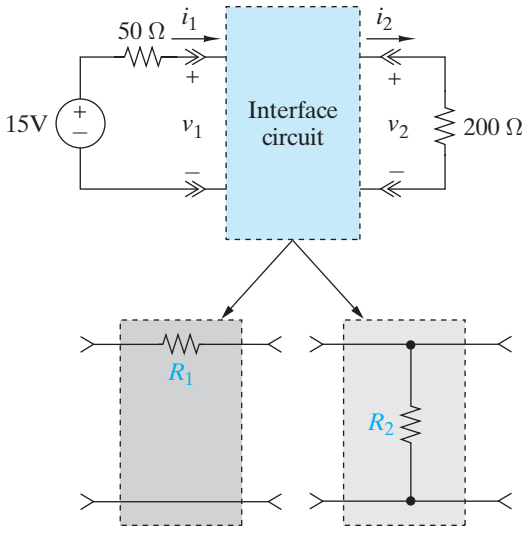

FIGURE 3–55

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EQA

SOLUTION:

If the 15-V source is directly connected to the load, the delivered voltage would be

$$v_2 = \left(\frac{200}{50 + 200}\right)15 = 12 \text{ V}$$

An interface circuit is required to reduce this voltage to the prescribed 5-V level.

The figure shows two possible interface circuits. In either case

$$i_2 = \frac{5}{200} = 0.025 \text{ A}$$

In the series case $i_1 = i_2 = 0.025$, and the same current flows through all elements in the loop. Applying KVL to the series loop

$$-15 + 0.025 \times (50 + R_1) + 5 = 0$$

and solving for R_1

$$R_1 = \frac{10}{0.025} - 50 = 350\ \Omega$$

In the parallel case $v_1 = v_2 = 5$ V. Applying KCL to the parallel resistor R_2

$$i_1 - \frac{v_2}{R_2} - i_2 = \frac{15 - 5}{50} - \frac{5}{R_2} - 0.025 = 0$$

and solving for R_2

$$R_2 = \frac{5}{0.2 - 0.025} = 28.57\ \Omega$$

We have two alternative designs, both of which deliver $v_2 = 5$ V to the 200-Ω load.

In practice, engineers use additional factors to evaluate alternatives that meet the same design goal. The power dissipation in the interface circuit is an important factor for two reasons. First, less interface dissipation means less power demand on the source. Second, less dissipation in the interface resistors means they can have lower power ratings, which are generally less expensive.

In the series case the power dissipated in R_1 is $i_2^2 R_1 = 0.219$ W. In the parallel case the power dissipated in R_2 is $v_2^2/R_2 = 0.875$ W. Clearly the power dissipation factor strongly favors the series design. ■

DESIGN EXAMPLE 3–21

Design the interface circuit in Figure 3–56 so that the 40-V source delivers $v_2 = 2$ V to the output load and the resistance seen at the input port is $R_{IN} = 300\ \Omega$. Note that this means that input resistance of the two port matches the source resistance.

SOLUTION:

This example places constraints at both the output port and the input port of the interface circuit. In most cases two independent constraints cannot be satisfied using only one resistor in the interface circuit. To see why, suppose

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EQA

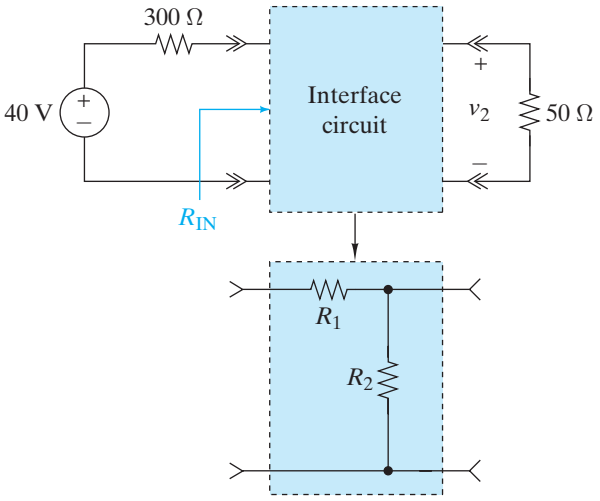

FIGURE 3–56

we use a single 650-Ω series resistor in the interface circuit. By voltage division, the output voltage would be

$$v_2 = \left(\frac{50}{300 + 650 + 50}\right)40 = 2 \text{ V}$$

as required. However, the input resistance would be $R_{IN} = 650 + 50 = 700\ \Omega$, which does not meet the input port requirement of 300 Ω.

To meet both requirements, we need a two-resistor L-circuit such as the one shown in the figure. To design this circuit, we first define $R_{EQ} = R_2 \| 50$. Using this notation, the input port constraint is $R_{IN} = R_1 + R_{EQ} = 300\ \Omega$ and the output port constraint becomes

$$v_2 = \left(\frac{R_{EQ}}{300 + R_1 + R_{EQ}}\right)40 = 2 \text{ V}$$

But $R_1 + R_{EQ} = 300$; hence, the output constraint reduces to $40R_{EQ} = 2 \times 600$, which means that $R_{EQ} = 30\ \Omega$. By definition

$$R_{EQ} = \frac{50R_2}{50 + R_2} = 30$$

which leads to $50R_2 = 1500 + 30R_2$, or $R_2 = 75\ \Omega$. Finally, since $R_{EQ} = 30\ \Omega$, the input port constraint then tells us that $R_1 = 300 - R_{EQ} = 270\ \Omega$. In sum, the L-circuit in the figure with $R_1 = 270\ \Omega$ and $R_2 = 75\ \Omega$ will meet both the input port and the output port constraints. ■

EVALUATION EXAMPLE 3–22

In Example 3–21 we designed the interface circuit in Figure 3–56 to meet the requirements $v_2 = 2$ V and $R_{IN} = 300\ \Omega$. It is claimed that the interface circuit in Figure 3–57 meets the same requirements.

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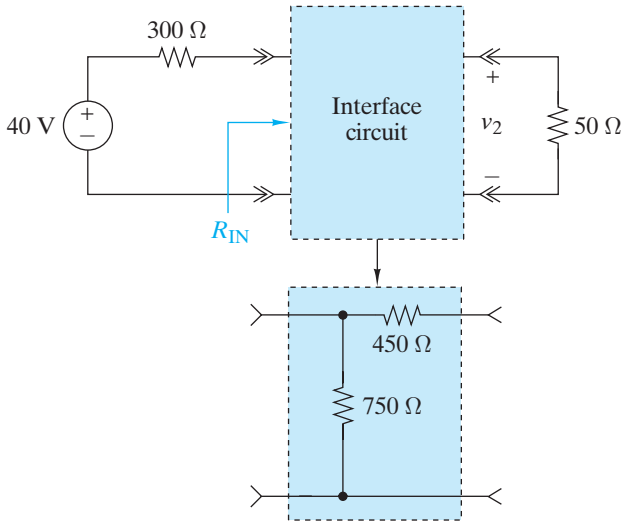
(a) Verify that the circuit in Figure 3–57 produces $v_2 = 2$ V and $R_{IN} = 300\ \Omega$.
(b) It is desired that the 50-Ω load "see" a low output resistance. Which of these two circuits best meets this requirement?

FIGURE 3–57



SOLUTION:

(a) The circuit in Figure 3–57 meets the input port constraint since

$$R_{IN} = 750\|(450 + 50) = 750\|500 = 300\ \Omega$$

as required. Using this fact and voltage division, we find the voltage at the input port of the interface circuit to be

$$v_1 = \left(\frac{R_{IN}}{300 + R_{IN}}\right)40 = \left(\frac{300}{600}\right)40 = 20\text{ V}$$

Using this voltage as the input to the voltage divider made up of the 450-Ω series resistor and the 50-Ω load gives us

$$v_2 = \left(\frac{50}{450 + 50}\right)v_1 = \left(\frac{50}{500}\right)20 = 2\text{ V}$$

This verifies that the circuit in Figure 3–57 produces $v_2 = 2$ V and $R_{IN} = 300\ \Omega$.

(b) To compare the output resistances, we turn the 40-V source off (replace it by a short) and find the lookback resistance seen at the output port. For the circuit in Figure 3–56

$$R_{OUT} = R_2\|(R_1 + 300) = 75\|(270 + 300) = 66.3\ \Omega$$

For the circuit in Figure 3–57

$$R_{OUT} = 450 + 750\|300 = 664\ \Omega$$

Clearly the circuit in Figure 3–56 has a much lower output resistance. ■

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EQA

DESIGN EXAMPLE 3–23

Design the interface circuit in Figure 3–58 so the 50-Ω load "sees" a Thévenin resistance of 50 Ω between terminals C and D, while simultaneously the input voltage source "sees" an input resistance of 300 Ω between terminals A and B. Meeting these two constraints produces matched conditions at the input and output ports of the interface circuit.

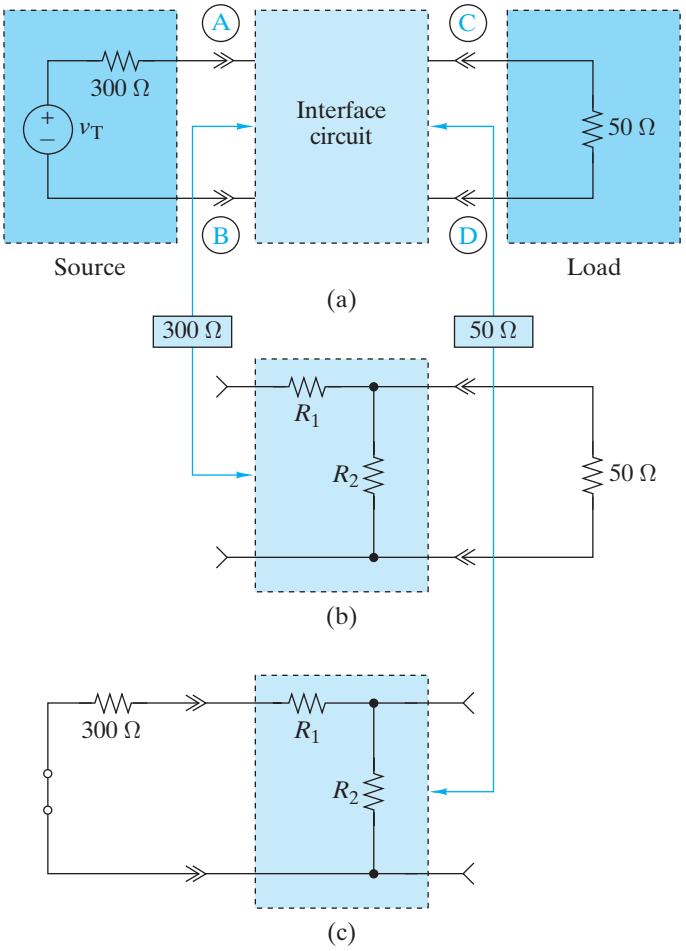

FIGURE 3–58

SOLUTION:

To meet the two constraints in this example, the interface circuit should be a two-resistors L-circuit. We have chosen the L-circuit configuration shown in Figure 3–58 for the following reasons. The source must see a larger resistance (300 Ω) at the input port than the load sees at the output port (50 Ω). This indicates that the source should "look" into a large series resistor R_1 while the load "looks" into a smaller parallel resistor R_2.

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EQA

The design constraints in this example can be expressed in equation form. At the input port (terminals A and B) the equation is

$$R_1 + \frac{50R_2}{R_2 + 50} = 300\ \Omega$$

At the output port (terminals C and D) the equation is

$$\frac{(R_1 + 300)R_2}{R_1 + 300 + R_2} = 50\ \Omega$$

The design requirements reduce to two equations in two unknowns. What could be simpler?

These equations can easily be solved using programs like Mathcad or MATLAB. Solving them using pencil and paper is a bit of a chore. At this point we encourage you to think about the problem in physical terms. For instance, if we simply set $R_2 = 50\ \Omega$, then the conditions at terminals C and D will be met, at least approximately. With $R_2 = 50\ \Omega$ the requirement at terminals A and B reduces to $R_{AB} = R_1 + 50\|50 = R_1 + 25 = 300\ \Omega$. In other words, by physical reasoning we conclude that $R_1 = 275\ \Omega$ and $R_2 = 50\ \Omega$ is an approximate solution. How good is the approximation?

These values yield input and output resistances of $R_{AB} = 300\ \Omega$ as required, and

$$R_{CD} = 50\|(275 + 300) = 50\|575 = 46\ \Omega$$

This value is not exactly 50 Ω, but it is within 10% of the desired value. Since electrical components may have tolerances in the 10% range, a design based on our first-guess approximation might be adequate.

Our first-guess solution can also serve as the starting place for improving the design. The fact that $R_{CD} = 46\ \Omega$ tells us that $R_2 = 50\ \Omega$ is just a bit too low. Suppose we increase R_2 slightly to, say, $R_2 = 56\ \Omega$ (a standard value—see Appendix A, Table A-l). Then at the input port we have

$$R_{AB} = R_1 + 50\|56 = R_1 + 26.42 = 300\ \Omega$$

which would require $R_1 = 273.58\ \Omega$. The nearest standard value to this is $R_1 = 270\ \Omega$. Using the standard values $R_1 = 270\ \Omega$ and $R_2 = 56\ \Omega$ as our second guess, the input and output resistances are

$$R_{AB} = 270 + 50\|56 = 270 + 26.42 = 296.42\ \Omega$$

$$R_{CD} = 56\|(270 + 300) = 56\|570 = 50.99\ \Omega$$

both of which are within 2% of the desired values. Thus, finding an approximate solution can serve as the first step in the design process. Finding that first step is often the most creative and challenging part of circuit design. ■

APPLICATION EXAMPLE 3–24

The source-load interface in Figure 3–59 serves to introduce an important concept that we will encounter many times in subsequent chapters. By simple voltage division, the interface voltage is

$$v = \frac{R_L}{R_L + R_T} v_T$$

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EQA

If the source is ideal ($R_T = 0$), then the interface voltage is $v = v_T$ regardless of the value of the load R_L. Conversely, if the load is an open circuit ($R_L = \infty$), then the interface voltage is $v = v_T$ regardless of the value of the source resistance R_T. Real-world applications typically fall between these two extremes with the result that $v < v_T$. Since $v_T = v_{OC} = v_{MAX}$, interface voltage is generally less than the maximum available voltage. The reduction in interface voltage is an example of an effect called *loading*. In general

Loading is the reduction in load voltage due to the effect of load resistance on the signal source driving it.

A loading problem is fundamentally different than the fixed-source, maximum power transfer problem. With loading, the source and load are both adjustable and the question is how they should be chosen to *minimize loading*. The undesirable effects of loading can be mitigated by making $R_T \ll R_L$, either by reducing the output resistance of the source or increasing the load resistance, or both. As a rule of thumb, the loading effect is less than 10% when $R_L \geq 10R_T$ and less than 1% when $R_L \geq 100R_T$.

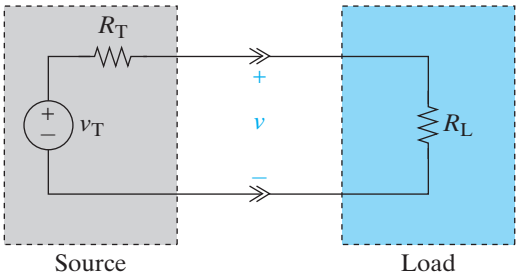

FIGURE 3–59

APPLICATION EXAMPLE 3–25

An **attenuation pad** is a two-port resistance circuit that provides a nonadjustable reduction in signal level while also providing resistance matching at the input and output ports. Figure 3–60 shows an example of an attenuation pad. The manufacturer's data sheet for this pad specifies the following characteristics at the input and output ports.

PORT	CHARACTERISTICS	CONDITION	VALUE	UNITS
Output	Thévenin voltage	600-Ω source connected at the input port	$v_S/4$	V
Output	Thévenin resistance	600-Ω source connected at the input port	600	Ω
Input	Input resistance	600-Ω load connected at the output port	600	Ω

Use Orcad to verify these characteristics.

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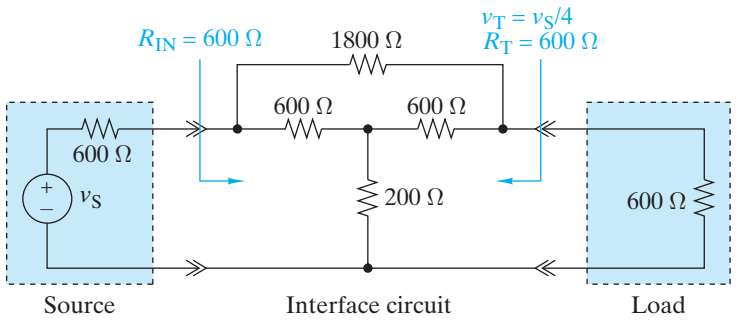
FIGURE 3–60

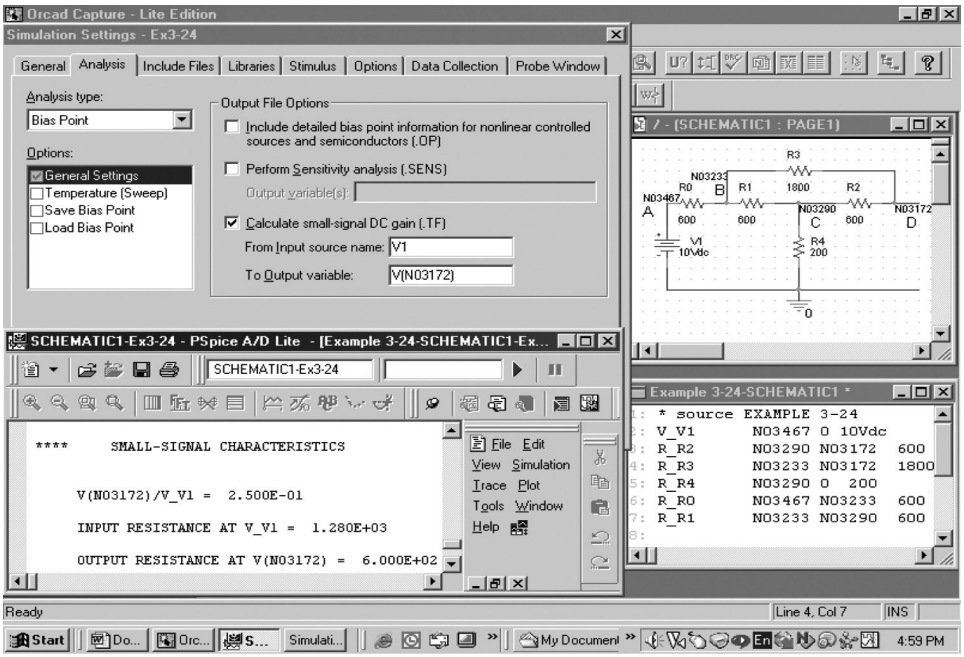


SOLUTION:

Orcad Capture can calculate the two-port characteristics of the pad in Figure 3–60. A circuit diagram created using Orcad is shown in the upper right of Figure 3–61. In this schematic a 600-Ω source is connected at the pad's input port. A 600-Ω load is *not* connected at the output port. The reason is that we need to find the open-circuit (Thévenin) voltage at the output port. We have labeled the pad's output as node D. Orcad has labeled our node D as N03172. This Orcad assignment is not under our control and will change with every new simulation.[3]

Selecting the **PSpice** and the **Edit Simulation Profile** commands causes the "Simulation Settings" dialog box shown in the upper left portion of

FIGURE 3–61



3 Every time a schematic is drawn (even the same schematic) Orcad generates a new random number for each node name. To display the Orcad assigned names, double-click on each node to open a new window that gives information about the node. Click on the node's name then select **Display**. This opens a second window. Select **Value Only**. Then click **OK**. Finally select **Apply** to place it on the drawing. Alternately, the Orcad assigned names can be viewed in the netlist file.

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EQA

Figure 3-61 to appear. We first check the "Calculate small-signal DC gain (.TF)" box as shown in the figure. To calculate a gain, Orcad must know the input and output variables. We inform Orcad of these variables by supplying entries in the "From Input source name" and "to Output variable" boxes. In this example, voltage source V1 is the input source and the output variable is the node voltage V(N03172) (the voltage at our node D). Note that V(N03172) is the open-circuit voltage at the output port. With these entries Orcad PSpice will calculate three things: (1) the small-signal gain V(N03172)/V_V1, (2) the input resistance seen by V1, and (3) the output resistance.

Returning to the main menu, we select **PSpice/ Run**. Orcad PSpice performs a dc analysis of the circuit and writes the results to the output file. Included in the output file are the small-signal characteristics shown at the bottom left in Figure 3–61. PSpice reports that the small-signal gain V(N03172)/V_V1 = 2.500E-01, the input resistance seen by V1 is 1.280E+ 03, and the output resistance is 6.000E+02. This means that the open-circuit (Thévenin) voltage at the output port is one-fourth of the source voltage and the output (Thévenin) resistance is 600 Ω as stated in the data sheet. The input resistance (1280 Ω) given in the output file is the resistance seen by the source V1 when the output port is open-circuited. The manufacturer's data sheet specifies the input resistance when a 600-Ω load is connected at the output port. Thus, the simulation has not directly verified the input resistance characteristic.

However, a moment's reflection shows that the two-port pad circuit is symmetrical. The simulation results show that the output resistance is 600 Ω when a 600-Ω source is connected at the input. It follows from the circuit's symmetry that the input resistance is 600 Ω when a 600-Ω load is connected at the output. In summary, the simulation has verified all of the entries in the manufacturer's data sheet. ■

SUMMARY

- Node-voltage analysis involves identifying a reference node and the node to datum voltages at the remaining $N - 1$ nodes. The KCL connection constraints at the $N - 1$ nonreference nodes combined with the element constraints written in terms of the node voltages produce $N - 1$ linear equations in the unknown node voltages.
- Mesh-current analysis involves identifying mesh currents that circulate around the perimeter of each mesh in a planar circuit. The KVL connection constraints around $E - N + 1$ meshes combined with the element constraints written in terms of the mesh currents produce $E - N + 1$ linear equations in the unknown mesh currents.
- Node and mesh analysis can be modified to handle both types of independent sources using a combination of three methods: (1) source transformations, (2) selecting circuit variables so independent sources specify the values of some of the unknowns, and (3) using supernodes or supermeshes.
- A circuit is linear if it contains only linear elements and independent sources. For single-input linear circuits, the proportionality property states that any output is proportional to the input. For multiple-input linear circuits, the superposition principle states that any output can be found by summing the output produced when each input acts alone.

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EQA

- A Thévenin equivalent circuit consists of a voltage source in series with a resistance. A Norton equivalent circuit consists of a current source in parallel with a resistance. The Thévenin and Norton equivalent circuits are related by a source transformation.
- The parameters of the Thévenin and Norton equivalent circuits can be determined using any two of the following: (1) the open-circuit voltage at the interface, (2) the short-circuit current at the interface, and (3) the equivalent resistance of the source circuit with all sources turned off.
- The parameters of the Thévenin and Norton equivalent circuits can also be determined using circuit reduction methods or by directly solving for the source i–v relationship using node-voltage or mesh-current analysis.
- For a fixed source and an adjustable load, the maximum interface signal levels are $v_{MAX} = v_{OC}$ ($R_L = \infty$), $i_{MAX} = i_{SC}$ ($R_L = 0$), and $p_{MAX} = v_{OC}i_{SC}/4$ ($R_L = R_T$). When $R_L = R_T$, the source and load are said to be matched.
- Interface signal transfer conditions are specified in terms of the voltage, current, or power delivered to the load. The design constraints depend on the signal conditions specified and the circuit parameters that are adjustable. Some design requirements may require a two-port interface circuit. An interface design problem may have one, many, or no solutions.

PROBLEMS

OBJECTIVE 3–1 GENERAL CIRCUIT ANALYSIS (SECT. 3–1 TO 3–2)

Given a circuit consisting of linear resistors and independent sources:
(a) (Formulation) Write node-voltage or mesh-current equations for the circuit.
(b) (Solution) Solve the equations from part (a) for selected signal variables or input-output relationships.
Node-voltage method:
See Examples 3–1, 3–2, 3–3, 3–4, 3–5, 3–6 and Exercises 3–2, 3–3, 3–4, 3–5, 3–6
Mesh-current method:
See Examples 3–7, 3–8, 3–9 and Exercises 3–8, 3–9, 3–10

3–1 **(a)** Formulate node-voltage equations for the circuit in Figure P3–1.
(b) Use these equations to find v_x and i_x.

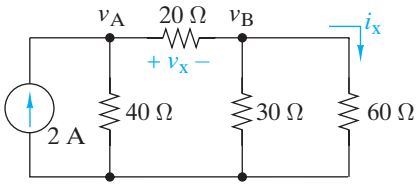

FIGURE P3–1

3–2 **(a)** Formulate node-voltage equations for the circuit in Figure P3–2.
(b) Use these equations to find v_x and i_x.

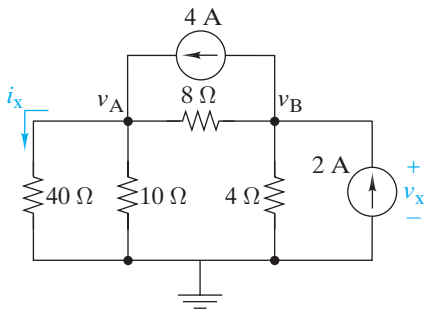

FIGURE P3–2

3–3 **(a)** Formulate node-voltage equations for the circuit in Figure P3–3.
(b) Use these equations to find v_x and i_x.

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EQA

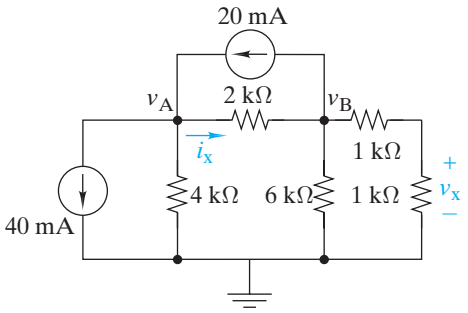

FIGURE P3–3

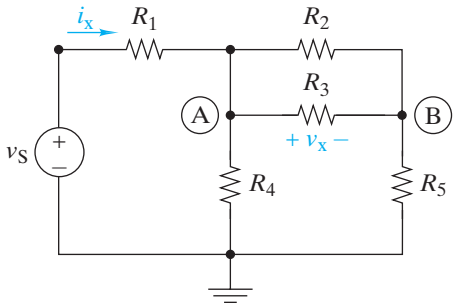

FIGURE P3–6

3–4 **(a)** Formulate node-voltage equations for the circuit in Figure P3–4.
(b) Use these equations to find v_x and i_x.

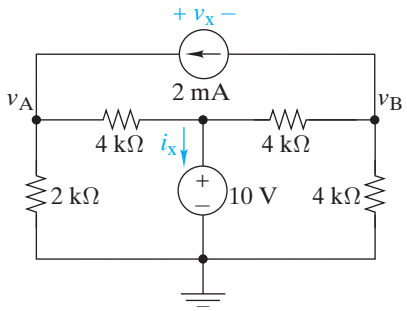

FIGURE P3–4

3–5 **(a)** Formulate node-voltage equations for the circuit in Figure P3–5.
(b) Solve for v_x and i_x when $R_1 = R_2 = R_3 = R_4 = 10\ \text{k}\Omega$, $v_S = 20$ V, and $i_S = 2$ mA.

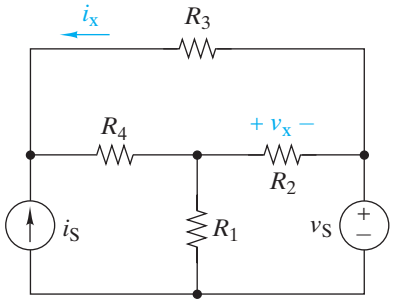

FIGURE P3–5

3–6 **(a)** Formulate node-voltage equations for the circuit in Figure P3–6.
(b) Solve for v_x and i_x when $R_1 = R_2 = R_3 = R_4 = R_5 = 10\ \text{k}\Omega$, and $v_S = 20$ V.

3–7 **(a)** Formulate node-voltage equations for the circuit in Figure P3–7.
(b) Solve for v_A, v_B, and v_C when $R_1 = 1\ \text{k}\Omega$, $R_2 = 2\ \text{k}\Omega$, $R_3 = 4\ \text{k}\Omega$, $R_4 = 2\ \text{k}\Omega$, and $i_{S1} = i_{S2} = 2$ mA.

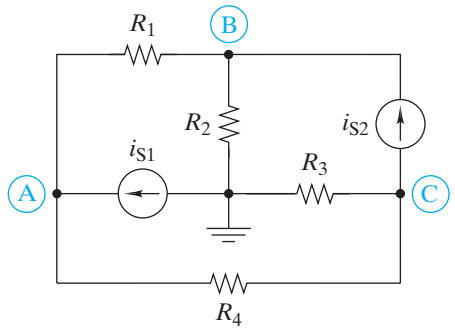

FIGURE P3–7

3–8 **(a)** Formulate node-voltage equations for the circuit in Figure P3–8.
(b) Solve for v_x and i_x when $R_1 = R_4 = 1\ \text{k}\Omega$, $R_2 = R_3 = 250\ \Omega$, $R_x = 500\ \Omega$, and $v_S = 15$ V.

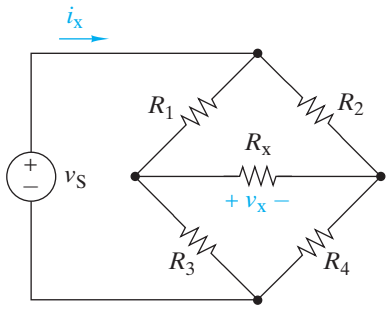

FIGURE P3–8

3–9 **(a)** Formulate mesh-current equations for the circuit in Figure P3–9.
(b) Use these equations to find v_x and i_x.

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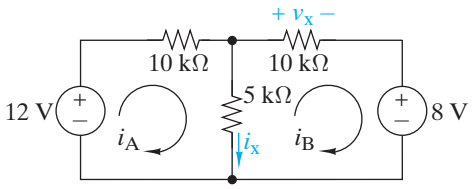

FIGURE P 3 – 9

3–10 **(a)** Formulate mesh-current equations for the circuit in Figure P3–10.
(b) Use these equations to find v_x and i_x.

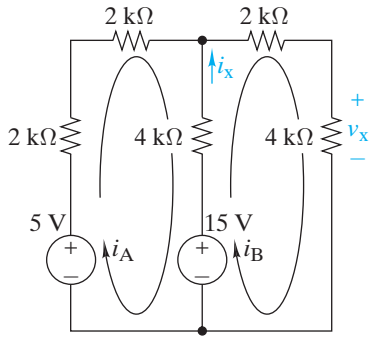

FIGURE P 3 – 10

3–11 **(a)** Formulate mesh-current equations for the circuit in Figure P3–11.
(b) Use these equations to find v_x and i_x.

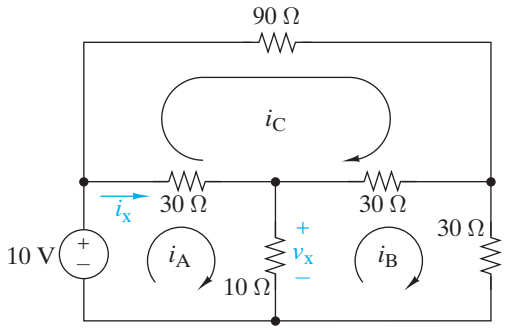

FIGURE P 3 – 11

3–12 **(a)** Formulate mesh-current equations for the circuit in Figure P3–12.
(b) Solve for v_x and i_x when $R_1 = 200\ \Omega$, $R_2 = 300\ \Omega$, $R_3 = 50\ \Omega$, $R_4 = 250\ \Omega$, $R_5 = 200\ \Omega$, $i_S = 50$ mA, and $v_S = 15$ V.
(c) Find the total power dissipated in the circuit.

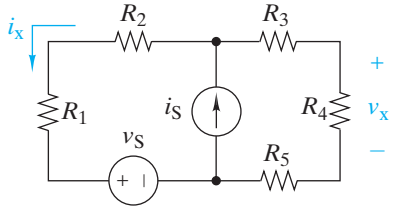

FIGURE P 3 – 12

3–13 **(a)** Formulate mesh-current equations for the circuit in Figure P3–13.
(b) Solve for v_x and i_x when $R_1 = R_2 = 10\ \text{k}\Omega$, $R_3 = 2\ \text{k}\Omega$, $R_4 = 1\ \text{k}\Omega$, $i_S = 2.5$ mA, $v_{S1} = 12$ V, and $v_{S2} = 0.5$ V.
(c) Find the power supplied by v_{S1}.

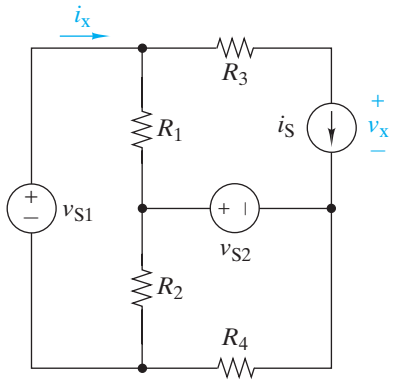

FIGURE P 3 – 13

3–14 The circuit in Figure P3–14 seems to require two supermeshes since both current sources appear in two meshes. However, sometimes rearranging the circuit diagram will eliminate the need for a supermesh.
(a) Show that supermeshes can be avoided in Figure P3–14 by rearranging the connection of resistor R_6.
(b) Formulate mesh-current equations for the modified circuit as redrawn in part (a).
(c) Solve for v_x when $R_1 = R_2 = R_3 = R_4 = 2\ \text{k}\Omega$, $R_5 = R_6 = 1\ \text{k}\Omega$, $i_{S1} = 40$ mA, and $i_{S2} = 20$ mA.

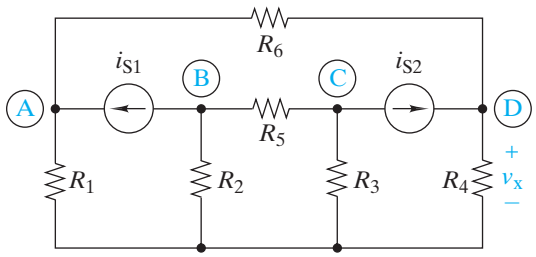

FIGURE P 3 – 14

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EQA

3–15 **(a)** Formulate mesh-current equations for the circuit in Figure P3–15.
(b) Use these equations to find v_x and i_x.
(c) Find the total power delivered to the resistors.

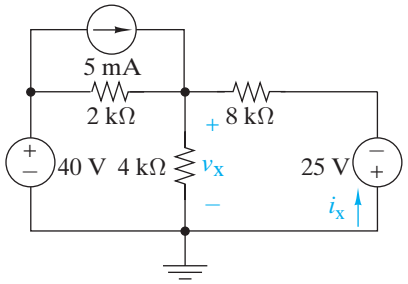

FIGURE P3–15

3–16 **(a)** Formulate mesh-current equations for the circuit in Figure P3–16.
(b) Use these equations to find the input resistance.

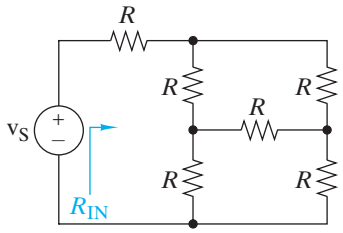

FIGURE P3–16

3–17 In Figure P3–17 all of the resistors are 1 kΩ. The voltage at node C is found to be $v_C = -2$ V when node B is connected to ground. Find the node voltages v_A and v_D, and the mesh currents i_A and i_B.

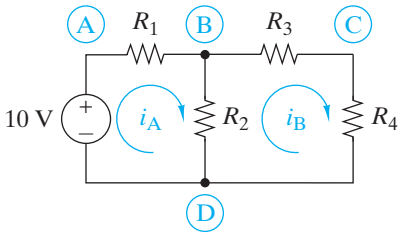

FIGURE P3–17

3–18 In Figure P3–17 all of the resistors are 1 kΩ. The voltage at node A is observed to be $v_A = 8$ V when node C is connected to ground. Find the node voltages v_B and v_D, and the mesh currents i_A and i_B.

3–19 Find the node voltages v_A and v_B in Figure P3–19.

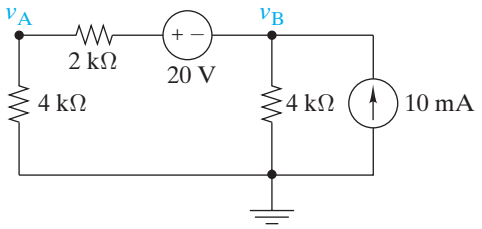

FIGURE P3–19

3–20 Find the mesh currents i_A, i_B, and i_C in Figure P3–20.

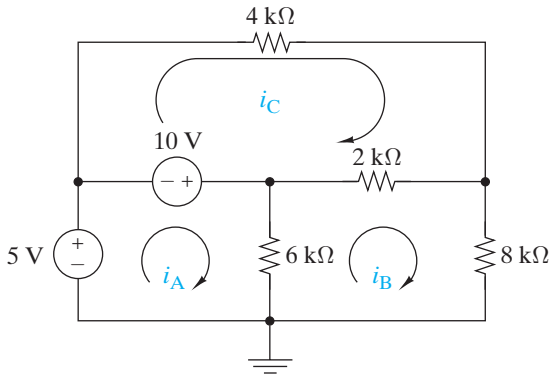

FIGURE P3–20

OBJECTIVE 3–2 LINEARITY PROPERTIES (SECT. 3–3)

(a) Given a circuit containing linear resistors and one independent source, use the proportionality principle to find selected signal variables.
(b) Given a circuit containing linear resistors and two or more independent sources, use the superposition principle to find selected signal variables.
See Examples 3–10, 3–11, 3–12 and Exercises 3–11, 3–12, 3–13, 3–14, 3–15

3–21 Find the proportionality constant $K = v_O/i_S$ for the circuit in Figure P3–21.

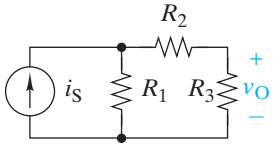

FIGURE P3–21

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EQA

3–22 Find the proportionality constant $K = i_O/v_S$ for the circuit in Figure P3–22.

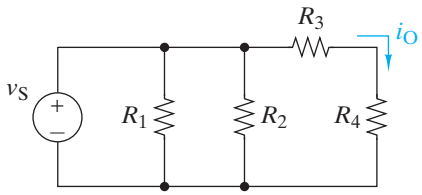

FIGURE P3–22

3–23 Find the proportionality constant $K = v_O/i_S$ for the circuit in Figure P3–23.

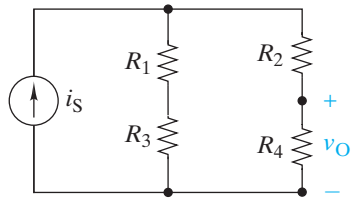

FIGURE P3–23

3–24 Use the unit output method to find v_O in Figure P3–24.

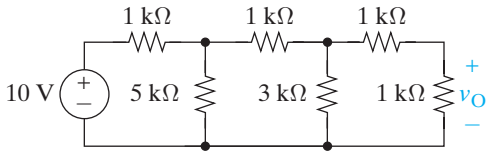

FIGURE P3–24

3–25 Use the unit output method to find i_O in Figure P3–25.

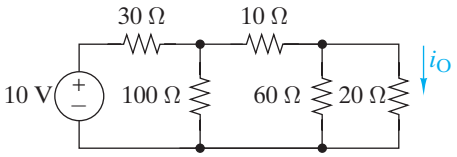

FIGURE P3–25

3–26 Use the superposition principle to find v_O in Figure P3–26.

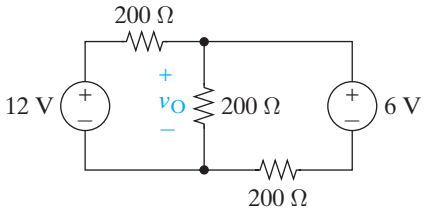

FIGURE P3–26

3–27 Use the superposition principle to find i_O in Figure P3–27.

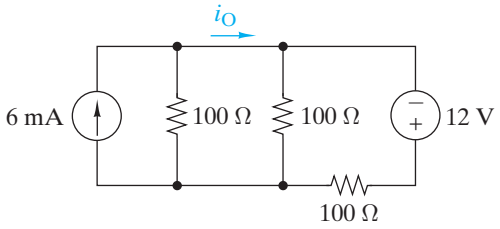

FIGURE P3–27

3–28 Use the superposition principle to find v_O in Figure P3–28.

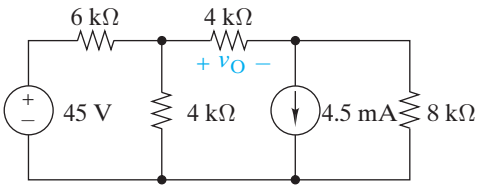

FIGURE P3–28

3–29 Use the superposition principle to find i_O in Figure P3–29.

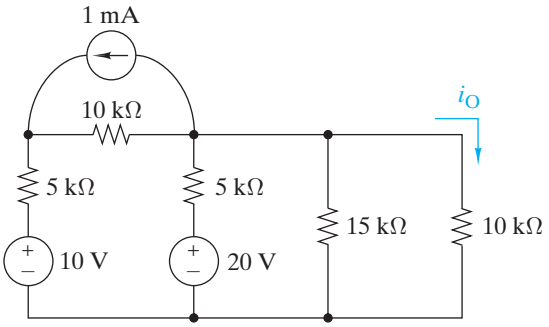

FIGURE P3–29

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3–30 Use the superposition principle to find v_O in terms of v_1, v_2, and R in Figure P3–30.

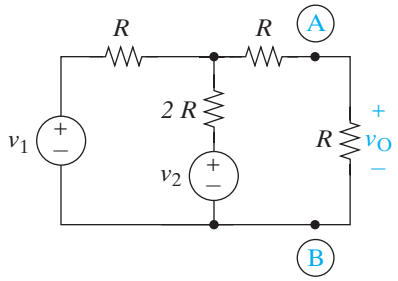

FIGURE P3–30

3–31 Use the superposition principle to find v_O in terms of i_1, i_2, and R in Figure P3–31.

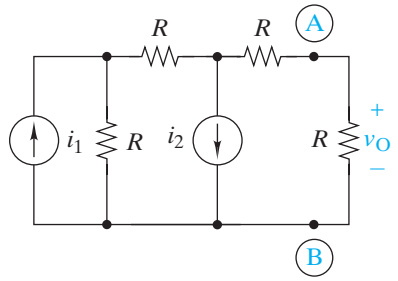

FIGURE P3–31

3–32 A linear circuit containing two sources drives a 100-Ω load resistor. Source number 1 delivers 250 mW to the load when source number 2 is off. Source number 2 delivers 4 W to the load when source number 1 is off. Find the power delivered to the load when both sources are on. *Hint*: The answer is not 4.25 W. Why?

3–33 A linear circuit is driven by an independent voltage source $v_S = 10$ V and an independent current source $i_S = 10$ mA. The output voltage is $v_O = 2$ V when the voltage source is on and the current source off. The output is $v_O = 1$ V when both sources are on. Find the output voltage when $v_S = 5$ V and $i_S = -10$ mA.

3–34 A certain linear circuit has three input voltages and one output voltage v_O. The following table lists the output for different values of the three inputs. Find the input-output relationship for the circuit.

v_{S1}(V)	v_{S2}(V)	v_{S3}(V)	v_O(V)
2	4	−4	1
1	2	2	1.5
1	4	2	2

3–35 This problem involves designing a resistive circuit with two inputs v_{S1} and v_{S2} and a single output voltage v_O. Design the circuit so that $v_O = K(v_{S1} + 4v_{S2})$ is delivered across a 500-Ω load. The value of K is not specified but should be greater than 1/10.

OBJECTIVE 3–3 THÉVENIN AND NORTON EQUIVALENT CIRCUITS (SECT. 3–4)

Given a circuit containing linear resistors and independent sources:
(a) Find the Thévenin or Norton equivalent at a specified pair of terminals.
(b) Use the Thévenin or Norton equivalent to find the signals delivered to linear or nonlinear loads.
See Examples 3–13, 3–14, 3–15, 3–16 and Exercises 3–16, 3–17, 3–18

3–36 **(a)** Find the Thévenin or Norton equivalent circuit seen by R_L in Figure P3–36.
(b) Use the equivalent circuit found in part (a) to find i_L in terms of i_S, R_1, R_2, and R_L.
(c) Check your answer in part (b) using current division.

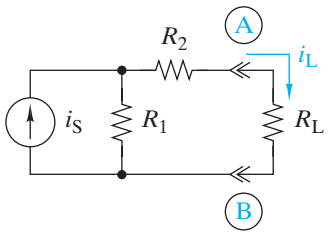

FIGURE P3–36

3–37 Find the Thévenin equivalent circuit seen by R_L in Figure P3–37. Find the voltage across the load when $R_L = 5\ \Omega$, 10 Ω, and 50 Ω.

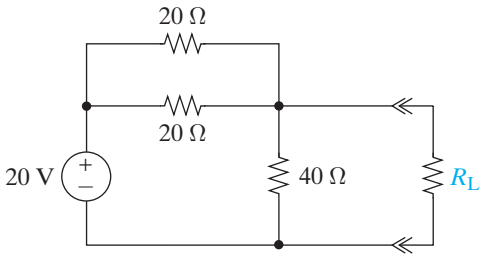

FIGURE P3–37

3–38 Find the Norton equivalent seen by R_L in Figure P3–38. Find the current through the load when $R_L = 6\ \Omega$, 12 Ω, and 60 Ω.

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EQA

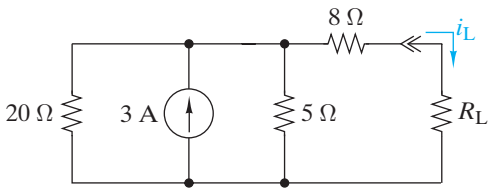

FIGURE P3–38

3–39 Find the Thévenin equivalent seen by R_L in Figure P3–39. Find the power delivered to the load when $R_L = 50$ kΩ and 200 kΩ.

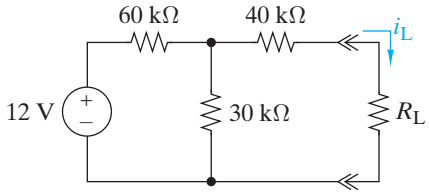

FIGURE P3–39

3–40 Find the Norton equivalent at terminals A and B in Figure P3–40.

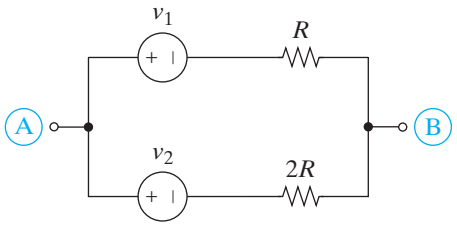

FIGURE P3–40

3–41 The purpose of this problem is to use Thévenin equivalent circuits to find the voltage v_X in Figure P3–41. Find the Thévenin equivalent circuit seen looking to the left of terminals A and B. Find the Thévenin equivalent circuit seen looking to the right of terminals A and B. Connect these equivalent circuits together and find the voltage v_X.

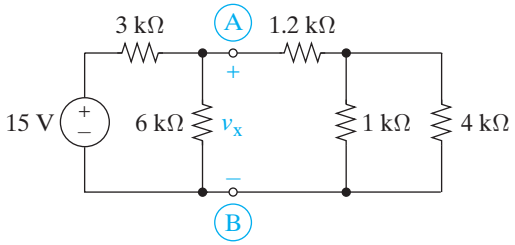

FIGURE P3–41

3–42 Figure P3–42 shows an active circuit with two accessible terminals. The output current is $i = 10$ mA when $v = 0$. The output voltage is $v = 6$ V when a 2.4-kΩ resistor is connected between the terminals. How much current would this source deliver to a 6-V battery?

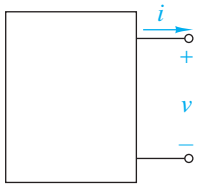

FIGURE P3–42

3–43 The i–v characteristic of the active circuit in P3–42 is $5v + 500i = 60$. Find the output voltage when a 500-Ω resistive load is connected across the two accessible terminals.

3–44 Figure P3–42 shows a source circuit with two accessible terminals. Some voltage and current measurements at the accessible terminals are

v(V)	−10	−5	0	+5	+10	12	13	14
i(mA)	+5	+4	+3	+2	+1	0	−1	−2

(a) Use these data to plot the source i–v characteristic.
(b) Develop a Thévenin equivalent circuit valid on the range $|v| < 10$ V.
(c) Use the equivalent circuit to predict the source v_{OC} and i_{SC}.
(d) Compare your results in part (c) with the given measurements and explain any differences.

3–45 The Thévenin equivalent parameters of a practical voltage source are $v_T = 25$ V and $R_T = 150$ Ω. Find the smallest load resistance for which the load voltage exceeds 15 V.

3–46 Use a sequence of source transformations to find the Thévenin equivalent at terminals A and B in Figure P3–46.

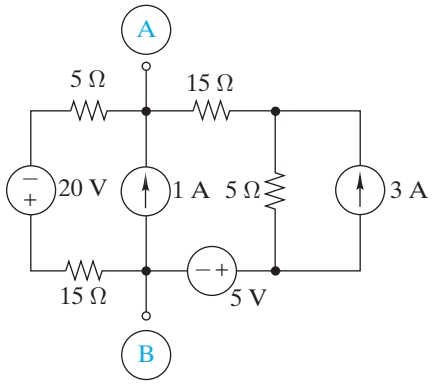

FIGURE P3–46

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EQA

3–47 Select the value of R_L in Figure P3–47 so that $i_O = 80\ \mu A$.

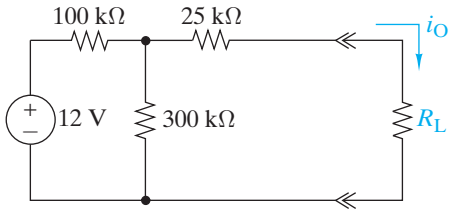

FIGURE P3–47

3–48 Find the Thévenin equivalent at terminals A and B in Figure P3–48.

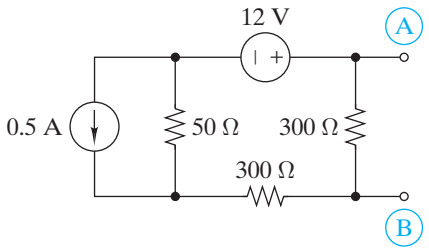

FIGURE P3–48

3–49 A nonlinear resistor is connected across a two-terminal source whose Thévenin equivalent is $v_T = 5$ V and $R_T = 500\ \Omega$. The i–v characteristic of the resistor is $i = 10^{-4}(v + 2v^{3.3})$. Plot the i–v characteristic of the source and the resistor and graphically determine the voltage across and current through the nonlinear resistor.

3–50 A nonlinear resistor is connected across a two-terminal source whose Thévenin equivalent is $v_T = 10$ V and $R_T = 200\ \Omega$. The i–v characteristic of the resistor is $v = 4000\, i^2$. Plot the i–v characteristic of the source and the resistor and graphically determine the voltage across and current through the nonlinear resistor.

3–51 Find the Norton equivalent seen by R_L in Figure P3–51. Select the value of R_L so that 100 mW is delivered to the load.

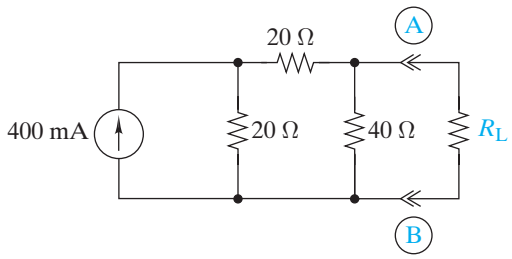

FIGURE P3–51

3–52 Find the Norton equivalent seen by R_L in Figure P3–52.

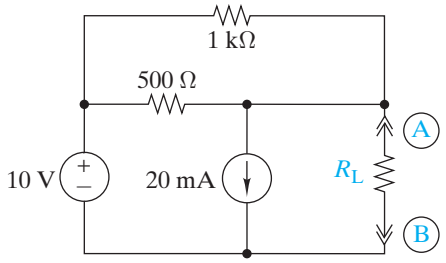

FIGURE P3–52

3–53 Find the Thévenin equivalent seen by R_L in Figure P3–53.

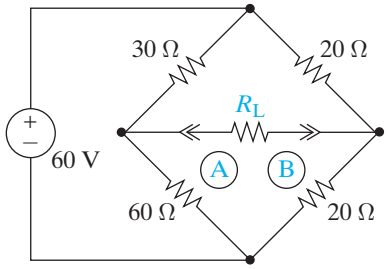

FIGURE P3–53

OBJECTIVE 3–4 MAXIMUM SIGNAL TRANSFER (SECT. 3–5)

Given a circuit containing linear resistors and independent sources:
(a) Find the maximum voltage, current, and power available at a specified pair of terminals.
(b) Find the resistive loads required to obtain the maximum available signal levels.
See Example 3–17 and Exercise 3–19

3–54 The resistance R in Figure P3–54 is adjusted until maximum power is delivered to the load consisting of R and the 6-kΩ resistor in parallel. Find the required value of R.

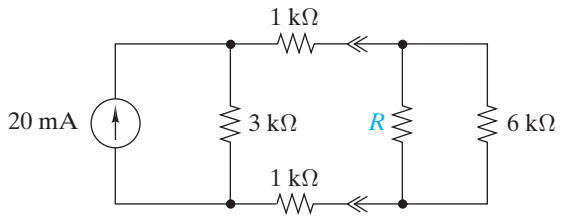

FIGURE P3–54

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EQA

3–55 When a 5-kΩ resistor is connected across a two-terminal source, a current of 15 mA is delivered to the load. When a second 5-kΩ resistor is connected in parallel with the first, a total current of 20 mA is delivered. Find the maximum power available from the source.

3–56 Find the value of R in Figure P3–56 so that maximum power is delivered to the 4-kΩ load. Find the value of the maximum power.

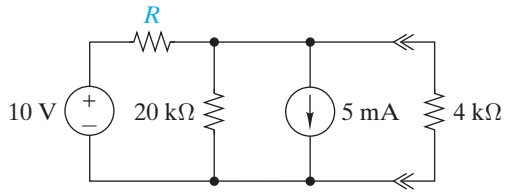

FIGURE P3–56

3–57 Find the value of R_L in Figure P3–57 such that $v_L = 80$ V.

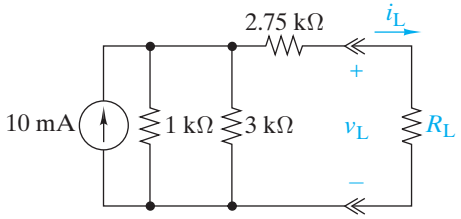

FIGURE P3–57

3–58 Find the value of R_L in Figure P3–57 such that maximum power is delivered to the load. Find the value of the maximum power.

3–59 A 15-V source with negligible internal resistance is connected in series with a resistor R_S. The purpose of R_S is to limit the signals delivered to any load to the ranges $i < 50$ mA and $p < 200$ mW. Find the range of R_S that will meet both constraints.

3–60 A practical source delivers 50 mA to a 300-Ω load. The source delivers 12 V to a 120-Ω load. Find the maximum power available from the source.

OBJECTIVE 3–5 INTERFACE CIRCUIT DESIGN AND EVALUATION (SECT. 3–6)

(a) D Given the signal transfer objectives at a source-load interface, adjust the circuit parameters or design one or more two-port interface circuits to achieve the specified objectives within stated constraints.

(b) E Given two or more circuits that perform the same interface function, rank-order the circuits using stated criteria.

See Examples 3–18, 3–19, 3–20, 3–21, 3–22, 3–23 and Exercise 3–20

3–61 D The output current of the voltage source in Figure P3–61 must be less then 100 mA. Design an interface circuit so that the load voltage is $v_2 = 4$ V and the source current is $i_1 < 100$ mA.

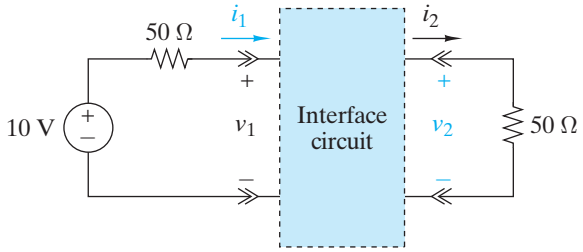

FIGURE P3–61

3–62 D Figure P3–62 shows an interface circuit connecting a 15-V source to a diode load. The i–v characteristic of the diode is

$$i = 10^{-14}(e^{40v} - 1)$$

Design an interface circuit so that $v = 0.7$ V.

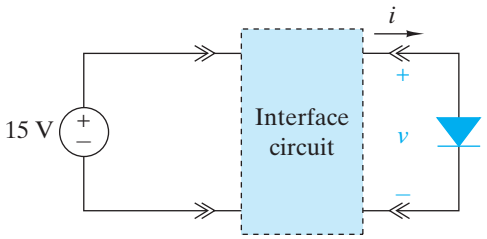

FIGURE P3–62

3–63 D Design the interface circuit in Figure P3–63 so that the voltage delivered to the load is $v = 10$ V ± 10%. Use the following standard resistors in your design: 130 Ω, 200 Ω, 300 Ω, 430 Ω, 620 Ω, and 910 Ω. These resistors all have a tolerance of ±5%, which you must account for in your design.

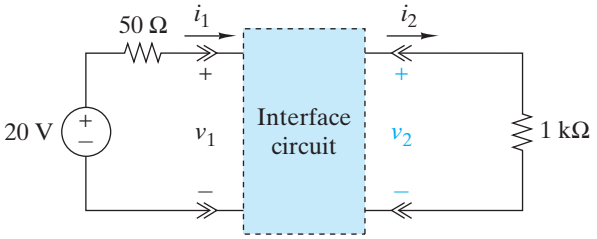

FIGURE P3–63

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EQA

3–64 D Design the interface circuit in Figure P3–63 so that 25 mW is delivered to the 1-kΩ load resistor.

3–65 D Use the resistor array in Figure P3–65 to design a voltage divider with $K = v_2/v_1 \geq 0.6$ and an input resistance close to 100 Ω.

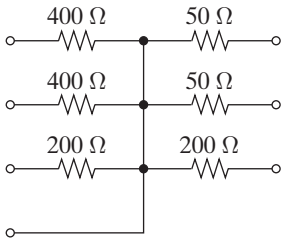

FIGURE P3–65

3–66 D Select R_L in Figure P3–66 so that the power delivered to the load is 400 mW.

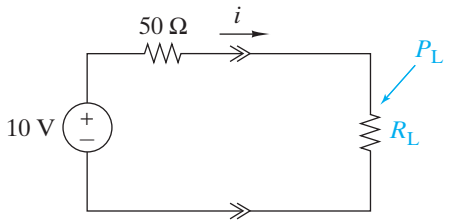

FIGURE P3–66

3–67 D Design the interface circuit in Figure P3–67 so that $R_{IN} = 100\ \Omega$ and the current delivered to the 50-Ω load is $i = 50$ mA.

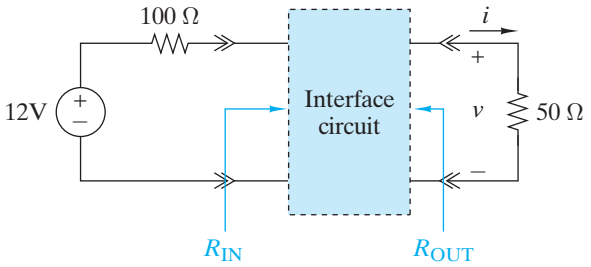

FIGURE P3–67

3–68 D Design the interface circuit in Figure P3–67 so that $R_{OUT} = 50\ \Omega$ and the voltage delivered to the 50-Ω load is $v = 2$ V.

3–69 D The circuit in Figure P3–69 has a source resistance of 75 Ω and a load resistance of 600 Ω. Design the interface circuit so that the input resistance is $R_{IN} = 75\ \Omega \pm 10\%$ and the output resistance is $R_{OUT} = 600\ \Omega \pm 10\%$.

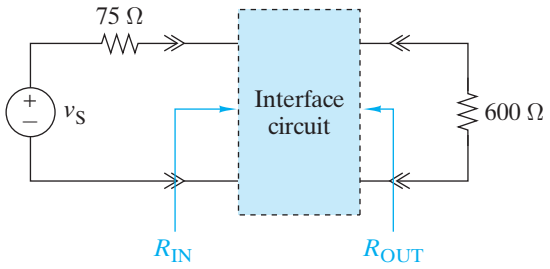

FIGURE P3–69

3–70 E It is claimed that both interface circuits in Figure 3–70 will deliver $v = 4$ V to the 75-Ω load. Verify this claim. Which interface circuit consumes the least power? Which has an output resistance that best matches the 75-Ω load?

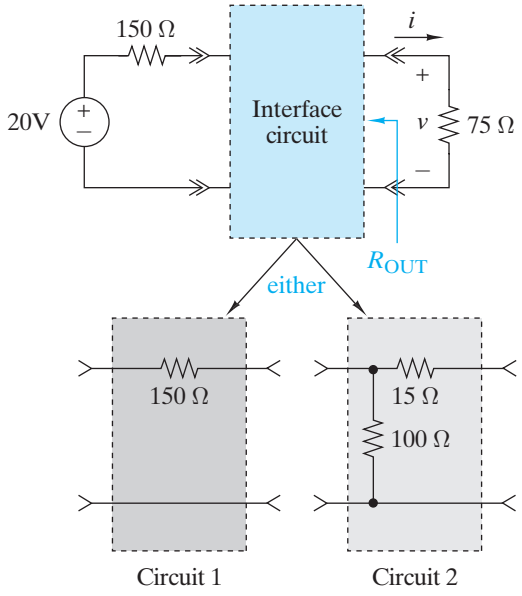

FIGURE P3–70

INTEGRATING PROBLEMS

3–71 A Composite Circuit Analysis

The i–v characteristic of network N in Figure P3–71 is $i = (5 \times 10^{-3}v - 0.5)$ A. Find the voltage at node A.

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EQA

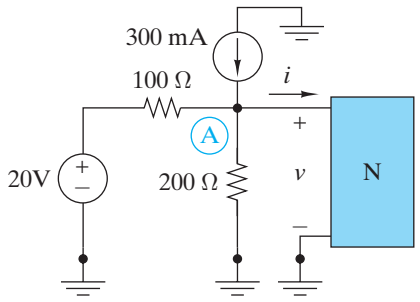

FIGURE P3–71

3–72 A Attenuation Analysis

In Figure P3–72 a two-port attenuator connects a 600-Ω source to a 600-Ω load. Find the power delivered to the load in terms of v_S. Remove the attenuator and find the power delivered to the load when the source is directly connected to the load. By what fraction does the attenuator reduce the power delivered to the 600-Ω load? Express the fraction in dB.

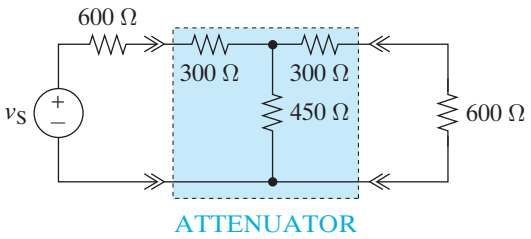

FIGURE P3–72

3–73 D Interface Circuit Design

Using no more than three 50-Ω resistors, design the interface circuit in Figure P3–73 so that $v \le 4$ V and $i \le 100$ mA regardless of the value of R_L.

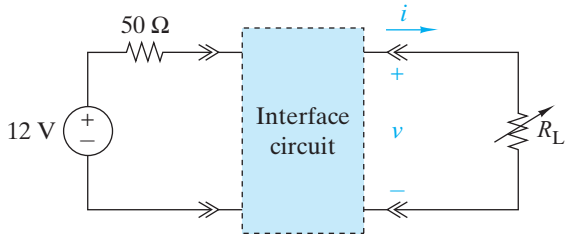

FIGURE P3–73

3–74 D Battery Design

A satellite requires a battery with an open-circuit voltage $v_{OC} = 36$ V and a Thévenin resistance $R_T \le 10\ \Omega$. The battery is to be constructed using series and parallel combinations of one of two types of cells. The first type has $v_{OC} = 9$ V, $R_T = 4\ \Omega$, and a weight of 40 grams. The second type has $v_{OC} = 4$ V, $R_T = 0.5\ \Omega$, and a weight of 15 grams. Design a minimum-weight battery that meets the open-circuit voltage and Thévenin resistance requirements.

3–75 E Design Evaluation

A requirement exists for a circuit to deliver 0 to 5 V to a 100-Ω load from a 20-V source rated at 2.5 W. Two proposed circuits are shown in Figure P3–75. Which one would you choose and why?

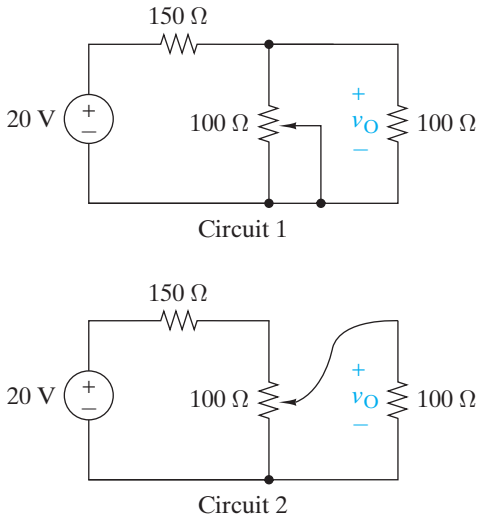

FIGURE P3–75