Chapter 1 INTRODUCTION AND OVERVIEW OF MICROELECTRONICS PACKAGING

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1.1 INTRODUCTION

An exact date for the advent of "electronic packaging" is difficult, if not impossible, to establish due to the diversity of opinion on what constitutes an electronic package. However, there is no doubt that, in general, nearly all structures which are involved with the generation, transmission, and utilization of electrical signals are packaged in some manner, even if the packaging method and material are somewhat primitive. For example, the insulation surrounding a wire is technically a package. Thus, an "electronic package" might be defined as that portion of an electronic structure which serves to protect an electronic/electrical element from its environment, and the environment from the electronic/electrical element. However, in addition to providing encapsulation for environmental protection, a package must also allow for complete testing of the packaged device and a high-yield method of assembly to the next level of integration [1.1].

With the commercialization of the silicon transistor in the 1950s, electronic packaging technology development took on a new level of intensity resulting in the proliferation of standard electronic packages, a few of which are shown in Fig. 1.1. However, for several years, the performance of packaged electronic components was limited by the component itself and was impacted little, if any, by packaging technology. At some later date, parasitics associated with the package housing the component began to adversely affect the performance of the device. Consequently, packaging of electronic components, in particular integrated circuits (ICs), became the focus of an intense developmental effort and continues to challenge the microelectronics industry today [1.2–1.3]. Essentially, the point has been reached where advancement in integrated circuit performance now drives packaging technology.

The multichip module (MCM) is the most recent attempt to realize maximum performance from integrated circuits, and thereby electronic systems, by minimizing the impact of the package [1.4–1.5]. This is realized through

- improved electrical performance
- increased IC packaging density
- further miniaturization

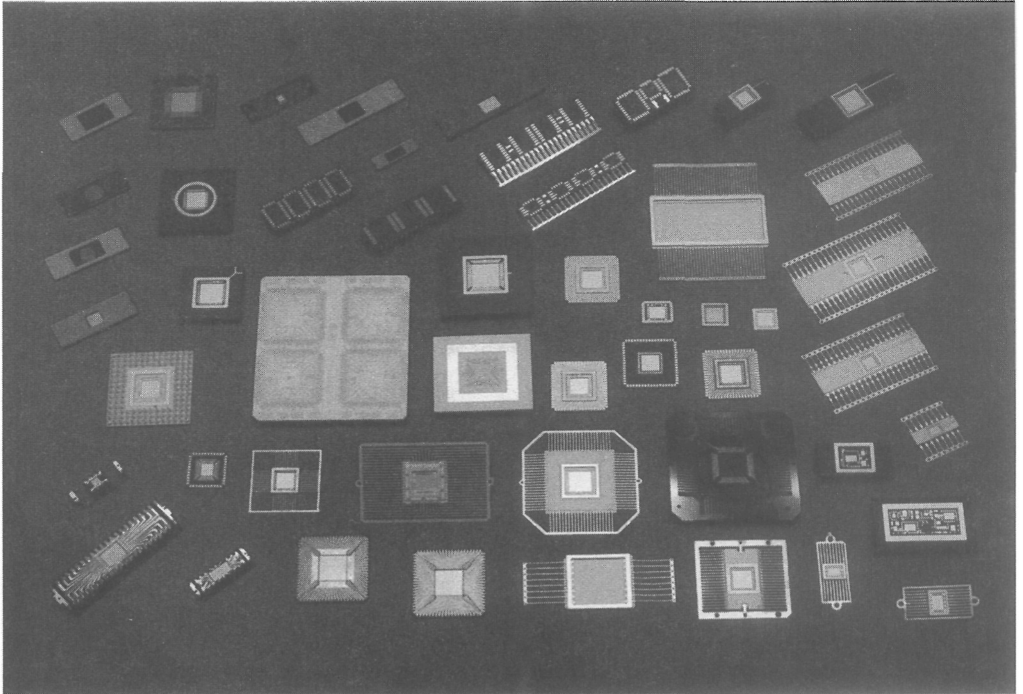


Figure 1.1 Photograph of a number of standard electronic packages (courtesy of Kyocera).

- reduced power consumption, and
- increased reliability

It is the intent of this book to discuss all aspects of electronic packaging which impact the performance of electronic devices which they house. The primary focus of the discussion is MCM technology. However, material on all aspects of IC packaging is included in each chapter.

This book addresses all aspects of electronic packaging beginning with an overview including definitions, functions, and classifications of microelectronics packaging. Subsequent chapters provide a thorough treatment of technical subject matter important to both the package designer engaged in developing custom packages and the design engineer who must choose from the available standardized packages. The subjects covered include packaging materials and configurations, packaging tradeoffs and decisions, electrical design considerations, thermal design and management, mechanical design considerations, modeling and simulation, and computer-aided engineering and design. Other chapters address processing technologies, processing considerations and limitations, reliability considerations, testing and qualification, analytical instruments and techniques, several case studies, and economic considerations. The final chapter discusses advanced topics and future trends in MCM technology.

1.2 FUNCTIONS OF AN ELECTRONIC PACKAGE

In the previous section, a very simple definition of an electronic package was given. If we restrict the definition of an electronic package to the housing and interconnection of integrated circuits (also referred to as "silicon chips," "chips," or "die") to form an electronic system, then we can restrict the discussion to a subset of the multitude of electronic packages that would otherwise have to be considered. For this reduced set of packages, the functions which the package must provide include a structure to physically support the chip, a physical housing to protect the chip from the environment, an adequate means of removing heat generated by the chips or system, electrical connections to allow signal and power access to and from the chip, and a wiring structure to provide interconnection between the chips of an electronic system [1.6–1.8]. Thus, the package must provide for:

- signal distribution
- heat dissipation
- power distribution
- circuit support and protection

Figure 1.2 illustrates these various functions for both single chip and multichip packaging schemes.

In addition to providing the four basic requirements listed above, an electronic package must also function at its designed performance level while still allowing for a product that is high quality, reliable, serviceable, and economical [1.9]. The rearrangement or addition of functional features, such as upgrading the memory of a computer, is also a desirable feature of an electronic packaging technology.

1.3 PACKAGING HIERARCHY

Typical electronic systems are made up of several layers or levels of packaging, and each level of packaging has distinctive types of interconnection devices associated with it. One way in which this hierarchy of interconnection levels can be divided is as follows:

Level 0: Gate-to-gate interconnections on a monolithic silicon chip.

Level 1: Packaging of silicon chips into DIPs, SOICs, chip carriers, multichip modules, and so on, and the chip-level interconnects that join the chip to the leadframes. Occasionally, this level is skipped when TAB or COB technologies are utilized.

Level 2: PWB level of interconnection. Printed conductor paths connect the device leads of components to PWBs and to the electrical edge-connectors for off-the-board interconnection.

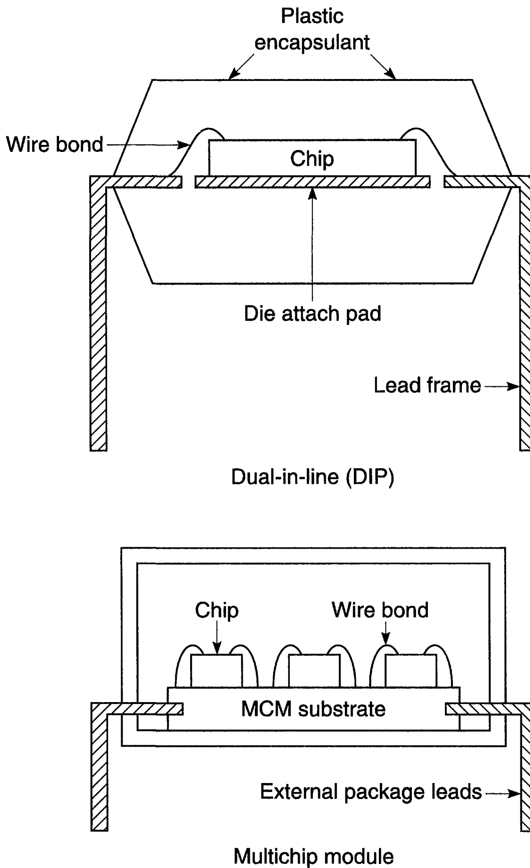


Figure 1.2 Single chip and multichip packages illustrating signal distribution, heat dissipation, power distribution, and circuit support and protection (signal and power distribution are accomplished through leads and wire bonds, heat dissipation is accomplished through leads and chip support, and support and protection are accomplished through the lead frame, substrate, and external package).

Level 3: Connections between PWBs. This may include PWB-to-PWB interconnections or card-to-motherboard interconnections.

Level 4: Connections between two subassemblies. For example, a rack or frame may hold several shelves of subassemblies that must be connected together to make up a complete system.

Level 5: Connections between physically separate systems such as host computer to terminals, computer to printer, and so on.

The various levels of interconnection are illustrated in Fig. 1.3.

Gate-to-gate interconnections categorized as level 0 are formed during IC fabrication. They will not be discussed in this text. Persons interested in learning more about this level of interconnection should consult one of the many books on IC fabrication. Likewise, levels 3 through 5 are not pertinent to multichip module packaging, so they will not be discussed either. Although not considered a part of the packaging hierarchy, die attach (or die bonding) is a crucial step in multichip module technology, so it is discussed prior to addressing levels 1 and 2.

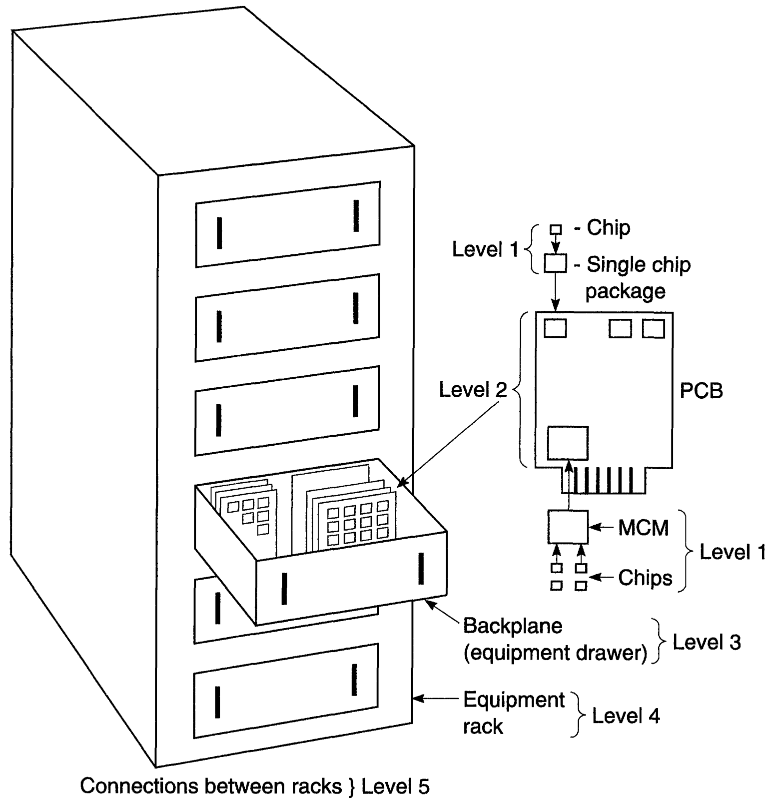


Figure 1.3 Electronic packaging hierarchy.

1.3.1 Die Attach

An IC must be mounted on a substrate or metal leadframe by a die attach material which will permit heat conduction while assuring mechanical stability. The die attach may also provide for electrical grounding if the material used to secure the chip is sufficiently conductive. The three primary types of die attach materials used are soldering (both soft and hard solders can be used) which is also referred to as eutectic bonding, metal-filled polymers (epoxies), and metal-filled glasses. Hard solders, such as a silicon/gold alloy, can present reliability problems due to mismatched thermal expansion coefficients. Soft solders generally do not suffer from this problem because they exhibit plastic flow which prevents chips from seeing high stresses. However, they can result in failure due to fatigue and creep.

Metal-filled epoxies and polyimides are another alternative for die bonding. As a general rule, they are less expensive, produce lower stress levels, and require significantly lower processing temperatures. Metal loading, generally silver, yields acceptable values of electrical and thermal conductivity although normal thermal cycling during use can cause drift in these parameters over time. Polyimides require

higher processing temperatures for complete curing, but also exhibit a higher stability at high temperatures than materials containing metal fillers.

Glass adhesives have also been used for die attach. The primary problems with glasses are the excessively high processing temperatures and the possible presence of oxidizing agents which can corrode the IC. Silver-loaded glass adhesives have been used in ceramic packages.

1.3.2 First-Level Interconnection

First-level packaging (or interconnection) refers to the technology required to get electrical signals into and out of a single transistor or integrated circuit—in other words, the connections required between the bonding pads on the IC and the pins of the package. This is generally accomplished by wire bonding, flip chip bonding, and tape automated bonding (TAB), all of which are illustrated in Fig. 1.4(*a–c*).

1.3.2.1 Wire Bonding

Wire bonding is the oldest method used for first-level interconnection and is still the dominant method used today, particularly for chips with a moderate number of I/O (i.e., $\leq$200). This technique involves connecting gold or aluminum wires between the chip bonding pads, located around the periphery of the chip, and contact points

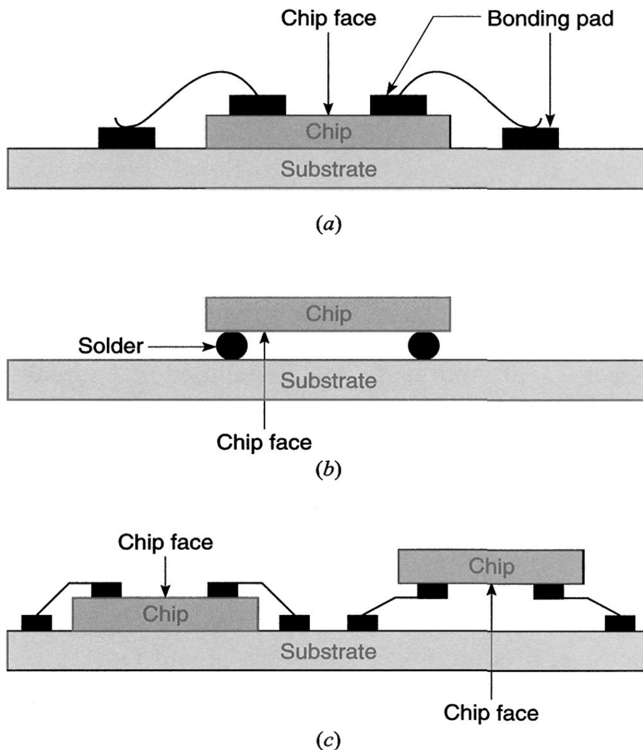


Figure 1.4 Illustrations of (*a*) wire, (*b*) flip chip, and (*c*) tape automated bonding.

on the package. Although this process has been automated for many years, it is still time consuming because each wire, requiring two bonding operations, must be attached individually. Limitations of wire bonding include the requirement for minimum spacing between adjacent bonding sites to provide sufficient room for the bonding tool, the number of bonding pads that can be located around the periphery of the chip, and signal delay and crosstalk between adjacent wires.

1.3.2.2 Flip Chip Bonding

In this interconnection technology, the chip is mounted upside-down onto a carrier, module, or PWB. Electrical connection is made by way of solder bumps much like those used in TAB, which is discussed in the next section. The solder bumps are located over the surface of the chip in a somewhat random pattern or an array so that periphery limitation, such as that encountered in wire bonding, does not limit the I/O capability. The I/O density is primarily limited by the minimum distance between adjacent bonding pads on the chip and the amount of chip area that can be dedicated to interconnection. Additionally, the interconnect distance between chip and package is minimized since bumps can essentially be located anywhere on the chip. Although this technique is attractive for use in MCM technology because chips can be located very close together, fatigue of solder joints due to thermal expansion mismatch of the chip/bond/substrate, heat removal from the back of the chip, and difficulty inspecting the solder joints after the chip has been attached to the substrate offer special challenges to the packaging specialist.

1.3.2.3 Tape Automated Bonding (TAB)

Tape automated bonding, developed in the early 1970s, is rapidly becoming a popular method for accomplishing first-level interconnection. It is most often used with chip carriers or PWBs. In this technique, ICs are first mounted on a flexible polymer tape, such as polyimide, containing repeated, flat, wide copper interconnection patterns formed lithographically from a metal laminate. Each pad on the IC is aligned to a metal interconnection stripe on the tape and attachment is effected by thermocompression bonding. All bonds are formed to the IC at the same time by a process called *gang bonding*. This is referred to as *inner lead bonding* (ILB). At this point, the IC can be tested and burned-in allowing poorly bonded or defective chips to be eliminated prior to packaging. Good chips are then *outer lead bonded* (OLB) to leadframes or PWBs using the thermocompression process. The shape of the interconnections and the use of copper with its lower resistivity results in low inductance and low resistance which minimizes signal distortion. However, TAB requires the use of complex metallurgy, multilayer solder bumps either on the tape or IC or both in order to effect a bond. Generally, the bumps utilize gold or copper as the primary constituent along with titanium or tungsten as a diffusion barrier to prevent alloying. Finally, a TAB tape can only be used for a chip and package which matches its interconnection pattern. Thus, each TAB tape is, in effect, a custom tape. However, they will continue to gain popularity for bonding chips directly to a PWB and for large chips with high I/O requirements.

1.3.3 Package Lid and Pin Sealing

Lid and pin sealing generally utilize materials that are similar or identical to those used elsewhere in packaging technology. Low melting temperature glasses are used for sealing both the lid and I/O pins in hermetic packages. Required properties of these sealing glasses include: (1) the ability to form a hermetic seal; (2) temperatures required to effect the seal must be compatible with the other materials in the package; (3) strong adherence to the materials being sealed; (4) must have a thermal coefficient of expansion compatible with the materials being sealed; and (5) the sealing glass must be electrical insulating. The primary problems encountered with glass seals are low strength and brittleness.

Metal hermetic lid seals are effected by low-melting temperature brazing, alloy soldering, or welding. Solders used for lid sealing are dictated by the temperature hierarchy of the processes that precede and follow the sealing operation, the required seal strength, and cost. It is less desirable than brazing because of its lower strength, tendency to become embrittled by intermetallic formation, and the use of fluxes. *Brazing*, which consists of reflowing a preform of a eutectic, for example Au-Sn (80-20), yields a stronger, more corrosion-resistant seal although it is a little more difficult to perform consistently. On the other hand, welding is still the most popular method of realizing high-reliability hermetic seals because of the high yield and the fact that the high-current pulses used to effect the weld produce only local heating.

1.3.4 Second-Level Interconnection

As noted above, level 2 interconnection refers to the electrical connection of an IC to a circuit board, the most common one being a conventional printed wiring board (PWB). Following level 1 interconnection, single IC chips normally undergo encapsulation in either plastic or ceramic-based packages prior to connection to a PWB. In other cases, the IC is bonded directly to a PWB either by a die attach/wire bonding scheme or using TAB. The chip is then protected by a "glob-top" encapsulant such as a topical epoxy or a silicone. This interconnection technique, referred to as Chip On Board (COB), has the advantages of reduced PWB area and cost because of the elimination of an extrinsic package. For multichip modules, second-level interconnection is the connection between a package containing multiple chips, which are interconnected by way of an imbedded conductor network in a substrate, and a PWB. However, the substrate on which the chips are mounted in a multichip module prior to being inserted into a package actually qualifies as a PWB in the broadest sense of the definition of a PWB.

1.4 A BRIEF HISTORY OF MICROELECTRONIC PACKAGING TECHNOLOGY

It is probably impossible to determine the exact date that electronic packaging began to be viewed as an engineering and science technology. However, microelectronics packaging technology began in earnest in response to the discovery of the transistor in the late 1940s, and has continued to evolve to serve the increasing complexity and

performance of integrated circuits since that time. Early transistors were of the alloy structure and were housed in plastic packages providing little in the way of protection for the device. However, once the military became interested in these new devices for high reliability applications, the need for hermeticity to prevent transistor gain degradation and junction leakage current due to contamination and moisture led to the development of the metal transistor outline (TO) package shown in Fig. 1.5. This package consists of a gold-plated metal base containing external leads (generally three or four leads for discrete transistors), commonly referred to as a header, and a metal lid which is sealed to the header by welding in an inert atmosphere, such as nitrogen or argon, to ensure that moisture and other contaminants are excluded from the ambient surrounding the electronic device.

With the development of silicon planar technology, electronic packages were developed to accommodate the large number of input/output (I/O) leads of integrated circuits. Initially ICs were merely packaged in higher pin count versions of the TO can described above, which quickly became inadequate to handle the more complex and higher I/O integrated circuits. Consequently, the 1960s saw a rapid proliferation of new packages for integrated circuits. Because of cost considerations, the lack of standards for package design, and difficulty mounting some packages onto printed wiring boards (PWBs), also referred to as printed circuit boards (PCBs), only the "flatpack" and "dual-in-line package" (DIP) survived. Examples of these two major types of integrated circuit packages are shown in Fig. 1.6. It should be noted that the flatpack leads, which extend from all four sides, are essentially planar

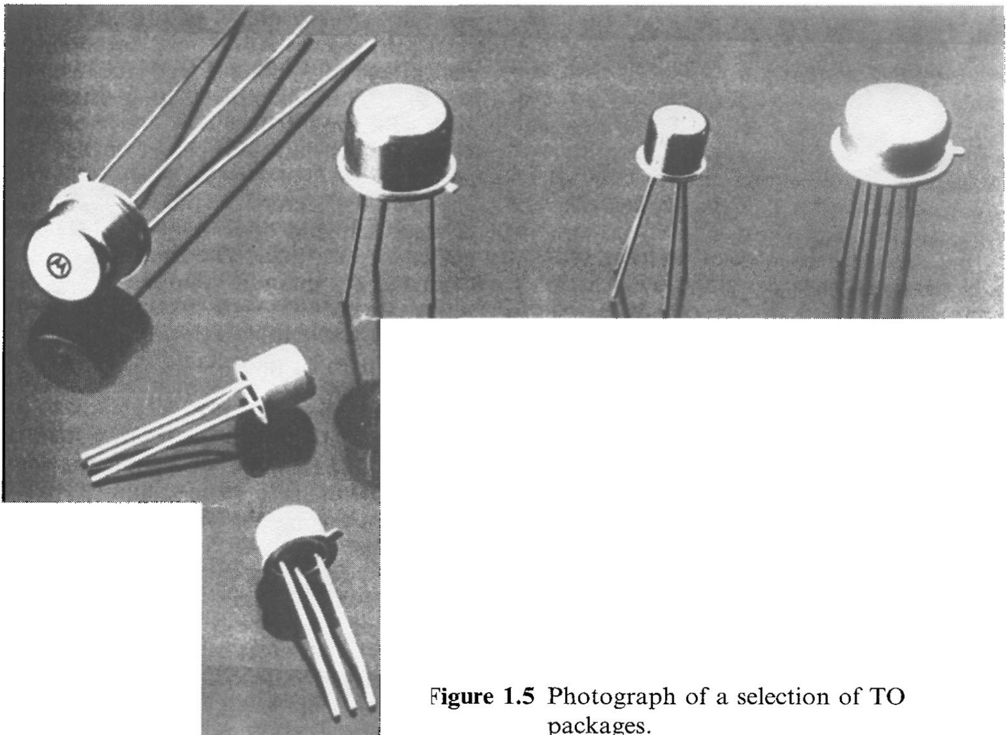


Figure 1.5 Photograph of a selection of TO packages.

with the package while those of the DIP are perpendicular to the body of the package and exit on two sides. This has some implications in terms of mounting to PWBs. In particular, the DIP is ideally suited for insertion mounting onto PWBs by way of plated-through holes (PTHs) by automatic insertion machines and wave soldering, whereas the flatpack has to be mounted using special methods and tools. Consequently, the DIP became the primary package for ICs and, along with through-hole PWBs, has long dominated the electronics assembly market.

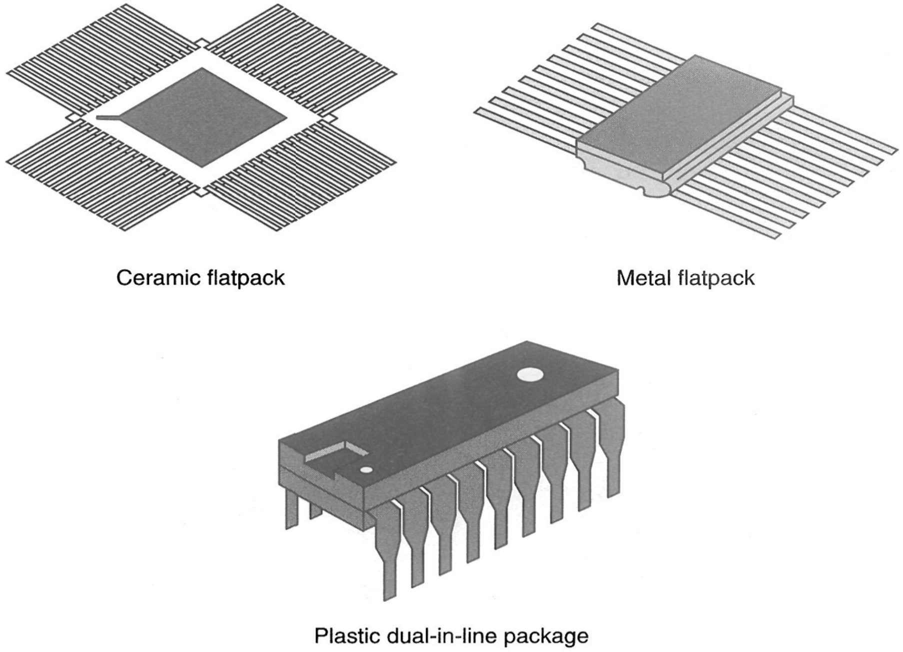


Figure 1.6 Dual-in-line and flatpack package.

Packaging costs also received considerable attention during the 1960s while the industry was deciding which package or packages would become standard. One of the early attempts to develop a low-cost, hermetic package resulted in the CerDIP which was a DIP constructed of two pieces of sandwiched ceramic with the leads protruding from between the slabs of ceramic as shown in Fig. 1.7. The two pieces of ceramic were held together using a low melting temperature glass which also acted as a seal, thereby providing hermeticity. Unfortunately, the glass used originally outgassed moisture which created reliability problems. The development of vitreous sealing glasses, which do not outgas moisture, coupled with performance of the sealing operation in a nitrogen ambient reduced the reliability problem to a tolerable level.

Driven by the need to further reduce packaging costs, the industry pursued fully automated manufacturing of plastic DIPs. The result of this effort was a low-cost plastic package which was transfer molded around an IC chip which had previously

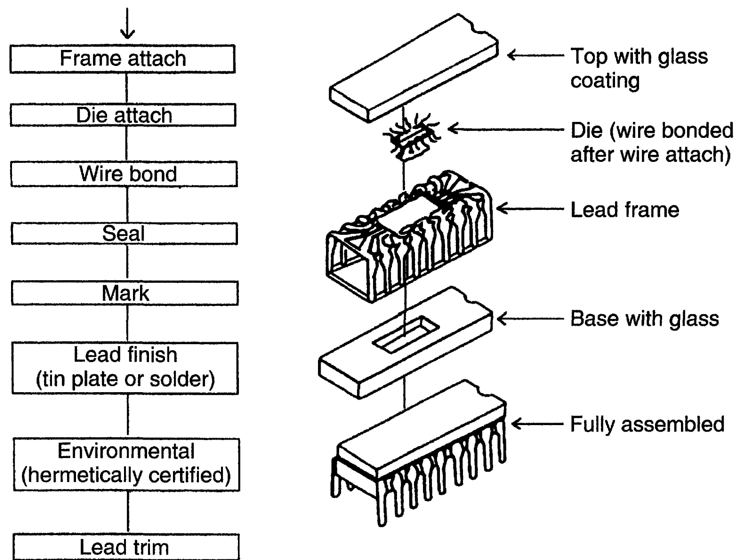


Figure 1.7 Assembly sequence for CERDIP.

been die and wire bonded to a leadframe. Unfortunately, plastics are not hermetic because of their high permeability to moisture and poor adhesion to the metal leads which provide a path for water vapor to access the IC. Furthermore, the resins and fillers either initially contained undesirable contaminants (for example, Cl and Na) or were polymerization by-products of the plastics leading to degradation of the IC. These problems were eventually resolved by improving the encapsulation applied to the chip prior to plastic packaging and improvement in the properties of the plastics themselves.

The 1970s and 1980s saw the development of several types of integrated circuit packages including surface-mount packages (SMPs), in response to a need for higher density PWBs. When mounted on a PWB, the SMP's leads do not penetrate the PWB like those of through-hole mounted packages. Thus, they can be mounted on the side of the PWB containing conductor traces. Consequently, SMPs can be mounted on both sides of a PWB. Mounting of SMPs to printed wiring boards is accomplished by reflow solder technology which gave new life to the flatpack, actually the first surface mount package. Also, small outline packages (SOPs), which resemble miniature versions of DIPS as shown in Fig. 1.8, were developed for use in surface mount technology (SMT). The two types of small outline packages are the small outline transistor (SOT) and the small outline integrated circuit (SOIC) shown in Fig. 1.9. This same period saw the development of chip carriers, quadpacks (or quad flatpacks), and pin grid arrays (PGAs). The chip carrier is available in both leadless and leaded versions, as well as, with plastic and ceramic bodies (see Fig. 1.10). These type packages conform very closely to the size of the ICs they contain and have leads on all four sides. The quadpack, one of the earliest plastic surface mount IC packages, comes in a variety of sizes and lead configurations, and also has leads on all four sides as shown in Fig. 1.11. Thus, the quadpack (I/O $\approx$ 200) is generally used when the chip I/O requirements are greater than can be addressed

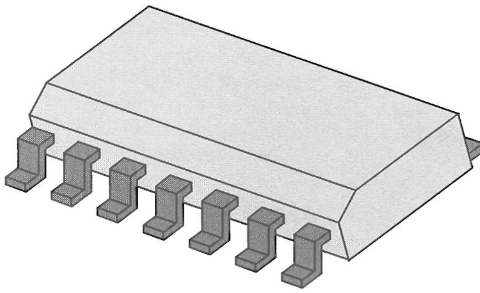


Figure 1.8 Small outline package (SOP).

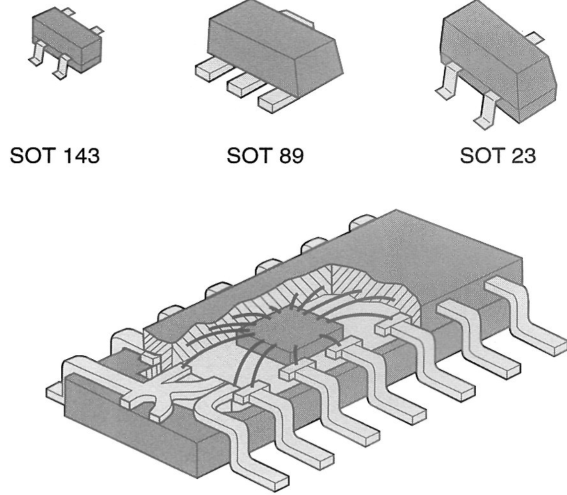
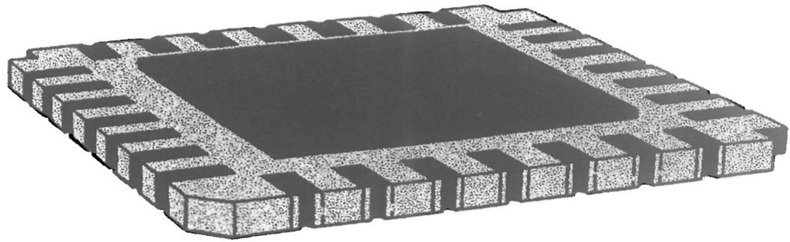


Figure 1.9 Small outline transistor (SOT) and small outline integrated circuit (SOIC) packages.



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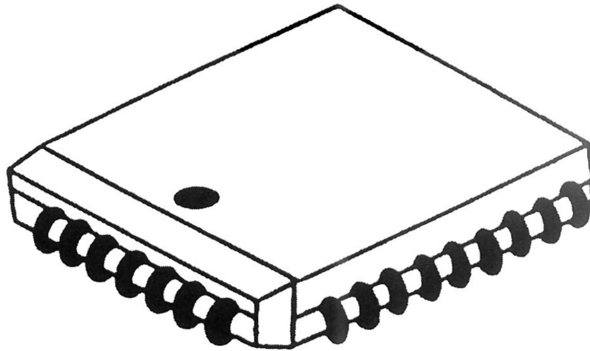

(*b*)

Figure 1.10 (*a*) Ceramic leadless chip carrier and (*b*) plastic leaded chip carrier.

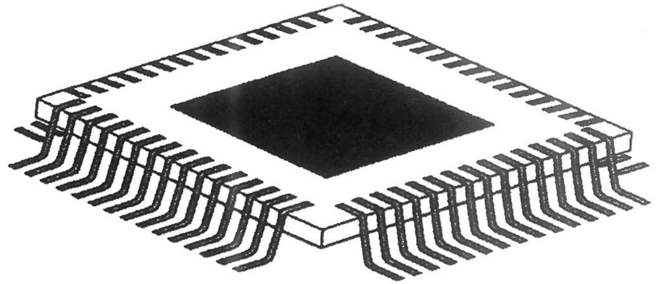

Figure 1.11 Quad flatpack (or quadpack).

using a DIP (I/O $\approx$ 64). Similarly, the PGA package (I/O $\approx$ 600), illustrated in Fig. 1.12, is used when the I/O requirement is higher than that provided by quadpacks.

There always has been and will continue to be motivation to pack more electronic functionality and higher speed performance into a smaller volume of space. Packaging of ICs is one area which offers attractive benefits for reducing size and improving performance by either eliminating the package or reducing the size to the point where it takes up very little more space than the IC. Elimination of the package [i.e., direct chip attach (DCA)] still presents some problems where full functionality and reliability testing are concerned. In other words, the ability to test and burn-in bare die has not yet reached the quality and reliability levels comparable to the same die in a package. Consequently, packaging ICs for testing and burn-in is still very attractive. The most recent approach to packaging, which is still under development, is referred to as chip scale or chip size packaging (CSP) [1.10–1.13]. CSPs are essentially "packages" that ruggedize the IC for ease of handling, testing, and assembly. Thus, CSPs are a viable substitute for "known good die" (KGD) if low-cost test and burn-in methods are not available for bare die [1.13]. CSPs, also referred to as slightly larger than IC carrier (SLICC), are generally defined as packages that are equal to or smaller than 1.2 times the bare die size. Micro-ball grid array, mini-ball grid array, and micro-SMT packages fit this definition since they are of minimum size and employ direct surface mounting instead of wire bonds. CSPs are designed to be flip chip mounted using conventional equipment and solder reflow. Essentially, CSPs take advantage of the attributes of a flip chip in a surface mountable package. The primary difference is the material layers, which serve as compliant members, space transformers, and mechanical protection, between the silicon and the bump array. These material layers also serve to categorize the CSPs into tape carrier, resin mold, ceramic carrier, and lead-on-chip (LOC) types. Thus, CSPs offer a method for subjecting ICs to full functional and reliability testing using a packaging technology while essentially maintaining the size and performance of bare die.

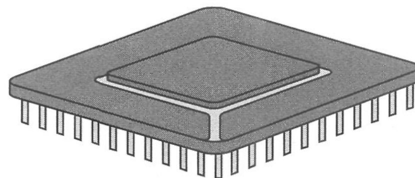

Figure 1.12 Pin grid array package.

The ultimate goal for high performance electronic systems is generally to pack devices as close together as possible in order to minimize circuit path length. In response to this need, the past few years have also seen the emergence of ball grid array (BGA) packages as a replacement for quad flatpacks (QFPs), primarily because of their high I/O density, minimum footprint, and shorter electrical paths which means that they have better electrical performance. For QFPs, lead counts higher than 200 require lead spacings of 0.5 mm, and for 300 leads, the spacing approaches 0.3 mm. Unfortunately, as spacings become tighter, the yield falls exponentially with lead spacing. For I/Os greater than 250, the BGA has an advantage over the QFP in that it always occupies less space than a QFP. However, BGA construction is inherently more expensive than that of the QFP because of costs associated with the component carrier substrate, although the cost should decrease as the production volume increases. The cost may never drop to those of QFPs, but a good assembly yield could offset some of the package cost.

The BGA package has evolved from flip chip technology, also referred to as controlled collapse chip connect (C4) for ICs [1.14–1.21]. Thus, the BGA package can be identified by the solder bumps on the bottom of the package. The solder bumps can be arranged in a uniform full matrix array (i.e., over the entire bottom surface), a staggered full array, or around the perimeter in a multiple number of rows (see Fig. 1.13). No matter how the bumps are arranged, the result is a smaller footprint than that of conventional packages. As noted previously, for a given amount of real estate, the BGA package provides more I/O than quad flatpacks

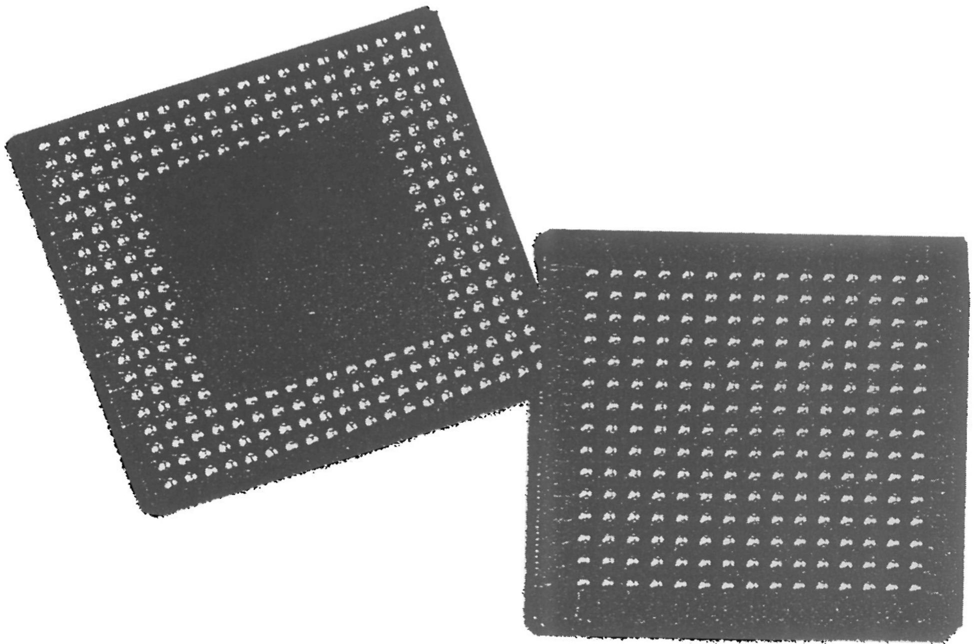

Figure 1.13 Examples of full matrix and perimeter array BGA I/O solder bumps.

(QFPs). Thus, the BGA package is considered the package of choice for high-density and high I/O ICs and, since high chip density MCMs often require high I/O, the BGA appears to be a natural package selection for MCMs.

As is the case with other packages, BGAs have been broadly classified according to the type and form of the die carrier substrate material. Thus, the packages have been classified as CBGAs (ceramic), CCGAs (ceramic column), PBGAs (plastic), MBGAs (metal), and TBGAs (tape). These packages, some of which are conceptually illustrated in Fig. 1.14, can house either a single chip or multiple chips.

As noted previously, one of the big advantages of BGA packages is that they offer high I/O. At the present time, 400 I/O PBGAs, 736 I/O TBGAs, and 625 I/O CBGAs are available. Ceramic column GAs are available with I/Os greater than 1000. Current and planned designs have solder-bump-array pitches in the range of 0.030 to 0.060 in. (0.75 to 1.5 mm). The solder bumps are generally of tin/lead or tin/lead/silver composition. Thus, the BGA is a leadless package that is not susceptible to bent or skewed leads which means that it can be easily handled. However, there are some aspects of BGA packages of concern. In particular, solder joint defects,

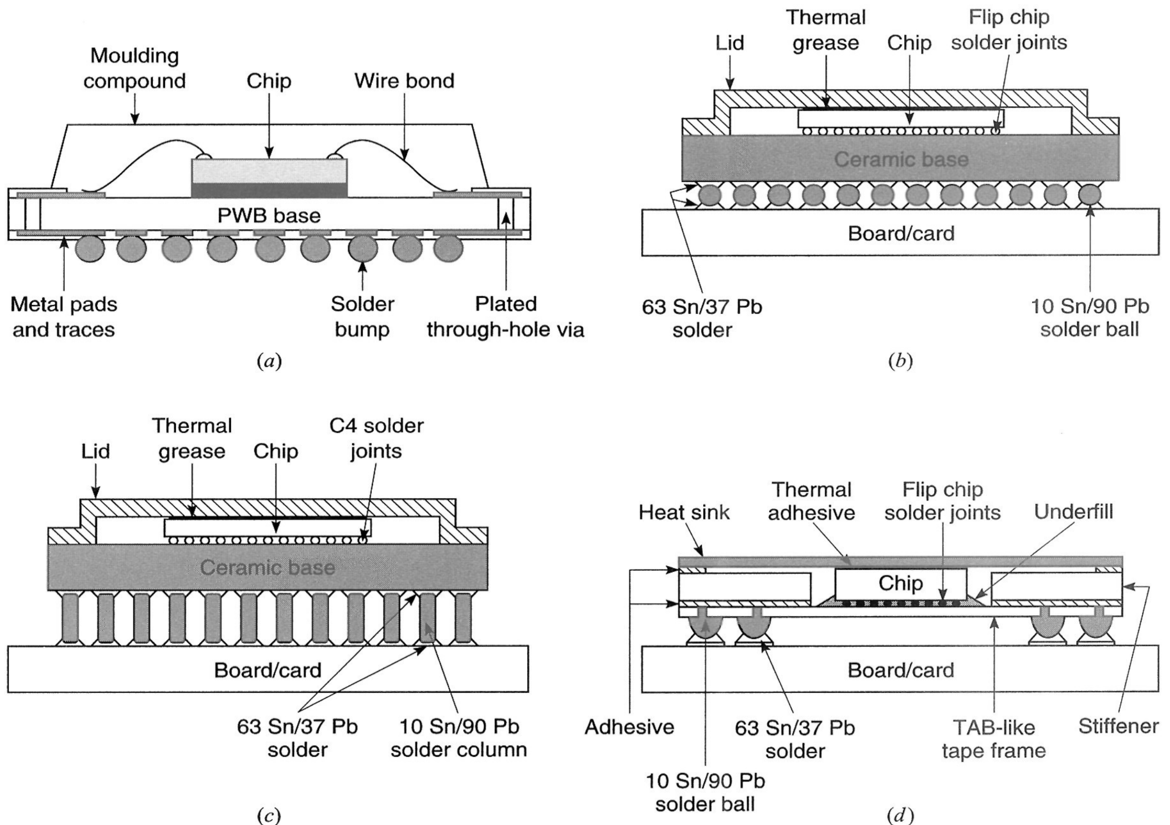

Figure 1.14 Conceptual sketch of (*a*) plastic ball grid array, (*b*) ceramic ball grid array, (*c*) ceramic column grid array, and (*d*) tape ball grid array.

warpage during reflow, large variation in solder ball size, the inability to visually inspect the solder joints, and problems associated with rework. These can be overcome with good design, process development, and process control so that the resulting yield makes inspection and rework of minor importance. Considering all the pluses and minuses, BGA still appears to be the surface mount package of the future for both single chip and multichip module (MCM) packaging.

The 1980s also marked the turning point in the way electronic engineers viewed IC packaging technology. As noted previously, for many years the electronics industry had been concentrating on increasing the performance of integrated circuits (i.e., more circuitry/silicon area operating at higher speeds) with little consideration of the fact that ICs in an electronic system must communicate with each other through the packages which contain them. As a result of the trend toward higher circuit densities and operating speeds on a chip, the following effects became important considerations for packaging engineers.

- I/O requirements increased sharply.
- Signal transition time between chips became a factor limiting system speed.
- Signal integrity between silicon chips degraded.
- Power requirements per chip increased.
- A problem with heat dissipation was created.

All of these factors forced electronic packaging technology into the spotlight resulting in a reconsideration of how ICs were being packaged. From this reconsideration evolved multichip module (MCM) packaging technology, examples of which are shown in Fig. 1.15. Although the basic concept of a multichip module was not new (hybrid circuits had been around for nearly 50 years), interest was renewed in mounting a multiple number of ICs in a single package in order to take advantage of inherently shorter interconnection distances between ICs. Thus, the development of cost-effective and highly reliable MCM technology has become the latest industry effort to push the performance of electronic systems to higher and higher levels.

1.5 DRIVING FORCES ON PACKAGING TECHNOLOGY

Historically, packaging has always been a substantial fraction of the price of an IC (10%–50%), and consequently, reducing packaging costs while maintaining reliability and performance has been the focus of packaging engineers for many years [1.22]. During this time, IC technology has transitioned from small-scale integration (SSI) in the 1960s to submicron minimum dimension very-large-scale integration (VLSI) at the present time. Since packaging technology has not enjoyed anywhere near the performance advancement of ICs over the past 30 years, electronic system performance has become increasingly limited by IC packages. Thus, design decisions facing packaging engineers today are becoming increasingly driven by system performance for a market which is still very cost conscious.

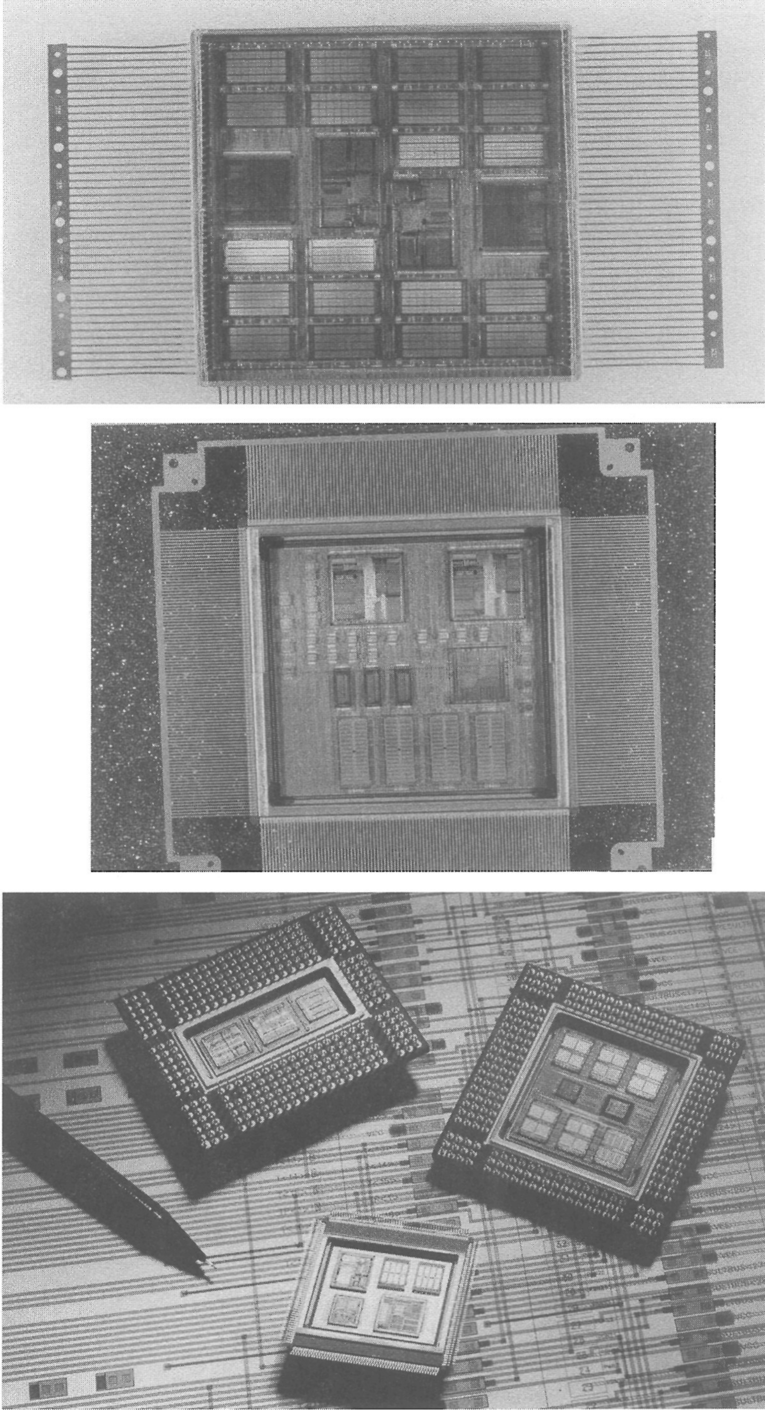

Figure 1.15 MCM packages (courtesy of nCHIP).

Given that cost and performance are the primary concerns in electronic packaging, it is important to examine the factors which relate performance and cost to packaging technology choices. Some factors which must be considered are manufacturability, reliability, serviceability, size, weight, signal integrity, mechanical stability, and power consumption with its accompanying heat dissipation problem [1.23]. In general, packaging costs are driven by materials and fabrication requirements associated with actual manufacturing and by testing and rework associated with manufacturability. In the case of MCMs, manufacturing costs include the cost of the IC chips, generally referred to as "known good die." On the other hand, performance is a function of electrical, thermal, and mechanical design constraints, material selection, and fabrication limitations. A few of these cost/performance factors, treated in detail in later chapters, are briefly discussed below.

1.5.1 Manufacturing Costs

As noted previously, manufacturing costs include all the materials and fabrication steps required to produce each packaged IC including the cost of the IC itself. The materials include not only the actual material that goes into the package, but also materials such as chemicals, required to process the material which ultimately is part of the package. Manufacturing costs vary widely for packaging and interconnection elements, as can be seen in Table 1.1. It should be noted that high pin count PGAs, high layer count ceramic MCMs, and thin film MCMs are significantly more expensive to manufacture than are plastic packages, PWBs, and laminate MCMs.

TABLE 1.1 Packaging Costs (from [1.25])

Packaging Type	Typical Cost
Plastic package	\$0.05–\$5.00
Ceramic PGA < 144 pins	\$5,000 NRE + \$0.10 per pin (\$14.00 or more for 144 pins)
Ceramic PGA > 144 pins	\$25,000 NRE + \$0.10 per pin (\$50.00 or more for 500 pins)
Cofired ceramic MCM	\$3.00/in^2/layer (\$10.00/in^2 for 10 layers)
Thin film MCM	\$60.00/in^2 (expected to decrease to \$20.00)
Laminate MCM	\$3.00–\$5.00/in^2
PWB	< \$1.00/in^2
CMOS chip wafers	\$25.00–\$150.00/in^2

1.5.2 Manufacturability Costs

Manufacturability costs, because they are generally associated with how well the product was designed for manufacturability, are incurred as a result of testing, reworking when possible, retesting after rework, and fabrication yield loss. Since

testing is, at the present time, the only way to ensure full functionality and high reliability for both single chip and multichip packaged parts, packaging technology should provide for full testing of the finished product. Furthermore, since the final yield can be increased above initial yield by reworking some of the parts which fail initial testing, it is important that packaging technology also allow for an inexpensive and easy rework process. Although chips usually cannot be repaired, such is not the case for MCMs. Reworking MCMs, which generally refers to the replacement of a chip or chips within the module, is an important cost issue because rework costs are generally high. Consequently, high value chips should be thoroughly tested prior to mounting in an MCM.

1.5.3 Size and Weight

Because of the many environments in which packaged electronic systems must operate, size and weight are often considered performance goals. Restrictions placed on these two physical parameters may be the result of personal preferences or system requirements. For example, weight may be a critical factor if the system is to operate in a satellite or a portable computer. Size (either area or volume or some combination of the two) may be critical in applications such as calculators and cellular phones. Most important, specifying these parameters can impact other design aspects of the electronic package such as material specifications and cooling requirements.

1.5.4 Electrical Design

As noted previously, the on-chip switching speeds of ICs are continuously increasing. Furthermore, noise margins are generally decreasing at the same time. Unfortunately, chip I/O count and interconnection speed have not kept pace so that packaging interconnects now play a dominant and limiting role in determining overall system performance. Each lead from the chip to the package and each package lead to the outside world has some parasitic capacitance, resistance, and inductance that limits switching speed, distorts the shape of signals passing through it, and serves as a source of electrical noise. These leads are also a source of reliability problems. Likewise, the pattern of metal and dielectric that forms the circuitry between chips and from chips to the outside world of an MCM contribute to the degradation of electrical performance. Consequently, some electrical design factors which must be considered include signal lead length (short parallel runs to minimize mutual inductance and crosstalk, and short runs near ground planes to minimize capacitive loading), use of matched impedances to avoid signal reflection, low ground resistance for minimum power supply voltage drop, and power supply spiking caused by signal lines switching simultaneously. All of these factors are functions of geometries and materials.

1.5.5 Thermal Design

The primary objective of thermal design is to remove heat from the junctions of ICs to ensure that they operate properly and to avoid triggering temperature-

activated failure mechanisms. This is generally accomplished by conducting the heat away from the chips and into a gas or liquid coolant. Although the power dissipation per gate of ICs has decreased in recent years, the power dissipation per chip has increased during the same time since power per gate scales linearly with feature size, while on-chip circuit power density increases as the square of the feature size reduction ratio. Even CMOS circuit densities and operating frequencies are becoming great enough that thermal design cannot be ignored when packaging these chips.

Thermal issues are even more significant in MCM design because the heat density is generally high as a result of closely spaced, high-density, high-performance chips. Consequently, thermal design of MCM packages must consider such factors as: (1) how heat is to be removed from the IC (through the substrate or directly off the backside of the chip); (2) whether to use forced air or liquid cooling (forced air is generally much cheaper and the system is more likely to survive a fan failure than a pump failure); (3) the use of a high thermal conductivity substrate (high thermal conductivity usually implies a high dielectric constant, diamond being an exception) or thermal *vias* which can consume a large area of the substrate thereby reducing interconnect capacity; and (4) stresses induced in the chips and substrate due to mismatches in thermal coefficients of expansion (TCEs). A thermal via is a special heat conductor patch that is intentionally inserted into and passes through a material which is a poor conductor of heat. All of these considerations impact performance, cost, and reliability.

1.5.6 Mechanical Design

In the previous section, it was noted that mismatches in thermal coefficients of expansion cause stresses to be induced in ICs, MCM substrates, and packages of an electronic system as the temperature changes. Such stresses can be very localized, for example, under a small portion of a chip, or universal such as across an entire layer of an MCM substrate. Thus, the mechanical design aspect of electronic packaging technology is, in general, closely related to changes in temperature. Another mechanical property that may need to be considered is stiffness, characterized by the tensile modulus (E), which is important in areas such as chip attach where three materials (chip, substrate or package, and adhesive) form two interfaces. Thermal stresses increase with increasing E and decreasing thickness of the adhesive layer. Thus, for example, a thin layer of high E adhesive material should only be used with large area chips if the TCE of the substrate or package closely matches that of the chip.

1.5.7 Manufacturability

No matter how much effort and preciseness goes into the design of an electronic package, ultimately high-quality packages must be manufacturable in sufficient quantities to allow for competitive pricing. Successful manufacturing depends on many factors such as the availability of materials, process technologies, and automated fabrication equipment at acceptable costs, cost of piece parts, manufacturing yield, manufacturing cycle time, and repairability. Design specifications must not overly challenge fabrication technology, because the limitations of fabrication pro-

cesses and equipment for any microelectronic technology essentially establish the ultimate capability of the technology. Although zero-defect manufacturing is possible, it is not realistic because of high costs and possible loss of competitive edge due to conservative dimensions, tolerances, materials, and process choices which would all impact performance in a negative way. Thus, the alternative is to balance the above noted variables against loss of products due to defects, which must be screened out by testing.

Although MCMs offer significant benefits in terms of greater densities, smaller size, and better performance, implementing this technology requires significant changes in design and manufacturing methodologies, fabrication processes, and equipment. Manufacturers have, to some degree, avoided making these changes by "pushing" conventional technologies to achieve higher density/performance levels. MCM technology will continue to offer challenges to manufacturing that are somewhat unique, and thus, will continue to require the development of new materials, new processing technologies, and specialized fabrication equipment.

1.5.8 Testability

A primary motivation for testing is to find and eliminate manufacturing-induced defects. Other reasons for testing include the need to prove a new design, to verify that manufacturing processes are under control, and to predict product performance under normal operating conditions. Generally, testing can be divided into two broad categories: *in-process* and *stress* testing. In-process testing is nondestructive and is used to screen for defects that occur as a result of manufacturing and prevent the product from ever operating properly. Such testing can be performed at almost any stage of the fabrication process. At every testing point, factors to consider include testing costs, investment in the product to the point of test, and the scrap and possible repair costs. On the other hand, stress testing, which is often destructive to the product, is most frequently performed on the finished product to evaluate long-term reliability. Thus, stress testing finds product defects that do not initially prevent the product from operating, but do so later. The results of both types of testing are used as feedback to improve both product design and manufacturing.

MCM packages must be subjected to the same test requirements as the single chip packages they replace. However, MCMs present unique challenges in testing compared to single chip packages because of their unique structure. The usual approach to MCM testing is to perform separate testing of the substrate on which the chips are to be mounted and interconnected, the ICs prior to mounting on the substrate, and the assembled module prior to sealing in case rework is required. Since the completed MCM is a complex electrical system which must be tested as a single unit, electrical testability must be integrated into the MCM package design. At the present time, not all of the problems associated with assembled MCM testing have been solved.

1.5.9 Reliability

In recent years, highly reliable products have become commonplace in the electronics industry. Consequently, sustained success in this market has depended

on a company's ability to provide superior products that are reliable. Reliability assurance is tied very closely to thorough product testing. However, consistently high product reliability requires the interaction of product design, manufacturing, and testing. When properly performed and integrated, these three functions produce a reliable product. At the system level, reliability is highly dependent on the failure rate of its component parts. Thus, in the case of MCMs, reliability of the final module is the combined result of the reliabilities of each of its components, pointing out the need to thoroughly in-process test the substrate, ICs, and assembled module, and then stress test the functional modules.

1.5.10 Serviceability

Serviceability of a product refers to the demand placed on it by the need to replace failed components. For MCMs containing expensive ICs, this capability may be important when failure of a module is a result of chip failure. Given that rework costs are lower than the price of a new module, the design of the module must allow for chip replacement. Factors which impact this capability are chip spacing, method and material used to attach the die, and method and material used for electrical interconnects. In many cases, the design of this capability into the product may be in complete opposition to the performance criteria, for example, when close spacing of the ICs is extremely important.

1.5.11 Material Selection

Packaging materials play critical roles in the proper functioning of a packaged electronic system [1.24]. For example, metals provide the means for conducting signals throughout the system via thin film conductors, wires, contacts, vias, etc. On the other hand, insulating materials are used to prevent loss of signal currents by confining them to the metal paths. Other materials are used to provide physical and structural support. Finally, there are materials whose primary function is to protect the system from the environment.

The packaging industry is concerned with the electrical, mechanical, thermal, chemical, and physical performance of all materials that are used in electronic packages. Table 1.2 lists some specific material properties in each of these areas that impact the fabrication, performance, and reliability of electronic packages. Because of the wide variation in these properties, material selection for electronic packaging technology is not an easy task. As is generally the case throughout the microelectronics industry, the final choice of a material for a specific application most likely results from a series of compromises or trade-offs aimed at achieving and/or optimizing one or more performance criteria. For MCMs, the selection of materials can be a particularly challenging task because of their complex multi-layered structure.

TABLE 1.2 Material Properties of Importance in MCM Technology

Electrical Properties	Thermal Properties	Mechanical Properties	Physical Properties	Chemical Properties
Dielectric constant (ε_r)	Coefficient of thermal expansion (CTE) (ppm/°C)	Young's modulus (E) (GPa of kpsi)	Microstructure (grain size)	Metal oxidation
Loss tangent (tan δ)	Decomposition temperature	Poisson's ratio (ν)	Flatness and planarization	Metal migration
Resistivity (Ω-cm) volume surface	Melting point	Stress (dynes/cm^2) Shear strength (MPa)	Viscosity (poise)	Reactivity
Dielectric strength (V/cm)	Glass transition temperature (T_g)	Curing temperature	Hermeticity	Adhesion
Temperature coefficient of resistance (Ω-cm/°C)	Thermal conductivity (W/m·K)	Glass transition temperature (T_g)	Melting point	Toxicity
	Shrinkage Curing temperature Thermal stability	Dimensional stability Tensile strength (GPa) Flexural strength (GPa)	Eutectic temperature Density (g/cm^3) Glass transition temperature (T_g)	Environmental
	Temperature coefficient of resistance (Ω-cm/°C)	Adhesion strength	Hardness (Brinell)	
		Peel strength		
		Ductility		
		Maleability		
		Interface energy		

1.6 MCM DEFINITIONS AND CLASSIFICATIONS

The simplest definition of a multichip module (MCM) is that of a single electronic package containing more than one IC [1.25]. Based on this simple definition, an MCM combines high performance ICs with a custom-designed common substrate structure which provides mechanical support for the chips and multiple layers of conductors to interconnect them. This arrangement takes better advantage of the performance of the ICs than does interconnecting individually packaged ICs because the interconnect length is much shorter. The really unique feature of MCMs is the complex substrate structure which is fabricated using multilayer ceramics, polymers, silicon, metals, glass-ceramics, laminates, etc. Thus, multichip modules are not really new. They have been in existence since the first multichip hybrid circuit was fabricated. Conventional PWBs utilizing *chip-on-board* (COB), a technique where ICs are mounted and wire-bonded directly to the board, have also existed for some time. However, if *packaging efficiency* (also called silicon density), defined as the percentage of area on an interconnecting substrate that is occupied by silicon ICs, is the guideline used to define an MCM, then many hybrid and COB structures with less than 30% silicon density do not qualify as MCMs. In combination with packaging efficiency, a minimum of four conductive layers and 100 I/O leads has also been suggested as criteria for MCM classification. A packaging density analysis, based on the ratio of silicon chip area to package area, yielded the graph shown in Fig. 1.16. It has been suggested that this graph could be used as the basis for an improved MCM definition.

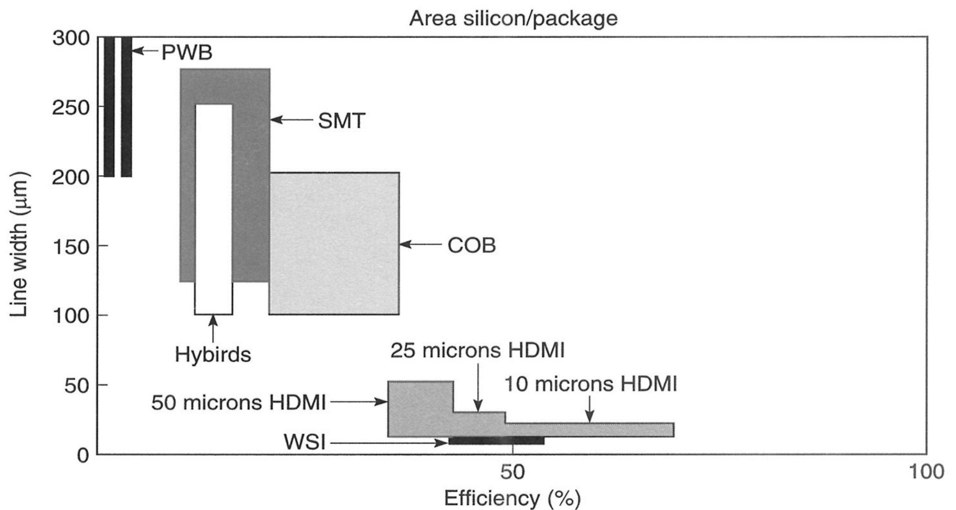

Figure 1.16 Packaging efficiency (from Reche [1.28]).

A formal definition of MCMs has been established by the Institute for Interconnecting and Packaging Electronic Circuits (IPC) [1.26–1.27]. They defined three primary categories of MCMs, illustrated in Fig. 1.17, which are designated as MCM-L, MCM-C, and MCM-D.

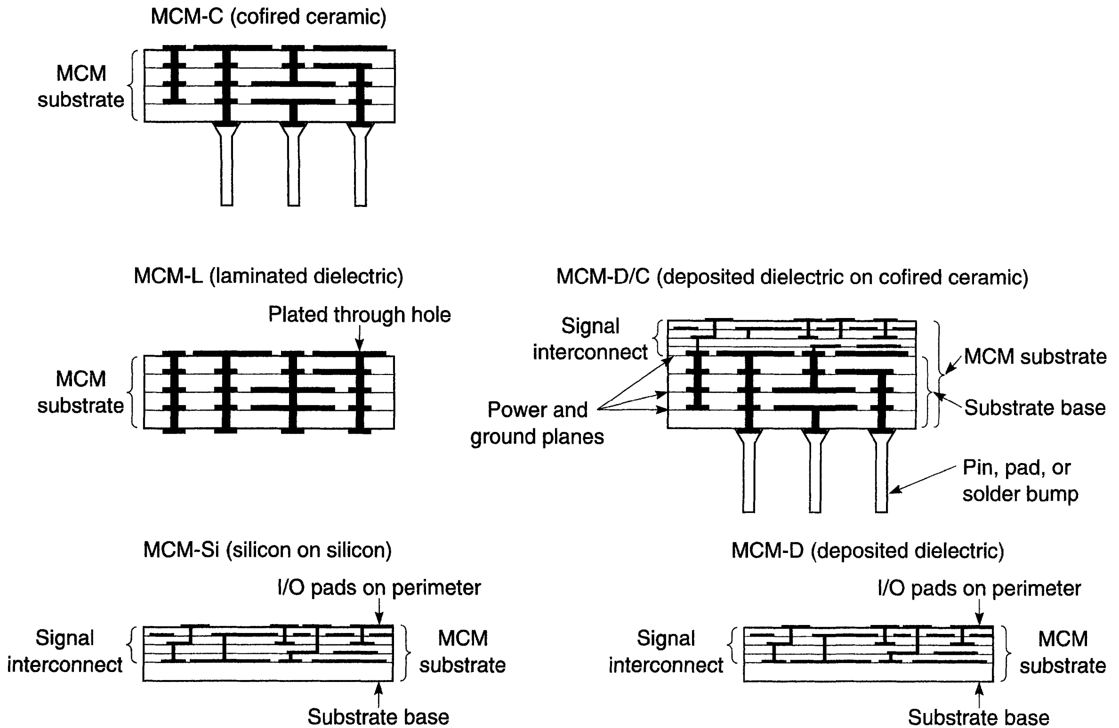

Figure 1.17 Illustrations of common MCM structures (from [1.26]).

- MCM-L: Modules which are constructed of plastic laminate-based dielectrics and copper conductors utilizing advanced forms of printed wiring board (PWB) technologies to form the copper interconnects and vias. They are commonly called "laminate MCMs."
- MCM-C: Modules which are constructed on cofired ceramic or glass-ceramic substrates using thick film (screen printing) technologies to form the conductor patterns using fireable metals. The term "cofired" implies that the conductors and ceramic are heated at the same time. These are also called thick film MCMs.
- MCM-D: Modules which are formed by the deposition of thin film metals on dielectrics, which may be polymers or inorganic dielectrics. These are commonly called thin film MCMs.

It is important to note that these are simple definitions. Consequently, many IC packaging schemes, which technically do not meet the criteria of any of the three simple definitions may incorrectly be referred to as MCMs. However, when these simple definitions are combined with the concept of packaging efficiency, chip population, and I/O density, there is less confusion about what really constitutes an MCM. The fundamental (or basic) intent of MCM technology is to provide an extremely dense conductor matrix for the interconnection of bare IC chips.

Consequently, some companies have designated their MCM products as *High Density Interconnect* (HDI) modules [1.28].

From the above definitions, it should be obvious that MCM-Cs are descended from classical hybrid technology, and MCM-Ls are essentially highly sophisticated printed circuit boards, a technology which has been around for over 40 years. On the other hand, MCM-Ds are the result of manufacturing technologies that draw heavily from the semiconductor industry. It is obvious from the title that the focus of this book is MCMs, and more specifically MCM-Ds. However, much of the material presented is equally relevant to all MCM technologies, and to some degree, electronic packaging in general. Thus, the remainder of this chapter will be devoted to brief descriptions of the three MCM technologies, and further delineation of differences in their construction and performance. Advantages, disadvantages, and prospects for the future of each technology will also be noted.

1.6.1 MCM-L

This technology is easily understood by those familiar with conventional PWB technology that has been around for nearly 50 years. MCM-L structures are essentially laminated PWBs that have been scaled to meet the requirements and dimensions of multichip modules [1.29–1.31]. Although there is some variation in manufacturing methods, most follow the basic processing technology developed for conventional PWBs. Organic materials, such as epoxy-glass, on which copper conductors have been formed on one or both sides using photolithographic definition, copper cladding, and copper plating (using either additive or subtractive processing), are laminated together to form the substrate on which the ICs are mounted and through which they are interconnected. The number of these laminates needed for a particular module is determined by the required chip interconnect density. Electrical contact between the various layers of copper interconnections is provided by vias that are drilled prior to final lamination. Following lamination, the vias are plated to provide electrical connection between the different layers of the PWB. The PWB is then populated with bare ICs, mounted directly onto the PWB (commonly referred to as COB), instead of individually packaged devices as is generally done in conventional PWB technology.

The greatest advantage that MCM-L has over the other two technologies is low cost as a result of an existing infrastructure for high volume production. High volume production is realized through large process units, parallel processing, and the ability to pattern both sides of a double clad laminate simultaneously. Generally, laminates are fabricated in large panels from which individual module substrates are cut. *Parallel processing* means that substrate yields can be high because the layers that ultimately make up the substrate are fabricated and inspected (or tested) prior to final lamination into a multilayer unit. Thus, a layer containing a defect can be reworked or discarded instead of being incorporated into a completed module. Other advantages are high electrical conductivity interconnects and intermediate values of dielectric constant.

MCM-L also has some major disadvantages such as low routing density, poor thermal conductivity through the substrate, a high CTE, high crosstalk, and moisture sensitivity. Elimination of these problems will require the development of new

dielectric materials, the use of thinner dielectric layers, and the ability to create smaller vias. Fortunately, all of these problems are presently being addressed and the efforts should yield improvement in the performance of MCM-Ls in the near future.

1.6.2 MCM-C

MCM-C technology has, as a foundation, many years of experience with hybrid circuit technology [1.32–1.33] which utilizes ceramics, usually alumina, for the substrate and multiple thick film layers of screen-printed conductor inks (or pastes) in combination with dielectrics to provide the signal interconnections [1.34–1.40]. MCM-Cs may be considered as nothing more than more complex extensions of this earlier technology.

There are three ceramic-based technologies that can be classified as MCM-Cs. These are thick film multilayer (TFM), high temperature cofired ceramic (HTCC), and low temperature cofired ceramic (LTCC). Each of these is discussed in the following sections.

1.6.2.1 Thick Film Multilayer (TFM)

As noted above, thick film technology, historically referred to as hybrid circuit technology, utilizes inks (or pastes), consisting of some combination of metal or dielectric powder, vitreous or oxide powder, and organic binders, which are screen printed onto ceramic substrates. This technique can be used to form conductors, resistors, capacitors, and inductors depending on the properties of the ink. Following application to the substrate, the inks must be properly dried and fired in order to realize their final property values. Because of the higher interconnect density requirements of MCMs, multiple levels of conductors and via fill must be formed one layer at a time, separated by dielectric material, which may consist of multiple layers deposited one layer at a time. Thus, this technology requires a supporting substrate and fabrication of the interconnects occurs in a serial fashion, requiring a large number of processing steps which adds to its cost. Additionally, the substrates generally suffer from poor planarity, so dielectric layer thickness control using screen printing is difficult. However, the tooling costs for initial pieces is low and dimensional control is quite good. The future of this technology lies with reducing the pitch of conductor traces and the development of dielectric materials with lower dielectric constants.

1.6.2.2 High Temperature Cofired Ceramic (HTCC)

Cofired ceramic technologies are merely variations of TFM technology and were developed to increase packaging density by building individual conductor/dielectric layers and then laminating them by firing at high temperatures ($\approx 1600\,^{\circ}$C) under pressure. The individual layers are formed by screen printing conductor material onto sheets of dielectric tape, called green tape, formed by doctor blading from a slurry mixture of alumina, glass, and organics. Vias are formed by punching and filling with a conductive material prior to screen printing the conduc-

tor traces. After the requisite number of sheets are prepared to provide for the circuit interconnect, they are stacked, aligned, and laminated together under pressure and temperature. Because of the high firing temperature, only low conductivity refractory metals such as tungsten and molymanganese can be used as conductors.

HTCC is a relatively low cost, high density interconnect technology. Both the processing and material technologies are mature. A finished module can have an almost unlimited number of layers, has good thermal conductivity, and exhibits low dielectric loss at high frequencies. On the other hand, it suffers from size shrinkage due to firing, a high dielectric constant, and a poor CTE match to silicon. Recent applications of this technology depend on the reduction of conductor trace pitch, dielectric material with a lower dielectric constant, and a better CTE match to silicon.

1.6.2.3 Low Temperature Cofired Ceramic (LTCC)

Because of the necessity of using low conductivity refractory metals in HTCC packaging, development efforts have led to LTCC packaging which combines the advantages of the cofired process (dielectric tape) with standard thick film conductor materials which have significantly higher electrical conductivities. In this case, dielectric and conductor materials were borrowed from TFM technology so that the lamination firing temperature can be reduced to around 850 °C. This lower temperature allows the use of much higher conductivity interconnects, such as gold, silver, and copper.

The same green tape used in LTCC packaging has also been utilized in TFM technology by replacing multiple screen printings with a single layer of cast tape in a process referred to as *Tape Transfer* (TTRAN). In this process, sheets of dielectric tape are laminated to alumina substrates. This approach reduces the number of processing steps because the dielectric layer is provided by one layer of tape while several screen printings are required to produce an equivalent thickness using conventional processing. Thus, the use of tape reduces processing costs and has been shown to be a higher yield process for TFM technology, but it is a more costly process than cofired multilayer ceramic.

The biggest advantage that LTCC has is high conductivity interconnects. Also, because the dielectric substrate material is either an alumina-filled glass or a crystallizable-ceramic, broad dielectric constant and TCE ranges are available. On the negative side, the dielectric tape shrinks upon firing and its thermal conductivity, although better than that of TFM and MCM-D, is about one-tenth that of HTCC. Thus, future developments must focus on the development of dielectric materials which will reduce or eliminate shrinkage and improved thermal conductivity.

1.6.3 MCM-D

MCM-D is a recent developing technology with roots in the semiconductor industry. MCM-Ds are fabricated by a sequential deposition of conductor and dielectric layers on a substrate base [1.41–1.52]. The substrates are generally round or square and made of metal, ceramic, or silicon. The dielectric layer usually consists of silicon dioxide or a liquid polymer such as polyimide, benzocyclobutene (BCB), or

some fluoropolymer, deposited by conventional spin coating. Variations of this basic technology include MCM-D/C (deposited dielectric on cofired ceramic) and MCM-Si (also referred to as silicon-on-silicon).

MCM-D/C combines dielectric layers on a multilayer cofired ceramic substrate yielding a product with the high-frequency and high-density attributes of MCM-D and the physical attributes of MCM-C. The cofired substrate acts as the package, containing the substrate base, signal interconnect, package body, and module level I/O. Additionally, the conductors can be embedded in low dielectric constant material while power and ground planes can be surrounded by high dielectric constant ceramic.

MCM-Si technology uses semiconductor fabrication equipment and techniques to deposit, define, and etch the dielectric and interconnect layers. The substrate is silicon, the inorganic dielectric material is usually silicon dioxide, and the metal is aluminum or copper. Silicon surface smoothness, metal and dielectric vacuum deposition, photolithographic feature definition, and etching (wet or dry) all combine to produce MCMs with an excellent CTE match to silicon ICs, very fine lines, and high routing densities. Unlike MCM-D/C, however, MCM-Si modules usually do not function as part of the package.

The advantages of MCM-D, in general, are low dielectric constants, dimensional accuracy, smallest feature sizes, lowest weight interconnect, and highest interconnect volumetric density. However, the cost is high, the dielectric layer thickness is limited by stress, and the number of conductor layers is somewhat limited. Also, in some variations of the technology, conductor bonding to the dielectric is complex and the electrical performance is moisture sensitive. Nevertheless, the unmatched high performance of MCM-D assures its future if efforts to reduce costs and improve the properties of organic dielectric materials continue.

1.7 SUMMARY

Because of the diversity of opinion on what constitutes an electronic package, an exact date for its origin is not possible. However, the beginning of modern electronic packaging can probably be dated around 1950, shortly after the discovery of the transistor. Since that time, myriad electronic packages and packaging materials have evolved. In all cases, the package must provide a structure to physically support the electronic device and protect it from the environment, a means of removing heat generated by the device, and electrical connections to and from the device. The most recent electronic packaging technology, referred to as multichip module (MCM), is used to house an electronic system by interconnecting a multiple number of ICs within a single packaging structure. Three classifications of MCM have been defined: MCM-L constructed of plastic laminate-based dielectric and copper conductors; MCM-C constructed on cofired ceramic or glass-ceramic substrates; and MCM-D which uses deposited thin film metals on polymers or inorganic dielectrics. Each of these MCM technologies has its advantages and disadvantages from both fabrication and performance points of view. Table 1.3 is a tabulation of some properties and parameters of MCMs.

TABLE 1.3 Properties and Parameters of MCMs

Parameter/Property	MCM-C		MCM-D		MCM-L
	Conventional Ceramic	Low K Ceramic	Inorganic	Organic	Printed Circuit Boards
Substrate materials	Al_2O_3	Glass-Ceramic	SiO_2	Polyimide, BCB, PPQ	Epoxies, Polyimides, Cyanate Esters
Substrate costs	Moderate	High	Moderate		Low
Number of metal layers	6–12 typ.		2–4 typ.		4–8 typ.
Conductor resistivity	2–20 mΩ/sq.		3–35 mΩ/sq.		0.15–3 mΩ/sq.
Line width (min) μm	100		15–20	10–25	25–125
Line spacing (min) μm	125–250		15–30	15–50	25–125
Via diameter (min) μm	125		7–20		laser-25; mech-150
Thermal conductivity (W/m·C)	1.5–20		0.15–1		0.15–0.35
Dielectric constant	9	5	4	2.4–4	3–5
Pin out					
per cm^2	15–60 (pins)		NA		15–30 (BGA)
peripheral (per cm)	10–20 (leadframe)		40–100 (wirebond)		10–20 (leadframe)
CTE (ppm/°C)	3–8		3–7.5		4–16

EXERCISES

1.1. What do you think is meant by the phrase, "the point has been reached where advancement in integrated circuit performance now drives packaging technology"?

1.2. What are the four basic functions that an electronic package must provide? In addition to these functions, give four other desirable characteristics of an electronic package.

(a) (c)
(b) (d)

1.3. Define the six levels of packaging hierarchy.

1.4. Which level of the packaging hierarchy is relevant to MCMs and why?

1.5. What are the three primary types of die attach materials?

1.
2.
3.

1.6. What are the three methods used to provide connections between an IC and the package which holds it?

1.
3.
2.

1.7. Lid and pin sealing material must possess five important properties. What are they?

1.
2.
3.
4.
5.

1.8. What features of the dual-in-line package (DIP) helped it survive the package evolution and become the primary package used today?

1.
2.
3.

1.9. What package feature distinguishes a flatpack from a DIP?

1.10. Describe the construction of a CerDIP package.

1.11. What is the most attractive feature of a surface mount package (SMP) and why is it important?

1.12. What five effects were created by the trend in the IC industry toward higher circuit densities and operating speeds that gave impetus to the development of MCM technology?

1.
2.
3.
4.
5.

1.13. What are some of the factors that relate performance and cost to packaging technology choices?

1. 5.
2. 6.
3. 7.
4. 8.

1.14. Distinguish between manufacturing costs and manufacturability costs associated with packaging.

1.15. Leads from an IC to a package and from the package to the outside world deleteriously impact electrical signals in three ways. What are they?

1.
2.
3.

1.16. What electrical design factors must be considered in order to minimize the deleterious effects (from previous exercise) that packaging interconnects have on electrical signals?

1.
2.
3.
4.

1.17. Distinguish between in-process and stress testing of electronics packages. What factors must be considered at every testing point in the fabrication sequence?

1.18. Distinguish between MCM-L, MCM-C, and MCM-D based on the substrate structure. To which existing technology is each one most closely related?

1.19. What are the advantages and disadvantages of each of the three primary MCM technologies?

1.20. What are the advantages and disadvantages of LTCC MCM-C with respect to HTCC MCMs?

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