1 Failure Analysis and ESD

1.1 INTRODUCTION

Failure analysis is invaluable in the learning process of electrostatic discharge (ESD) and electrical overstress (EOS) protection design and development [1–8]. In the failure analysis of EOS, ESD, and latchup events, there are a number of unique failure analysis processes and information that can provide significant understanding and illumination [4]. Today, there is still no design methodology or computer-aided design (CAD) tool which will predict EOS, ESD protection levels, and latchup in a semiconductor chip; this is one of the significant reasons why failure analysis is critical to the ESD design discipline. ESD prediction is also a difficult task because ESD phenomena span both the microscopic and macroscopic physical scale. ESD phenomena involve semiconductor device, circuit, and package effects and their interactions. Although significant resources have been placed on semiconductor design tools, ESD analysis and prediction remain significantly behind other semiconductor disciplines and design applications. Today, a simulation tool that can insure first-time success is still not available, yet all semiconductor fabricators and design houses need this capability and are dependent on it for proper qualification and release of semiconductor components. As a result, today there is still significant dependence on failure analysis.

So, the question is how do we build an ESD failure analysis discipline and methodology that provides the information that we desire to understand in order to build better ESD robust technologies, devices, circuits, and systems?

This is achievable if the failure analysis (FA) is not the end result, but the beginning of the analysis process. Many FA engineers feel it is their responsibility to find the defect, report the location, and define the class of failure. In this text, we want to provide a new view of how to use FA for ESD analysis, learning, and development of semiconductor chips which will be helpful to FA engineers, semiconductor device engineers, circuit designers, and ESD engineers [1–10]. In essence, to establish an ESD FA discipline.

The perspective which will be discussed in the text is to treat FA as the beginning of the investigation process, and to stimulate new questions from the information gleaned.

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For example, how do you use FA to build better semiconductor components and nanostructures? How do you use FA to determine ESD device operation? How do you use FA to determine power distribution? How do you define ESD metrics based on the ESD failure patterns? How do you use FA to determine the temperature inside the device from an ESD event? How do you determine the location of the peak temperature in the device? What fails first, and why? How do you determine the power distribution? How do you know how long the pulse event is? How can you determine the sequence of events in time? How can you tell from the materials what the sequence of events must be? How do you choose the materials to provide a robust technology? How do you use FA to determine if you are doing a good job or measure your success as an ESD engineer? How do you combine electrical measurements and FA? How do you combine FA tools to understand ESD mechanisms? In this text, these kinds of questions open the door to looking at ESD FA differently. With the understanding of how to utilize the information, we can build ESD robust products.

One of the things about FA is that it can provide visualization in space and time. FA can assist the design and development process by providing visualization of the mechanisms leading to ESD failure. The trick is to transfer the understanding into providing ESD robust implementations.

1.1.1 FA Techniques for Evaluation of ESD Events

For the evaluation of ESD events, there are many different techniques applied today. In ESD events, it is critical to understand the location of the defect, changes in the material properties of the physical films, and regions where the ESD event occurred. Electrical testing is a typical method for the evaluation of ESD events. Direct current and functional electrical testing methods are used for failure verification. In ESD FA of the circuit response, the following transmission line pulse (TLP) techniques are also used today. For radio frequency (RF) applications, a.c. electrical test techniques are applied to evaluate the impact of ESD on the failure of electrical components [10]. In the FA methodology, non-electrical methods are also used. FA techniques utilize photon emissions for the purpose of visualization of regions associated with ESD and latchup events [4,7,9]. These photon emission microscopy techniques can be used to determine current distribution within a device, or circuit, as well as the time sequence of events. Electron beam tools can also be used for FA caused by ESD events. Electron beam tools and techniques can determine the voltage state of regions within a semiconductor chip. Optical beam techniques and tools are used for the evaluation of ESD events. These methods utilize light (e.g., typically coherent sources) and voltage drop analysis. Thermal detection techniques are useful for determining the location of ESD and latchup failure. Recently, new scanning probe techniques have been developed that have been applied for ESD analysis. In the analysis of ESD events, the packaging can be damaged by the ESD event. Typical damage can include package discoloration, package cracking, wire bond damage, and melting. In most short pulse ESD events, the melting of the packaging does not occur; melting of package materials typically is associated with CMOS latchup or EOS events. In the FA technique, de-capsulation and back-side sample preparation are also needed.

Hence, today it is clear that there is a wide variety of tools to evaluate the electrical, electro-thermal, electro-optical, and thermal response in time and space for the evaluation of ESD

events. These techniques utilize current and voltage pulses of different pulse widths and magnitude. They also utilize different frequencies from infrared to the optical spectrum. These will be discussed in more depth in Chapter 2.

1.1.2 Fundamental Concepts of ESD FA Methods and Practices

For ESD FA, there are fundamental methods and practices to diagnose, evaluate, and design micro-electronics [1–4,7]. The fundamental concepts and practices of ESD FA of semiconductor components are as follows:

- Root cause evaluation of ESD failure.
- Identification of ESD failure mechanism.
- Determination of the ESD current path.
- Determination of the role of parasitic devices.
- Power distribution evaluation.

ESD FA also provides significant additional capability to the ESD device physicist, ESD circuit designer, and ESD reliability engineer. A fundamental part of the ESD design practice is the usage of FA and methods; this establishes an ESD FA discipline as follows:

- Visualization.
- Visualization: spatial visualization.
- Visualization: temporal visualization.
- Visualization: spatial and temporal visualization.
- Visualization: integration with semiconductor device electro-thermal simulation.
- Visualization: integration with a plurality of FA tools and techniques.
- Evaluation: integration of failure defect and electrical measurement.
- ESD circuit operability evaluation.
- ESD parasitics operability evaluation.
- ESD guard ring operability evaluation.
- Spatial distribution evaluation of ESD design area effectiveness.
- Spatial distribution evaluation of peripheral circuit design area effectiveness.
- Internal temperature evaluation (melting point).
- Internal temperature evaluation (phase transition).
- Internal temperature evaluation and thermal stress (chemical techniques).

- Categorizing "good" and "bad" semiconductor circuits using ESD failure distribution.
- Evaluation of power bus design quality using FA and ESD failure distribution.
- Evaluation of substrate ground quality using FA of multi-finger structures.
- Evaluation of ground-to-ground coupling using FA defect evaluation.

1.1.3 ESD Failure: Why Do Semiconductor Chips Fail?

Why do semiconductor chips fail? ESD failure in micro-electronics can be viewed from many different perspectives. A first perspective is the power of the ESD event exceeding the power-to-failure of the material, device, or component. Micro-electronic components can also fail due to the semiconductor chip power distribution; these also fail due to inadequacy in the architecture of a semiconductor chip, and flaws in the design synthesis. From a material perspective, ESD failure can occur as follows:

- Breakdown voltage of a material is exceeded.
- Melting temperature of a material is exceeded.
- Alteration of a material influences the device characteristics.

Within a chip, ESD failure can occur in many sections in the semiconductor. Semiconductor chip design is segmented into different physical domains due to different application voltages, and functions. In system-on-chip (SOC) applications, semiconductor chips are segmented into digital, analog and RF power domains. Semiconductor designs are also segmented for noise isolation.

There are typically at least two current paths in a semiconductor chip. The first path is the signal path. The second path is an alternative current path to divert the ESD current from the signal path. In semiconductor chip design, the ESD current is shunted to a power or ground rail to avoid damage to the signal path. From a power-to-failure (P_f) perspective, there are four reasons for failure of the semiconductor chip:

- P_f of the I/O circuitry (e.g., receivers, off-chip drivers) was exceeded.
- P_f of the wiring (e.g., signal path or power grid) was exceeded.
- P_f of the ESD element was exceeded.
- P_f of the ESD power clamp was exceeded.

One of the reasons why a semiconductor device or element fails is due to poor power distribution within the physical element, circuit, or sub-function, core, or chip sector. Hence, some of the reasons for ESD failure in a semiconductor chip are associated with the following:

- Power distribution through an element.
- Power distribution through the circuit.
- Power distribution through the semiconductor chip.

Another perspective for ESD failure of a semiconductor chip is associated with architecture. Semiconductor components must be designed to allow the ESD current to flow in a current path between the tested pin and the grounded reference node (e.g., signal pin, V_{DD} or V_{SS}). The ESD standards define the requirements for the pin combinations of the components between the pulsed and grounded pin. Hence, a semiconductor chip must have an architecture that satisfies these requirements. From an architecture and chip synthesis perspective, ESD failures occur because:

- No current path exists.
- No forward-biased current path exists.
- Current path robustness is inadequate.
- Elements in the ESD current path are too resistive.
- Turn-on voltages or trigger voltages are too large.

In ESD design, if a design does not establish a path between the pulsed pin and the grounded reference pin, ESD failure can occur. For effective ESD protection, elements must have low resistance or low trigger voltages to allow current flow without excessive internal voltage buildup in the semiconductor chip. High resistance elements prevent adequate current flow through the semiconductor chip. High resistance elements also can fail due to Joule heating. Additionally, high voltage trigger elements also prevent the current flow until the trigger condition is established. Dielectrics, capacitors, and high impedance elements can fail in the path between the pulsed pin and the grounded reference pin.

1.1.4 How to Use FA to Design ESD Robust Technologies

FA can be used to design ESD robust technologies [1,4,7]. First, one of the reasons that material failure occurs is due to melting. As the power increases in a physical region, Joule heating can lead to failure of semiconductor devices. As a result, the current density and the conductivity of a material highly influence the local temperature. When the melting temperature is reached, material failure occurs leading to device failures. As a result, the following can be stated:

- Improving the conductivity of a material reduces the heating in a region.
- Choosing materials with high melting temperatures can decrease the likelihood of thermal failure.

Hence, in a simplistic perspective, by increasing the doping concentration, or using more conductive films, it is possible to reduce the Joule heating and lower the local temperature. This delays the onset of thermal failure. Also note that as the doping concentration is more uniform, the heating will also be more uniform.

Second, simplistically, choosing materials with high melting temperature improves the ESD robustness of a technology. In fact, simply by knowing the materials contained within the technology, it is possible in many cases to understand the time sequence of failure based on the temperature in the structure. If we know the power is distributed equally, or the temperature

field and gradient over a region are uniform, the time sequence of failure of the different materials will occur in the order of the melting temperatures.

1.1.5 How to Use FA to Design ESD Robust Circuits

In many semiconductor corporations, FA is used by the quality or qualification organization for evaluation of achieving the product specification [6]. In the qualification process, ESD testing is completed to the product specification. ESD testing is completed to the various ESD models (e.g., human body model (HBM), machine model (MM), and charged device model (CDM)). In many quality organizations, given that the product achieves the ESD specification, no FA is required. FA is initiated when some of the pins of the component do not achieve the qualification. In this methodology, ESD learning is only achieved on the pins that fail the qualification: the "bad pins." Whereas this method is good for verification of passing the product specification, it does not serve as a tool to provide learning for the semiconductor product development team for building ESD robust circuitry and how to synthesize the semiconductor product chip. It also does not quantify the failure levels of the specific pins nor quantify the means of failure. As a result, ESD learning is not achieved on the majority of pins.

FA can be used for the design of ESD robust circuitry [7]. Further, FA can be used to determine the following [1–4,7]:

- Evaluation of primary current paths.
- Evaluation of secondary parasitic current paths.
- Evaluation of device operation.
- Current spatial distribution within a device within the circuit.
- Evaluation of spacing sensitivity between circuit elements.
- Evaluation of parasitic devices within the circuit elements.
- Evaluation of guard ring interaction.
- Temporal evolution of circuit elements in the network.
- Statistical variations of the identical pins.
- Power distribution effects.

Using non-qualification testing methodologies combined with FA, FA techniques can be used to understand how to design ESD robust circuits. For example, using a testing procedure where all pins are "tested to failure" provides information on the ESD robustness of every pin and every circuit. A step-stress procedure that tests all pins will provide a valid test for semiconductor chips.

As another way of understanding, one can learn just as much from the "good pins" as the "bad pins"; it is important to learn the information on how all the circuits respond to the high current stress for ESD learning.

Another perspective is that the ESD stress is a "single-pulse high current probe" to evaluate the response of the chip at high currents and different pulse frequencies. In that fashion, significant design information is obtained in the circuit, power bus, and chip architecture.

An ESD testing methodology to maximize semiconductor chip ESD learning of failure mechanisms is to test incrementally [6].

1.1.6 How to Use FA for Temperature Prediction

FA can be used to evaluate the temperature in the region of the failure mechanism [7]. From the FA and the failure mechanism, the temperature of the physical damage can be determined by the following observations [5]:

- Molten or melted material.
- Evaporation of material.
- Displacement of the material.
- Displacement of the material into a secondary region.
- Agglomeration of the material.
- Material phase transformation.
- Crystal structure transformation.
- Coloration.
- Cracking.

The failure mechanism can provide the following information:

- Temperature.
- Location of the peak temperature.
- Thermal gradients in the region of failure.

Molten or Melted Material From a simplistic understanding, EOS, ESD, and latchup events can lead to failure mechanisms associated with melting. Given during an event that the material melts, then it is obvious that the region reached the melting temperature at that location. Hence in FA, it is clear that a region reached at least that critical temperature. By knowing the material type, the melting temperature is known, and it is clear that the region was at least at the melting temperature. In addition, the location of where the melting occurred can also determine the location of the peak temperature.

Evaporation of Material From FA, the lack of the presence of the material indicates that the melting temperature of the material was achieved, or in the case of a compound, disassociation temperature was achieved in the region of the failure mechanism. For example, given that silicon dioxide is not present in the region of the failure mechanism, and only silicon is observed, indicates that the temperature of the silicon dioxide led to a separation of the silicon and oxygen atoms, leaving behind only molten silicon. As a result, it is clear that the temperature in that physical region achieved a temperature above the bonding energy to form silicon dioxide (SiO_2).

Displacement of the Material From FA, it is evident that material is displaced from its original location. In the case of metallurgy in semiconductor wiring, it is evident that the melting temperature was achieved in the region of the failure mechanism.

Displacement of the Material into a Secondary Region In the region of the failure mechanism, material displacement can be observed. For example, in an ESD event, aluminum is evident in the region of the dielectric. In this process, this indicates a physical change in the dielectric, and melting of the aluminum into those physical regions. In the case of dopants, it can indicate that the activation energy was achieved for diffusion of the dopant in the junction or at an interface. Junction leakage can occur when the motion of the dopants on both sides of a metallurgical junction are displaced. As a result, it is clear that a temperature was achieved which led to activation of the diffusion process.

Agglomeration of the Material FA may show evidence of agglomeration of material. This process occurs at a given temperature in the material. Hence, from evidence of the agglomeration of a given material, it is clear that this temperature was achieved in the physical region of the defect. For, example in a cobalt silicide film, agglomeration will occur at a given temperature.

Material Phase Transformation From FA, phase transformations are evident in a material. These phase transformations occur at some temperature in the region. For example, in titanium silicide, ESD failure regions indicate a change in the material structure in the region around an ESD defect. Since silicides have multiple material states, transformation from one state to another state can initiate from ESD events in the region of failure due to the temperature in the region. Knowledge of the physics of the silicide transformation allows the temperature in the region to be predicted.

Crystal Structure Transformation FA can determine the temperature in the region of the defect by evaluation of crystal structure transformation. Crystal structure can be altered in a material which is activated at a critical temperature. For example, the grain structure of polysilicon lines can be altered by a heating process. ESD events can lead to grain structure changes in polysilicon resistors in CMOS technology. In bipolar technology, the crystal structure can be modified from a polysilicon emitter or polysilicon base by self-heating during an ESD event.

Coloration FA can determine the local temperature based on observation of the coloration in a given region. Coloration changes are evident in metal lines upon observation due to film or insulator changes.

Cracking FA can determine the temperature and thermal gradients from observation of cracking in the region of the ESD failure. For example, insulators adjacent to interconnects crack due to ESD events in the wire interconnects.

1.1.7 How to Use Failure Models for Power Prediction

With technology scaling, the ESD robustness changes due to the material changes as well as the physical size of the structures [10–26]. Hence it is important to understand ESD from

a fundamentals level. From FA, the power-to-failure can be predicted knowing the melting temperature. In the ESD models, the power-to-failure, pulse width, geometry, material properties, and melting temperature are related [26–34]. Hence, given that one knows the FA location, pulse width, material properties, and melting temperature, the power-to-failure can be predicted. Hence also, given FA where the melting temperature is reached, the power-to-failure can be approximated. From the equations for power-to-failure, one can solve for temperature.

1.1.8 FA Methods, Design Rules, and ESD Ground Rules

FA can also be used to develop specific ESD ground rules [7]. In a technology, "ground rules" are established for successful yielding of the technology. Typically, these rules are established based on semiconductor process and lithography limitations.

ESD ground rules are design rules which are specifically used to minimize the effect of parasitic elements or ESD failure. Using the failure damage patterns, and ESD robustness levels, these spacings can be decided.

For example, it was found that by adjusting the spacing between the n-diffusion and the guard ring, the "ESD current robbing" could be eliminated. It is found that an optimum ESD result is possible when the spacing of the n-resistor to the n-well guard ring was tuned to the spacing between the n-well ESD diode and its adjacent guard ring. Hence an ESD ground rule was established so that the spacings provided the highest ESD level. Hence, using FA damage patterns, the spacing of guard rings and ESD ground rules can be defined.

With a second example, interactions between n^+ floating gate tie downs and the pull-down MOSFET of a mixed voltage off-chip driver (OCD) circuit also were evident using FA of the peripheral circuit. The MOSFET drain and the n^+ diffusion tie down formed a parasitic bipolar junction transistor (BJT) when designed local to each other in the substrate. In this work, it was found that in negative V_{DD} test modes, the lateral npn was active in LOCOS isolation, but not in STI-bound MOSFETs. Ground rules were established to avoid interaction between the floating-gate tie downs and the peripheral circuit pull-down OCD network.

1.1.9 FA and Semiconductor Process-Induced ESD Design Asymmetry

FA is a means to verify semiconductor process or design asymmetry which can have an influence on ESD robustness of circuits [7]. Process-induced design asymmetries can occur on all design levels. For example, photo and etch processing can have both macroscopic and microscopic effects [16]. In the processing of polysilicon gate structures, "across chip linewidth variation," known as ACLV, can vary the MOSFET polysilicon gate linewidth. The placement of the circuit in the chip globally leads to ACLV effects because of macroscopic photo-tool source–intensity effects, and within a multi-finger MOSFET because of microscopic photo and etch effects. It is found that, depending on the type of photo-resist, "nested" linewidths and "isolated" linewidths can be different [16]. With positive tone resist, nested lines are smaller than isolated lines, and with negative tone resist, this reverses. The implication of this effect is that MOSFET second breakdown is a non-random phenomenon and will be

evident on the MOSFET fingers with smaller linewidths because of the lower MOSFET snapback. Using a two-dimensional "boot tip" atomic force microscope (AFM), two-dimensional (2-D) mappings of topography provided significant accuracy of both the lateral and vertical dimensions. Boot tip AFM devices allow for the ability to address sidewall slopes of polysilicon gate structures and vertical trench profiles. FA verified that the MOSFET second breakdown in the multi-finger MOSFET structure was non-random in a positive tone photo-resist system. FA results showed that the "nested" lines with the smaller MOSFET linewidths had damage between the source and drain [16]. Combining the 2-D AFM tool with the scanning electron microscope (SEM) analysis of the ESD-damaged MOSFETs, verification of the reason for the non-random component associated with linewidth was quantified and explained the ESD results.

1.1.10 FA Methodology and Electro-thermal Simulation

Using a heuristic understanding of the design layout, FA followed by electro-thermal simulation can provide a higher intuition allowing the ESD designer to bridge from the physical to the electro-thermal results. Failure patterns can teach the regions of peak thermal heating and failure [1–3,7]. Electro-thermal device simulation can help understand the location and the root cause of the ESD failure. As an example, the corner of a shallow trench isolation (STI) bound p^+ diffusion/n-well diode was failing on the diffusion-to-STI corner. Using an SEM, an emission microscope (EMMI) tool, and a Kelvin force probe microscope (KPFM) tool, the ESD damage was imaged. The SEM provided a bird's eye view of the ESD device after removal of the metal films. The EMMI tool provides a photon mapping of the ESD structure during direct current (d.c.) measurement (Figure 1.1). The KPFM tool provided both a topographic as well as electrical potential mapping (Figure 1.2). Using a 3-D semiconductor electro-thermal tool FIELDAY III, our analysis demonstrated and verified that the peak lattice temperature was at the end of the p^+ diode implant (Figure 1.3) [1]. FA combined with the electro-thermal simulation establishes good intuition and a good methodology for ESD protection networks and circuit design.

1.1.11 FA and ESD Testing Methodology

For FA to be effective for ESD learning, a good ESD testing methodology and strategy is needed to maximize the ESD learning on ESD networks, circuits, and products. The ESD testing methodology is key in providing a valuable correlation between ESD failure and the failure mechanism (Figure 1.4). In the testing and FA strategy, developed by V. Gross, S. Voldman, and W. Guthrie [6], all pins are tested to a given power rail. Second, each pin is tested from zero volts on the source, and step stressed in small increments. It is also key that all pins are tested to failure. The failure distribution function of all the pins is plotted and evaluated to determine the "mean failure distribution," standard deviation, and other statistics of the whole chip. In many corporations, the FA focus is primarily on the worst case pins. In this methodology, the FA of the "good" pins is as important to evaluate as well. This allows documentation and classification of the pin types, the failure mechanism, and ESD results. This methodology allows us to verify at what level different failure mechanisms are evident as well as quantify what mechanisms are occurring in which circuit function. This testing

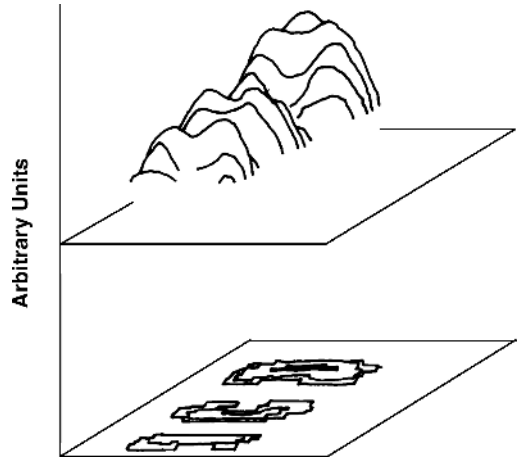

Figure 1.1 Emission microscope tool photon map of a p^+ diode

methodology highly incorporates FA as a key source to drive ESD learning in chip development. An ESD FA testing methodology to maximize semiconductor chip ESD learning is to test as follows [6]:

- Choose a polarity for the test.
- Choose a pin and ground a reference pin.
- Apply only one pulse polarity to the test pin (e.g., HBM positive polarity pulse).
- Begin testing at the lowest test increment of the test system.
- Step stress in the smallest test increment of the test system (e.g., 50 V HBM increments).
- Test all pins to ESD failure (according to a failure criterion).

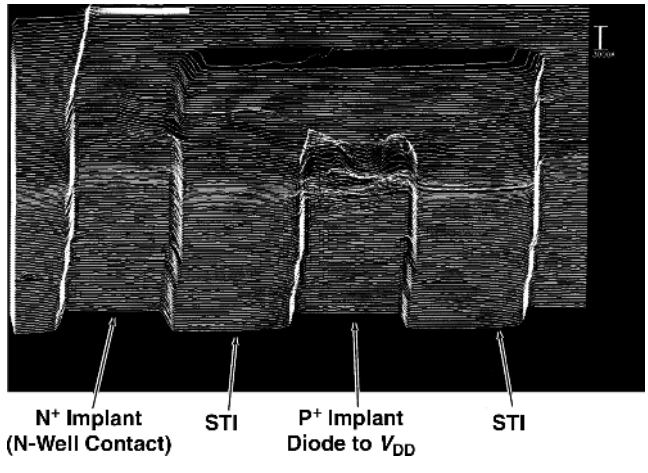

Figure 1.2 Kelvin probe force microscope topography image of p^+ diode

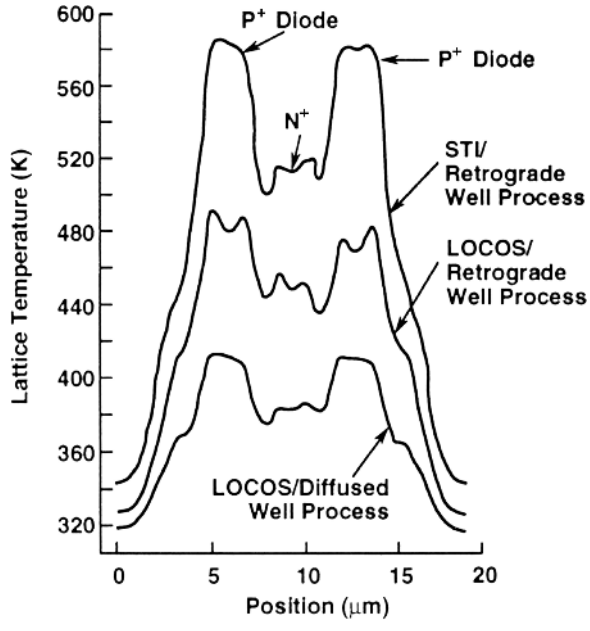

Figure 1.3 Electro-thermal simulation results

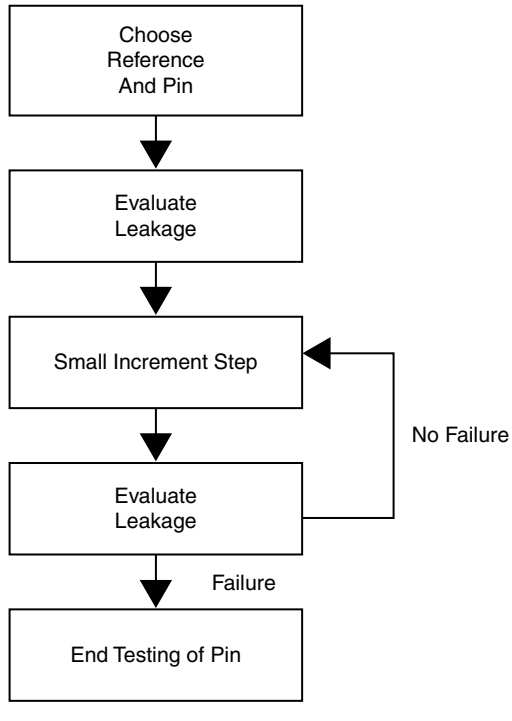

Figure 1.4 Test sequence for ESD characterization test to maximize ESD learning

- Plot the frequency of failure versus failure level.
- Overlay ESD results by pin type and test mode.
- Determine ESD metrics of ESD failure mean, standard deviation, and worst case pins.
- Failure analyze each test by pin type and test mode.
- Document the failure locations and devices.

1.1.12 FA Methodology for Evaluation of ESD Parasitics

FA provides significant insight into the current flow of parasitic elements and how they interact with an ESD element [7,9]. Three situations can exist: 1. the parasitic element draws the current, becomes damaged, and leads to low failure levels; 2. the ESD network draws the current flow, becomes the limiting value, and fails at a high current; and 3. the parasitic and the ESD element are working in conjunction where both are damaged at the same failure voltage. The first case is sometimes referred to as "ESD current robbing."

For example, a parasitic npn is formed between an n-diffusion resistor and a guard ring structure. Additionally, an ESD n-well diode is also in parallel with the n-well diode element which is also adjacent to the same guard ring structure (Figure 1.5). Figure 1.6 shows experimental results of the parasitic npn in parallel with an ESD n-well diode element. The parasitic npn reduced the failure level to -3 kV HBM whereas the ESD element n-well diode would have produced -7 kV by itself. At -3 kV, no damage is evident in the n-well diode but in the parasitic npn damage is evident between the guard ring and the

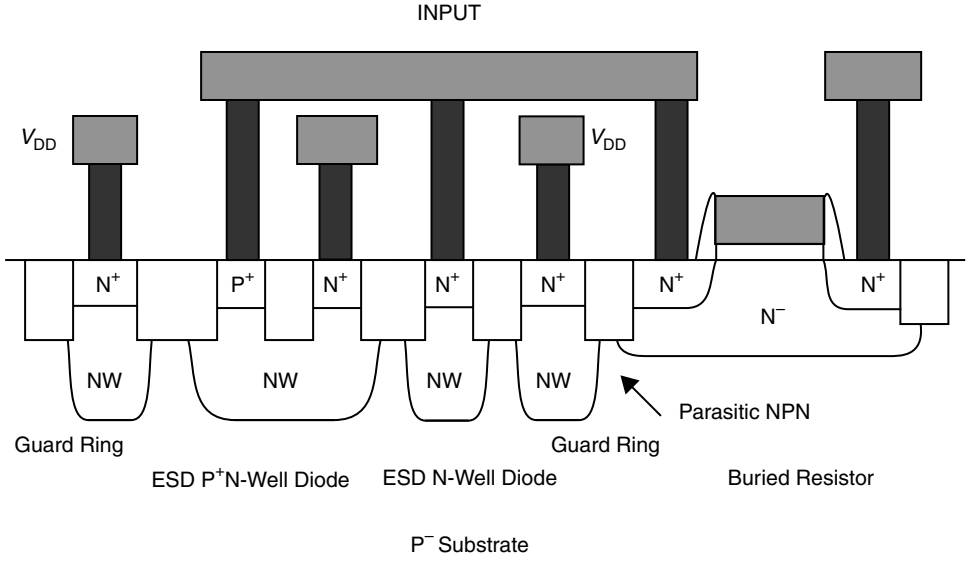

Figure 1.5 Example of parasitic element parallel to ESD network

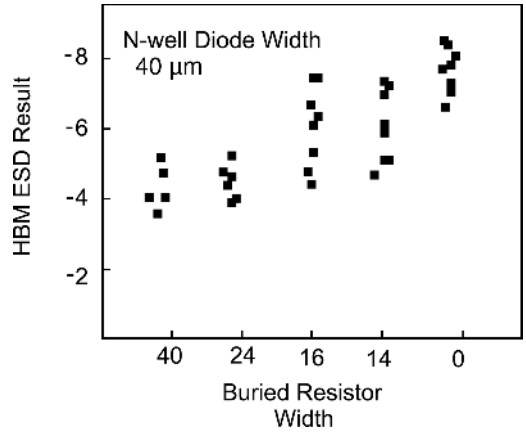

Figure 1.6 ESD results of parasitic element parallel to ESD network

resistor element. FA is able to determine that "ESD current robbing" was occurring leading to the low failure level.

1.1.13 FA Methods and ESD Device Operation Verification

FA can be used as a means of verifying ESD device operation [7,9]. At times, it is not clear how an ESD device is operating or the current paths taken by the ESD current. Failure analysis is a key means of verification of the current transfer based on the location of the damage on given shapes, or between shapes. The ESD damage is a verification of current transfer and clearly can show device operation and the path of the ESD current transfer.

For example, in an integrated cascode MOSFET, the electrical schematics would not explain the nature of the failure mechanism (Figure 1.7). Early measurements of cascode MOSFETs anticipated that the MOSFET snapback voltage would serve as the sum of the two MOSFETs. Experimental results verified that the integrated series cascode MOSFET was significantly less than the sum of the two MOSFETs. It is clear from FA that the interaction for the cascaded MOSFET second breakdown occurs in the same local region, providing a response which behaved as a single MOSFET [16]. From the AFM FA, it is clear that the parasitic bipolar transistor is interactive locally as one device (Figure 1.8). The AFM FA results then show that treating the series cascode MOSFET structure cannot be modeled as two independent components. Since this early work, the issue of analysis of series cascode MOSFETs has received increased interest in mixed voltage interface networks in microprocessors and peripheral circuits.

1.1.14 FA Methodology to Evaluate Inter-power Rail Electrical Connectivity

FA can be used to verify and evaluate the electrical connectivity between two power busses and how they interact with a peripheral circuit. When electrical connectivity is not adequate

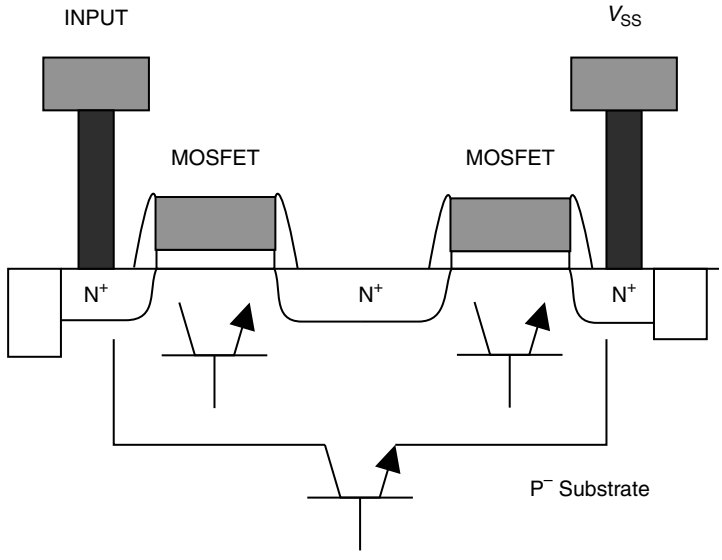

Figure 1.7 Example of parasitic element in a cascade MOSFET circuit

between devices with more than one ground connection, the failure and operation of the devices are altered during ESD events. Hence, FA can in fact determine the electrical connectivity during ESD events from the failure pattern. For example, the ESD robustness level, the element ESD response, and FA of a multi-finger MOSFET circuit are significantly dependent on the relationship between the chip substrate and the other ground rails. In a CMOS chip, typically the off-chip driver (OCD) bus or peripheral circuits bus is separated from the core or chip substrate bus. In mixed signal designs, the digital and analog grounds are also

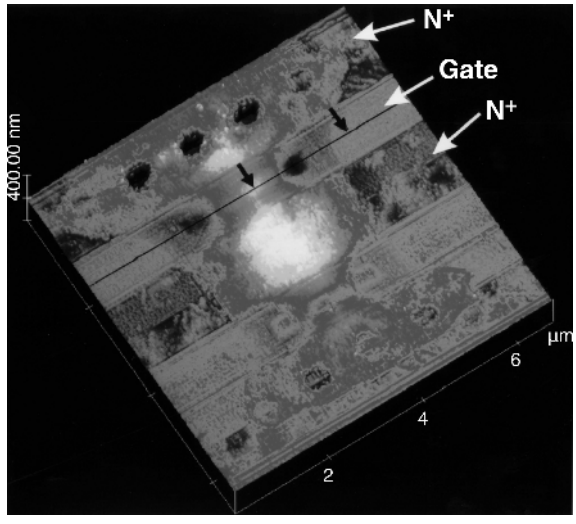

Figure 1.8 ESD failure between the top MOSFET drain and lower MOSFET source

separated. In RF applications, different RF functional blocks also have separated grounds. In the case when there is strong bidirectional coupling between the grounds, the failure damage pattern in a multi-finger shows damage in many of the MOSFET fingers. When the circuit is tested referenced to a substrate-decoupled peripheral ground, the ESD results are significantly lower and only one damage spot in a single finger is evident. Hence from the FA pattern in the MOSFET, it can be determined whether there is strong or weak coupling between the rails.

1.1.15 How to Use FA to Eliminate Failure Mechanisms

In semiconductor components and ESD design, FA can be used to eliminate failure mechanisms [7,9]. It can be utilized to eliminate the failure mechanisms through different methods. FA can also help to identify the region of the failure. Failure mechanisms can be eliminated by the following means:

- Spatial and geometrical variation in the region of the failure mechanism.
- Spatial and geometric variation to establish a secondary or parallel current path.
- Semiconductor process variation in the region of the failure mechanism.
- Semiconductor process variation to establish a secondary or parallel current path.
- Circuit variation by the addition of resistance.
- Circuit variation by establishing an alternate or parallel current path.
- Circuit variation by establishing a different voltage state.

ESD failures can be eliminated on a semiconductor device level through process variation, design layout, or circuit topology modifications.

1.2 ESD FAILURE: HOW DO MICRO-ELECTRONIC DEVICES FAIL?

A key question is how does the failure occur? Micro-electronic and nano-electronic "failures" from ESD events occur due to material property changes, motion of a first material into a second material, separation of a first material from a second material, or removal of the material. Dependent on the material and the surrounding materials, and geometries, these can occur at different ESD current magnitudes.

Semiconductor chips consist of the following materials:

- Single-crystal semiconductors (e.g., silicon).
- Amorphous semiconductors (e.g., polysilicon).
- Single-crystal compounds (e.g., gallium arsenide, silicon–germanium).
- Insulators.

- Metals.
- Silicides.

In each case, the material properties influence the ESD failure. The material properties that influence the failure are:

- Melting temperature.
- Phase transitions.
- Thermal expansion coefficient.
- Material maximum breakdown voltage.

Material property changes can be a change of state from solid, to liquid, to gas. ESD events can lead to the melting of a solid to a liquid when the temperature in the region of the ESD event exceeds the melting temperature of the medium. In some compound materials, the temperature in the region of the ESD failure mechanism can lead to disassociation. ESD events can also cause changes in crystalline structure. In non-single-crystal materials (e.g., amorphous), ESD events can lead to local heating which can change the material state and grain structure. Material property changes can occur due to exceeding the electrical breakdown of the material. In all these cases, the electrical properties (e.g., resistance, leakage current) may change.

ESD events can lead to the motion of a first material into a second material. In the case of dopant atoms, the heating process from the ESD event can lead to the diffusion of dopants. The thermal diffusion of the materials from one region into a second region can lead to changes in the material properties. In these cases, where motion of the material is involved, the length of time of the pulse and the amount of heat are involved in the process. In these cases, the failure will manifest itself as changes in the electrical properties.

A third means of failure is separation of a first material from a second material. An ESD event can lead to current magnitudes where the first surface separates from a second surface. For example, given two materials of different thermal expansion coefficients this can lead to a separation between the two regions. An ESD event can lead to self-heating and thermal strain. Thermal strain occurs at the interface between dielectrics and metal interconnects when ESD current flows through an interconnect wire. Failures in micro-electronic wiring can lead to material separation. ESD events can lead to separation between the following:

- Semiconductor-to-insulator interface.
- Semiconductor-to-metal interface.
- Metal-to-insulator interface.
- Silicide-to-semiconductor interface.
- Silicide-to-metal interface.

ESD events can also lead to the removal of material. In the transition from solid to liquid or gaseous states, material can be removed leading to electrical failure. For example, metals can agglomerate, sputter, or be displaced. In this process, the electrical signature may be a high resistance or electrical “open.”

In micro-electronics, and nanostructures, ESD failure can occur in the bulk volume or at an interface. The properties in the bulk volume can be homogeneous or non-homogeneous. The interface region can be an interface of the same material or different materials. In a semiconductor material junctions can be homojunctions and heterojunctions; ESD failure can occur in both homojunctions and heterojunctions.

1.2.1 ESD Failure: How Do Metallurgical Junctions Fail?

In a semiconductor metallurgical junction, there is a p-type region which abuts an n-type region. In the process of an ESD event, for a forward-biased junction, power is being dissipated in the anode volume, the cathode volume, and the metallurgical junction. In the process of an ESD event, for a reverse-biased junction, power is being dissipated in the metallurgical junction region. As the power increases, the temperature near the metallurgical junction begins to increase, as well as the doped regions on both sides of the metallurgical junction. In many cases, the failure of the metallurgical junction is associated with the motion of the dopants.

One point of interest is that, given an equal temperature on both sides of the metallurgical junction area, which region moves—the p-doped side or the n-doped side of the metallurgical junction? The p-type dopant is typically boron, and the n-dopant is typically phosphorus or arsenic. Since it is well understood that B diffusion occurs prior to P or As diffusion, then it is anticipated that the motion of the B dopants plays a role in the junction failure given the equal temperature on both sides of the metallurgical junction.

A second part of the issue is the penetration of silicide films. Metallurgical junction failure can be associated with the penetration of refractory metals in the metallurgical junction region. As a semiconductor device is heated, the silicide will penetrate into the junction region, and can lead to ESD failures.

A third part of the issue is the penetration of the contact structure. In older technologies, the contacts were large enough to avoid melting of the contact structures. As technologies are scaled, the contact and via structure will penetrate into the metallurgical junction region.

1.2.2 ESD Failure: How Do Insulators Fail?

Insulators fail due to maximum electric field across the insulator being exceeded. Insulator breakdown occurs at the anode or cathode interface or within the bulk of the medium. At the interfaces of materials, electric field enhancement at the surface can initiate electrical breakdown. In spark gaps and air breakdown phenomena, defects at the electrodes can initiate electric field enhancement and can initiate breakdown phenomena. In ESD phenomena, air discharge occurs between charged sources and semiconductor chip packages. Air discharge events also occur from cables when connections are made between the cables and systems. In charged device model (CDM) testing, air breakdown occurs as the CDM test system pogo pin approaches the charged semiconductor part.

Inside semiconductors, insulators are present in the silicon wafer, isolation regions, MOSFET gate oxides, MOSFET spacers, and inter-level dielectric films. Electrical breakdown can occur as a result of overvoltage across the insulators.

MOSFET gate dielectrics are present in MOSFETs, polysilicon-gated diode elements, buried resistor (BR) elements, and decoupling capacitors. Polysilicon-gated diodes are used in ESD networks for both advanced CMOS development, silicon-on-insulator (SOI) technology, and RF applications. BR elements are used in OCD networks for impedance matching, tuning, and ESD resistor ballasting. Decoupling capacitors are used in semiconductor chips to add capacitance to the power rail or semiconductor chip. In all these structures, ESD failures can occur due to electrical stress across the thin insulator. MOSFET gate dielectrics have been historically silicon dioxide films, and silicon dioxide–silicon nitride films. Today, new gate dielectric materials are being used, and dual- and triple-gate films are being applied.

Inter-level dielectric (ILD) films are present between metal interconnects forming both vertical and lateral metal–insulator–metal regions. In the back end of the line (BEOL), vertical and lateral passive element capacitors are being formed for functionality as well. These include vertical metal–ILD–metal capacitors, and vertical natural plate (VNP) and vertical parallel plate (VPP) capacitors. The BEOL capacitor elements are being used today for RF components from wired and wireless applications. Electrical overstress between metal lines or metal plates can lead to ESD failure and to dielectric breakdown.

In SOI technologies, the buried oxide (BOX) film can undergo ESD electrical breakdown during ESD events. Given that a substrate wafer is charged, and the thin silicon film and its corresponding interconnects are grounded, electrical breakdown across the buried oxide region can occur. Given that there is no good electrical connection between the substrate and the active device surface, a capacitor is formed across the wafer with the top plate being the active device region and the bottom plate the substrate wafer. Electrical breakdown can occur on either a wafer level or a semiconductor chip level.

Whether as intentional or non-intentional capacitor structures, electrical breakdown of dielectrics can occur during human body model (HBM), machine model (MM), and charged device model (CDM) events. These will be discussed in the text below.

1.2.3 ESD Failure: How Do Metals Fail?

In semiconductor chips, metal is present in many sectors of the semiconductor. Metal exists in the wiring levels, the vias between the wiring levels, the contacts to the silicon surface, the V_{DD} power bus, the V_{SS} ground bus, signal and power bond pads, as well as bond wires in the packaging. Silicides are compounds formed between a refractory metal and silicon. In regions of the semiconductor chip where the current density is high during ESD events, this can lead to Joule heating in the metal regions. Typically, the highest current density exists in the thin silicide films, contacts, vias, and metal levels that are in the current path of the ESD event.

Metal lines typically have a refractory metal liner surrounding the metal regions for adhesion to insulators, as well as electro-migration [15]. In aluminum interconnects, the refractory metal is titanium, with titanium nitride at the interconnect–insulator boundary. In the case of copper interconnects, the refractory metal is tantalum, with tantalum nitride at the interconnect–insulator boundary.

Metal wiring failure occurs in a three-step process [15]. First, the Joule heating leads to cracking due to high thermal stress; this is followed by metal film melting once the melting temperature of the interconnect is reached. Melt flows into the insulator region leading to a change in resistance of the metal film. Electrical connectivity is still established due to the

residual metal as well as the refractory metal cladding. When the metal film is compromised, the current flows through the cladding materials leading to high current density in the cladding film. When the melting temperature of the refractory metal is reached, melting of the cladding film occurs leading to an electrical open.

Vias are typically formed from tungsten material. Tungsten has a very high melting temperature. Tungsten wiring also has a high resistance. ESD failure can occur in tungsten M0 wiring levels, to vias and contacts. Typically, failure of tungsten stud vias is not observed; in advanced CMOS technology below 65 nm, melting of the tungsten stud via has been observed.

Metal regions such as bond pads and bond wires have low current density due to the area. Bond pads typically fail due to dielectric breakdown from the pad to the lower metal levels. Bond wire adhesion can fail at the bond wire–pad interface due to thermal stress in ESD, latchup, and EOS events. Bond wire mismatch can lead to $L\,\mathrm{d}i/\mathrm{d}t$ mismatch which can lead to CMOS latchup failure in large scale systems.

1.3 SENSITIVITY OF SEMICONDUCTOR COMPONENTS

ESD sensitivity of different semiconductor components can be a function of the following:

- Material properties.
- Device type.
- Technology generation.
- Application.
- Physical size.

In the early development of semiconductors, physical models were established noting the power handling capability of different materials. The material properties do play a large role in ESD sensitivity [26–30]. Key material properties that influence ESD results are as follows:

- Heat capacity.
- Thermal conductivity.
- Maximum electric field.
- Saturation velocity.
- Melting temperature.

1.3.1 ESD Sensitivity as a Function of Materials

Figure 1.9 shows a plot of the semiconductor sensitivity as a function of the material property. E. Chase first showed the relationship of the different materials [35]. A key point is that the power-to-failure is a function of the thermal conductivity, heat capacity, and melting temperature of the materials.

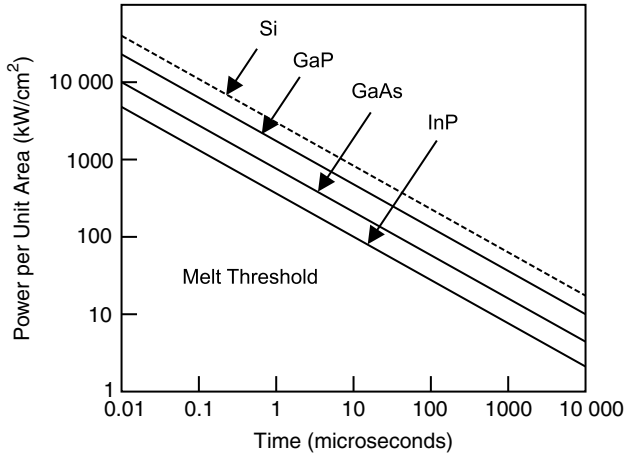

Figure 1.9 ESD sensitivity versus material property

1.3.2 ESD Sensitivity as a Function of Semiconductor Devices

A second issue that influences ESD robustness is the type of semiconductor device. Different types of devices are more sensitive than others. Some semiconductor devices conduct current through the semiconductor device volume, and others conduct along the device surface. For example, vertical diode elements or bipolar transistors conduct current through the bulk of a semiconductor device. MOSFET devices are surface conduction devices. A bulk device will have a lower current density than a surface conduction device.

In semiconductor devices, the geometry and the physical size also play key roles in ESD failure levels [26–33]. For example, high performance lateral bipolar transistors were typically more sensitive compared to MOSFET devices. This was partly due to the small emitter structure of the bipolar transistor, in comparison to early MOSFET drain and source size. One of the most sensitive semiconductor elements manufactured today is magneto-resistive (MR) recording heads [23–25]. MR heads are significantly smaller than most semiconductor chip applications purely due to the physical size. These devices are being scaled to thinner films leading to a strong sensitivity to ESD events. Continued scaling of MR elements for the magnetic recording industry is performed to improve the signal as well as achieve higher areal density. Each generation of the disk drive industry decreases the MR stripe width, decreasing the ESD robustness of the MR head device.

Figure 1.10 shows ESD sensitivity as a function of device type.

1.3.3 ESD Sensitivity as a Function of Product Type

Product application also plays a key role in the sensitivity. This is due to circuit choices, chip architecture, and application performance objectives. Product application architecture in mixed signal chips, system-on-chip (SOC), and network-on-chip (NOC) leads to segmentation of the power grid in a single chip. With improper architecture between the different power

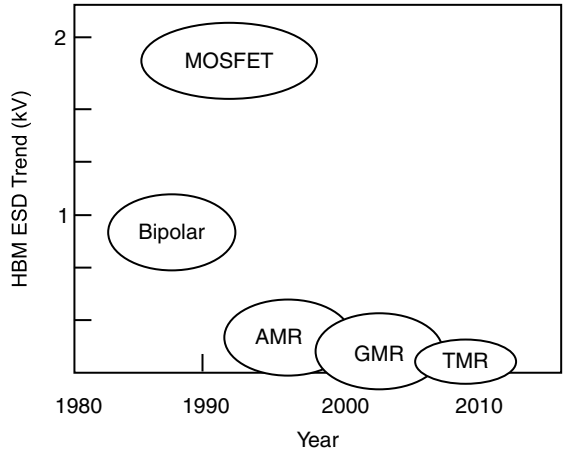

Figure 1.10 ESD sensitivity versus technology type

domains, ESD events can occur. In many product applications, such as RFID chips and low noise amplifiers (LNAs), there are stringent cost, performance, noise, and leakage specifications, limiting the ability to adequately protect these product applications. Hence, the product application limits can lead to ESD-sensitive applications (Figure 1.11).

1.3.4 ESD and Technology Scaling

A significant issue today is the implication of technology scaling [12–22]. In the early 1970s, the understanding of ESD protection was focused on the power-to-failure of single-component semiconductors [26–34]. The focus was based on quantifying components' resistance to electromagnetic pulse (EMP) events. In the 1980s, with the introduction of the MOSFET, ESD learning increased in n-channel MOSFET technology. With the introduction of CMOS technology, convergence of cross-corporate ESD learning focused on diode- and MOSFET-based ESD protection networks.

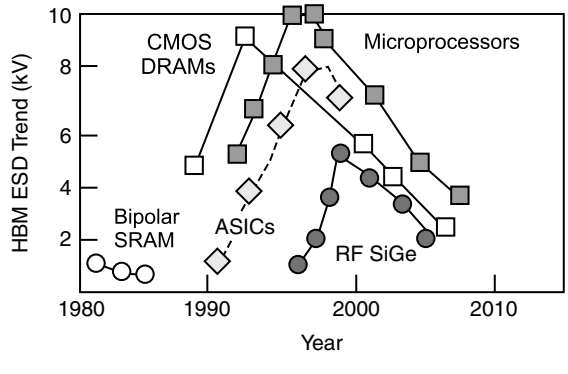

Figure 1.11 ESD sensitivity versus product application

From 1985, ESD learning was driven by major corporations, with the introduction of experimental design, design layouts, ESD mechanism understanding, standards development, and new ESD circuits. In this time frame, the transition to silicided junctions, low doped drains (L_{DD}), and double-diffused low doped drains (DD-L_{DD}) also led to the reduction of ESD capability followed by accelerated ESD learning. This trend continued into the 1990s. Evolutionary and revolutionary changes began in the CMOS technology with the migration from LOCOS to STI, titanium silicide ($TiSi_x$) to cobalt silicide ($CoSi_x$), L_{DD} to extension implants, aluminum to copper interconnects, and introduction of low-k materials [1,12–22]. With the proliferation of common ESD design practices and ESD knowledge dissemination, the learning trend overcame many of the technological evolutionary changes [17–22]. In fact, the upturn continued since many of the technological process changes for chip performance were also favorable for ESD robustness of semiconductor components. High corporate ESD quality/reliability objectives and targets in HBM, MM, and CDM were established, as well as ESD margins relative to the ESD specification levels. In turn, customer expectations also increased placing more pressure on achieving better ESD protection. Additionally, design rule checking (DRC), logical to physical checking (LVS), and verification methods were installed to prevent ESD-related design errors.

But, as we approached the millennium, performance limitation and scaling had been a concern due to the struggling ability to maintain Moore's law performance objectives [17,20,22]. As a result, the peak ESD protection levels occurred in the time frame between 1997 and 2000. After 2000, the electronic industry continued to scale micro-electronic structures to achieve faster devices. Technological advancements, material changes, design techniques, and simulation could have fended off this growing concern, but the physical limitation of interconnect widths, ESD devices sizes, and ESD device capacitance load pressured the semiconductor industry to accept lower ESD protection levels in order to preserve the circuit and chip performance objectives. Since 2000, CMOS technology scaling has continued to encounter technological, material, and yield limitations. MOSFET constant electric field scaling theory decreases the transistor dimensions to maintain the same electric field across the oxide film. With oxide scaling, the gate dielectric breakdown voltage also decreases. For reasons of dimensional similitude, the MOSFET channel length (L_{eff}) and other physical dimensions decrease. MOSFET L_{eff} scaling decreases the MOSFET avalanche breakdown and MOSFET snapback trigger voltage. MOSFET scaling theory leads to higher doping concentration. As a result, the scaling of MOSFETs plays a profound role in the ESD robustness of the MOSFET transistor.

Scaling and the desire for improved performance have influenced both the silicon devices and wiring interconnects used in silicon technology. To improve the speed of high performance chips, and to maintain dimensional similitude with the MOSFET transistor, interconnects are also scaled and material changes continue to change. To achieve faster devices, interconnects have moved from aluminum (Al) based to copper (Cu) based interconnect systems to reduce resistance [15]. To reduce the line-to-line coupling capacitance, new ILD materials with lower dielectric constants have continued interest. ESD robustness of the wire interconnect and ILD are a strong function of the material melting temperature, stress characteristics, and dimensions. The material change, wiring hierarchy, and architectures of the wire interconnects/dielectric system have significant influence on the ESD robustness of high pin count advanced technology.

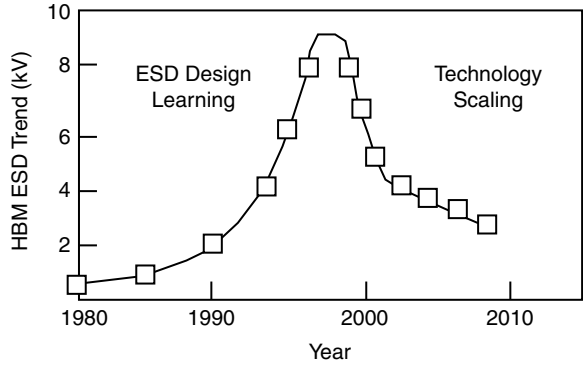

Figure 1.12 ESD technology roadmap. Reproduced by permission of the ESD Association [36]

With the growth of mobility and portability of today's society, RF technology and applications continue to grow at rapid pace. With cellular telephones, and the Internet, the wired and wireless marketplace will experience rapid growth in the next decade. In the last four years, significant progress has been demonstrated in the performance of SiGe ESD protection [1–3]. But, in the field of GaAs devices, solutions and progress in ESD protection have been slower and more difficult due to the lack of integration with silicon technology. Off-chip solutions, field emission devices (FEDs), spark gaps and surge protection devices may be the path to address these future issues [3].

1.3.5 ESD Technology Roadmap

During the 1980s and 1990s, ESD protection was limited by the lack of proliferation, dissemination, and development of ESD knowledge across the industry. ESD learning in many sub-disciplines increased leading to a 15-year increase in ESD protection levels in the semiconductor industry. In this time frame, evolutionary technology changes were overcome by accelerated discovery, learning, and compensation methods. But, in recent years, with the rapid acceleration of circuit performance objectives, ESD results have begun to decrease because of the inability to address the capacitive loading issues as well as areal limitations. As a result, the capability to protect semiconductor chips with on-chip ESD solutions has been showing a decreased trend which will continue in each technology generation forward. This ESD technology roadmap focuses on the high performance application space, where the technology generation continues to be reduced (Figure 1.12) [17].

1.4 HOW DO SEMICONDUCTOR CHIPS FAIL—ARE THE FAILURES RANDOM OR SYSTEMATIC?

A key question is whether ESD failure of components is a random phenomenon, or a non-random systematic process. ESD product sensitivity is a function of the statistical variations of the structure as well as the statistical variations of the pulse event. So, the question really has two parts to be answered. A first question: Is the ESD component sensitivity

a random process? A second question: Is the ESD source event a random or systematic process? Then, a third question: Is the ESD failure rate a random or systematic process?

Statistics of failure are important in order to predict failure in a real environment. The statistical variation of a nanostructure device is dependent on the variations of the geometrical dimensions, and doping concentrations. In semiconductor processing there are both random and systematic processes. In a semiconductor device, the variations of the geometrical dimensions are dependent on the photolithography, etch process, implant, and diffusion processes. In these processes, random as well as systematic effects exist. There are microscopic and macroscopic variations leading to both "local" or "global" changes. For example, in a photolithography process there are both systematic and random phenomena that lead to non-Gaussian distributions.

Additionally, the macroscopic global variations have a higher scale associated with manufacturing process variations. Such manufacturing process variations can consist of within-wafer die-to-die, wafer-to-wafer, lot-to-lot, and semiconductor fabricator site-to-site variations. These variations can be caused by process variations within a semiconductor tool, tool-to-tool, as well as incoming wafers. It is also not uncommon that multiple suppliers produce a given semiconductor chip identical in design or product with completely different semiconductor processes. In a semiconductor chip, there are also variations on a higher scale. Wire bond, package, and board design can also influence the failure on a chip, or packaged level. As a result, ESD variation contains both systematic and random variation.

In practice, one can observe both the random and systematic variation associated with the process statistical variation as well as poorly controlled parameters that influence the ESD circuits. For example, epitaxial variations of a wafer can have a strong influence on the p-well and n-well sheet resistance, which can lead to strong variations in the ESD performance of ESD diodes [1]. These are strongly systematic changes associated with a dominant variable that plays a key role in ESD device operation.

For the second issue there is the issue of the pulse source itself or the ESD event that is occurring. There are two issues. First, there are the actual events observed in the shipping, handling, and equipment environment. Second, there are the ESD test simulators to verify the ESD robustness of semiconductor components.

In the case of ESD testing, statistical variations also exist in the ESD testers. The electrical discharge imposed on the semiconductor chips has both voltage and current variations in the electrical discharge applied. As a result, there are random statistical variations within the testers associated with the arc discharge in the system. Yet, there are also some systematic effects that influence the simulators. There are pre- and post-charging phenomena prior to the application of the pulse stress, which are highly systematic and dependent on the ESD test simulator design.

In the manufacturing environment, there are both systematic and non-systematic random events. In the majority of cases when semiconductor chip failure occurs, it is systematic. The systematic dependence is associated with a manufacturing tool or process that does not conform to the ESD test floor requirements. Example processes that lead to systematic ESD failures are as follows:

- Handling tool out of specification.
- Manufacturing workers handling chips differently based on their finger lengths.
- Manufacturing worker proximity to the product in a sealed environment.

- Lack of ionization process in dicing saw.
- Air ionizer ion spatial distribution.
- Conductive table tops and improper handling procedures.
- Improper loading of chips into shipping tubes.
- Insulating films on improperly grounded manufacturing conveyer belts.
- Improper carbon distribution in wafer carriers and boxes.
- Improper carbon extrusion in chip shipping trays.

These processes are non-random processes that occur in the manufacturing process. Whereas many of us would like to think of simple statistical models, in reality the actual manufacturing floor issues are non-random processes but more associated with non-compliant business practices, materials, or uninspected tooling. When these occur, significant hardware can be damaged by the ESD events. Whereas many engineers believe the ESD problem has a small yield impact, in many of these cases the failure rate can be as high as 100% of the shipped product.

In the case of a known controlled ESD event, statistical models can be applied to the analysis, such as Gaussian statistical analysis applied for predictive analysis. In the early development of semiconductors, it was important for applications to be able to provide good prediction capabilities of failure. The relationship between ESD failures and the statistics of failure were investigated by D. Alexander and E. Enlow [32], E. Enlow [33], W. Brown [31], and lastly D. Pierce and R. Mason [34]. Statistical methods were developed which utilized the physics of failure models combined with variation assumptions in the semiconductor industry. This will be discussed in greater depth in Chapter 2 on physical models.

1.5 CLOSING COMMENTS AND SUMMARY

In this chapter, the text opened with a discussion of the fundamental concepts of failure analysis and ESD. The chapter discussed what failure is, and how we use the failure analysis to design better semiconductor chips. The chapter discussed how to go beyond determining the root cause and failure, and to utilize the information to diagnose the semiconductor chip and the circuits; this is achieved by evaluation of the temperature, the power, the power distribution, and the current paths. The chapter also provides a brief introduction to the failure analysis tools used today to evaluate ESD failures in semiconductor chips.

In Chapter 2, the text will discuss failure analysis tools, ESD pulse models, and electro-thermal models.

PROBLEMS

1.1. List the ways in which failure analysis can help build better semiconductor chips.

1.2. List the failure analysis tools used today. Highlight the reasons why you would use each specific failure analysis tool, and what advantages it would have.

1.3. List the failure analysis tools used today. Explain the difficulties of each method, what it provides, and the necessary time needed to prepare. Which tools are the most effective in providing quick feedback of semiconductor chip problems?

1.4. List all the materials used today in semiconductor chips. List the melting temperature of each of the materials. Assuming that all regions of a semiconductor device are at the same temperature, list the order of failure.

1.5. Given a semiconductor chip, which is tested in small increments, provide a list of all ESD metrics which are useful for quantification. Assume that all identical pins form their own Gaussian distribution.

1.6. Given a chip with "array I/O," the pads are not always placed over the standard cell, and must be wired with a design level "transfer wire" to reach the standard cell containing the ESD element. In some cases, the ESD and standard cell are directly under the pad. Experimental results showed two distributions: the case of the pad over the ESD/standard cell, and a second where it was not directly underneath. What is the cause of failure? Why? Draw the failure distribution.

1.7. Semiconductor chips are diced using a saw. In the dicing process, water is sprayed on the region of the dicing. In semiconductor chips, solder balls are placed on metal pads, but are not electrically connected to circuitry. Describe the failure mechanism and charging process. How do you fix the ESD failure? How do you fix the manufacturing dicing saw process?

1.8. A magneto-resistive (MR) head is placed in a conductive tray which has poorly distributed carbon in the plastic. Explain the potential failure of the MR head. How do you quantify the distribution of carbon in the shipping tray? Define a test method. What conductivity of the plastic is a good value to prevent ESD concerns?

1.9. A semiconductor chip has a metallic outer package. To prevent scratches to the paint, non-conductive tape is placed on the conveyer belt. Charging occurs at the wheel of the conveyer belt, transferring the charge to the semiconductor chip package. At the end of the conveyer belt, a manufacturing line person picks up the chip and places it in a tray. Describe the possible failure mechanism. Is it HBM, MM, or CDM? What circuits are most likely to fail?

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