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Fan-Out Wafer and Panel Level Packaging Market and Technology Trends

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1.1 Introduction to Fan-Out Packaging

1.1.1 Historical Perspective

All great technological revolutions have been driven by relentless innovation and commercialized out of need. Each breakthrough compounds existing and past technologies to create a product that is much better than the previous one. Semiconductor packaging has been unfolding on many fronts for many decades. When surface mount technology (SMT) was established in the 1980s and ball grid array (BGA) was introduced in the 1990s, they enabled a major reduction in size of all electronic systems. In the twenty-first century, newly emerged end-user systems in consumer electronics and mobile devices have become the core pillars of modernized progress and economic growth. One major evolution of mobile devices is the smartphone. Diversified application needs coupled with the slowing down of Moore's law has turned the attention of the semiconductor industry to advanced packaging technology for enhanced system-level performance and functionality as well as a smaller form factor, reduced power consumption, and cost-effectiveness. In fact, key platforms of advanced packaging technologies, such as flip-chip, fan-out (FO), and fan-in, as illustrated in Figure 1.1, have enabled better performance with new functionality, all achieved in the smaller form factor that makes today's sleek yet powerful smartphone a reality.

Since 2000, there has been a widespread adoption of wafer-level packaging (WLP), in which most of the packaging and testing is accomplished in full wafer form. WLP does not require an intermediate integrated circuit (IC) substrate, thus allowing a thinner package profile, and it can be directly mounted onto the motherboard. Specific to fan-out packaging (FO) are interconnects that go

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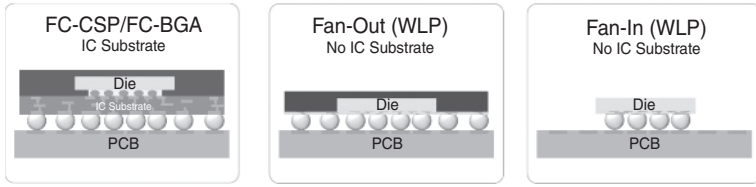


Figure 1.1 Schematic of flip-chip chip-scale package (FC-CSP) and flip chip BGA (FC-BGA), fan-out, and fan-in.

beyond the chip edge and allow multi-chip and 2.5D and 3D packaging solutions. FO technology can be used to fabricate a redistribution layer (RDL) interposer, which is a low-cost alternative to 2.5D packaging. Also, FO technology facilitates multi-die stacking in the vertical direction to enable 3D packaging solutions. These benefits of input/output (IO) density scalability and the integration of passive and active chips in the same package with drastic miniaturization potential by means of 2D, 2.5D, and 3D structures have made FO one of the top options in semiconductor packaging. Since then, there have been unprecedented levels of integration breakthroughs, with an overlap in design, manufacturing, and with companies between front-end (FE) and back-end (BE). Figure 1.2 represents a "middle-end" zone, where bumping and packaging can be executed at the wafer level, with a FO package teardown as an example.

The commercialization history of FO dates back more than a decade, as shown in Figure 1.3. In 2006, Freescale established its first 200 mm pilot line for the redistributed chip package (RCP) in Tempe, Arizona, USA. [1] Back then, RCP was viewed as a disruptive technology that could not only eliminate interconnects such as flip-chip bumps and wire bonds and IC substrates but also did not require

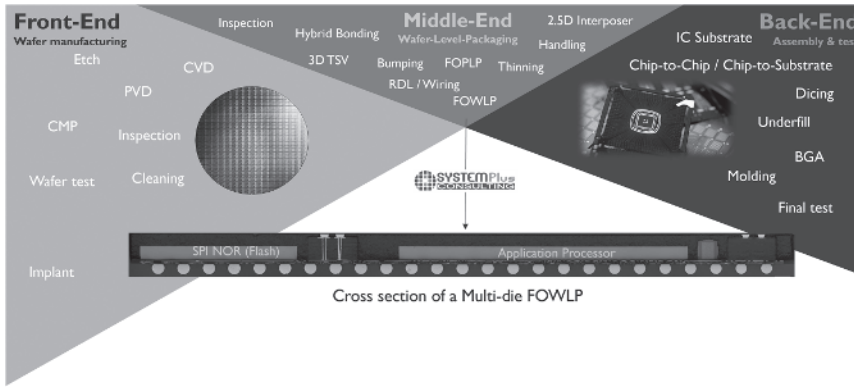


Figure 1.2 WLP is the "middle-end" between FE and BE.

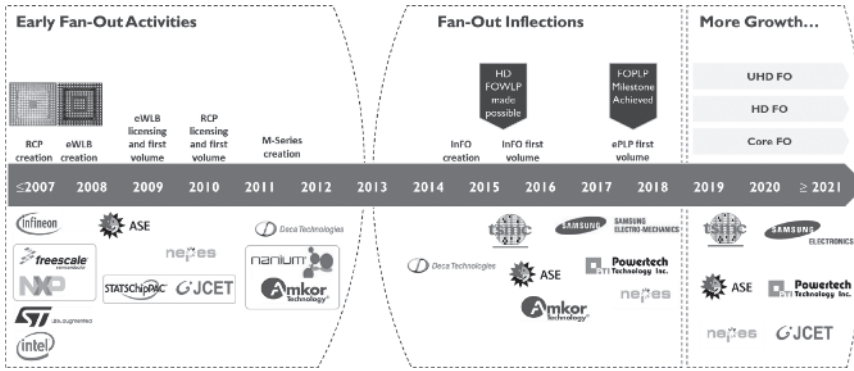


Figure 1.3 FO-WLP evolution.

thinned die to achieve thin package profiles. Then in 2010, Freescale and Nepes collaborated in a joint development effort to enhance further the capabilities of RCP technology, setting up a 300 mm RCP line in Nepes' Singapore facility. Nepes was Freescale's first large-scale partner for RCP licensing. In 2015, NXP acquired Freescale, so NXP now owns and manufactures the RCP technology.

In addition, Infineon is the originator of embedded wafer-level BGA (eWLB), a chip-first face-down solution that was developed from 2001 to 2008. [2] In 2007, Infineon and ASE declared an eWLB manufacturing partnership under a license model. [3] Knowing that a legal licensing partnership can combine the developed eWLB technology with the packaging know-how of an outsourced assembly and test (OSAT) supplier, Infineon started to license more liberally. Since 2007, Infineon has licensed eWLB solutions to ASE, Amkor Portugal (formerly known as Nanium), JCET Group (formerly known as STATS ChipPAC), and STMicroelectronics. [4, 5] The licensee has the right to manufacture eWLB. Intel, by virtue of its acquisition of Infineon's wireless business, also has access to eWLB technology. [6]

From 2008 to 2009, ASE installed a 200 mm production line for fan-out wafer-level packaging (FO-WLP) based on eWLB but subsequently stopped production in 2012 because the market at that time was not big enough to maintain manufacturing activities. In 2014, ASE reentered the market and invested in a 300 mm FO production line, which proved to be successful in gaining Qualcomm's business in 2016. ASE also developed and invested in other FO-WLP technologies and licensed Deca Technologies' solution in 2016. So ASE has a highly diversified FO-WLP portfolio with eWLB license, M-Series license, as well as their own in-house fan-out chip on substrate (FOCoS) and fan-out panel-level packaging (FO-PLP).

In 2009, STATS ChipPAC first qualified eWLB in its 200 mm production line to be a second source of Infineon's eWLB for its baseband products. JCET acquired STATS ChipPAC for $780 M in November 2014 and is driving the company to a major position in the FO-WLP market. STATS ChipPAC at the time led the market, and by May 2016 they had shipped more than 1 billion units of eWLB packages since 2009, reaching more than 2 billion units in 2018. [7] STATS ChipPAC is essentially focusing production on core FO-WLP volume applications, which means lower-end packages for baseband modems (BB), power management ICs (PMIC), and radio frequency (RF) devices, but is also positioned in the system-in-package (SiP) market. Due to cost reduction pressure, there are both 300 mm and 330 mm production lines. The 330 mm panel size allows for economy of scale.

In 2011, Nanium was the second company to qualify 300 mm eWLB in high-volume production and shipped 200 million eWLB components in less than two years. [8] The company quickly developed eWLB based on its 300 mm RDL capability, initially developed for the stacked dynamic random-access memory (DRAM) market. Nanium's eWLB packaging production lines (two 300 mm lines) have been fully operational since 2012. Nanium's business model was to develop more high-integration applications such as multi-chip package (MCP) and SiP in the mobile, industrial, medical, and automotive markets to create more added value and not rely only on single die packages in mobile, which was the main market and where competition only got tougher. In February 2017, Nanium was acquired by Amkor [9].

In 2011, Deca Technologies released their M-Series using their adaptive patterning (AP) technology. Deca's M-Series offers a different type of solution—it is a chip-first face-up solution using an AP software technology to solve pattern misalignment issues. [10] Deca Technologies reported in 2015 having sold more than 100 million units since 2011 and have achieved much larger volumes based on the investment of $60 M from ASE to license the technology and $50 M from Qualcomm. In 2019, Nepes acquired Deca's Philippines operation, liberating Deca from the manufacturing business. [12] Beyond 2019, Deca repositioned its business model from manufacturing to licensing.

In 2015, Amkor presented two chip-last solutions: SWIFT (silicon wafer integrated fan-out technology) and SLIM (silicon-less integrated module). [13] While SWIFT's target markets are sweet spots for FO-WLP (BB for mobile, RF, etc.) and high-density FO-WLP such as application process engines (APE), SLIM is more focused on applications requiring very high I/O counts or high-resolution connections, such as memory with central process units (CPU) or graphics processing units (GPU) or system-on-chip (SoC) partitioning, and complex SiP. Through the purchase of Nanium in 2017, Amkor redefined its strategy regarding FO-WLP. Nanium's know-how and eWLB technology will focus on core FO-WLP

while SWIFT solutions will target more advanced applications, high-density (HD) FO-WLP or ultra-high-density (UHD) FO-WLP. Due to some overlap with SWIFT and with a higher cost, SLIM technology is no longer actively offered.

It was not until 2016 that FO-WLP experienced a significant inflection point when TSMC's integrated FO-WLP (InFO) technology first broke into the market, resulting in a whole new higher-end market segment, defined as high-density fan-out (HD FO) due to its embedding of large die (> 10 mm × 10 mm), with finer line and space (L/S) RDL and higher I/O (> 1000), commercialized for Apple's iPhone APE. [14] It was during this phase that the industry started to realize how important the use of FO-WLP is for higher-end applications. This inflection point was a massive boost for the FO-WLP platform as it was then proven for one of the most important applications in smartphones for one of the biggest original equipment manufacturer (OEM) brands, Apple.

Thus, a new wave of FO-WLP innovations followed, with newcomers entering the supply chain. Since 2016, InFO remains a key FO-WLP product offered by TSMC to support mobile smartphones, wearable smartwatches, and even high-performance computing with new InFO variants such as InFO on substrate (InFO_oS), which is defined as ultra-high-density fan-out (UHD FO).

The invention of HD FO was highly beneficial for the FO-WLP market space as another major player, Samsung Electronics, started to invest in Samsung Electro-Mechanics' (SEMCO) HD FO solution with panel-level packaging in 2017. [15] In 2018, SEMCO successfully developed the FO-PLP-based APE-PMIC solution and commercialized it in the Samsung Galaxy Watch. SEMCO's FO-PLP technology set an unprecedented milestone with the penetration of FO-PLP into the consumer market. This is viewed by many as direct competition against TSMC's InFO in the mobile market although FO-PLP does not have the L/S density of InFO. In 2019, Samsung Electronics acquired SEMCO's FO-PLP for $750 M. [16] The synergy between FE and packaging technologies may bring more efficiency under one umbrella, as with TSMC's model (FE + packaging).

In 2017, Powertech announced the production of different FO-WLP technologies: CHIEFS (chip integration embedded fan-out solution) and CLIP (chip-last integration package). This offer was rounded off by PiFO (pillars in fan-out) and BF^2O (bump free fan-out). Backed-up by their strong position in memory and field programmable gate array (FPGA) packaging, Power Technology Incorporated's (PTI) FO-PLP will be a promising alternative to replace part of the high-cost 2.5D and 3DIC market. They also targeted high I/O counts and multiple-chip integrations, such as SoC and memory, baseband, wireless modules, and wide I/O memory. Being one of the first companies to go to panel meant many challenges and risks in process making and reliability but if achieved, it could bring down the cost by 30 to 40%. In 2018, PTI announced a $1.6B investment plan to construct a new advanced packaging plant at the Hsinchu Science Park. [17]

1.1.2 Key Drivers: Why Fan-Out Packaging?

FO-WLP is a versatile semiconductor packaging technology that can be used for various key applications, such as departitioned large processor die, mobile APE, automotive radar and RF, audio codec, PMIC and potentially 5G antennae in package (AiP). It has the advantage of a thinner package size, improved RF performance, higher I/O density, and lower thermal resistance as compared with the conventional flip-chip. Besides fanning out of the electrical I/O, it can also be used for various 2.5D and 3D multi-chip integrations. Today, FO-WLP has evolved from a low-end packaging technology into high-performance and cost-effective integration platforms, as shown in Figure 1.4.

A strong demand for high performance compute (HPC) systems and data centers has emerged in recent years. Fabless and OEMs are delivering technology solutions to drive the hyper-scale data centers and accelerate the growth of artificial intelligence (AI) and machine learning (ML). 2.5D/3D heterogeneous packaging is known to greatly increase computing power. Due to process node scaling limitations in the Si wafer fab, performance scaling requires a bigger die, and yield-cost is a big concern simply because the die is bigger. Hence, the industry is now cutting the big die into smaller pieces and relying on advanced packaging solutions to integrate die together with the shortest and densest interconnections. Flip-chip BGA (FC-BGA) substrate manufacturing is a mature process. However, if we go below a L/S of 8 μm/8 μm for the multilayer FC-BGA substrate, the yield decreases. Moreover, reliability concerns have emerged when testing under high and low temperature and humidity conditions. Therefore, many fabless companies, such as MediaTek and HiSilicon, have been actively qualifying HD FO-WLP. Preliminary

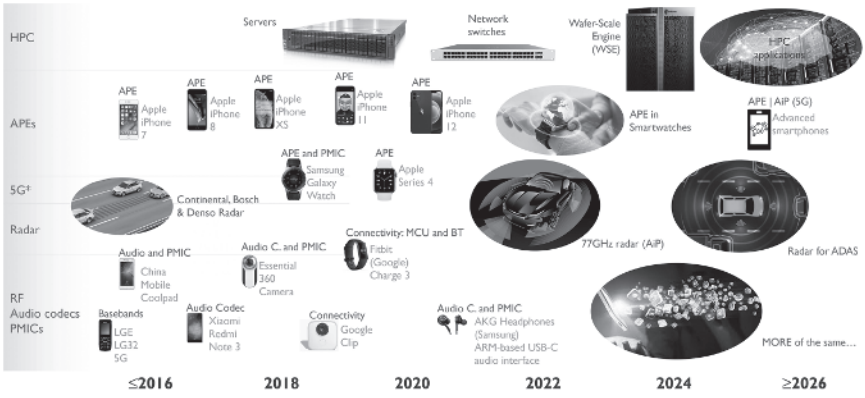


Figure 1.4 Roadmap of fan-out packaging market drivers.

data has shown that FO-WLP can handle the bandwidth and high speed SERDES signal. So FO-WLP can indeed increase the gross die size by combining smaller die in the package as an alternative to improving the wafer yield when the silicon die size is usually enormous and suffers from low yield issues, especially in advanced wafer processes.

In 2016, TSMC with its FE 10 nm logic and BE InFO package-on-package (InFO_PoP) technology (HD FO) successfully obtained orders for Apple's A11 APE, powering the iPhone 7. Apple APE continues to be packaged in InFO_PoP today. In 2018, Samsung used HD FO-PLP for its APE and PMIC for smartwatches as has Apple for its smartwatches. This trend will probably continue because HD FO will continue to be used for devices that need higher performance yet a reduction in total package dimension.

One of the early adopters of FO-WLP is automotive radar, especially at the higher frequencies of > 76–81 GHz. In 2012, the first 77 GHz radar monolithic microwave integrated circuit (MMIC) was commercialized by Infineon with their eWLB technology. Since then, the use of radar sensors has become widespread as companies have been trying to implement radar and other components in a package, thus integrating more die at a lower system cost. Advancements in packaging (especially FO-WLP) enables the integration of antenna and RF chips to perform at a higher efficiency level. This is opening the door to meet the demands of automotive radar for next-generation automotive capabilities such as advanced driver assistance systems (ADAS).

77 GHz radar sensors with FO-WLP are already well adopted in the automotive market for cabin or infotainment and ADAS safety. 5G mmWave, which operates at similar high frequency range > 60 GHz, requires higher data rates along with wider bandwidth. As we enter this new decade, one thing is certain: 5G mmWave adoption will continue to grow since companies are accelerating toward this common goal. To achieve wide bandwidth, a higher frequency (thus mmWave solution) is needed. However, this wavelength is similar to the interconnect length in an IC package. For this reason, signal loss from the RF chip to the antenna is expected. In order to reduce the loss with shorter interconnect lines, the antenna is designed into the package.

TSMC has published multiple technical papers to demonstrate how InFO_AiP can enable low transmission loss and high antenna performance for mmWave system integration, as compared to flip-chip IC substrates. [18, 19] However, the implementation of InFO_AiP will depend on Apple's decision. Apple is now internally developing the various 5G RF chipsets including modem and RFIC. Currently mmWave AiPs in iPhones use Qualcomm chipsets. Apple will likely implement FO-WLP AiP when they develop their own chipsets.

1.1.3 FO-WLP vs. FO-PLP

FO-WLP is still considered a costly platform as compared to a conventional packaging platform such as flip-chip or wire-bond. Hence, FO-WLP is adopted in limited applications, such as audio codecs, connectivity, microcontroller units (MCU), power management ICs (PMICs), and RF. It is still too expensive for many low-end applications.

Purchasers of FO-WLP have been trying to drive down the manufacturing cost. A significant cost reduction is highly attractive for the companies to achieve strong profit margins. Within the FO-WLP market, FO-PLP is a possibility for cost-reduction due to the economies of scale of its manufacturing process. Qualcomm and MediaTek are two prominent companies demanding it.

FO-PLP does not make sense if volume is not high, and capital expenditure (CapEx) and return on investment (ROI) are not justifiable. Some view FO-PLP as one of the ways to by-pass the intellectual property (IP) of FO-WLP, which is saturated. Some believe FO-PLP is the only way to reduce cost. Opinions are highly divided. Pro-FO-WLP companies are no longer underestimating FO-PLP penetration. In fact, more companies are currently being swayed toward FO-PLP. Pro-FO-WLP companies are concerned that if FO-PLP really takes off, then the price point of FO-WLP is no longer competitive. Coupled with a strong end-customer push for cost reduction, we are seeing more companies such as PTI, SEMCO, ESWIN, ASE, Nepes, and Deca venturing into FO-PLP. On the other hand, some companies prefer to wait and observe the progress first, unwilling to invest in FO-PLP without volume. To them, panel-level needs to see very-high volume to really take off.

To understand the theoretical benefit of FO-PLP, an equipment throughput model is established to compare the impact on the number of tools needed for production between FO-WLP vs. FO-PLP, as shown in Figure 1.5.

In this model, the production volume needed for the FO-WLP market is 1 941 605 wafers (300 mm equivalent) which Yole Développement reports was the total FO production volume for 2018. With similar throughput, FO-PLP needs fewer tools than FO-WLP when trying to produce the 1.941M wafers mentioned above. The difference in the number of tools required between FO-WLP and FO-PLP are more significant at a lower throughput of 10 carriers per hour (difference of 17 tools) as compared to 40 carriers per hour (difference of 4 tools). The difference in number of tool units is bigger when the process throughput is lower because more tools will be needed to meet the 1.941M wafer requirement at this low throughput. From a ratio point of view, FO-PLP needs about 3 times fewer tool units as compared to FO-WLP, assuming same yield and tool throughput.

1.1.4 Future of Fan-Out Packaging for Heterogeneous Integration

The trend is to go for more integration, and FO-WLP is a potential candidate for future scaling into heterogeneous integration. This opens the way for new

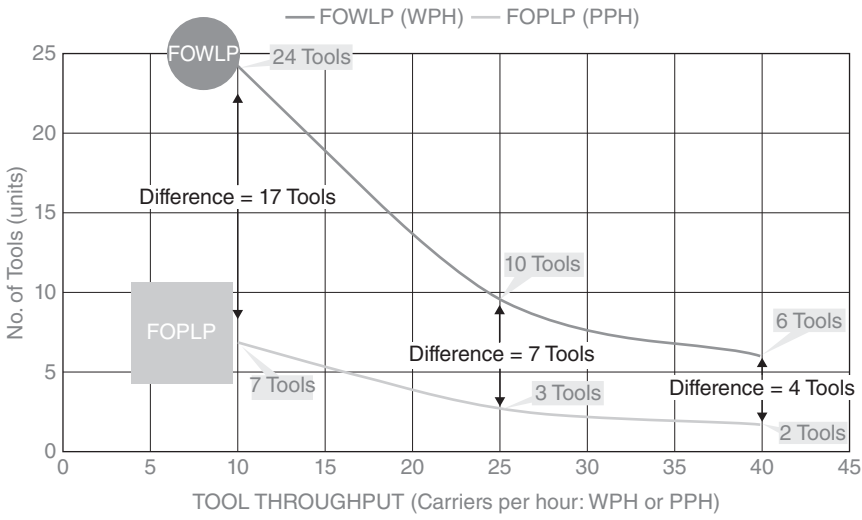


Figure 1.5 FO-WLP vs. FO-PLP: carrier impact on No. of tools.

MCMs (multi-chip module), PoPs (package-on-package), and SiPs. FO-WLP's differentiating characteristic is the ability to embed a wide range of die (independent of die type, size, or side) allowing many integration possibilities: small die, large die, stacked, or side-by-side multi-die; 2D solutions in single and multi-chip configurations; 2.5D interposer solutions; 3D SiP and PoP solutions that could include face-to-back (active die face to die back) or face-to face (active die face to active die face or F2F) options; or heterogeneous integration with both passive and active components.

FO-WLP is compatible with MCM architecture and enables the inclusion of different die of different types and sizes in the same package. It easily connects them on the same plane, allowing better coupling. FO-WLP solutions can also work in PoP architecture, which enables a 3D approach to reduce footprint and improve electrical and thermal performance even further. FO-WLP allows flexibility in the die to embed: standard IP in IC in the bottom package and multiple die with specific IP in the top package, for instance, to benefit from any appropriate node and die size and all with a small form factor. FO-WLP enables SiP architecture too, which means the capability of embedding and/or connecting numerous die and components in a flexible way to get a single system with only one package.

Moore's law is slowing down, and despite chips becoming smaller and smaller, there are accompanying cost, power management, and heat dissipation challenges. In such a context, more-than-Moore solutions help improve form factor, performance, and cost via innovative ideas. A promising way is to package different die together to gain space and performance at a lower cost. This trend is consistent with the FO solution and is even more favorable because of FO-WLP integration capabilities.

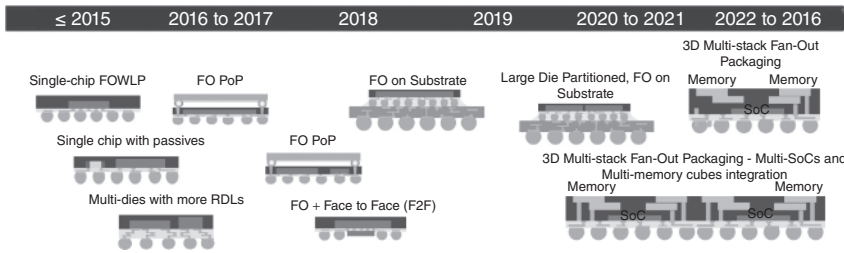


Figure 1.6 Timeline of FO-WLP integration capability.

From Figure 1.6, it is evident the path that FO-WLP will open new ways for MCMs, SiPs, and PoPs manufacturing. Mold compound embedding permitted flexibility in type and size of components to be embedded together in one package. Between 2016 and 2018, the industry further improved the technical capabilities of FO-WLP in the direction of thinner interconnection solutions (RDL, fab back-end of line or BEOL) and more RDL layers, up to 4 layers, moving into HD FO. A combination with RDL on top-face and multiple FO packages brings even thinner PoP, SiP, and face-to-face/face-to-back packaging capability. From 2019 onward, FO packages placed on a substrate that enables larger packages results in a 2.5D-like approach but without the expensive Si interposer with thru silicon vias (TSV) for the high-end application domain. Also, reducing the large single unit die size through the integration of several smaller die using FO-WLP helps to improve the gross die yield. Moving forward, more variants of 3D FO-WLP (such as PoP) are expected for yet thinner profiles, with high memory capacity and memory bandwidth.

1.2 Market Overview and Applications

1.2.1 Fan-Out Packaging Definition

A recognized characteristic of FO packages is that, as the name suggests, interconnections are fanned out on the chip, and because of that, bumping is not dependent on die surface. This means that FO has the potential to achieve any number of interconnects with standard pitches at any shrink stage of the wafer node technology. If the only definition of FO is a package from which connections and bumping are out of the chip scale, then almost all packages can be defined as FO, including FC-BGA, FC-CSP, and embedded die. To make a fair comparison the situation is clarified as shown in Figure 1.7. FO-WLP technologies should have at least one of these two key characteristics: (i) FO-WLP solutions that use mold compound to embed the die—not laminated materials, or (ii) FO-WLP solutions that do not use IC substrates to fan out I/O from chip area.

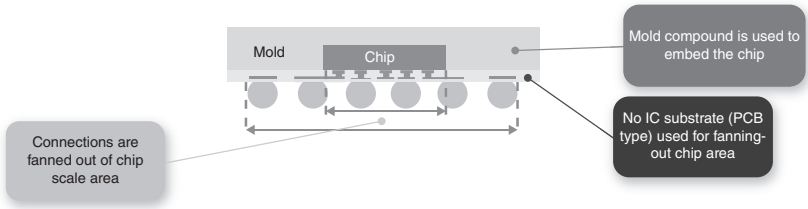


Figure 1.7 Definition of FO-WLP.

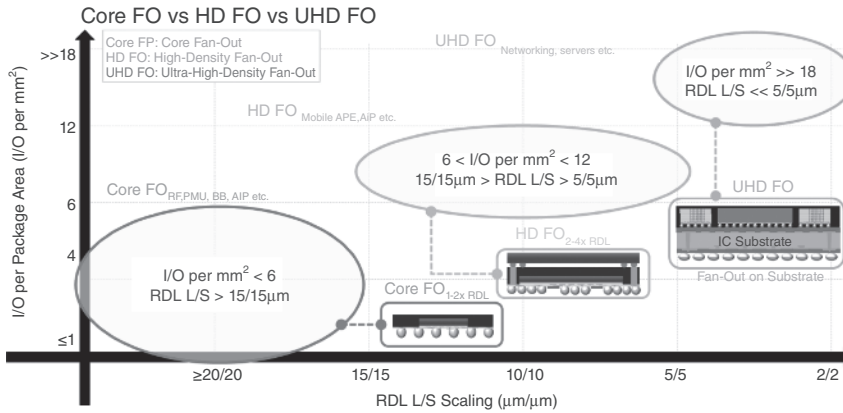


Figure 1.8 Market segmentation of FO.

1.2.2 Market Segmentation: Core FO vs. HD FO vs. UHD FO

FO packaging is penetrating higher-end IO densities, much greater than 18 per mm^2, and finer RDL, with L/S measurements far below 5 µm/5 µm. Along with the proliferation of new technologies and new commercialized products, industry companies are having difficulty segmenting the market.

Figure 1.8 illustrates the market class segmentation of FO packages by UHD FO, HD FO, and core FO. UHD FO is classified as $\gg$ 18 I/O per mm^2 and L/S $\ll$ 5 µm/5 µm, HD FO has between 6 and 12 I/O per mm^2 with L/S between 5 and 15 µm/15 µm, and core FO has $<$ 6 I/O per mm^2 with L/S $>$ 15 µm/15 µm. This technical definition allows the industry to understand and make informed decisions on developments and strategies to gain a competitive advantage within an individual market class and/or different individual market classes. This helps in understanding what capabilities each segment is looking for or offering.

1.2.3 Market Valuation: Forecast of Revenue and Volume

The FO platform is increasingly viewed as one of the top packaging options. FO remains a fast-growing market with revenue growth of 15.9% from 2019 ($1256 M) to 2025 ($3046 M). The revenue varies between different market classes; see Figure 1.9. UHD FO is valued at $504 M in 2019 and is set to reach $1523 M by 2025 at a 20.2% compound annual growth rate (CAGR). Projected at 15.8% CAGR, HD FO is estimated to grow from $534 M in 2019 to $1291 M by 2025. On the other hand, Core FO is expected to reach $231 M by 2025 with a moderately stagnant CAGR of 1% from $218 M in 2019. UHD FO is finding its own market space and is experiencing the fastest growth of 20.2% CAGR. HD FO is already dominant in the market, and the continued expansion indicates that HD FO is driving the overall FO market forward, in a league of its own. For core FO, growth is stagnant with limited expansion.

The current FO-WLP installed based is enough to sustain existing core FO demand. There is no significant expansion for existing end products. Yet, fabless companies continues to push packaging houses for wider adoption at a lower cost. FO production is expected to grow from 1703 kwspy (kilo wafer starts per year) in 2019 to 3419 kwspy by 2025, at a CAGR of 12.3%, as shown in Figure 1.10.

1.2.4 Current and Future Target Markets

Within FO, mobile, consumer, telecom, and infrastructure end markets are influencing the overall trend of FO. These trends are represented in Figure 1.11. Within FO, the mobile and consumer end market leads the market with a revenue of $741 M in 2019, projected to reach $1498 M by 2025 at a 12.5% CAGR. Likewise, the telecom and infrastructure end market is growing strongly with a 20.2% CAGR from $504 M in 2019 to $1523 M in 2025. Automotive and mobility is also

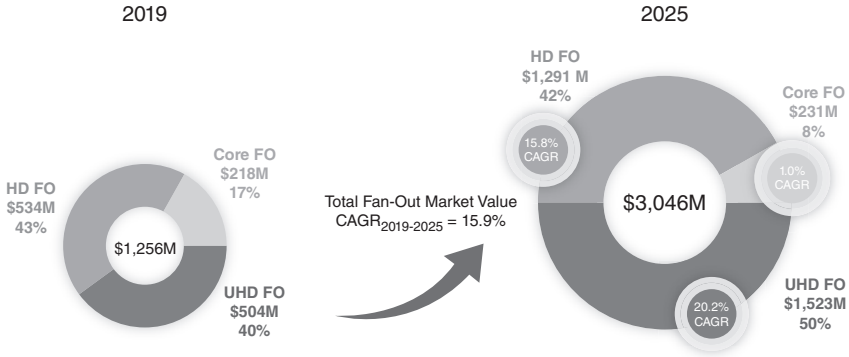
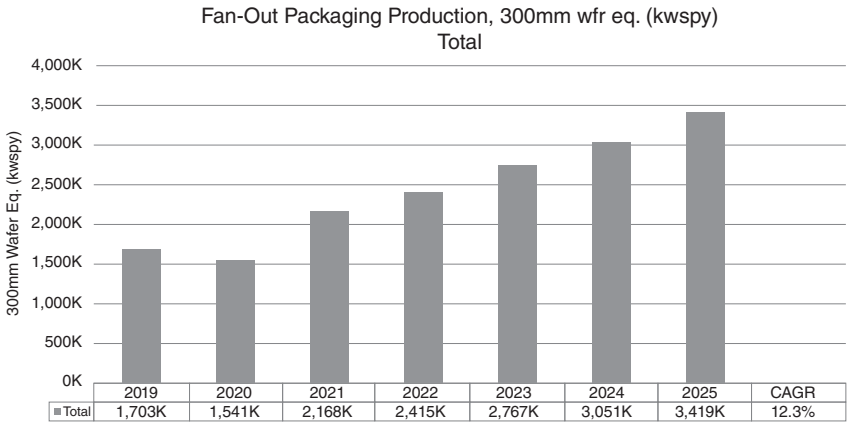
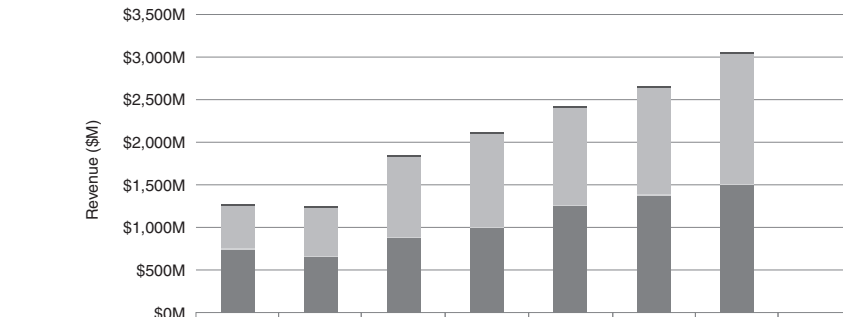


Figure 1.9 Revenue market forecast of fan-out packaging, split by market class.



	2019	2020	2021	2022	2023	2024	2025	CAGR
Total	1,703K	1,541K	2,168K	2,415K	2,767K	3,051K	3,419K	12.3%

Figure 1.10 Production volume forecast of fan-out packaging.



	2019	2020	2021	2022	2023	2024	2025	CAGR
Medical	$0.01M	$0.01M	$0.01M	$0.01M	$0.01M	$0.01M	$0.01M	–4.1%
Telecom & Infrastructure	$504M	$570M	$944M	$1,103M	$1,130M	$1,255M	$1,523M	20.2%
Automotive & Mobility	$11M	$9M	$13M	$17M	$20M	$23M	$24M	13.8%
Mobile & Consumer	$741M	$658M	$883M	$996M	$1,257M	$1,376M	$1,498M	12.5%
Total	$1,256M	$1,237M	$1,840M	$2,115M	$2,407M	$2,654M	$3,046M	15.9%

Figure 1.11 Revenue forecast of fan-out packaging, split by end market.

increasing significantly with 13.8% CAGR from $11 M in 2019 to $24 M in 2025. The medical end market, however, being a relatively smaller-sized market, is expected to see a decline in adoption.

There is an impact in 2020 due to COVID-19. In 2020, the world experienced an unprecedented pandemic, as this novel coronavirus, COVID-19, spread rapidly on a global scale. The number of infected cases continued to increase in the first half of 2020, which triggered lockdowns in various countries, one after another. This has caused a pandemic-driven contraction of economic activity, negatively affecting semiconductor development and production.

FO revenue is heavily dependent on the mobile and consumer end market, with 59% exposure as of 2019. Thus, it was inevitable for FO revenue to experience a decline in 2020, reflecting the COVID-19 effect on mobile and consumer applications. By 2021, on the other hand, data-driven end systems will grow in popularity as COVID-19 is being quelled. Industry companies are prepared to deliver more digital functionalities. Consequently, 5G-led adoption is expected to grow rapidly thereafter.

FO revenue for telecom and infrastructure improved moderately in 2020 and has bounced back strongly in 2021. In fact, FO is experiencing a massive uptick in the demand by telecom and infrastructure end market. End users are not only coming to recognize the crucial role of technology (from supporting remote working to scaling digital operations due to lockdown) but will also invest in and utilize it even more. Hence, more end-system demand will accelerate in HPC applications, shaped by new end-user behavior.

In summary, pent-up demand has returned in 2021. There is a light at the end of the tunnel as more technology-related business leaders are increasingly optimistic that businesses and consumers will stabilize at a new normal. FO will unquestionably ride this wave in 2022 and 2023.

1.2.5 Applications of Fan-Out Packaging

Figure 1.12 shows a comprehensive overview of the most widely used FO applications. There are different levels of classification highlighting key granularities, including end market, application, device, and product model/name. Through this classification, readers can have an overall understanding of FO adoption. With the evolution of FO technologies, the application range is broadening. Because of this, the technology can be targeted toward a wider range of applications.

Since the turn of the twenty-first century, FO has been expanding to encompass a wide range of devices in different applications. Within the mobile and consumer end market, the adoption of FO-WLP is often driven by the reduction in package thickness with higher level of performance integrity. For example, the APE device in Apple's iPhone 7 and beyond is packaged by TSMC InFO_PoP, and Samsung Exynos 9110 APE and PMIC (multi-die) is packaged using FO-PLP and is found in the Samsung Galaxy Watch. Apart from the APE, devices such as PMIC, audio codec, RF transceiver, BB, RF Chip and AiP, MCU and bluetooth (BT), APE and NOR memory, and PMIC are all packaged using FO for mobile smartphones, smartwatches, wearables such as headphones, and internet of things (IoT) applications.

For smartphones, APE packaging is the main contributor to package thickness. It is not strictly linear due to different options in the memory packaging thickness, because there is not much progress seen at memory packaging thickness level.

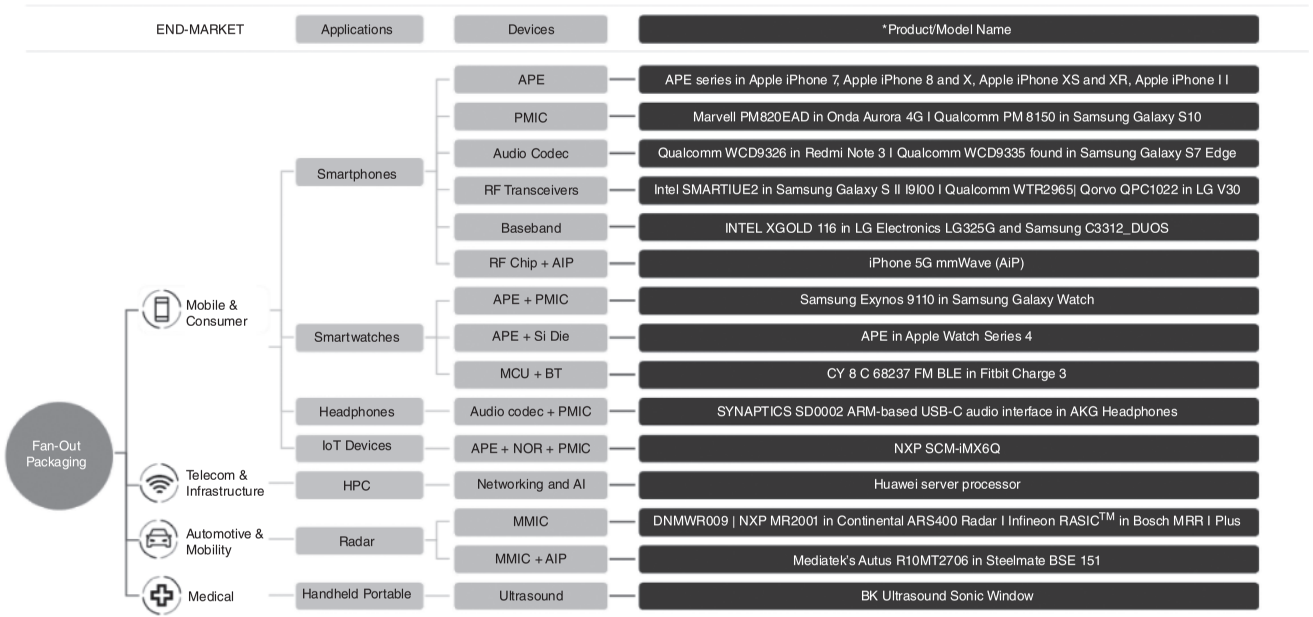


Figure 1.12 Application overview of fan-out packaging. *Non-exhaustive list of companies and products.

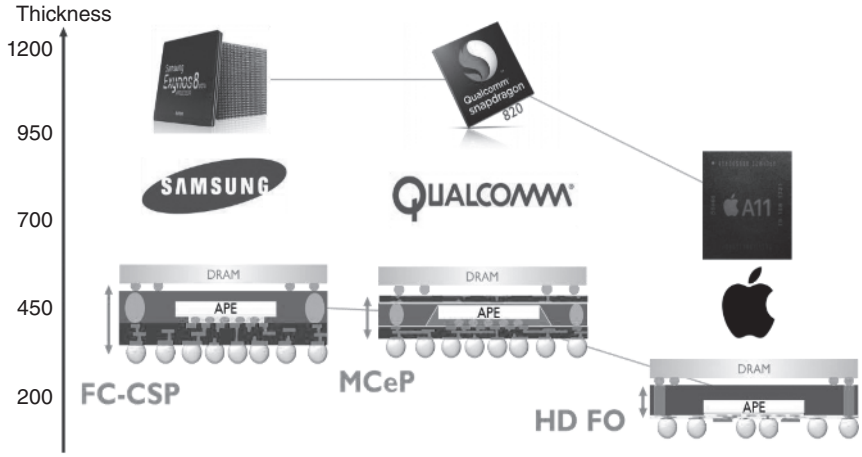


Figure 1.13 Application processing engine (APE): package thickness is significant.

Instead, it is the package choice between FC-CSP versus molded core embedded package (MCeP) versus HD FO that makes a difference. From Figure 1.13, it is clear that FO packaging enables a drastic reduction in thickness of full APE and memory PoP. The package thickness is reduced from 550–425 µm to 231 µm because of HD FO. Thickness is not the only parameter of interest for APE packaging, but it is of high importance for slimmer smartphone design because of a well-managed form factor. Trends in recent years show Apple has leapfrogged other leaders with TSMC's InFO_PoP (HD FO), packaging the APE at lower thickness. Other leaders are keen to decrease thickness to compete. It is known that Qualcomm prefers MCeP and drives innovation via the IC substrate. In 2018, however, Samsung utilized SEMCO's newly developed FO-PLP solution (ePLP) in Samsung Galaxy Watch's APE-PMIC. Although this is a smartwatch (not mobile) and still considered core FO in terms of IO, the APE package thickness is now comparable to TSMC's InFO. This is a milestone for Samsung Electronics on the path to a possible migration of FO technology into Mobile APE–HD FO.

In recent years, FO has been expanding beyond the mobile and consumer markets and penetrated the telecom and infrastructure markets. Currently, the 2.5D Si interposer is one of the best solutions to handle high-end device integration needs, but the 2.5D Si interposer is very expensive. FO offers an alternative solution to 2.5D Si interposer for mid-to-high-end HPC applications that seek cost/performance optimization. Significant cost reduction is achieved by splitting a large-advanced-node networking chip, such as network processor and network switch, into several small networking chips and reconstituting them with UHD FO packaging thus enabling high-density, high-speed interconnects on an IC

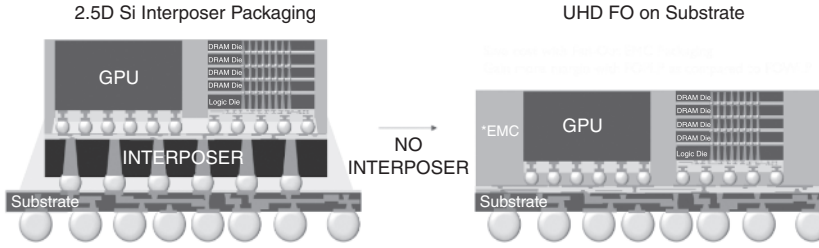


Figure 1.14 Architectural comparison between 2.5D Si interposer vs. UHD FO on substrate.

substrate. Similarly, UHD FO can integrate advanced node GPUs or ASICs with high bandwidth memory (HBM) to support HPC applications, such as fine pitch SERDES interconnects featuring high data rate and high memory data bandwidth communication between compute die and HBM memory. These products make up the heart of UHD FO. A comparison between 2.5D Si interposer vs. UHD FO on substrate can be observed in Figure 1.14.

Within the automotive end market, radar is the device that mainly utilizes FO, for RF performance to transmit and receive signals. Radar for automotive applications now has more functionalities and is becoming widespread. It can precisely locate vehicles in blind spots or approaching from behind. More and more radar sensors are required in cars to improve safety and driving assistance. So far, it is essentially used for adaptive cruise control (long range) and collision / blind spot detection (medium/short range). This trend will become even more pronounced as cars are becoming more and more autonomous. More recently, in 2020, new innovations in AiP FO can be found in MediaTek's Autus R10 MT2706 in the Steelmate BSE151, as shown in Figure 1.15. Key highlights of MediaTek's AiP radar with eWLB are:

- Printed circuit board (PCB) substrate has a ground plane underneath the antennas to bounce back the radiation from the antenna. Easy shielding solution to minimize signal loss.
- Package Area: 39.0 mm^2 | 25% is taken by die | 28% is taken by antennas | Min L/S: 13.6 µm/11.8 µm.
- With AiP, antenna being integrated into package, package area is significantly reduced: −83% as compared with TI antennae on package (AoP) radar and −27% vs. Acconeer AoP radar.
- Note that AoP is mainly done by FC with IC substrate currently.

Similarly, another potential application awaits, FO AiP in 5G applications. In 5G, the challenge is higher-frequency operation. All the packages must be redesigned to optimize signal gains for higher frequencies. It is understood that a

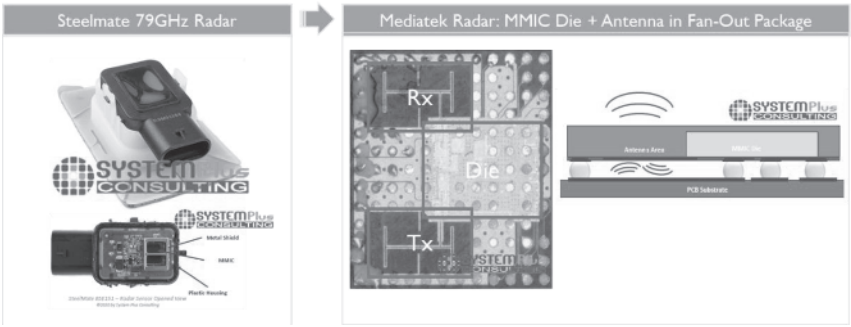


Figure 1.15 Steelmate 77 GHz radar and MediaTek chipset with AiP.

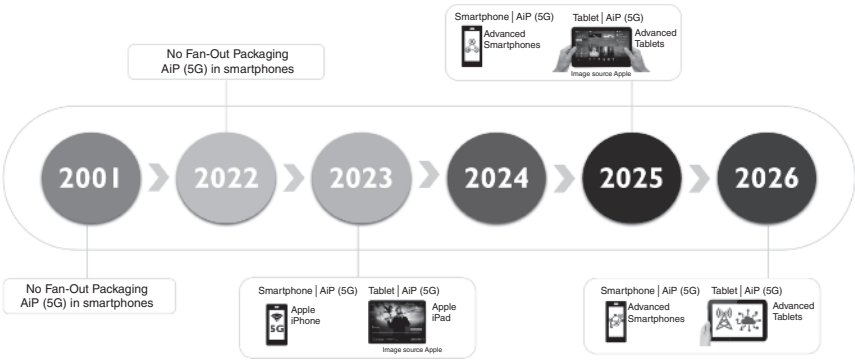


Figure 1.16 Roadmap of FO AiP.

one-millimeter wavelength (mmWave) 5G iPhone will require three to four AiP modules. FO packaging minimizes antenna signal loss in a thinner form factor offering desirable AiP in higher-end phones pursuing sleeker designs. Presently, it is understood that Apple may consider using a phased array antenna in its iPhone, with two parts that work together to form a radio signal beam. This beam can be electronically steered in different directions without moving the antenna. The modem chip and the antenna module work closely together to provide this functionality. We do note that mmWave itself is not new. For example, cars make use of mmWave radar chips operating at 77 GHz. These radar chips, essentially packaged by FO, are used for lane detection and other safety features typically in luxury cars. It is known that TSMC has been highly active in this regard. A potential roadmap is FO AiP being adopted in Apple iPhone, as shown in Figure 1.16.

1.3 Technology Trends and Supply Chain

1.3.1 Fan-Out Packaging Technology Roadmaps

FO is penetrating even higher-end I/O densities, much greater than 18 per mm^2, and finer RDL, with L/S measurements far below 5 μm/5 μm. TSMC and ASE with their FO on substrate technology InFO_oS and FoCoS, respectively, are already in production for networking applications. In the next five years, the package size will exceed 25 mm × 25 mm, and the L/S will go to 2 μm/2 μm and below. The number of RDLs will increase to 4 and above, and the package thickness (without BGA) will go to 150 μm. The FO technology roadmap is shown in the figure below. The roadmap described here in Figure 1.17 is for volume production and an expected average of the different technologies on the market.

The FO architectures with more integration, such as PoP and SiP, will be widespread as the technologies improve (higher I/O count, RDL number, TMV, chip-last, etc.). The FO technology roadmap for different end applications are shown in Figure 1.18.

1.3.2 Fan-Out Packaging Technology by Manufacturer

1.3.2.1 Amkor

Amkor Portugal, formerly Nanium, is well established in the FO landscape and one of the early adopters of eWLB technology. Nanium was purchased by Amkor in 2017 and is now officially referred to as Amkor Technology Portugal (ATEP). Thanks to its long history in the FO market (since 2009), Nanium has developed a wide portfolio of products based on eWLB technology. Willing to diversify from

Figure 1.17 FO technology volume production roadmap.

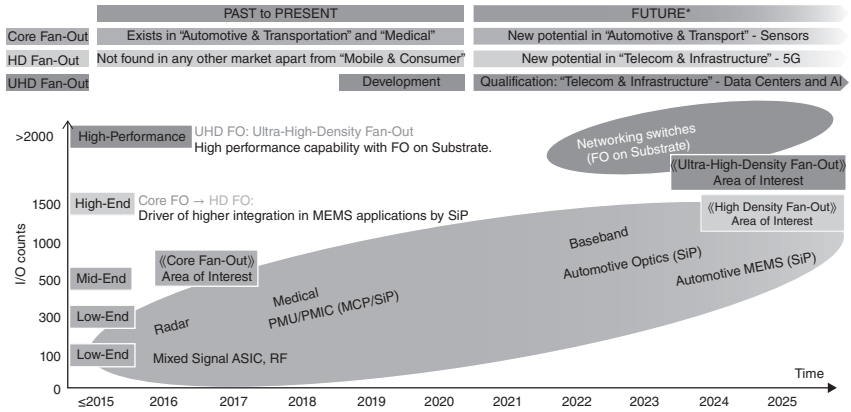


Figure 1.18 FO technology roadmap for different end applications.

single die packages, ATEP offers another level of FO integration, enabling them to embed more chips and passives and build more complex architectures (MCM, SiP, PoP, F2F). These complex architectures allow eWLB to compete with conventional substrate-based PoP and SiP and reach markets where high I/O count and complex products are necessary. These technologies are enabled by the development of processes to get more RDL (and so more connections), larger-sized die embeddable, and so forth. Amkor Portugal's brand name for FO-WLP based on the eWLB technology from Infineon is now WLFO (wafer-level fan-out), and all the products of their portfolio start with "WL": WLBGA, WL-land grid array (WLLGA), WLSiP, WL3D, WLPoP, WLMCM.

1.3.2.2 JCET

STATS ChipPAC, acquired by JCET in 2015, is the leading provider of eWLB and announced that it shipped more than 1.5B FO-WLP devices in March. Willing to diversify its markets and gain market share with the BB, PMIC, RF single die packages (sweet spot of FO-WLP), STATS ChipPAC has also established a roadmap and is offering MCM, PoP, and SiP. This includes hybrid offers in which FO packages are attached to substrates that have the potential for high-density applications. JCET/STATS ChipPAC is pushing development of higher integration with eWLB technology: MCM with several RDLs of different L/S as well as thin SiP and PoP with large die and high I/O count. JCET's advanced 3D eWLB technology provides a smaller form factor and performance value-add and is proving to be a new 3D SiP packaging platform that can expand its application range to various types of emerging mobile and IoT applications, including sensors, MEMS, and automotive applications.

1.3.2.3 NXP

NXP developed the RCP technology which, was licensed by Nepes. The main differences between eWLB and RCP are that RCP uses a dispensed encapsulant rather than a compression molded one and has an additional copper structure that helps limit the die shift during wafer molding and provides electromagnetic shielding and more rigidity to the package, but adds costs. eWLB has the advantage of an easier process due to fewer steps (no copper structure) and a long history with several companies in carrier and molding technology selection. RCP seems to have better performance in die shift but despite that had more limited success in the market, being provided only by Freescale (now NXP) and Nepes. With the maturity of the process and an approach similar to eWLB, RCP providers are promoting a second generation of products with more complex applications and higher integration (MCM, SiP, PoP). Freescale (NXP) is the main provider of RCP, and its packages are used for its own products. It has a large portfolio because of the high positioning of NXP in automotive, IoT, and wearables. Products benefiting from RCP's high electrical capability are seen in automotive, such as NXP MR2001 radar (77 GHz). Due to the higher integration, targeted applications for RCP are wider and include MEMS, RF, wearable, and IoT. RCP will probably remain a niche product though, since even NXP themselves use with other FO solutions, such as eWLB, in some applications.

1.3.2.4 DECA Technologies

Deca developed the M-Series FO technology. It is a chip-first face-up solution using an AP software technology. Deca has developed this breakthrough adaptive patterning™ approach to solve the die shift problem in FO-WLP technology by creating a unit-specific pattern for every device on every wafer or panel to perfectly match actual device locations. Deca has 40 issued and pending patents on AP. Deca has a complete production solution, in partnership with industry-leading electronic device automation (EDA) vendors and equipment suppliers. With this technology, the company reports that it has a fast product qualification capability and has solved issues of pattern misalignment that are critical in other chip-first FO technologies.

The AP software technology includes optical inspection and design capabilities to measure and correct for die shift and to recalculate device I/O to ball interconnects directly during processing. Connection from the die pads to the RDL are made by copper studs that can be placed either directly on the bond pad or routed along the RDL. This technology is licensable by Deca and is already licensed to a major manufacturer, ASE.

In February 2020, Deca officially became an independent technology development and licensing company. At the same time, Nepes acquired Deca's manufacturing operations in the Philippines, with licensed M-Series. With such a move, the

M-Series has the potential to take a large share of the market and become a new reference. Deca's M-Series is established in Taiwan, Korea, and the Philippines thanks to licensing from ASE and now Nepes. A notable development within the original application is the use of Deca's M-Series FO technology to create a protected WLP.

1.3.2.5 ASE

ASE has a multitude of packages using the FO nomenclature: chip-first, chip-last, face-up, face-down, PoP, SiP, and FO on substrate. They have also licensed various technologies: eWLB from Infineon since 2009 and M-Series from Deca Technologies since 2016, after investing $60 M for the license, and started to build a panel line in 2018.

Some technologies have already been accepted by the industry for a long time: chip-first face-down eWLB is the benchmark for all FO-WLP and demonstrated its potential for single die embedding and for further integration in high-volume manufacturing (HVM) first. Chip-first face-up M-Series demonstrated its capability in dealing with the die shift issue. Other platforms are addressing different markets and are using different technologies: FOCLP is a flip-chip of the die on a coreless substrate that are embedded in a molding compound in a subsequent step. FOCoS is an FO package on an advanced substrate. FO SiP is a chip-last solution. FOCLP addresses a market in which I/O count is limited. ASE FOCoS technology is starting to be positioned as a competitor for 2.5D Si interposer for large SoC applications at a lower price. Consequently, the ASE Group with its FOCoS is in a good position to follow that trend. FOCoS has already been in volume production since 2018. The RDL can be as narrow as 2 µm/2 µm L/S. It can be performed face-up or face-down before being placed on a substrate.

ASE is also working on panel FO with different approaches: They are building a 615 mm × 625 mm panel line to produce Deca Technologies' M-Series. ASE is also building a 300 mm × 300 mm panel line but with more aggressive L/S, targeting more advanced applications than those that M-Series will address.

ASE identified FO opportunities for high frequency, such as automotive radar (76–81 GHz), 5G backhaul (> 20 GHz), 5G fronthaul (> 20 GHz), WiGig (60 GHz), and AiP.

1.3.2.6 TSMC

TSMC was the first company to develop FO InFO technology to target application processor packaging for high-end smartphones. In 2015, they purchased a plant for $85 M in Taoyuan. TSMC then invested more than $500 M in equipment and refurbished the plant for InFO production. The investment reached $1 B in 2019. The first main product target was Apple's APE A10 for its iPhone 7, and InFO

captured that market. The PoP structure was accepted by Apple because of its thin size versus standard flip-chip. Apple confirmed that choice with APE A11 in 2017, APE A12 in 2018, and again with APE12 in 2019. InFO has made TSMC's 7 nm process technology more competitive than its counterparts, and TSMC won all orders for A14 chips that Apple released in 2020 and A15 orders in 2021.

InFO_PoP challenges the standard FC-PoP market with thinner packages and better performance. InFO's market of interest is PoP and SiP for complex mobile applications such as APE and DRAM PoP, for which customers are always pushing for ever thinner packages. Customers are now asking for sub-0.8 mm package thickness, which is not possible with PoP based on current laminate substrate technology. A11 reverse engineering has revealed that InFO technology could cut the thickness of an APE package down to 0.23 mm, with 3 RDLs and a minimal L/S of 8 μm/11 μm. This allowed Apple to get a full PoP thickness (without BGA balls) below 800 μm. TSMC will continue reducing the thickness of these PoPs with higher L/S resolution, RDL on top of the bottom package, and other improvements. Another added value is electrical performance thanks to shorter interconnections compared to a FC-CSP PoP. The yield achieved by TSMC, and consequently the impact on the cost, are questionable. However, most likely, cost was not as important for TSMC as it could be for an OSAT since they can compensate for it with Si wafer foundry earnings.

TSMC has developed various variants of InFO such as InFO_oS (on substrate similar to FOCoS by ASE) and InFO_MS, InFO_AiP, and InFO MUST-in MUST, where MUST stands for multi-stack (InFO_MiM) for various applications. For 5G mmWave wireless communication, InFO_AiP integrates the dipole and patch antenna with a mmWave front-end module (FEM) chip leveraging HD RDL and fine pitch. [18] TSMC's low dielectric constant polymer passivation material and uniform RDL enables high gain and low loss. It has been revealed that TSMC has qualified InFO_AiP with a package dimension of 12 mm × 12 mm × 0.9 mm with 2 RDL layers [19].

TSMC is also positioning UHD InFO derivatives, such as InFO_oS and InFO_MS (memory on substrate) for networking and AI inferencing applications, respectively, in the mid- to high-end HPC market. InFO_oS leverages InFO technology and features higher density 2 μm/2 μm RDL line width and space to integrate multiple advanced logic chiplets for 5G networking applications. It enables hybrid pad pitches on system-on-a-chip (SoC) with a minimum 40 μm I/O pitch, minimum 130 μm C4 Cu bump pitch and > 2X reticle size InFO on > 65 mm × 65 mm substrates. TSMC is expected to integrate more chips as customers continue to accelerate the adoption of a chiplet packaging scheme for their next generation products.

UHD FO packaging platforms, such as TSMC's InFO_MS and InFO_oS, offer alternative solutions to TSMC's CoWoS (chip-on-wafer-on-substrate 2.5D Si interposer technology) for applications that seek cost/performance optimization in the mid- to high-end of the HPC market. TSMC developed 3D multi-stack (MUST) system integration technology and 3D MUST-in-MUST (3D-MiM) FO as the next generation wafer-level FO technology. [20] 3D-MiM technology utilizes a more simplified architecture that eliminates BGAs between packages for system-level performance, power, and form-factor (PPA) purposes. This technology also makes use of a modularized approach for both design and integration flow to improve design flexibility and integration efficiency. Known-good pre-stacked memory cubes and/or logic-memory cubes are fabricated by leveraging the established integrated FO technology platform (InFO) in tools, materials, design rules, and processes to shorten development cycle time and achieve cost effectiveness. Near memory processing is attractive for high bandwidth, low latency, and power saving. 3D-MiM, a next generation integrated FO technology, is proposed to be an alternative heterogeneous integration solution to FC-PoP for mobile and 3DIC stacking for HPC applications, to realize in-package near-memory computing.

Currently, TSMC InFO research and development (R&D) results have been highly enticing and promising for next generation FO-WLP. Near memory processing is attractive for high bandwidth, low latency, and power saving. 3D InFO_MiM is positioned by TSMC as an alternative heterogeneous integration solution for advanced mobile and HPC applications to meet 5G/AI-driven application demands for years to come.

TSMC recently developed a novel wafer-scale system integration solution, InFO_SoW (system-on-wafer), to integrate known-good chip arrays with power and thermal modules for HPC. [21] InFO_SoW eliminates the use of substrate and PCB by serving as the carrier itself. Close packed multiple chip arrays within a compact system enable the solution to reap wafer-scale benefits, such as low latency chip-to-chip communication, high bandwidth density, and low impedance, for greater computing performance and power efficiency. In addition to heterogeneous chip integration, its wafer-field processing capability has enabled a chiplet-based design for greater cost saving and design flexibility.

1.3.2.7 PTI

PTI is considered a new entrant in the FO landscape with FO-PLP. PTI FO-PLP was production-ready in 2018, and PTI commenced running volume production in 2018. PTI offers four technologies, called CHIEFS, CLIP, PiFO, and BF^2O: a chip-first face-up, a chip-last, a FO-PoP, and a chip-first face-down, respectively. Thanks to this diversity, PTI can address numerous applications. PTI has set an aggressive roadmap to compensate for its delay compared to companies that already have a long history in FO-WLP: small L/S (2 µm/2 µm) and high RDL count (3 RDL). PTI is betting high on FO-PLP technology. See the last paragraph of Section 1.1.1 for more details about PTI.

1.3.2.8 Samsung Electronics

As a reaction to TSMC's InFO, Samsung Electronics and Samsung Electro-Mechanics (SEMCO) announced in June 2016 that they were joining forces to staff a packaging project and launch a solution to compete for the Apple APE market. In 2016 $200 M was invested to change LCD assembly lines in Cheonan into IC packaging lines. In 2019, it was reported that Samsung Electronics acquired the FO-PLP business unit from Samsung Electro-Mechanics (SEMCO) to enhance its capability in the FO-WLP market. [16] The technology developed by SEMCO is a new type of FO: die are embedded in a substrate (PCB type) after being placed in cavities created in the substrate. This brings several potential advantages: it is easier to work with panels since equipment already exists to process substrates at panel level, while handling reconstituted panels made of mold compound is still challenging. It may also bring advantages in dealing with warpage since an organic substrate may be more rigid. Standard RDL made of dielectric material slit-coated on the panel surface and copper deposition constitute the interconnections. This is competitive with FO-WLP. Samsung FO-PLP has run production for its own smartwatch, but it is not a HD or UHD FO solution.

1.3.2.9 Huatian

Huatian developed embedded silicon fan-out (eSiFO) technology and is currently in HVM. The principle is to create cavities into Si wafers and to use them as carriers to embed thinned die. This would effectively replace mold compound. The subsequent RDL process is standard. The eSiFO technology is compatible with PoP architecture.

1.3.3 Supply Chain Overview

FO-WLP involves a simplification and consolidation of the packaging, assembly, and testing in a "middle-end" type of infrastructure, where the legacy is controlled by experienced OSAT companies in the semiconductor industry, but it requires collaboration at the design level. Figure 1.19 shows the global map of key companies involved in FO activities.

For the OSATs, eWLB pioneers (JCET, Amkor, and ASE) are still supplying consistent volumes of core FO, mainly core FO-WLP. Furthermore, some OSATs (Nepes, PTI, and ASE) are positioning FO-PLP to catch existing business by reducing packaging cost. They are also focused on large die size applications for the future. This attracts fabless customers such as MediaTek. It is noted that SPIL and Amkor Korea are running qualification lots for FO. Also, companies and institutes such as 3D Plus, Aurora semiconductor, CEA-Leti, Fraunhofer IZM (FIZM), and Institute of Microelectronics (IME Singapore) are all in collaboration to assess new FO capability.

Regarding foundries, it is only TSMC that is shipping FO-WLP in HVM. TSMC is the only supplier of APE FE and packaging for Apple's iPhones and smartwatches.

Figure 1.19 Global map of companies active in FO.

TSMC is expected to utilize InFO for HPC and 5G applications, tapping into a new pool of customers such as MediaTek, HiSilicon, and Nvidia for FO-WLP. GlobalFoundries collaborated with R&D institutes before assessing FO capability and now leverages OSAT capabilities.

Regarding integrated device manufacturers (IDM), Samsung Electronics (previously through SEMCO) has commercialized FO-PLP with APE/PMIC for the Galaxy watch (consumer). The focus is to enable HD FO for Samsung's internal smartphone and, if possible, to secure FE and packaging business for Apple's APE, which was lost to TSMC in 2015. NXP and Infineon outsourced a majority of their production to OSATs. They run R&D and low volume manufacturing (LVM) within internal units and are focused on the automotive market.

Deca has changed its business model and adopted a licensing model. The goal now is to do technology transfers of M-Series and AP to leading manufacturers. Fabless companies such as Qualcomm, Apple, MediaTek, HiSilicon, and Xilinx have been qualifying FO-WLP for megtrend-driven applications (5G, HPC, IoT). New companies in IoT and AiP have also emerged in recent years. For example, Sivers IMA, Synaptics, and Synergy have all been running LVM qualification lots since 2019.

1.3.4 Analysis of the Latest Developments in the Supply Chain

In this section, the supplier-customer relationships of leading companies within each business model, foundry, IDM, OSAT, and licenser, as shown in Figure 1.20,

are explored. Not all suppliers are listed as the focus is on suppliers who have had more developments within the supply chain in recent years; therefore, this is a non-exhaustive list of companies. Customers are connected to suppliers in a more complex manner than purely existing customers, new customers, and speculated customers. Analyzing supplier-customer relationships by business model can help us better understand the impact on the dynamics of the business because the relationships have various facets. The structure of supplier-customer relationships is complex and reflects capability, resources, activities, and technology positioning.

As seen in Figure 1.20, TSMC is the leading foundry supplying FO-WLP. TSMC is not only positioning itself as an advanced foundry but also a high-end packaging house in BE. This unique business model will continue to lead the way in creating higher value and innovative breakthroughs. As such, FO-WLP will attract more end customers with new applications at the right cost.

InFO_oS (on substrate) technology is now being utilized for HPC running in LVM for MediaTek, Nephos, and Xilinx. Nvidia, AMD, and Qualcomm are believed to have expressed interest and have qualified test chips.

HiSilicon used to be TSMC's customer for UHD FO. However, the US enacted legislation in May 2020 that prevented foreign manufacturers of semiconductors that use US software and technology in their operations from shipping their products to Huawei unless they got a license from the US. TSMC stopped supplying new orders of UHD FO for Huawei. This essentially cut Huawei off from the supply of leading-edge chips, limiting Huawei's competitiveness. At the same time, TSMC lost a significant revenue stream from one of its major customers, Huawei.

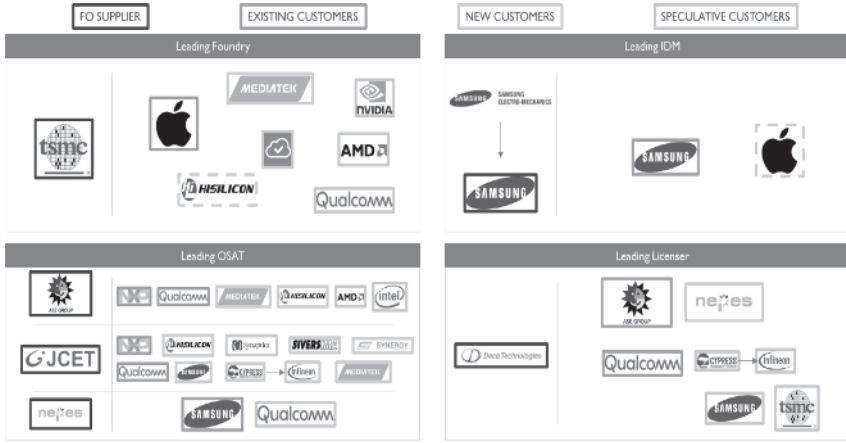


Figure 1.20 Leading supplier-customer relationship by business model (non-exhaustive list of companies).

As shown in Figure 1.20, Samsung Electronics is the leading IDM actively manufacturing FO-WLP internally. Samsung Electronics, being a leading IDM, had strong reasons and resources to invest in SEMCO for a FO-PLP solution and subsequently to reacquire it to expedite yield improvement and synergies with FE die internally. Consequently, Samsung Electronics' new model is the same as TSMC's model, which won the Apple APE die and packaging business in 2015.

Samsung has been instrumental in design, memory, logic, packaging, chipset assembly, and end product, so it can now drive innovation efficiently and decisively. Currently, HD FO-PLP is still in production for the Samsung Galaxy Watch APE and PMIC. Next, it will be for APE in smartphones. This is, however, easier said than done with new FO-PLP technology because the yield and reliability will prove to be another technical challenge when it comes to the larger die size and increased I/O counts required for mobile APE. Samsung will continue to innovate cost-effective HD FO in order to compete with TSMC for Apple's packaging and FE business. As of 2021, however, it will still be for internal customer use within Samsung.

As illustrated in Figure 1.20, the leading OSATs include the ASE Group, JCET, and Nepes, all of which have more developments in recent years. ASE's FOCoS is gaining traction for HPC. JCET is starting to enjoy the 5G boom. MediaTek is a confirmed ASE customer running LVM. These are all mainly for server applications. HiSilicon is looking to ASE for FO-WLP because TSMC's production is mostly dedicated to Apple. HiSilicon practices a dual or multi- vendor policy. However, because of similar legislation by the US, the ASE Group is expected to stop supplying HiSilicon.

JCET China is very HiSilicon-oriented. In fact, it is noted that an HD FO line was built in China supporting HiSilicon's HD FO request. HiSilicon is trying to enable domestic OSATs whenever possible due to the trade war. In a way this benefitted JCET. JCET Singapore used to enjoy large volumes from Qualcomm. Although the volume is not as significant as before, JCET Singapore has started to attract many new customers, such as Synergy, Synaptic, Sivers IMA, and NXP for 5G-driven applications. Also, there are new applications with existing customers for AiP and PMIC, also thanks to 5G. In summary, JCET is enjoying good business from existing PMICs and is qualifying for new applications with the start of the 5G boom.

In 2020, Nepes announced that it has spun off its FO-PLP business division into an independent subsidiary company called Nepes Laweh. A new independent management will be leading this company. This is a significant and rather bold move by Nepes to restructure and reinvent the new and old businesses in order to grow faster, especially after acquiring Deca's FO-PLP technology and line. Apart from Samsung, we believe it is Qualcomm driving this initiative. Moving forward,

we are expecting Nepes to go full force on the development of advanced semiconductor process services with FO technology and achieve business competitiveness within core FO.

As shown in Figure 1.20, Deca repositioned itself as a leading industry licensor with its propriety technologies. With strong endorsement from Qualcomm, ASE, Nepes, and Cypress (acquired by Infineon), Deca has transformed from a manufacturer into a fully-fledged independent technology development and licensing company in 2020. Deca's manufacturing line in the Philippines has been sold to Nepes. This liberated Deca from the manufacturing business. Presently, Deca Technologies' focus is to enable applications in the mobile and consumer markets. Moving forward, it will target HPC and advanced networking. The targeted audience in the future could be Samsung or TSMC.

1.4 Fan-Out Panel-Level Packaging (FO-PLP)

1.4.1 Motivation and Challenges for FO-PLP

The demand for lower cost with higher performance has driven the semiconductor industry to develop innovative solutions. Similarly, the OSATs and their customers are always asking for ever-lower prices. One approach to reduce overall cost is to switch from wafer and strip level to a larger-size panel format to take advantage of efficiencies and economies of scale. Going from wafer to panel (for example 12-in. wafer to 18-in. × 24-in. panel) could enable cost reductions up to 50% if the technologies are ready and the yield is higher than 90%. Moving from wafer to panel format has major cost and productivity advantages due to higher efficiency and economies of scale. The usage area of a panel-shape carrier is higher than round wafer format. Panel level packaging process can produce more FO because of this high panel area usage ratio. The carrier area usage ratio of 8-in./12-in. wafers is < 85% due to the influence of edge incomplete packages, whereas carrier area usage of panels for FO can reach 95% with rectangular chips on rectangular panel carrier. Panel manufacturing has higher throughput due to reduced handling/transfer time compared to round wafer processing. Also, there is a huge decrease in the number of packages obtained per wafer because of increasing package size, which provides an incentive to move to larger panel carriers to boost profitability, as shown in Figure 1.21.

Certain criteria must be fulfilled and certain challenges overcome for the broad adoption of FO-PLP. These challenges are linked to large capex investment, standardization, multi-source availability, and most important, market availability to keep the panel line running. There are technical challenges too, such as warpage control, die placement accuracy, and fabrication of sub-10/10 μm line on large panels. Standardization of the panel size and assembly process is the biggest hurdle

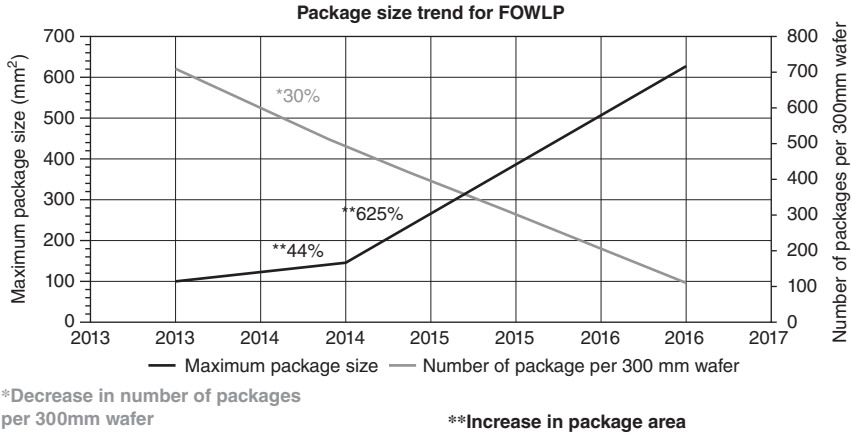


Figure 1.21 Package size trend for FOWLP showing decrease in number of packages per 300 mm reconstituted wafer.

for the adoption of FO-PLP. Each player is developing their own process using different panel sizes and infrastructure (PCB/LCD/WLP/PV/mix) catering to specific applications and customers. In this scenario, it is exceedingly difficult for end customers to multisource. Also, it is not profitable for equipment suppliers to design and manufacture equipment according to different customers' requirements. Warpage minimization of the panel is another big issue so that it can be processed using standard semiconductor processing tools. The larger the panel, the more complicated it gets because the loss of one panel represents a much higher value. Another challenge is the feasibility and reliability of new processes needed in case wafer solutions are difficult to adapt. For instance, spinning deposition of materials is more complicated for panels, and the use of sheets (for mold compound, for instance) or spray (for photoresist, for instance) could be a replacement.

1.4.2 FO-PLP Market and Applications

The applications for FO-PLP can be defined by segmenting the technical specifications required for RDL technology in terms of L/S: 2 μm for high-end applications such as CPU/GPU, FPGA; 5–8 μm for mid-end applications baseband, processors, power management module, and RFIC; and 10–15 μm for low-end applications such as mobile, consumers, RF, Wi-Fi, and power management. Currently FO-PLP in production targets low- and middle-end applications. Because of the technical challenges associated with fine L/S on panel, companies such as Nepes and PTI entered FO-PLP production targeting low-end applications (L/S > 10/10 μm). Samsung/Samsung Electromechanics (SEMCO) entered FO-PLP production targeting mid-end applications with an integrated APU for the Galaxy Watch. We believe the sweet spot for FO-PLP applications is larger

package size ($> 15\,\text{mm} \times 15\,\text{mm}$) and L/S $\leq 5/5\,\mu\text{m}$, and this is the goal toward which many companies such as PTI, ASE, and ESWIN, are working toward.

Panel will progressively take a share of production but still in a limited way. FO-PLP is expected to take off much later when big die applications are adopted. By 2025, we expect FO-PLP to account for 18% of the total fan-out packaging production by wafer (300 mm eq), as shown in Figure 1.22. The readiness of key companies for FO-PLP can be seen in Figure 1.23.

1.4.3 FO-PLP Supplier Overview

Panel-level manufacturing has the potential to leverage the knowledge and infrastructure of the WLP and the PCB / flat-panel display / photovoltaic industries. There are various factors that are driving the development of PLP and attracting various companies from the supply chain (including equipment and materials) to invest in panel infrastructure. On the one side, top fabless companies want OSATs to reduce the cost of high-density FO-WLP, and panel is seen as the key step to significantly reduce the package price. FO-PLP is on the roadmap of every big OSAT. On the other side, there are companies who are investing in and developing PLP capability and are really pushing for its adoption as part of their strategy. These companies are mainly driven by the success and publicity around FO-WLP and are those who:

- Missed the early FO-WLP (eWLB) wave (e.g. PTI);
- Are affected by the loss in substrate business and want a new business model while leveraging their experience in substrate manufacturing (e.g. SEMCO, Unimicron);

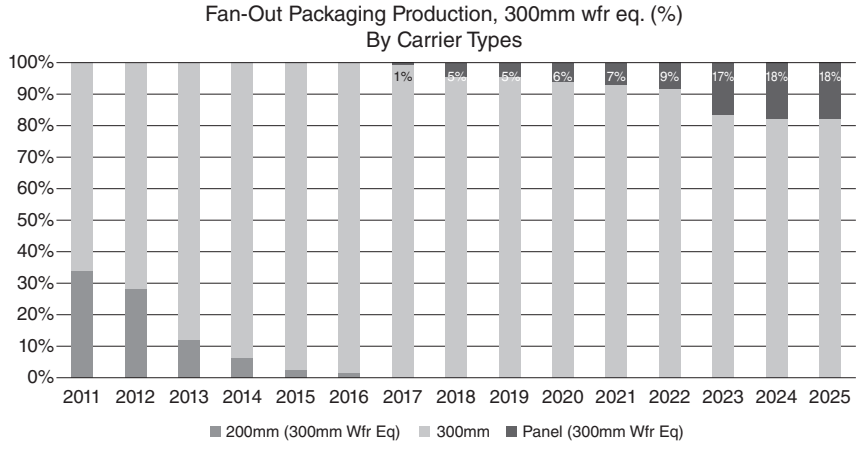


Figure 1.22 FO packaging production trend by carrier types.

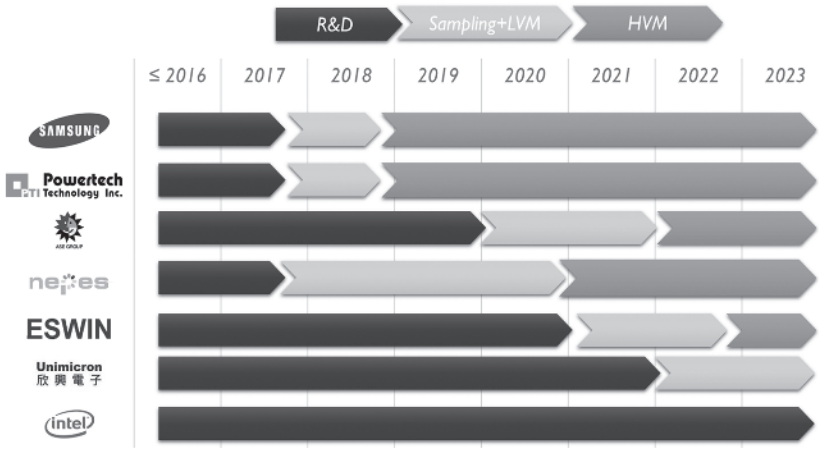


Figure 1.23 Readiness of key companies for FO-PLP production.

- Already have experience in panel processes such as LCD packaging and think they can leverage their experience to PLP (e.g. Nepes);
- Want to develop HD yet low-cost packaging to support their FE chip business (e.g. Samsung Electronics, Intel).

There are many companies developing FO-PLP technology, and after years of development, qualification, and sampling, many companies are going into HVM, such as Samsung, Nepes, and PTI. Nepes has been in low volume production since 2017. ASE in partnership with Deca Technologies is in an advanced stage of development and will go to volume production in 2022. Each player has its own business strategy and is working on its own FO-PLP technology (panel size, leveraging different infrastructure, etc.). For example, Nepes will initially focus on a coarse design (> 10/10 μm L/S) targeting automotive, sensors, and IoT application and will go into high-density design at a later stage, whereas the long-term aim of PTI and SEMCO is to target mid- and high-end applications that require 8/8 μm or lower L/S. ESWIN is potentially the first FO-PLP player in China to run LVM production by 2022. Unimicron is working on a different business model where they will manufacture the HD RDL, and further assembly will be done by a foundry, OSAT partner, or customer. On the other hand, prominent OSATs such as Amkor and JCET/STATS ChipPAC are currently in a wait-and-watch stage and are evaluating various options and will not go into volume production before 2022. Figure 1.24 shows the status of the key companies involved in FO-PLP.

Players	Production status	Technology	Panel manufacturing type	Panel size	*L/S minimal features (2018)	Driving applications
ASE	• Panel production ready • Target for volume production is 2022	• eWLB license (Chip-First Face-Down) • M-Series license (Chip-First Face-Up)	• PCB-based	• 300*300m^2 • 615*625m^2 (for M-series with Deca) (Yole estimation)	• 2µm L/S (for 300*300m^2 panels) • 10µm L/S (for M-series with Deca)	BB, PMU, RF
Samsung	• Production ready for low-end apps (PMIC, etc..) • Production for APE commenced in 2018	• SEMCO PLP	• PCB-based	• 510×415mm^2	8/14µm L/s	• RF SiP • BB, PMU, RF • APE + PMIC
Powertech Technology (PTI)	• LVM started in 2018 • New fab construction still in progress as of 2020	• CHIEFS (Chip-First) • CLIP (Chip-Last) • PiFO • BF^{2}O	• Mixed between LCD and PCB	• 510*515mm^2	• 5/5µm L/S expected	• BB, PMU, RF • APE • FPGA, CPU, GPU
nepes	• Production started in Q2 2017 • Production of M-series after 2019 acquisition	• VF-FOWLP	• LCD-based	• Gen 3 (~650×550mm^2) (Yole estimation)	• 10µm L/S	• BB, PMU, RF
Eswin	• Panel line ready in 2021 • Production to start in 2022	• eMFO (Embedded Molded Fan-Out, Chip-First) • ESWIN-FOPLP	• Mixed between LCD, semiconductor and PCB	• 510*515mm^2	• 5/5µm L/S for 2021; • 2/2µm L/S for 2022	• BB, PMU, RF • APE, • Logic, • SiP

Figure 1.24 Status of the key companies involved in FO-PLP.

Equipment readiness for PLP is not the bottleneck today. Tools are available in the market supporting various process steps in panel processing. However, the tools that support high-density panel packaging are especially expensive, so availability is not the issue, but the cost of the tool is. For some process steps (e.g. plating, physical vapor deposition [PVD], molding, die attach, and dicing), most of the tools are readily available in the market and can be adapted from the PCB, flat-panel display, or LCD industries and are likely to be reused to produce panels. However, some key process steps inherent to advanced packaging, such as lithography, necessitate the development of new upgraded tool capabilities to support fine L/S patterning on panels. Thick-resist lithography, panel-handling capabilities, exposure field size, and depth of focus have been developed by equipment suppliers in recent years. Equipment suppliers are adopting different strategies to enter the PLP business: by acquisition (e.g. Rudolph Technologies has developed tools suitable for PLP based on the knowledge they acquired through the acquisition of AZORES Flat Panel Display Panel Printer), by leveraging tool experience in other businesses and upgrading it (e.g. Evatech, Atotech, SCREEN), or by organically developing tools for PLP from scratch (e.g. ASM). Also, some tool suppliers have a strong position in the FO-WLP market. However, they are skeptical of the PLP business and thus are taking a wait-and-see approach. Ultratech, Applied Materials, and Lam Research are part of this group of companies. On the materials side, the trend for key materials suppliers is to use their current market-ready products for LCD and advanced packaging applications and optimize them to meet panel package requirements.

1.5 System Device Teardowns

1.5.1 Teardown of End-Systems with Fan-Out Packaging

FO technology has a very wide application space. From automotive to consumer, the market is large as described above. With many applications this packaging technology has brought many advantages, as described in Figure 1.25 below. Among them, we can list:

- Thermal dissipation;
- Simplified supply chain and manufacturing;
- Cost simplification;
- IC protection;
- Interconnection;
- High flexibility;
- Thin package;
- High BLR (board level reliability);

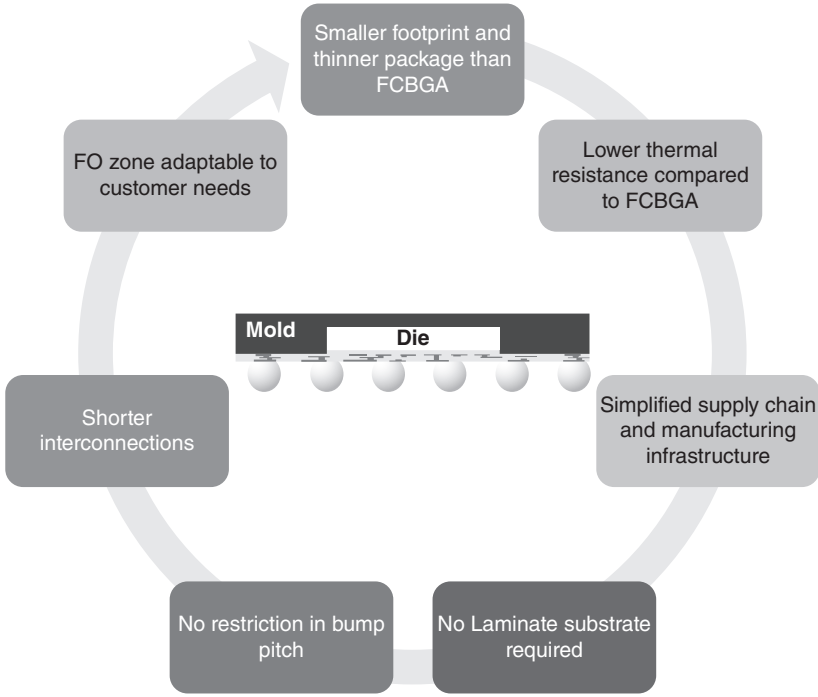


Figure 1.25 Key differentiators for fan-out packaging.

In automotive, the only system that uses FO technology is radar. This system is based on an MMIC die that transmits and receives the signal to sense the car's environment. Previously, the system was implemented in discrete mode on a dedicated RF board. In the MMIC implementation, several technologies are used on bulk silicon substrate, CMOS, and SiGe BiCMOS. As MMIC power is high, the diffused heat could rise rapidly. The main advantages of FO include thermal management using solder balls around the main power amplifier in the transmit path. Another advantage is the shorter interconnections for the receiver (Rx) and transmitter (Tx) path. Using shorter interconnections allows a reduction of parasitic signal. Two technologies have appeared in the market. RCP was developed by NXP in partnership with Nepes. Infineon was the first MMIC manufacturer to use this packaging technology. Now, as the technology has been licensed to several OSATs, newcomers, such as Calterah Semiconductor and MediaTek, are using the packaging technology for radar systems. For MediaTek, the small size and reduced cost of the system was also achieved with the use of FO technology by including the antenna system in the RDL.

These advantages can change for the consumer application. As consumer systems use low power, heat is not a concern in choosing the packaging. Specific factors here are more related to the cost and the size. Indeed, FO technology can provide a small form factor and thinner packaging while keeping to a relatively low-cost solution. Since 2011, the number of references on the market using FO technology has exponentially grown year over year as shown in Figure 1.26. The graph counts the number of component reference models per year. For example, since 2018, Qualcomm has released a huge volume of PMICs with the reference model PM8150. This reference appears in 2018, 2019, and 2020 and counts for one in each year.

Other companies have tried to integrate the packaging technology into their components, but no one else has really succeeded like Qualcomm. The first device from Qualcomm was a PMIC that used eWLB to spread out the die interconnections to fit the ball pitch of the PCB board. At the time, the proportion of the die on the component was close to 70%. Now, depending on the final application, the proportion of the die in the packaging can be close to 90%, as shown in Figure 1.27. The tendency is clearly toward die densification in the packaging and not toward real fan out of the interconnects over a larger area than the die size. In this case, the goal of the FO has become only for protection. Indeed, today FO-WLP technology allows the packaging of any die on 12-in. wafer or panel and provides side wall protection for any die size. In this way, the final OEMs can provide a packaging for a high technology node (0.18 μm), based on 8-in. wafer, on a 12-in. wafer with molding all around the die. This not only provides protection but also reduces the cost of the packaging compared to a WLP.

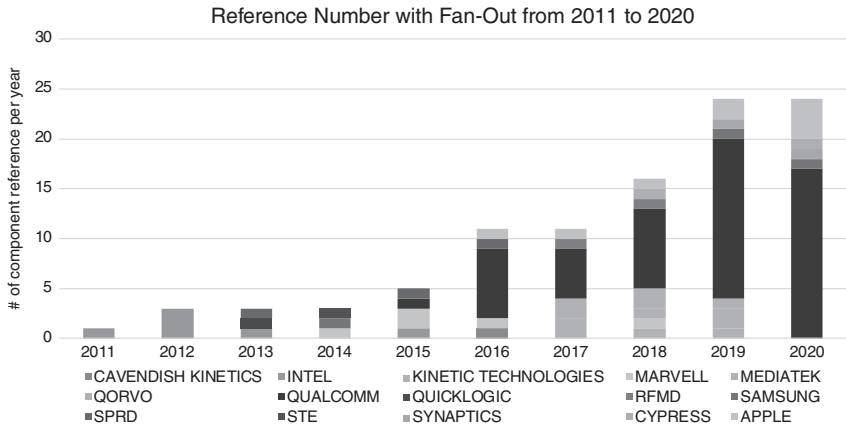


Figure 1.26 Fan-out packaging evolution by reference model from 2011.

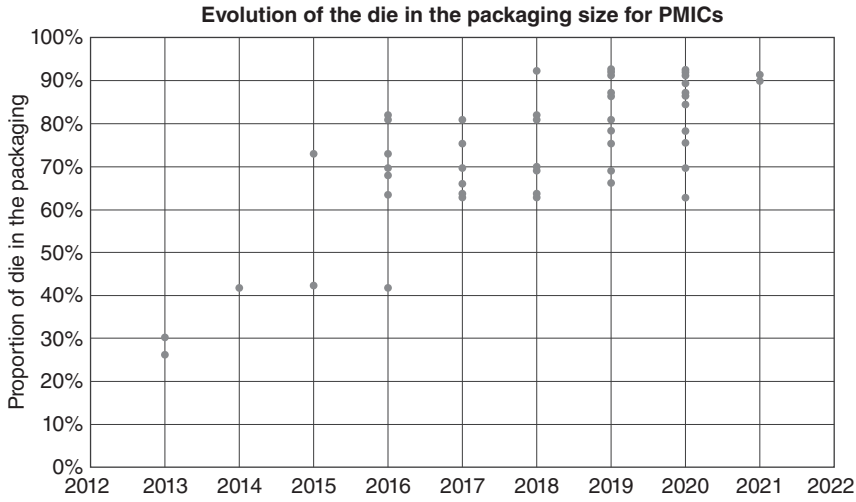


Figure 1.27 Evolution of die proportion for FO packaging from 2013 until 2021.

Now, practically all the PMICs from Qualcomm are using FO technology from ASE to provide 5-side wall protection for the ICs. Only the backside of the die is not covered with molding, but it could be covered with backside laminate and is offered as an option in the M-Series packaging process. One other application of FO in the consumer world is for application processors. As shown in Figure 1.28, the application processor (AP) percentage is small in the market but as the components are much larger than a typical PMIC, the opportunity is large.

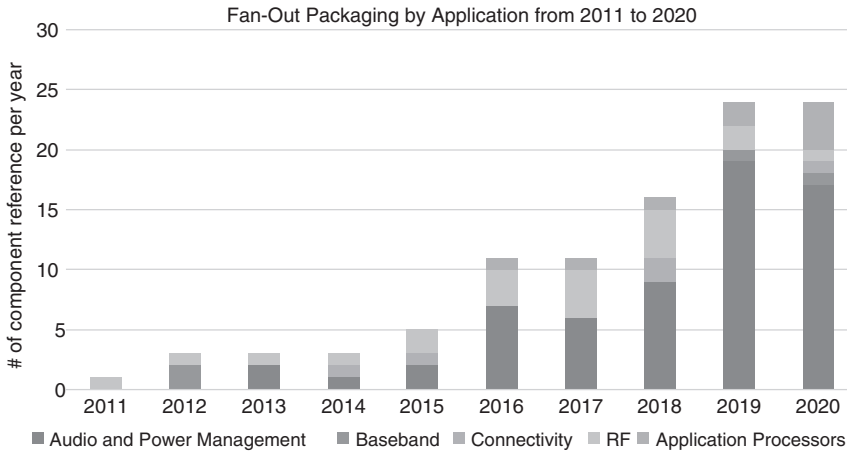


Figure 1.28 Fan-out packaging evolution by application from 2011.

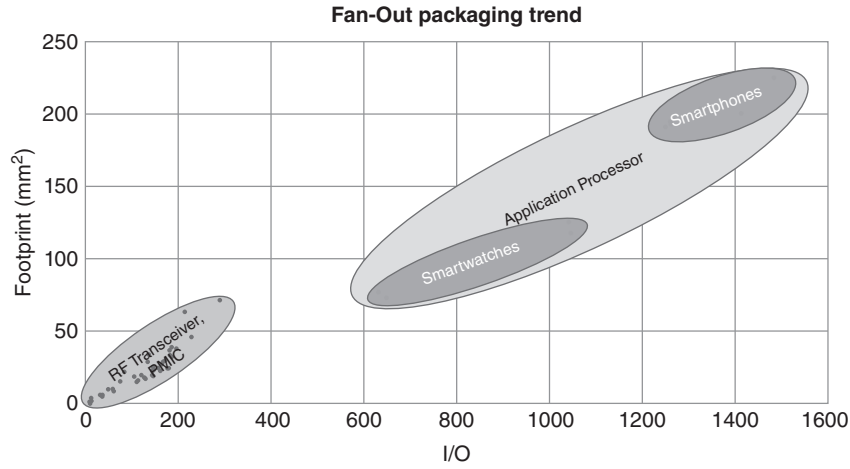


Figure 1.29 Fan-out packaging bump density trend.

Finally, based on a database of consumer components since 2011, a trend in the bump density and the component size can be found and is illustrated in Figure 1.29.

Two main regions can be identified. One is dedicated to small components such as the RF transceiver in the past and PMIC now, with a low number of I/Os and small area mainly using FO for side wall protection. The other, a more spread-out region, is dedicated to APE. In this region, two smaller areas can be defined. One is for smartwatch components with a medium number of I/Os. The other is for

the APE of smartphones with a very high level of bump density as the component performs multiple tasks and requires a very high number of IOs.

1.5.2 Technology Comparison

In this section, a comparison by application will be made for each FO technology found in the market, from radar to the SiP. eWLB technology will be presented in several applications as it is the most popular FO packaging technology today. To start with the radar MMIC, a comparison between RCP technology will be made with eWLB from Infineon and its application to the AiP system from STATS ChipPAC for MediaTek.

1.5.2.1 Radar IC: eWLB vs. RCP

The first implementation of RCP technology, chip-first face-down configuration as developed by NXP (formerly Freescale) had an issue that every FO manufacturer has faced, die shifting. Freescale had an interesting solution with the implementation of a copper frame that hardens the structure and prevents a large die shift during the molding. Moreover, the frame was grounded in the package to enhance the isolation of the MMIC. The eWLB implementation is like the RCP technology with a chip-first face-down configuration, but the molding needs to be controlled to avoid any die shifting. As mentioned before, the form factor was not the prime driver in this kind of application. The thermomechanical enhancement was the main concern and the criterion of choice for the FO technology. Indeed, by looking at the die relative to the packaging size, only 25% of the packaging was occupied by the MMIC. All the rest was for grounding, thermal dissipation, BLR, and short interconnections with the PCB substrate. Today, as the MMIC die technology evolves, the tone is not the same. As shown in Figure 1.30, the form factor became one of the main criteria.

The first generation of MMIC was made of three 6 mm x 6 mm components with different die functions integrated in the SiGe BiCMOS process. The last generation by Infineon is larger, but a view of the bump side shows a very small area with RDL compared to the previous generation. Moreover, Infineon managed to get particularly good thermomechanical behavior with solder bumps directly under the die. Finally, advanced RFCMOS technology with eWLB packaging can offer a very small form factor and allows a radar sensor in the parking sensor application. MediaTek managed to fit an integrated antenna system into the same packaging as the MMIC die to fit in a device with a form factor close to the ultrasonic sensor available on the market. To do so, STATS ChipPAC added a very large area of copper RDLs to provide thermal dissipation and antenna isolation. In this configuration, no interconnect is used in the RF path. The antennas are directly connected to the die I/O.

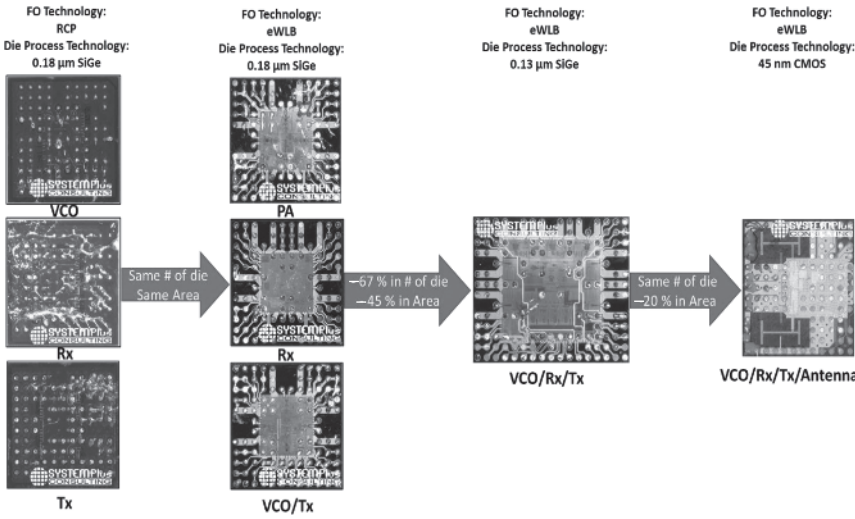


Figure 1.30 MMIC FO packaging technology comparison.

1.5.2.2 MCM/SiP: RCP-SiP vs. eWLB

Both previous technologies can be also used for SiP design. Two designs can be found in the market for industrial and consumer purposes. Both use FO packaging technology for the form factor. For the industrial application, NXP and Nepes developed the RCP into a version that uses a PCB via frame as a replacement for the copper frame used to prevent die shifting; in this case, the via frame is also used to provide interconnects between the bottom RDL and a memory package enabling a PoP configuration.

In very small packages, the components feature a MCU, a PMIC, and a flash memory along with several passive components placed in SMD configuration. The die process is similar to the RCP packaging used for the radar MMIC. For the eWLB, the application of SiP in the market is limited to the consumer world, with two die and good yield losses. A device-like connectivity FE module can be found in the smartwatch application where the low-profile packaging is required. Cypress is the first company to provide such a solution in high volume manufacturing. The device integrated an MCU with a Bluetooth SoC in the same package.

Today, the number of die is limited because of the potential for severe die shifting with several die on a wafer. For a higher number of die, the AP technology developed by Deca Technologies is a promising solution. This technique allows a modification of the routing depending on the die shifting by using a laser direct imaging (LDI) system. It allowed Deca Technologies to develop their own FO packaging technology, called M-Series. In the case of Cypress's SiP, both technologies—eWLB

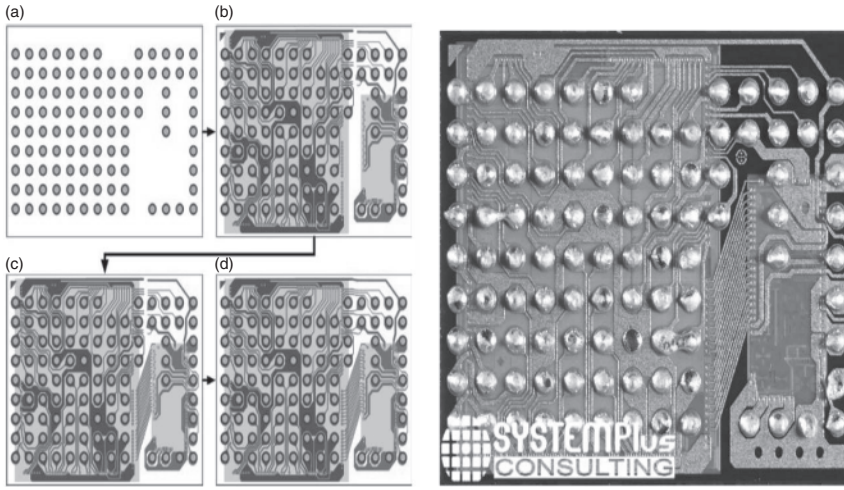


Figure 1.31 Adaptive patterning applied on Cypress SiP project and Cypress CY8C68237FM-BLE bottom side.

and M-Series—were in competition to produce the packaging of the system, as shown in Figure 1.31. Finally, it was STATS ChipPAC who made the SiP using eWLB technology. STATS ChipPAC managed to control the die shifting and realized a routing between the MCU and the SoC with the smallest state-of-the-art line/space value.

1.5.2.3 PMIC: eWLB vs. M-Series

For now, the FO market is moving toward M-Series. Indeed, anywhere Qualcomm uses FO-WLP, M-Series technology has been implemented. Qualcomm introduced FO packaging technology in smartphones in 2015. This was initially based on eWLB from Nanium and STATS ChipPAC. eWLB enabled side wall protection for these die (5 sides including backside). As it is a chip-first face-down process, the fifth side, which is the backside of the die, received protection with no additional process step. This was before the growth of the M-Series.

M-Series totally captured the FO market dedicated to eWLB since it uses a chip-first face-up configuration with active die side protection, AP lithography, and it can provide 6-side wall protection with an optional backside lamination step.

As described in Figure 1.32, the technology uses copper studs and overmold on the die face before the RDL manufacturing process. In this way, the die is completely protected with a molding layer on the top and it provides a very flat surface for RDL manufacturing. Moreover, by using AP technology in the process flow,

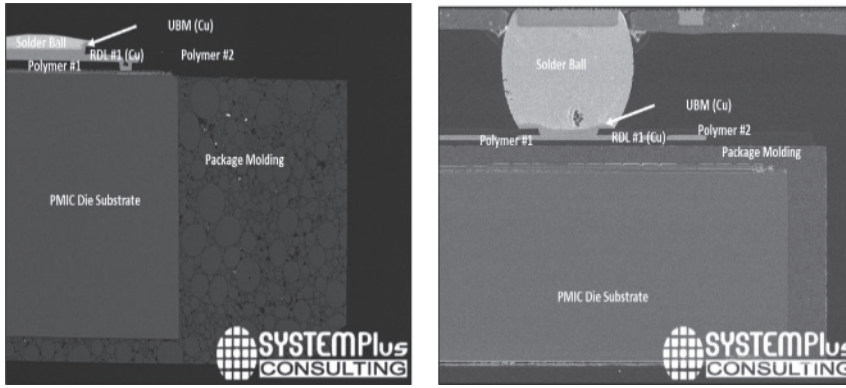


Figure 1.32 FO packaging of PMIC components: eWLB (left) and M-Series (right).

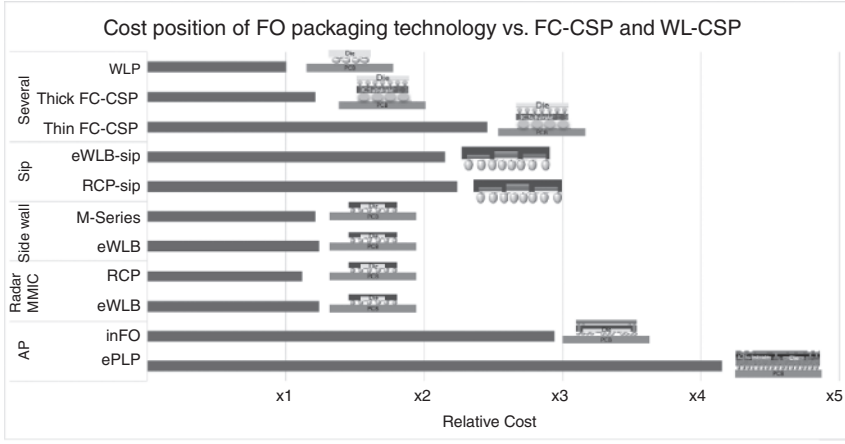


Figure 1.33 Cost comparison of FO packaging technology available in the market.

the package manufacturer can correct for die shifting without any redesign of the mask set using laser direct imaging (LDI) to compensate.

1.5.3 Cost Comparison

Each packaging type has been simulated to evaluate the cost of the FO packaging. Each step has been integrated describing the process flow with all the equipment and related consumables. In this way, the costlier steps of each process can be identified, and a comparison can be made. As shown in Figure 1.33, the relative cost of each FO packaging type can be obtained with reference to WLP.

For simple FO packaging, such as eWLB, RCP or M-Series, the difference compared to WLP is small. FO shows a 20% cost increase compared to a WLP. For all of them, the pick and place step is the costliest. The need for accurate placement of the die before molding is crucial. Only RCP is costlier because of the use of a metal frame to handle die shifting.

FO technology for integration in devices like a radar MMIC, side wall protection shows a relative cost in the same range as thick FC-CSP. One of the key differentiations is the BLR, which is obviously higher for FC-CSP compared to FO packaging. Yet M-Series technology, with its molding protection and hardening at the face of the die, allows the BLR of the technology to be closer to thick FC-CSP and makes a difference compared to eWLB.

Of course, for SiP versions of the FO technology, the relative cost is not the same. FO technology allows a multi-chip packaging level compared to a WLP, which clearly results in a cost increase. But the costlier step is not the same as for single chip FO packaging. Indeed, the use of a metal frame structure to enable PoP in this case creates a process step that makes up 10% of the total cost of the packaging. Also, as the surface to cover with molding is larger, the steps are costlier. All combined, the relative cost is almost twice that of single chip FO packaging.

Finally, by comparing the FO technology for thin packaging of an APE, the cost of the FO packaging from TSMC or SEMCO is three or four times more than WLP. Compared to a thin FC-CSP, the cost of these APE FO are only 20–70% higher. Between TSMC's InFO and a thin FC-CSP, the cost is not the main differentiator. Again, BLR is also one of the key specifications. As the cost is almost the same, for a better BLR clients will choose thin FC-CSP. Since InFO allows thinner packaging and the possibility to have integrated passive devices (IPD) in a face-to-face configuration, the choice would be InFO technology for performance. Moreover, if the ePLP solution from Samsung is considered, the estimated cost will be higher than InFO. Here the step that increases the cost is not related to the PoP enabler as with the copper pillar in InFO, but to the molding. Indeed, the amount and the type of the molding is quite different compared to other FO packaging technologies. Used at panel level, the required molding needs to be fluid enough to overmold the die and the via frame. Also, it needs to be reliable enough to be processed for backside RDL manufacturing.

1.6 Conclusion

FO is not new and has been in HVM since 2007. Recent technological progress is pushing the frontiers of what it can do, and FO is profoundly changing the industry's perception of its potential. This is especially so after TSMC's InFO HD FO technology was chosen to package the APE (A10) of the iPhone 7 in 2016. TSMC's InFO has pushed the high-end smartphone into a whole new higher-end market segment, defined as HD FO.

FO has a stronger appeal than conventional FC-CSP because of its thinner package dimension, increased I/O density, and lower thermal resistance. Additionally, the fanning out of the electrical I/O and the multi-die nature has produced significant scaling benefits for 2D, 2.5D, and 3D integration. The 2.5D FO structure as a replacement of the 2.5D Si interposer in the high-end applications domain has been featured and commercialized in the market. More evolutions of 3D FO-PoP are expected to result in a thinner profile, with more memory capacity and memory bandwidth. In essence, FO is becoming more dynamic than ever, offering solutions ranging from low-end packaging technology up to high-performing and cost-effective integration platforms.

Valued at $1256 M in 2019, the FO market value is set to reach $3046 M by 2025 at 15.9% CAGR. Total production volume of FO is projected to grow from 1703 kwspy in 2019 at a 12.3% CAGR, reaching 3419 kwspy in 2025. For FO, the mobile and consumer end-market dominates with overall revenue of $741 M in 2019 while it is projected to reach $1498 M by 2025 at 12.5% CAGR. Doing equally well is the telecom and infrastructure end-market, which is growing at an astounding 20.2% CAGR from $504 M in 2019 to $1523 M in 2025. Automotive and mobility is expected to grow by 13.8% CAGR from $11 M in 2019 to $24 in 2025. Lastly, the medical end market is expected to shrink with little adoption.

TSMC is all-in on FO for a new pool of customers. InFO_oS and InFO_MS are now being utilized in HPC for MediaTek and Xilinx. Samsung Electronics is hungry to recapture Apple's Si business with HD FO. Samsung Electronics, being a leading IDM, obviously had strong resources to initially invest in SEMCO for an FO-PLP solution and subsequently reacquire it to expedite yield improvements and synergies with FE die internally. Consequently, Samsung Electronics' new model is the same as TSMC's model which won the Apple APE die and packaging business deal in 2015. Samsung could enable HD FO-PLP in its own smartphone devices to self-endorse its performance, cost, and reliability to Apple.

ASE's FOCoS is gaining traction for HPC. HiSilicon and MediaTek are the confirmed new customers running LVM. JCET is starting to enjoy the 5G boom. HiSilicon is trying to enable domestic OSATs whenever possible due to the trade war. This, in a way, benefitted JCET China. JCET Singapore is enjoying good business from existing core PMICs and is qualifying for new applications with the 5G boom, which started in 2019.

Nepes has committed to a strong FO strategy by investing heavily in 2019 and 2020. In 2019, Nepes Laweh invested close to $35 M in acquiring Deca's M-Series and Philippines operations. Then in 2020, a new FO-WLP spin-off company called Nepes Laweh was established. Nepes Laweh started to lay down the groundwork for a new facility in Korea, targeting production by end of 2020. Nepes Laweh is expecting ~$330 M in revenue by 2024, which is about 40% of Nepes total forecast revenue in 2024.

With strong endorsement from Qualcomm, ASE, and Nepes, Deca transformed from a manufacturer into a fully-fledged independent technology development

and licensing company in 2020. Deca's business model now includes technology transfers to leading manufacturing companies (foundries, OSATs, semiconductor companies) and license agreements to over 40 issued and pending patents. This includes associated know-how in M-Series and AP and AP design systems in partnership with leading EDA providers combined with proven high-volume real-time manufacturing design.

Panel makers entering the FO game are struggling to achieve high-end products with good L/S and high reliability, though this is the sweet spot for FO-PLP. For FO-PLP companies, the challenge is technical and most likely will require some time to be addressed to ensure a good yield. Existing FO companies have different views. For them to scale-up to panel is more of a financial issue, since new equipment targeting the same performance as wafer manufacturing is required. ASE seems aggressive, with two panel lines been set up (300 mm × 300 mm for fine L/S and 600 mm × 600 mm for M-Series). They seem to be gearing up for a big battle in the core FO market and are planning an entry for HD FO. Given the technical challenges that adversely affect the yield, the FO-PLP that is going into HVM production will support a relatively simple design: > 10/10 µm L/S, < 10 mm × 10 mm package size, maximum 2-layer RDL. With the maturation of the technology and experience gained, FO-PLP will be adopted for HD design with < 10/10 µm L/S, multi-layer RDL, > 15 mm × 15 mm package size and multi-die SiP integration.

Today, the main player using the M-Series from Deca Technologies and ASE is Qualcomm. The die size as a percentage of the packaging area is now close to 90% for PMIC. The FO is not used for spreading the interconnection but for side wall protection and cost reduction. In RF applications, the market has evolved toward connectivity and SiP applications.

The APE has started to grow and represents a very large market potential in the next few years. Regarding trends in density, three patterns have been observed. One for PMIC with low density, small footprint, and side wall protection. The second for smartwatches, with medium footprint, medium bump pitch, and low z-height profile. The third for smartphones with HD, large footprint, and low z-height profile with bump pitch and size flexibility.

The goal of using FO has changed in most of the applications. For MMIC, the predominant factor is no longer thermomechanical behavior. It has now become integration and cost reduction. For SiP, cost reduction is now critical. For the PMIC, side wall protection is the main concern. With AP on the other hand, z-profile and high bump density is still the main concern. Compared to all the technology available for WLP, FO is still costlier due to additional processes such as pick and place and molding affecting the cost. Depending on the specification required by the customers, the technology could be more profitable than WLP in term of flexibility, simplicity of design, thermomechanical behavior, and in some case cost reduction.

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